RF and Wireless Systems

Data Sheet

MT6162 (Othello H)

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INTRODUCTION

The MT6162 is a single-chip multi-mode multi-band transceiver offering unparalleled integration and feature set resulting in industry's lowest eBoM. It is fully compliant with 3G mode (3GPP Rel. 6), as well as supporting GSM/GPRS/EDGE modes (GGE). It constitutes with MediaTek's baseband modem ICs a complete chipset solution for 3G and GGE cellular user equipment. Quad-band GGE and a wide range of 3G bands support (I - VI, VIII - X) is provided in terms of both frequency ranges and the flexibility of band allocation.

The direct conversion receiver is part of an over-sampled sigma-delta architecture, which shifts more signal conditioning to digital baseband (DBB) and results in optimum HSDPA throughput. The direct modulation transmitter (8PSK/3G), combined with a low noise GMSK constant envelope modulator or DFM (Direct-Frequency Modulation), delivers high modulation accuracy with exceptionally low noise and eliminates the need for transmit SAW filters in any of the supported GGE and 3G modes. On-chip impairments compensation is used to guarantee optimum 3G Rx and Tx performance. The 3G receiver operation is SAW-less and does not require any Rx SAW filters post LNAs. Two on-chip VCOs at 2xLO/4xLO frequencies provide the two local oscillators required for RX and TX sections; they are followed by frequency dividers and are locked to the system reference via two fast-settling RF Fractional-N PLLs.

All functional and PLL programming is done via a 3-wire serial bus. The chip operates from 2.8V and 1.8V regulated supplies from a PMT sub-system in the baseband section, and is housed in a 6.2x6.2mm^2 62-pin aQFN package with an offset array 0.666mm pin spacing (minimum pin to pin distance 0.47mm).

FEATURES

General

- **Fully integrated single chip RF Transceiver**
- **Quad-band GSM/EDGE operation**
- **Multi-band (I – VI, and VIII – X) 3G FDD operation**
- **Part of MTK's turnkey platform solutions with best-in-class performance and industry's lowest eBoM due to smart architecture choice**
- **Compliant with 3GPP HSDPA/HSUPA Release 6**
- **On-chip correction for RF impairments, with digital baseband support for optimum TRx performance and reduced chip calibration test time**
- **Lead free 62-pin aQFN package (6.2x6.2mm^2)**

Transmitter

- **Low noise GMSK/ 8PSK/ 3G TX modulator eliminating external SAW filters, with Direct-Frequency Modulation TX for GSM mode**
- **Dedicated Tx drivers that can support radio configuration with multi-mode multi-Band PAs**
- **Excellent 3G EVM performance over the full Tx dynamic range**
- **High dynamic range integrated synchronous power detector, with ultra-fast TX power control support**
- **Low Tx supply current from Vbat: Typical 48mA (3G avg. DG09, Band I); 36mA (GMSK DFM)**

Receiver

- **High performance SAW-less (3G only) direct conversion receiver, with differential input LNAs**
- **Receiver with superior sensitivity and blocking margins**
- **Low Rx supply current from Vbat: Typical 37mA (3G avg. DG09, Band I); 40mA (GSM/EDGE)**

Frequency Synthesizers

- **Fast settling synthesizers, with 26MHz internal DCXO or external VCTCXO reference**

APPLICATIONS

Single and multi band / mode 3G handsets
3G/HSDPA/HSUPA Wireless data modems (3GPP Release 6)
WEDGE / HEDGE solutions

FUNCTIONAL BLOCK DIAGRAM

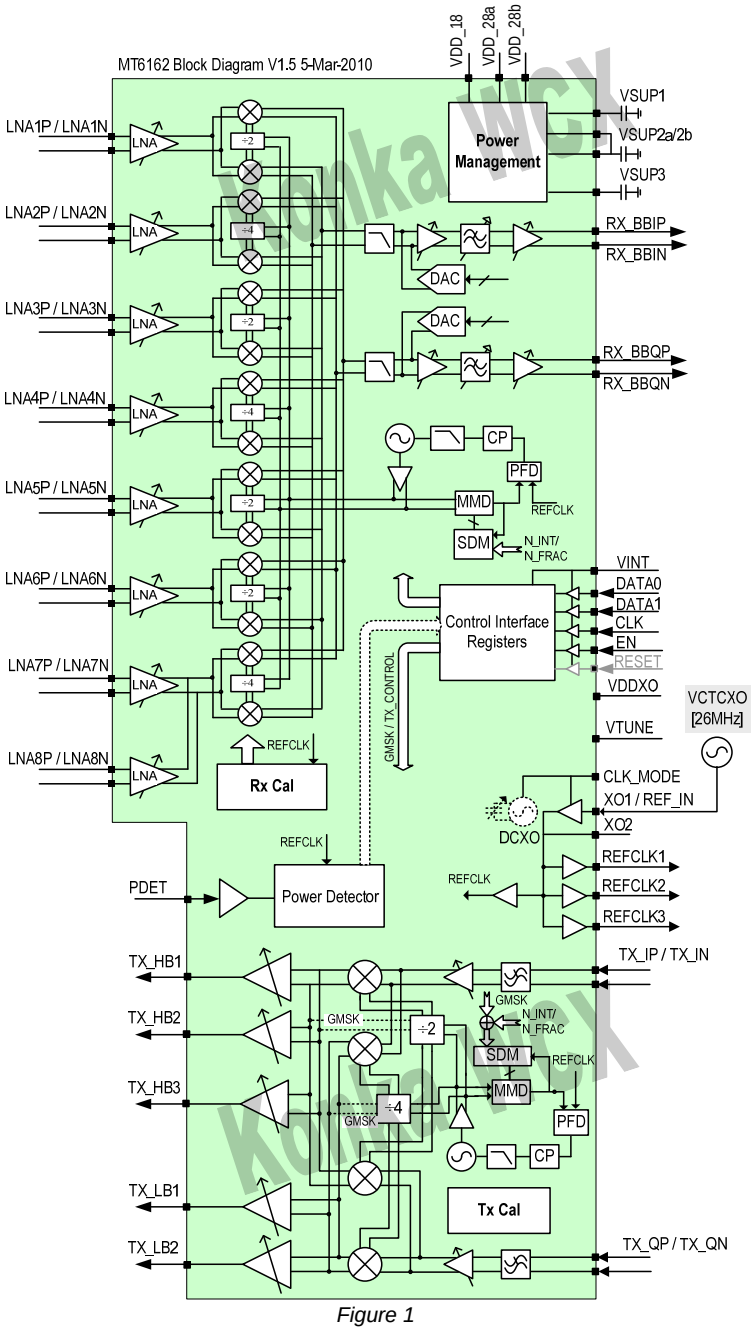

Figure 1

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OPERATING CONDITIONS

Table 1

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Reference Supply	V_{DD_28}	2.75	2.85	2.95	V	Linear regulated supply
	V_{DD_18}	1.75	1.825	1.9	V	Switching regulated supply
	V_{INT}	1.675	1.8	1.925	V	Serial interface control logic
VCXO/DCXO Supply	V_{DDXO}	2.7	2.8	2.9	V	Linear regulated supply
Ambient Temperature	T_{amb}	-30	25	85	ºC	
Rx baseband load capacitance	C_{LD}			10	pF	Equivalent Differential[1)]
Rx baseband load resistance	R_{Ld}	20	32	45	kΩ	Differential
Rx required amplitude balance	DA_{diff}	-1		1	dB	All Rx input pairs
Rx required phase balance	Df_{diff}	-10		10	deg	All Rx input pairs
Tx baseband I/Q common mode	V_{CM}	1.05	1.1	1.15	V	
		1.05		1.25	V	Acceptable range with slight degradation[2)]
Tx baseband I/Q differential Full-Scale input		940	990	1040	mVppd	2.4dB allocated for Tx RF impairments compensation; 750mVppd effectively used for I/Q Tx BB signal
Tx baseband I/Q Input Resistance		200			kΩ	Differential
Tx baseband I/Q Input Capacitance				2.5 4.0	pF pF	Differential Single-Ended
High Band (HB) Transmitter Frequency	F_{Tx}	1920		1980	MHz	3G Band I
		1850		1910		3G Band II / GSM1900
		1710		1785		3G Band III/IV/IX/X / GSM1800
Low Band (LB) Transmitter Frequency		824		849	MHz	3G Band V/VI / GSM850
		880		915		3G Band VIII / GSM900
High Band (HB) Receiver Frequency	F_{Rx}	2110		2170	MHz	3G Band I/IV/X
		1930		1990		3G Band II / GSM1900
		1805		1880		3G Band III/IX / GSM1800
Low Band (LB) Receiver Frequency		869		894	MHz	3G Band V/VI / GSM850
		925		960		3G Band VIII / GSM900
Reference Input Clock (VCTCXO) Frequency	F_{ref}		26		MHz	
Voltage Swing		700		1500	mVpp	
Duty Cycle		40		60	%	
Reference Input Clock (VCTCXO) Phase Noise				-106	dBc/Hz	@ F_{offset} = 100Hz
				-134	dBc/Hz	@ F_{offset} = 1KHz
				-144	dBc/Hz	@ F_{offset} = 10KHz
				-148	dBc/Hz	@ F_{offset} = 100KHz
Harmonic Content				-8	dBc	HD2 @ 52MHz
				-10	dBc	HD3 @ 78MHz
				-20	dBc	HD4 @ 104MHz

[1)] V_{CM} up to 1.25V causes no performance degradation for nominal silicon over ETC. For worst-case silicon, a ~1dB degradation in full chain ACLR can be expected.

[2)] The load capacitance can be either common mode (to AC ground) or differential. The specification is written in terms of an equivalent differential load capacitance. In reality, the split can be arbitrary between common mode and differential mode, and both scenarios must be considered. The maximum difference between C_{RX-GND} and $C_{RXB-GND}$ is 1pF.

ABSOLUTE MAXIMUM RATINGS

Table 2

Parameter	Rating
VSUP3, VDD_28a/b, VDDXO	-0.3 V to 3.6 V
VSUP1, VSUP2, VDD_18	-0.3 V to 2.0 V
Serial Interface supply VINT	-0.3 V to 2.0 V
Digital Input Voltage	-0.3 to VINT+0.3V
Analog Input Voltage	-0.3 to VDD28+0.3V
Storage Temperature	-55 ºC to 150 ºC
Operating Junction Temperature	+125 ºC
LNA Input Level	+3dBm RF differential input (100Ω)
Power Detector Input Level	+7dBm RF input (50Ω)
Maximum power dissipation	750mW

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes

1. No DC input should be directly applied to the Rx inputs. Matching network should either be a series capacitor/inductor or shunt inductor (RXn/RXnB)
2. Tx Output is DC shorted to ground internally no DC should be applied under any circumstances (AC coupling required for those PA's with DC at the input)
3. VSUP1-VSUP3:. No short circuit protect is implemented; no DC should be applied under any circumstances

THERMAL RESISTANCE

Thermal resistance data is with a JEDEC standard PCB board.

Table 3 Thermal Resistance

Package Type	Θ_{ja} (to ambient)	Ψ_{jb} (to board)	Unit
aQFN	26	5	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

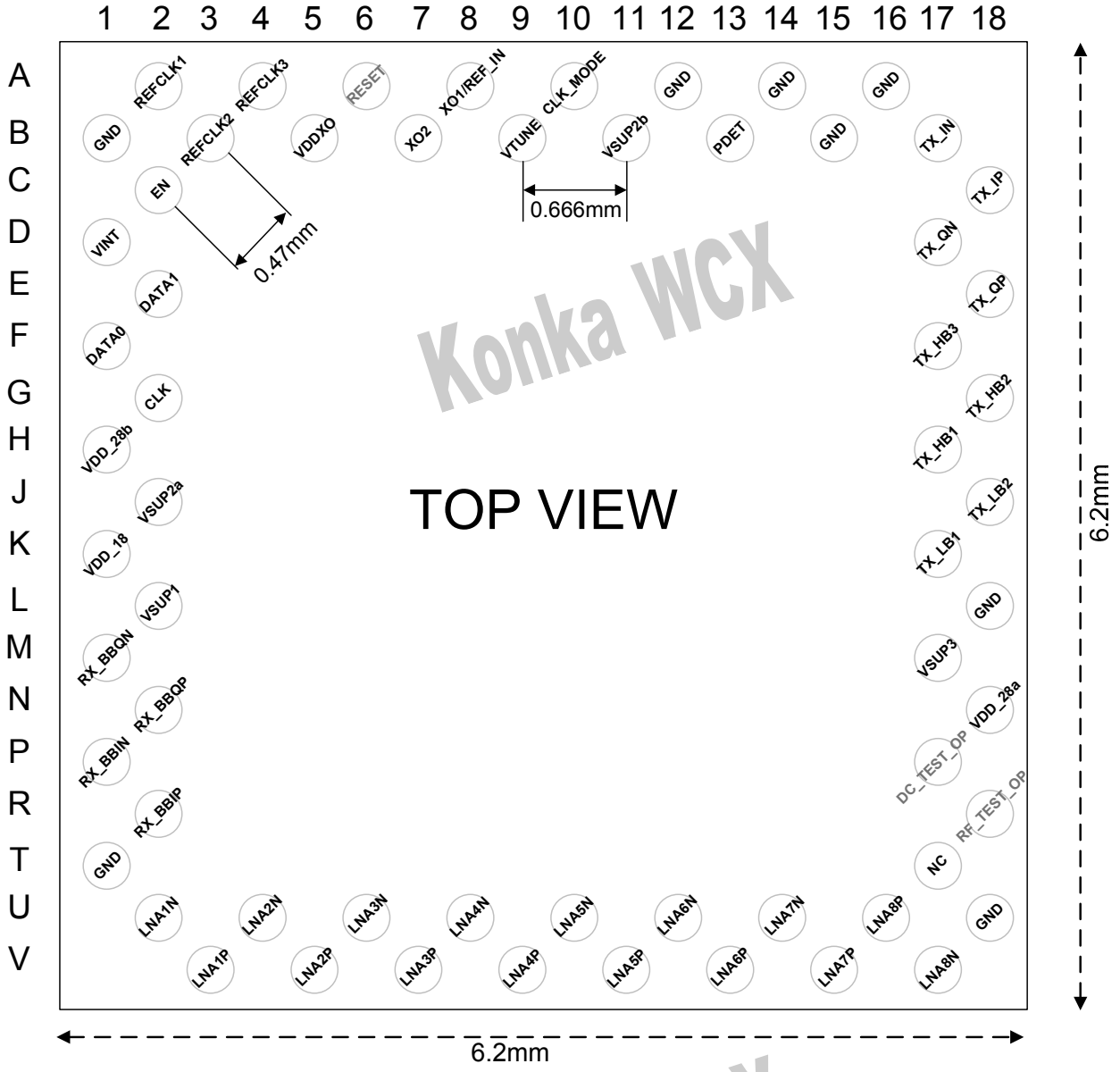

Figure 2

Table 4 Pin Allocation / Function Description

Pin	Name	Description	Pin	Name	Description
A2	REFCLK1	Reference Clock Buffer #1 main for digital baseband	K1	VDD_18	Regulated supply for IC
A4	REFCLK3	Reference Clock Buffer #3	K17	TX_LB1	Tx Low band Driver #1
A6	NC	No connect	L2	VSUP1	Internal Supply (ext. cap)
A8	XO1/REFIN	Crystal Pin #1 or Ref Clock Input	L18	GND	Ground; connect to GND plane on PCB
A10	CLK_MODE	Select DCXO or VCTCXO	M1	RX_BBQN	Rx Baseband Output – Q Channel
A12	GND	Ground; connect to GND plane on PCB	M17	VSUP3	Internal Supply (ext. cap)
A14	GND	Ground; connect to GND plane on PCB	N2	RX_BBQP	Rx Baseband Output – Q Channel
A16	GND	Ground; connect to GND plane on PCB	N18	VDD_28a	Regulated supply for IC
B1	GND	Ground; connect to GND plane on PCB	P1	RX_BBIN	Rx Baseband Output – I Channel
B3	REFCLK2	Reference Clock Buffer #2	P17	NC	No connect
B5	VDDXO	Regulated supply for VCXO/DCXO	R2	RX_BBIP	Rx Baseband Output – I Channel
B7	XO2	Crystal Pin #2	R18	NC	No connect
B9	VTUNE	AFCDAC Output	T1	GND	Ground; connect to GND plane on PCB
B11	VSUP2b	Internal Supply (ext. cap)	T17	NC	No Connect
B13	PDET	Power Detector Input	U2	LNA1N	Rx Path #1 Input
B15	GND	Ground; connect to GND plane on PCB	U4	LNA2N	Rx Path #2 Input
B17	TX_IN	Tx Baseband Input – I Channel	U6	LNA3N	Rx Path #3 Input
C2	EN	Serial Interface Enable (BSI)	U8	LNA4N	Rx Path #4 Input
C18	TX_IP	Tx Baseband Input – I Channel	U10	LNA5N	Rx Path #5 Input
D1	VINT	Serial interface control logic	U12	LNA6N	Rx Path #6 Input
D17	TX_QN	Tx Baseband Input – Q Channel	U14	LNA7N	Rx Path #7 Input
E2	DATA1	Serial Data I/O (BSI)	U16	LNA8P	Rx Path #8 Input
E18	TX_QP	Tx Baseband Input –Q Channel	U18	GND	Ground; connect to GND plane on PCB
F11	DATA0	Serial Data I/O (BSI)	V3	LNA1P	Rx Path #1 Input
F17	TX_HB3	Tx High band Driver #3	V5	LNA2P	Rx Path #2 Input
G2	CLK	Serial Interface Clock (BSI)	V7	LNA3P	Rx Path #3 Input
G18	TX_HB2	Tx High band Driver #2	V9	LNA4P	Rx Path #4 Input
H1	VDD_28b	Regulated supply for IC	V11	LNA5P	Rx Path #5 Input
H17	TX_HB1	Tx High band Driver #1 (2G only)	V13	LNA6P	Rx Path #6 Input
J2	VSUP2a	Internal Supply (ext. cap)	V15	LNA7P	Rx Path #7 Input
J18	TX_LB2	Tx Low band Driver #2 (2G only)	V17	LNA8N	Rx Path #8 Input

notes

1. VSUP2a and VSUP2b should be shorted on the PCB
2. VDD_28a and VDD_28b should be shorted on the PCB
3. Pin T17 is recommended a 'No Connect' pin to balance parasitics on the RF Input pins
4. CLK_MODE:
   GND = Internal DCXO (Crystal mode)
   Floating or connect to VDDXO = External Clock (VCTCXO)

TRANSCEIVER PIN CONFIGURATION

RECEIVER FRONT-END MAPPING

Each of the eight independent LNA/mixer/divider are dedicated to either high (VCO divide-by-2) or low (VCO divide-by-4) band. Furthermore, even though the LNA's are identical, some recommended configurations are required since performance may be limited by board/package isolation.

Table 5 Rx configuration

LNA #	High / Low	Configuration#1	Configuration#2	Configuration#3
1	HB	Band 2	Band2/GSM1900	Band 2
2	LB	Band 8	Band8/GSM900	Band 8
3	HB	Band 1	Band 1	Band 1
4	LB	Band 5	Band5/GSM850	Band 5
5	HB	GSM1900	N/C	Band 4
6	HB	GSM1800	GSM1800	GSM1800/1900 (Diplex)
7	LB	GSM900	N/C	GSM900
8	LB	GSM850	N/C	GSM850

TRANSMITTER FRONT-END MAPPING

Each of the five independent Tx output drivers are dedicated to either high (VCO divide-by-2) or low (VCO divide-by-4) band. Furthermore, two outputs (TX_LB2/TX_HB1) are dedicated to GSM/EDGE mode only, and the remaining three outputs are multi-mode (MM ≡ '3G and GSM/EDGE').

Table 6 Tx Configuration#1

Tx Output	GSM850/900	GSM1800/1900	B5/B8	B1/B2/B3/B4	Notes
TX_LB1			✓		Single Mode WCDMA or Multimode PA
TX_LB2	✓				Single Mode GSM/EDGE PA
TX_HB1		✓			Single Mode GSM/EDGE PA
TX_HB2				✓	Single Mode WCDMA or Multimode PA
TX_HB3				✓	Single Mode WCDMA or Multimode PA

Table 7 Tx Configuration#2

Tx Output	GSM850/900	GSM1800/1900	B5/B8	B1/B2/B3/B4	Notes
TX_LB1	✓		✓		Single Mode WCDMA or Multimode PA
TX_LB2					Single Mode GSM/EDGE PA
TX_HB1					Single Mode GSM/EDGE PA
TX_HB2		✓		✓	Single Mode WCDMA or Multimode PA
TX_HB3					Single Mode WCDMA or Multimode PA

ELECTRICAL CHARACTERISTICS

The Electrical Characteristics defined are valid for the Operating Conditions specified in Table 1, receiver pin configuration#1, and transmitter pin configuration#1, unless otherwise described. For ABB gain blocks settings based on a specific ABB gain. The dc-dc converter supplying V_{DD_18} is assumed to have 90% efficiency and operates from a nominal battery voltage, V_{bat} ~ 3.6V.

Typical specifications are for register settings are mid-band channel frequencies, and recommended operating conditions. Min/Max specifications are for Extreme operating voltage and temperature conditions, unless otherwise stated.

DC & VOLTAGE REGULATORS

Table 8

Parameter	Min	Typ	Max	Unit	Test Conditions / Comments
Idle mode		11		μA	V_{INT} on; All else off
Equivalent Battery Supply Current [3]					VDD_18 & VDD_28
Rx Alert		3.3	4	mA	All Rx power domain LDOs enabled
Rx On					RX signal path fully enabled; Tx off
3G mode, max gain		38	48	mA	LNA HI gain/ ABB gain: 32dB
3G mode, med gain		31	40	mA	LNA MED gain/ ABB gain: 14dB
3G mode, low gain		28	35	mA	LNA LOW gain/ ABB gain: -7dB
GGE mode, max gain		40	50	mA	LNA HI gain/ ABB gain: 32dB
GGE mode, med gain		33	41	mA	LNA MED gain/ ABB gain: 14dB
GGE mode, low gain		30	37.5	mA	LNA LOW gain/ ABB gain: -7dB
Tx Alert		2	3	mA	All Tx power domain LDOs enabled
Tx (HB) On					Tx high-band signal path on; Rx off
WCDMA mode @ Pout = +4.5dBm		92	112	mA	12.2k UL ref ch. (187mVd rms I/Q)
WCDMA mode @ Pout = +2.5dBm		91	110	mA	12.2k UL ref ch. (187mVd rms I/Q)
WCDMA mode @ Pout = -10dBm		51	62	mA	12.2k UL ref ch. (187mVd rms I/Q)
WCDMA mode @ Pout ≤ -58dBm		34	43	mA	12.2k UL ref ch. (187mVd rms I/Q)
GMSK mode		35	44	mA	TX_HB1 output
8PSK mode @ Pout = -2.5dBm		64	80	mA	TX_HB1 output; (180mVd rms I/Q)
MMMB GMSK mode		94		mA	TYP output power; RF gain = 1
MMMB 8PSK mode @ Pout = +3.5dBm		83	104	mA	
Tx (LB) On					Tx low-band signal path on; Rx off
WCDMA mode @ Pout = +2.5dBm		75	94	mA	12.2k UL ref ch. (187mVd rms I/Q)
WCDMA mode @ Pout = -10dBm		40	50	mA	12.2k UL ref ch. (187mVd rms I/Q)
WCDMA mode @ Pout ≤ -58dBm		34	43	mA	12.2k UL ref ch. (187mVd rms I/Q)
GMSK mode		36	45	mA	TX_LB2 output
8PSK mode @ Pout = +0.5dBm		71	89	mA	TX_LB2 output; (180mVd rms I/Q)
MMMB GMSK mode		87		mA	TYP output power; RF gain = 1
MMMB 8PSK mode @ Pout = +4.5dBm		90	110	mA	

[3] $$equivalent\_battery\_current = Idd(VDD\_28) + Idd(VDD\_18) \times \frac{1.8V}{3.6V} \times \frac{1}{0.9}$$

Table 9

Parameter	Min	Typ	Max	Unit	Test Conditions / Comments
VDDXO Supply Current					
External clock mode		2.2		mA	REFCLK1 output enabled with DS load condition; AFC DAC turned off
DCXO mode		3.5		mA	REFCLK1 output enabled with DS load condition; AFC DAC turned off

RECEIVER SYSTEM

All receiver characteristics are applicable for all RX frequency bands when operated under the recommended operating conditions and receiver pin configuration#1, unless stated otherwise. Receiver's differential input ports are matched to 100Ω (3G) / 100Ω (GGE) characteristic impedance (Z_0), with all power levels (in dBm) referenced to Z_0. The BB I/Q output ports are presented each with a differential load equivalent to 32kΩ||5pF. The reference oscillator's frequency used for the on-chip PLL is 26MHz. For ABB gain blocks settings based on a specific ABB gain.

Typical specifications are for register settings mid-band channel frequency, and recommended operating conditions. Min/Max specifications are for Extreme operating voltage and temperature conditions, unless otherwise stated.

Table 10

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions / Comments
3G Receiver						
Input Return Loss	S_{11}		-10		dB	Ref. plane (Z_0) at matching components
Voltage gain: Max. (HB)	$G_{V,max}$	67	70	72	dB	LNA HI gain; G_{ABB}= 32dB
Max (LB)		66	69	71	dB	
Voltage gain: Mid. (HB)	$G_{V,mid}$	38	41	43	dB	LNA MED gain; G_{ABB}= 14dB
Voltage gain: Min. (HB)	$G_{V,min}$	3	6	8	dB	LNA LOW gain; G_{ABB}= -7dB
Min. (LB)		5	8	10	dB	
DSB Noise Figure (HB)	NF_{HI}		2.5	3.9	dB	All frequency channels; LNA HI gain;
(LB)			2.6	4.0	dB	G_{ABB}= 29dB
DSB Noise Figure, Mid. gain	NF_{MID}		13	16	dB	LNA MED gain; G_{ABB}= 14dB
Rx Composite EVM*	EVM_{Rx}					-63dBm desired signal; Rx gain = $G_{V,mid}$;
(* not including digital baseband phase compensation)			5	8	%	// (HSDPA Hset-2 QPSK)
			6	9	%	// (HSDPA Hset-2 16QAM)
Input IP3 (ACS1)	$iIP_{3,ACS1}$	-3	2		dBm	df1= ±3.5M, df2= ±6.5M; –35dBm/tone; LNA MED gain; G_{ABB}= 23dB
Input IP3 (ACS2)	$iIP_{3,ACS2}$	0	5		dBm	df1= ±3.5M, df2= ±6.5M; –20dBm/tone; LNA LOW gain; G_{ABB}= 20dB
Input IP3 (10/20M) (HB)	$iIP_{3,IM}$	-7	-2		dBm	df1= ±10.1MHz, df2= ±20MHz //
(LB)		-5	0			–38dBm/tone; LNA HI gain; G_{ABB}= 29dB
Input IP3 (NB_IM)	$iIP_{3,NBIM}$					–35dBm/tone; LNA HI gain; G_{ABB}= 17dB
(HB)		-7	-2		dBm	df1/2= ±3.5MHz/ ±5.9MHz (band II/V/X);
(LB)		-4	1		dBm	df1/2= ±3.6MHz/±6.0MHz (band III/ VIII)
Input IP3 (GMSK w Tx Blocker)	$iIP_{3,NBwTx}$					–35dBm/tone; LNA MED gain; G_{ABB}= 29dB
Band II/V/X		-2	3		dBm	df1= ±2.7MHz, f2/f3=f_{Tx}-1.1/+1.1MHz
Band III/VIII		-2	3		dBm	df1= ±2.8MHz, f2/f3=f_{Tx}-1.1/+1.1MHz
Input IP3 (Out of Band blocker)	$iIP_{3,OBwTx}$					LNA HI gain; G_{ABB}= 29dB
Band I		-7	-3		dBm	2024.9M/ –38dBm, 1930M/ –28dBm
Band II		-7	-3		dBm	1830.2M/ –38dBm, 1910M/ –28dBm
Band V		-4	0		dBm	784.2M/ –41dBm, 829M/ –31dBm
Band VIII		-4	0		dBm	840.2M/ –41dBm, 885M/ –31dBm
Input IP2 (ACS2)	$iIP_{2,ACS2}$	50	>60		dBm	df1= ±4.5M, df2= ±5.5M; –20dBm/tone; LNA LOW gain; G_{ABB}= 20dB
Input IP2 (@15M inband blocker offset)	$iIP_{2,IB15}$	40	50		dBm	df1= ±14.5M, df2= ±15.5M; –27dBm/tone; LNA HI gain; G_{ABB}= 26dB
Input IP2 (@ Tx blocker offset)	$iIP_{2,Tx}$					
(HB)		45	55		dBm	f1= ±(f_{Tx} -0.5M); f2= ±(f_{Tx}+0.5M);
(LB)		45	55		dBm	–27dBm/tone; LNA HI gain; G_{ABB}= 29dB
Input-1dB compression	IP_{-1dB}	-9	-5		dBm	LNA LOW gain; G_{ABB}= -7dB

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions / Comments
Input-1dB gain compression (ACS2)	$IP_{-1dB,ACS2}$	-12	-8		dBm	Blocker level that results in 1dB gain reduction at desired signal; LNA LOW gain; G_{ABB}= 20dB
Input-1dB gain compression (Inband Blocker @ 15M offset)	$IP_{-1dB,IB15}$	-19	-15		dBm	Blocker level that results in 1dB gain reduction at desired signal; LNA HI gain; G_{ABB}= 26dB
Input-1dB gain compression (GMSK blocker @ 2.7M offset; band II/III/V/VIII/X)	$IP_{-1dB, GMSK}$	-38	-34		dBm	Blocker level that results in 1dB gain reduction at desired signal; LNA MED gain; G_{ABB}= 29dB
Input-1dB gain compression (Tx blocker)	$IP_{-1dB, TX}$	-19	-15		dBm	Blocker level that results in 1dB gain reduction at desired signal; LNA HI gain; G_{ABB}= 29dB
Uncal. I/Q phase mismatch	$\Delta\Phi_{IQ\_RX}$			±2	deg	Un-calibrated spec.; LNA MED gain //
Uncal. I/Q amplitude mismatch	ΔA_{IQ_RX}			±0.5	dB	G_{ABB}= 17dB; BB tone freq. = 200kHz
Quadrature phase mismatch	$\Delta\Phi_{IQ\_RX}$			±0.5	deg	Calibrated spec. using TTG RF tone //
Quadrature amplitude mismatch	ΔA_{IQ_RX}			±0.1	dB	LNA MED gain; G_{ABB}= 17dB; BB tone freq. = 200kHz
3G Receiver Analog Baseband section						
DC Common Mode Level	V_{RX_DCCM}	1.08	1.2	1.32	V	
Output-1dB Compression	OP_{-1dB}	1.7	1.9	2.1	Vpd	LNA HI gain; G_{ABB}= 29dB
Gain step variation	ΔG_{RX_3dB}	-0.2		0.2	dB	3dB gain step from any gain setting
	ΔG_{RX_XdB}	-0.5		0.5	dB	Any gain change
Baseband filter						
3dB corner frequency	A_{-3dB}	2.11	2.23		MHz	After corner frequency calibration
Stopband attenuation						
2.7/2.8M offset (GMSK)	$A_{GSM2.7M}$	6	8		dB	Integrated over 200kHz BW at 2.7/2.8M
3.5/3.6M offset (CW)	$A_{3.5M}$	14	17		dB	At 3.5/3.6M
5.9/6.0M offset (GMSK)	$A_{GSM5.9M}$	30	33		dB	Integrated over 200kHz BW at 5.9/6.0M
5M offset (WCDMA)	A_{W5M}	18	22		dB	Integrated over 3.84M BW at 5M
10M offset (WCDMA)	A_{W10M}	45	49		dB	Integrated over 3.84M BW at 10M
15M offset (WCDMA)	A_{W15M}	65	69		dB	Integrated over 3.84M BW at 15M

Table 11

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions / Comments
GGE Receiver						
Input Return Loss	S_{11}		-10		dB	Ref. plane (Z_0) at matching components
Voltage gain: Max. (HB)	$G_{V,max}$	67	70	72	dB	LNA HI gain/ G_{ABB}= 32dB
Max (LB)		66	69	71	dB	
Voltage gain: Mid.	$G_{V,mid}$	38	41	43	dB	LNA MED gain/ G_{ABB}= 14dB
Voltage gain: Min.	$G_{V,min}$	3	6	9	dB	LNA LOW gain/ G_{ABB}= -7dB
DSB Noise Figure (HB)	NF_{HI}		2.3	3.4	dB	All frequency channels; LNA HI gain;
(LB)			2.5	3.6	dB	G_{ABB}= 29dB
Input IP3 (HB)	$iIP_{3,IM}$	-5	-1		dBm	df1= ±0.81MHz, df2= ±1.6MHz;
(LB)		-3	1			–41dBm/tone; LNA HI gain; G_{ABB}= 29dB
Input IP2 (AM detection) (HB)	$iIP_{2,AM}$	45	55		dBm	df1= ±5.98MHz, df2= ±6.02MHz;
(LB)		50	60		dBm	–27dBm/tone; LNA HI gain; G_{ABB}= 29dB
Input-1dB compression	IP_{-1dB}	-9	-5		dBm	LNA LOW gain; G_{ABB}= -7dB
Input-1dB gain compression (ACI1)	$IP_{-1dB,ACI1}$	-31	-27		dBm	Blocker level that results in 1dB gain reduction at desired signal; LNA HI gain; G_{ABB}= 14dB

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions / Comments
Input-1dB gain compression (ACI2)	$IP_{-1dB,ACI2}$	-32	-28		dBm	Blocker level that results in 1dB gain reduction at desired signal; LNA HI gain; G_{ABB}= 20dB
Input-1dB gain compression (CW Blocker 0.8M offset)	$IP_{-1dB,0.8M}$	-30	-26		dBm	Blocker level that results in 1dB gain reduction at desired signal; LNA HI gain; G_{ABB}= 29dB
Input-1dB gain compression (CW Blocker 3M offset)	$IP_{-1dB,3M}$	-21	-17		dBm	Blocker level that results in 1dB gain reduction at desired signal; LNA HI gain; G_{ABB}= 29dB
2·Rx Suppression	H_{OOB_2RX}	37	55		dB	LNA HI gain; G_{ABB}= 29dB
3·Rx Suppression (HB)	H_{OOB_3RX}	20	25		dB	LNA HI gain; G_{ABB}= 29dB
(LB)		18	23		dB	LNA HI gain; G_{ABB}= 29dB
5·Rx Suppression (LB)	H_{OOB_5RX}	26	35		dB	LNA HI gain; G_{ABB}= 29dB
Uncal. I/Q phase mismatch	$\Delta\Phi_{IQ\_RX}$			±2	deg	Un-calibrated spec.; LNA MED gain//
Uncal. I/Q amplitude mismatch	ΔA_{IQ_RX}			±0.5	dB	G_{ABB}= 17dB; BB tone freq. = 200kHz
Quadrature phase mismatch	$\Delta\Phi_{IQ\_RX}$			±0.5	deg	Calibrated spec. using TTG RF tone //
Quadrature amplitude mismatch	ΔA_{IQ_RX}			±0.1	dB	LNA MED gain; G_{ABB}= 17dB; BB tone freq. = 200kHz
GGE Receiver Analog Baseband section						
DC Common Mode Level	V_{RX_DCCM}	1.08	1.2	1.32	V	
Output-1dB Compression	OP_{-1dB}	1.7	1.9	2.1	Vpd	LNA HI gain; G_{ABB}= 29dB
Gain step variation	ΔG_{RX_3dB}	-0.2		0.2	dB	3dB gain step from any gain setting
	ΔG_{RX_XdB}	-0.5		0.5	dB	Any gain change
Baseband filter						
3dB corner frequency	A_{-3dB}	148	156		kHz	After calibration
Stopband attenuation						
ACI2	A_{ACI1}	22	26		dB	400kHz offset (BW=200kHz)
ACI3	A_{ACI2}	35	39		dB	600kHz offset (BW=200kHz)
800kHz offset (CW)	$A_{0.8M}$	44	49		dB	At 800kHz
1.6MHz offset (CW)	$A_{1.6M}$	65	75		dB	At 1.6M
3.0MHz offset (CW)	$A_{3.0M}$		>90		dB	At 3.0M

TRANSMITTER SYSTEM

All transmitter characteristics are applicable for all TX frequency bands when operated under the recommended operating conditions and transmitter pin configuration#1, unless stated otherwise. Measured with 50ohm load at driver output; Input at BB is DC coupled (High Zin). In 3G and GGE modes, I/Q inputs are driven each with 185mVrms DIFF signal (WCDMA UL 12.2kbps reference channel) and 180mVrms (8PSK), respectively. The reference oscillator used with the on-chip PLL is 26MHz.

Typical specifications are for mid-band channel frequency, and recommended operating conditions. Min/Max specifications are for Extreme operating voltage and temperature conditions, unless otherwise stated.

Table 12

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions / Comments
3G Transmitter Output						
Output Return Loss	S_{22}		-12	-10	dB	50Ω load
Max Output Power						
All bands, except Band II	P_{max}	2.5			dBm	Worst case ACLR, EVM, noise emissions, and spurious emissions specs. are met
Band II only	P_{max}	4.5			dBm	
Min Output Power						
(HB)	P_{min}			-82	dBm	
(LB)	P_{min}			-81	dBm	
RF output Frequency response	ΔP		±0.2	±0.7	dB	Pout = min.P_{max}
ACLR1						±5MHz offset;
(HB)	ACLR1		-48	-43	dBc	Pout = min.P_{max}
(LB)	ACLR1		-50	-41	dBc	Pout = min.P_{max}
All bands	ACLR1		-52	-48	dBc	Pout = min.P_{max} – 11dB
ACLR2	ACLR2		-71	-65	dBc	±10MHz offset; Pout = = min.P_{max}
EVM						Measured over 1 slot/2560chips, after Tx I/Q imbalance and LO leakage calibration
(HB)	EVM		2.0	3.0	%	Pout= min.P_{max}
			2.0	3.0	%	Pout= min.P_{max} -11dB
(LB)	EVM		1.5	2.3	%	Pout= min.P_{max}
			1.5	2.3	%	Pout= min.P_{max} -11dB
Spectrum Emission Mask	SEM					Pout= min.P_{max}; 3.5M offset in 30kHz BW
(HB)			-60	-56	dBc	Note A
(LB)			-65	-61	dBc	Note A
Carrier Suppression				-20	dBc	Pout ≥ min.P_{max} -44dB; before calibration
			-48	-35	dBc	Pout= min.P_{max}; after calibration
			-39	-31	dBc	Pout= min.P_{max} -44dB; after calibration
Sideband Suppression			-45	-38	dBc	Pout ≥ min.P_{max} -44dB; after calibration
Harmonic Emissions in 1 MHz						
2nd harmonic				-25	dBc	Pout= min.P_{max}
3rd harmonic				-15	dBc	Pout= min.P_{max}
4th harmonic				-25	dBc	Pout= min.P_{max}
Ref. clock harmonics			-90	-70	dBc	52MHz; 104MHz; 208MHz

Note A: NTC1: Nominal Test Conditions (Low, Mid, High frequency channels; +15C … +35C ambient temperature; Vbat = 3.6 – 4.0V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions / Comments
Noise Emissions						
Band I, 12.5MHz offset			-145	-140	dBc/Hz	Pout= min.P_{max}; Note A
Band I, 40MHz offset			-159	-157	dBc/Hz	Pout= min.P_{max}; measured at 1880M with fTx = 1920M; Note A
Band I, noise in Rx			-162.5	-159.5	dBc/Hz	Pout= min.P_{max}; measured at 135M offset
				-153.5	dBc/Hz	Pout = -9dBm; measured at 135M offset
Band II, noise in Rx			-162	-160	dBc/Hz	Pout= min.P_{max}; measured at 80M offset
				-156	dBc/Hz	Pout = -6dBm; measured at 80M offset
Band V/VI, noise in Rx			-162	-160	dBc/Hz	Pout= min.P_{max}; measured at 45M offset
				-156	dBc/Hz	Pout = -8.0dBm; measured at 45M offset
Band VIII, noise in Rx			-162	-160	dBc/Hz	Pout= min.P_{max}; measured at 45M offset
				-156	dBc/Hz	Pout = -6.5dBm; measured at 45M offset
3G Tx baseband section						
Baseband Filter						
Selectivity, 10MHz offset		10	20		dB	After frequency corner calibration
Selectivity, 40MHz offset			55		dB	After frequency corner calibration
3G TX Gain Control						
Gain control resolution			1/32		dB	Average of LSB steps
Gain Control Step Accuracy		0.7	1.0	1.3	dB	Any 1dB step
		8.5	10	11.5	dB	Any 10dB step

Table 13

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions / Comments
GGE Transmitter Output						
Output Return Loss	S_{22}		-12	-10	dB	50Ω load
Max Output Power (GMSK)						
2G output, Mode1	P_{max}	1	3	5	dBm	GMSK Modulation, using DFM
2G output, Mode2, LB only	P_{max}	4	6	8	dBm	GMSK Modulation, using DFM
MM output	P_{max}	8	10	12	dBm	GMSK Modulation, using DFM
Max Output Power (8PSK)						
2G output, LB	P_{max}	0.5			dBm	Worst case ORFS, EVM, noise and spurious emissions specs. are met
2G output, HB	P_{max}	-2.5			dBm	
MM output, LB	P_{max}	4.5			dBm	
MM output, HB	P_{max}	3.5			dBm	
Minimum Output Power (8PSK)						
2G output, LB	P_{min}			-33	dBm	
2G output, HB	P_{min}			-38	dBm	
MM output, LB	P_{min}			-27	dBm	
MM output, HB	P_{min}			-32	dBm	
ORFS (GMSK)						
200kHz	$ORFS_{200k}$		-36	-33	dB	Pout= min.Pmax; BW=30kHz
400kHz	$ORFS_{400k}$		-66	-63	dB	Pout= min.Pmax; BW=30kHz
ORFS (8PSK)						
200kHz	$ORFS_{200k}$		-40	-36	dB	Pout= min.Pmax; BW=30kHz
400kHz	$ORFS_{400k}$		-65	-62	dB	Pout= min.Pmax; BW=30kHz

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions / Comments
Modulation accuracy (GMSK)						
RMS phase error, LB	Φ_{RMS}		1.2	3.0	deg	Pout= min.Pmax
RMS phase error, HB			1.3	3.0	deg	Pout= min.Pmax
PEAK phase error, LB	Φ_{Peak}		3.0	6.0	deg	Pout= min.Pmax
PEAK phase error, HB			4.0	8.0	deg	Pout= min.Pmax
Modulation accuracy (8PSK)						
RMS EVM, LB	EVM_{RMS}		2.0	3.0	%	Pout= min.Pmax
RMS EVM, HB			2.5	3.8	%	Pout= min.Pmax
Peak EVM, LB	EVM_{Pk}		6	10	%	Pout= min.Pmax
Peak EVM, HB			8	12	%	Pout= min.Pmax
Origin offset suppression	OOS			-20	dB	8PSK; Pout ≥ Pmin; before calibration
	OOS		-40	-35	dB	8PSK; Pout = min.Pmax; after calibration
	OOS		-39	-31	dB	8PSK; Pout = Pmin; after calibration
Sideband Suppression			-45	-38	dBc	Pout ≥ Pmin; after calibration
Tx Noise Emissions (GMSK)						
20MHz offset, LB			-165.8	-163	dBc/Hz	Pout= min.Pmax; Note A
20MHz offset, HB			-159	-156	dBc/Hz	Pout= min.Pmax; Note A
32MHz offset, LB			-166.5	-165	dBc/Hz	Pout= min.Pmax; Note B
32MHz offset, HB			-162	-159	dBc/Hz	Pout= min.Pmax; Note B
Tx Noise Emissions[1] (8PSK)						2G Output
20MHz offset, LB, Pout[1]			-159	-157	dBc/Hz	Pout = -4dBm; Note A
Pout[2]				-163.5	dBm/Hz	Pout ≤ -6.5dBm
20MHz offset, HB, Pout[1]			-154	-152	dBc/Hz	Pout = -7dBm; Note A
Pout[2]				-161.5	dBm/Hz	Pout ≤ -9.5dBm
32MHz offset, LB, Pout[1]			-160.5	-158	dBc/Hz	Pout = -4dBm; Note B
Pout[2]				-164.5	dBm/Hz	Pout ≤ -6.5dBm
32MHz offset, HB, Pout[1]			-155.5	-153	dBc/Hz	Pout = -7dBm; Note B
Pout[2]				-162.5	dBm/Hz	Pout ≤ -9.5dBm
Tx Noise Emissions[2] (8PSK)						MM Output
20MHz offset, LB, Pout[1]			-162	-158.5	dBc/Hz	Pout = 0dBm; Note A
Pout[2]				-161	dBm/Hz	Pout ≤ -2.5dBm
20MHz offset, HB, Pout[1]			-157	-153.5	dBc/Hz	Pout = -1dBm; Note A
Pout[2]				-157	dBm/Hz	Pout ≤ -3.5dBm
32MHz offset, LB, Pout[1]			-162	-158.5	dBc/Hz	Pout = 0dBm; Note B
Pout[2]				-161	dBm/Hz	Pout ≤ -2.5dBm
32MHz offset, HB, Pout[1]			-159	-155.5	dBc/Hz	Pout = -1dBm; Note B
Pout[2]				-159	dBm/Hz	Pout ≤ -3.5dBm
Tx Spurious Emissions						
2nd harmonic				-25	dBc	Pout= min.Pmax
3rd harmonic				-13	dBc	Pout= min.Pmax
4th harmonic				-25	dBc	Pout= min.Pmax
8PSK Tx baseband section						
Baseband Filter						
Selectivity, 20MHz offset			26		dB	

Note A: NTC1: Nominal Test Conditions (Low, Mid, High frequency channels; +15C … +35C ambient temperature; Vbat = 3.6 – 4.0V)
Note B: TTC: Typical Test Conditions (Mid frequency channel; +25C ambient temperature; Vbat = 3.7V)

TRANSMIT POWER CONTROL

Table 14

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions / Comments	
Power Detector							
RF Input Frequency	F_{det}	824		1980	MHz		
Input Return Loss	S_{11}		-12	-10	dB	Ref. impedance 50Ω	
Maximum Input Signal	$P_{det,max}$			0	dBm	1dB excursion from nominal slope	
Minimum Input Signal	$P_{det,min}$	-50			dBm	1dB excursion from nominal slope	
Measurement Accuracy		-0.3		0.3	dB	3 –sigma; WCDMA/ 8PSK only	
Temperature Stability		-15	2	15	mdB/ °C	Averaged over -40 to 100°C range	
Frequency response				±10	mdB/ MHz	Averaged over any supported band	
Measurement time			14		μs	With above Specifications	

SYNTHESIZERS AND REFERENCES

Table 15

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions / Comments	
Receiver Synthesizer							
Channel resolution			25		kHz		
Lock Time			120	150	μs	Phase within 10° of final lock conditions; frequency error removed	
Transmitter Synthesizer							
Channel resolution			3		Hz	3G / GGE mode	
Lock Time			120	150	μs	Phase within 10°. of final lock conditions; frequency error removed	
GMSK Lock Time				200	μs	In DFM mode (inc. loop gain calibration) after register CW1 is written; frequency error removed	
Reference Input (XO1)							
Frequency			26		MHz		
Reference Outputs (REFCLK1,2,3)							
Frequency			26		MHz	REFCLK pin	
Output Swing		0.7		1.2	Vpp	Square wave (3kΩ || 20 pF Load)	
Rise / Fall Time		2.5		9	ns	10% - 90% of signal swing (3kΩ || 20 pF Load)	
Duty Cycle		40		60	%	50% Input duty cycle	
Harmonic rejection			<-25	-22	dBc	2nd harmonic	
				-10	dBc	3rd harmonic	
				-30	dBc	4th harmonic	
SSB phase noise			<-138	-131	dBc/Hz	1kHz offset	
			<-147	-141	dBc/Hz	10kHz offset	
			<-150	-144	dBc/Hz	100kHz offset	

Table 16

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions / Comments
DCXO						
Center operating frequency	F_{DCXO}		26		MHz	
Duty Cycle		45	50	55	%	Square wave in high driving mode
Crystal C load	C_L	7	7.5		pF	
Crystal tuning sensitivity		27	32		ppm/pF	
Static range	SR		±50		ppm	CDAC from 0 to 255
Dynamic range	DR		±30		ppm	CAFC from 0 to 8191
AFC tuning step	$F_{res\text{-}AFC}$		0.007		ppm/ DAC	
AFC settling time	T_{AFC}		150	200	μs	CAFC from 0 to 8191; CAFC from 8191 to 0; Frequency error < 0.1ppm
Negative resistance	-R	100			Ω	
Start-up time			1	3	ms	Freq. error < 1ppm; Amplitude > 90 %
Pushing figure				1	ppm/V	

SERIAL PORT

Table 17

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions / Comments
DC Electrical Parameters (for DATA1/DATA2, CLK, and EN)						All inputs (DATA1/DATA2, CLK and EN) use a Schmitt trigger input stage with a Pull Down
Input High Voltage (V_{IH})		0.8* VINT			V	AC/DC
Input Low Voltage (V_{IL})				0.2* VINT	V	AC/DC
Input Current		5		30	□A	0.2*VINT≤ Vin ≤ VINT
Input Capacitance				5	pF	
Timing Parameters					ns	
Write Operation						
T_{CLK}		16.28			ns	Clock Period (1/61.44 MHz)
T1		16.28			ns	Enable High to CLK High
Ts		5			ns	Data SetUp time
Th		1			ns	Data Hold time
T2		8.14			ns	CLK Low to Enable Low
Tguard		16.28			ns	Enable Low to Enable High
Read Operation						
T1		16.28			ns	Read request clock (1/61.44 MHz)
T2		8.14			ns	CLK Low to Enable Low
T4		16.28			ns	CLK Low to CLK High (Write to Read)
T3		48.82			Ns	Read Clock Period (3/61.44 MHz)
T5		0			ns	CLK High to RX Output enable
T6				16.28	ns	CLK Low to Output Disable

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions / Comments
GMSK Data Write Operation						
Tgmskclk		16.28			Ns	CLK Period (1/61.44 MHz) Native Data rate in 2G filter is 4.33 MHz, 14 bit words.
T1		16.28			ns	Enable High to CLK High
T2		8.14			ns	CLK Low to EN Low
Tguard		16.28			ns	Enable Low to Enable High

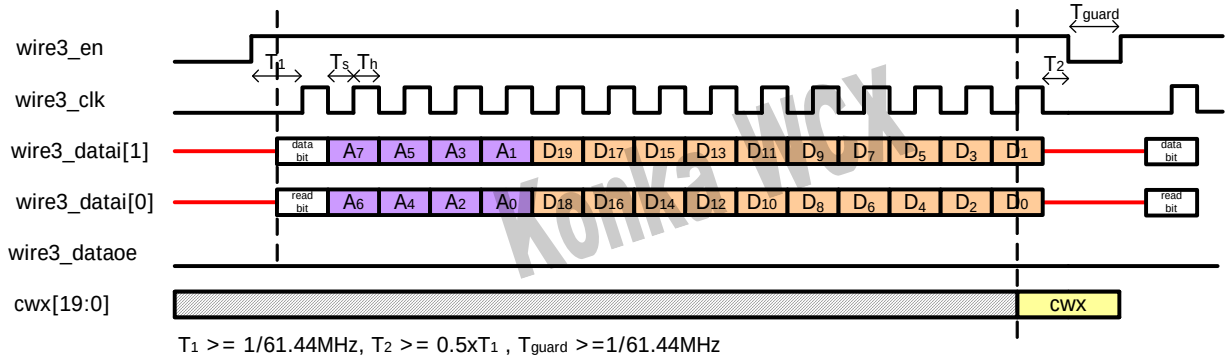

Figure 3: Serial Port Write Operation

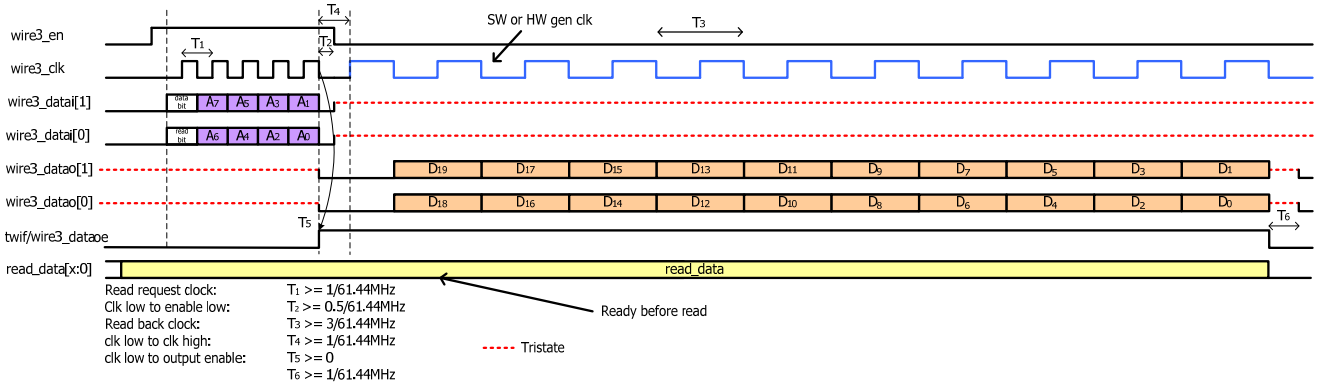

Figure 4: Serial Port Read Operation

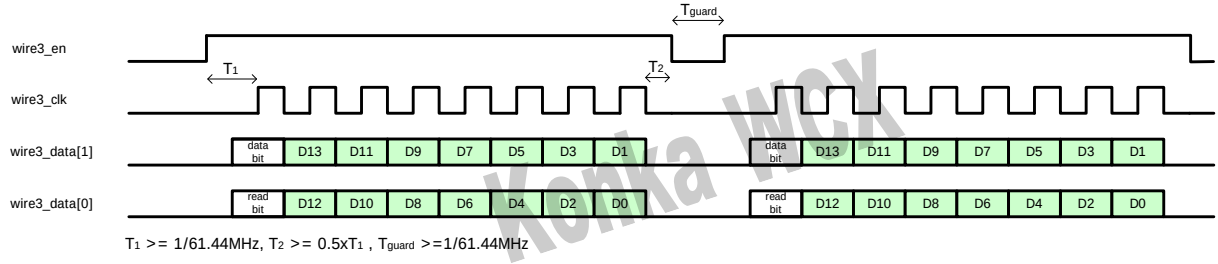

Figure 5. Tx Data Operation

TYPICAL PERFORMANCE CHARACTERISTICS

TBD

THEORY OF OPERATION

RECEIVER DESCRIPTION

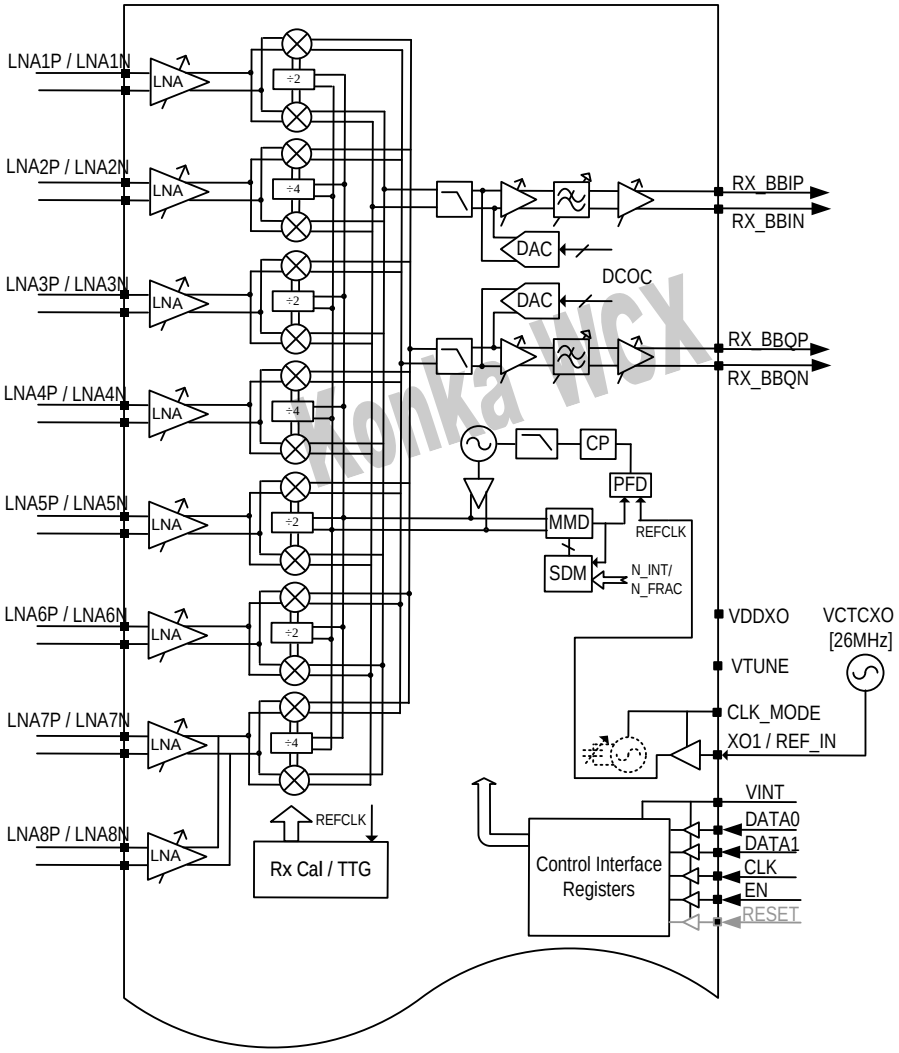

Figure 6: Block Diagram of Receiver Signal chain

The MT6162 direct conversion SAW-less receiver, designed to support 3GPP and GGE modes, includes the following functional blocks for each frequency band:

- Differential RF low noise amplifier (LNA)
- Differential I/Q demodulator
- Integrated frequency synthesizer with integrated VCO, LO buffers, and frequency divider-by-2
- Analog baseband channel select filter with automatic 3-dB corner frequency calibration mechanism
- Programmable gain amplifier with 3dB gain step
- DAC for DC offset cancellation
- Output drivers
- Image suppression calibration circuitry, which is activated at device initialization and supported by calibration routine in digital baseband

LNAs

There are eight differential LNA inputs in the receiver front-end specifically designed to be mode and frequency independent; the on-chip low-noise amplifiers require minimal external input matching network; each LNA comes with three gain steps (HI /MED/LO) to accommodate a larger receiver dynamic range, especially in Adjacent Channel Selectivity test case II as specified in 3GPP release 5,6, &7. The LNA settings are done through register LNA_GAIN[1:0]. The I/Q demodulator has a

differential topology to minimize LO leakage and second-order IM distortion products referred to receiver's input.

Mixers

High linearity quadrature mixer circuits are used to convert the RF signal to baseband in-phase and quadrature components. Two mixer sections exist, one optimized for the High band LNA outputs and one optimized for the Low band. The high band and low band mixer outputs are combined and then drive directly the first stage of the baseband low pass filter, which provides rejection for the largest blocking signals, prior to baseband amplification. Quadrature LO drive is provided to the mixers from the receiver synthesizer section via a DIV/2 or DIV/4 programmable divider, so that the same VCO can be used for both high and low bands. Excellent 90º quadrature phase and amplitude match are achieved by careful design and layout of the mixers and LO feeding network.

Baseband section

The Rx channel filter can be reconfigured based on the operation mode: GSM/EDGE or 3G WCDMA. Channel selectivity is done partially on-chip in the analog baseband low-pass filter and the rest in digital baseband with extra margin added on adjacent channel blocker rejection. A Phase equalizer of 2nd order all pass network is required in the digital baseband to minimize receiver EVM for optimum HSDPA operation. When the receiver is operating in HSDPA 64QAM mode, the filter can be reconfigured for a 10% wider BW to reduce further Rx channel filter impairments. An automatic 3-dB corner frequency calibration is performed whenever the receiver is initialized. Analog baseband gain programmability is done in 3dB gain steps with the settings in the BB_GAIN [3:0] register and according to BB gain. Calibration of DC offsets in the receiver is done at receiver initialization with an offset DAC connected at I/Q demodulator outputs to minimize differential DC offsets at receiver outputs for all RX gain steps.

DC Offset compensation

Compensating for DC offsets is an inherent part of any Direct Conversion receiver solution. DC offsets can be characterized as falling into two categories:

1) Static or slow varying
2) Time varying

The MT6162 architecture has been designed to reduce the amount of time varying DC offsets. At receiver power-up, static DC offsets at receiver I/Q outputs are sampled at the Rx I/Q ADC converters. In the baseband section, a digital signal processing block is used to estimate the static DC offsets at different Rx baseband gain steps and store in LUTs found in register settings GMSKOFFS_Q/_I[8:0] and WCDMAOFFS_Q/_I[8:0]. During normal Rx operation, DC-offset DACs at mixer outputs are used to introduce the error term back into the receive signal path based on the assigned gain setting.

Image Rejection Calibration and Test Tone Generator (TTG)

In conjunction with algorithms implemented in the baseband processor, the receiver can be calibrated for both quadrature phase and amplitude imbalance. This is important for higher order modulation systems to minimize impairments arising from the receiver. A test tone generator is used to produce a RF carrier that is then mixed down through the receiver produces a quadrature baseband tone. These tones are used by the baseband to calculate the quadrature error so that a correction can be applied. All corrections are applied in the digital domain within the baseband processor.

The intended operation is to apply the calibration when a new link is brought up i.e. at each specific RF channel frequency. Since reception is potentially continuous (for WCDMA/HSPA) then the accuracy of the corrections need to be maintained over temperature and gain setting without the need to re-calibrate.

The calibration is performed with the LNA off (and the external band select switch "open") to minimize the effects of any large interfering signals at the antenna and to avoid any leakage from the test tone to antenna causing spurious conducted emissions.

TRANSMITTER DESCRIPTION

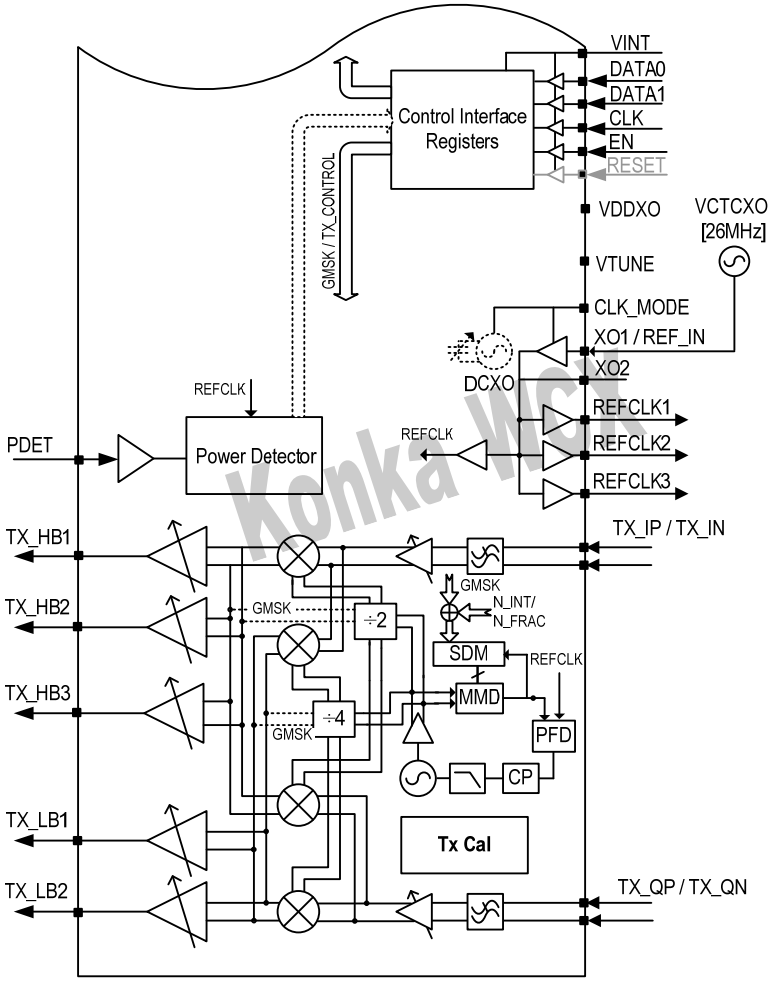

Figure 7: Block Diagram of Transmitter Signal chain

The MT6162 direct conversion SAW-less transmitter, designed to support 3GPP and EDGE modes, include the following functional blocks for each frequency band:

- 2nd order baseband low-pass filter
- Baseband programmable gain amplifier (PGA)
- Differential I/Q modulator
- Integrated frequency synthesizer with integrated VCO, LO buffers, and frequency divider-by-2/-4
- RF power amplifier driver with programmable variable gain and with single ended outputs
- LO feed-through and sideband suppression calibration circuitry, which is activated at device initialization and supported by calibration routines in digital baseband
- RMS power detector circuit, for use in the feedback path for closed-loop TX Power Control

In the GMSK mode, the high-resolution sigma-delta modulator in the synthesizer allows the direct digital modulation at RF of the synthesizer and VCO Tx blocks. GMSK data is fed over the serial bus; Gaussian pulse shaping and loop-filter compensation are implemented as digital blocks in the digital baseband section.

I/Q Baseband

The baseband interface for the I and Q channels is a differential, DC coupled input, supporting a common mode voltage (V_{CM}) centered at 1.1±0.05V. The maximum supported single-ended signal amplitude is 500 mV peak to peak, which corresponds to 1.0V peak-peak differential on the I and Q channels.

Prior to the Quadrature Modulator, the I and Q channels each pass through a second order filter with a nominal cutoff frequency of ~6.0 MHz. The filter provides the required rejection for DAC images and noise emissions from digital Baseband IC. The filter also helps to reject any spurious signals that can be coupled to the baseband terminals on the PCB.

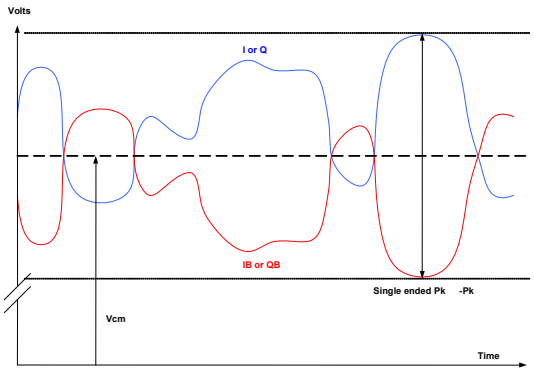

Figure 8: TX I/Q Modulator input levels

Special Considerations: (i) HSUPA Mode, (ii) MMMB operation mode

(i) In typical WCDMA TX mode, constant I/Q input signal RMS voltage is used for all TX output power levels. In HSUPA TX modes (with HS-DPCCH only or with E-DCH), the digital baseband IC is required to reduce the input signal I/Q RMS voltage accordingly, based on the Maximum Power Reduction (MPR) as specified in 3GPP standard. As a result, no additional Tx BB gain adjustment is required. (ii) Two TX outputs (1LB, 1HB) are dedicated for GGE mode only, and they are designed to drive GGE mode only quad-band PAs. For the case in which the power amplifier can operate in both GGE and 3G modes and over different bands, the 3G mode TX outputs are used to drive the Multi-Mode Multi-Band PA (refer to Table7). In GGE mode, the TX output power is variable and can be set to a level higher than that of GGE mode only outputs.

TX LO Feed-Thru and Sideband Suppression Calibrations

Upon powering up, TX carrier leakage or LOFT and sideband suppression calibrations are performed automatically for each band's center frequency channel. In MT6162, the carrier leakage calibration is performed before the sideband suppression calibration. The carrier leakage calibration requires both RX and TX frequency synthesizers to be ON. The digital baseband IC is required to output a constant DC signal during this calibration process. For sideband suppression calibration, the digital baseband IC is required to deliver CW tones at Tx BB I/Q inputs. During both carrier and sideband suppression calibrations, the transmitter gain is varied in order to perform the calibration at different output power levels.

RMS Power Detector

The MT6162 power detector is a direct conversion receiver optimized for very stable gain to allow accurate power measurements. The power detector absolute accuracy is calibrated with a single calibration at ambient temperature in each 3GPP band. It contains I/Q mixers and uses the TX synthesizer to downconvert the feedback signal to baseband; the signal is filtered and sampled by detector ADC (Figure 2.1). To allow fast measurements without data dependency an additional reference signal path is provided. The ADC is shared between this reference path and the main power detector path. The system is designed to work with a coupler and attenuator so that the PA output power can be sensed. The RMS voltage is digitally estimated both at the baseband inputs and at the RF feedback pin, so that the gain of the Tx chain including PA, etc. can be calibrated within microseconds, regardless of short-term statistical variations in the AM envelope of the baseband signals. This technique ensures the RMS power is accurately measured independent of type of modulation or traffic channel configuration. The power detector features fast settling time, typically 5us, and can be powered down during the majority of the time, adding little current consumption to the total solution.

For LO feed-through and sideband suppression calibration purposes, the detector measurement path can be re-used together with a separate feedback LNA to measure the output of the Tx drivers. In this case, the internal ADC is no used and instead the calibration signal is connected to the receiver baseband output pins.

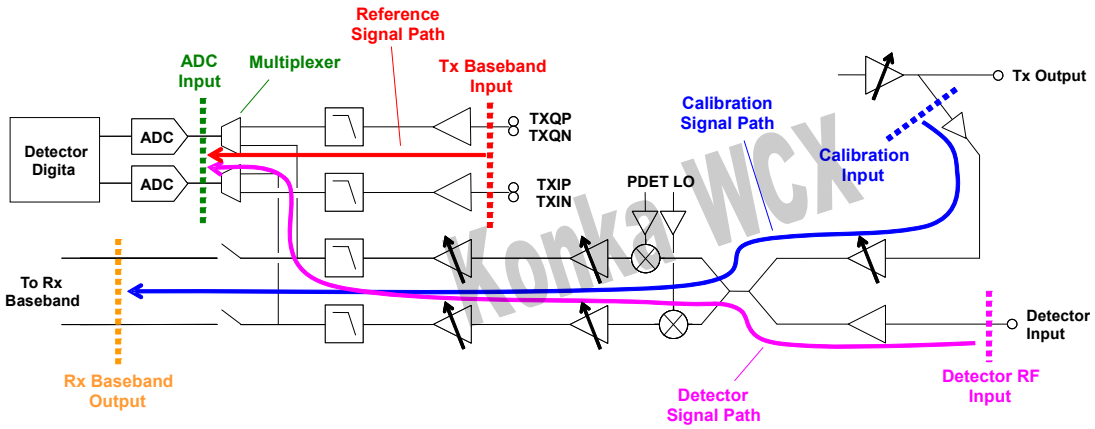

Figure 9: Power Detector Interface and Signal Path Definition

POWER MANAGEMENT

For optimum power efficiency the MT6162 operates from several external supplies some of which are intended to be supplied by linear regulation of the system supply/battery and some via a switched mode power supply. On chip regulation ensures that noise and switching transients on these supplies are rejected so a well conditioned internal supply network is available. The required supplies to the IC are specified in Table 18.

The internal supplies VSUP1-VSUP3 are those connected to external pins and require a decoupling capacitor to achieve the required noise and AC power supply rejection. These LDO's are described in more detail in Table 19 with the recommended component values.

FREQUENCY SYNTHESIS

The MT6162 contains two independent frequency synthesizers; one for Transmit and one for Receive. The principle of operation for both systems is essentially the same, although the respective VCOs are tuned for the appropriate TX or RX frequency bands. In GMSK Tx mode, the frequency synthesizer is operated in Direct-Frequency Modulation mode (DFM), with data being to the DFM engine over the serial port interface. The block diagram for Rx synthesizer is shown in Figure 10.

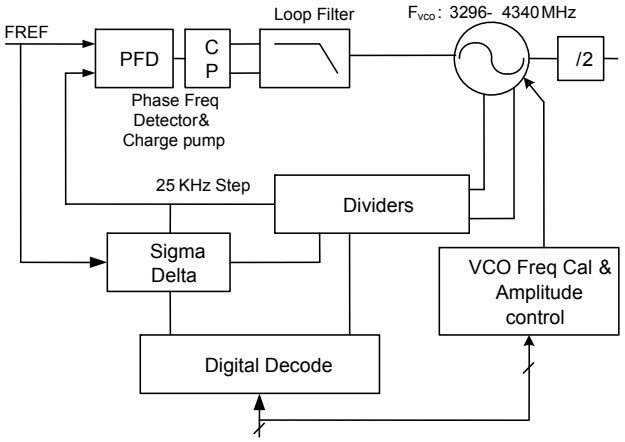

Figure 10: Frequency Synthesis Block Diagram (Receiver)

All the components are fully integrated for both TX and RX, including dividers, VCOs, respective tank components, and loop filters. The VCOs have a wide tuning range, necessary to cover all the major 3GPP bands. The VCOs run at 2x the high frequency band and 4x the low band frequency. This minimizes VCO leakage power at the wanted frequency, and tuning range requirements of the VCO. The design incorporates both frequency and amplitude calibration to ensure the oscillator is always operating with its optimum performance. The calibrations occur during the PLL lock time and are fully self-contained requiring no user inputs. VCOs are configurable for both GGE & 3G requirements. The on-chip nature of all the components allow for optimum matching conditions, and minimal power consumption for the entire system. Careful layout and VCO shielding techniques are used to minimize any unwanted coupling effects. The dividers employ advanced design techniques to achieve very low power in operation translating to an extended standby time of the handset.

For a high performance loop, the MT6162 PLLs implement fractional-n architectures, with a high comparison frequency used in the Phase Frequency Detector (PFD). This gives the advantages of faster lock time and lower in-band noise floor. The fractional-N functionality is implemented with a 3rd order Sigma Delta modulator which is designed for low current operation. The Phase Frequency Detector (PFD), Charge pump and loop filter are internally trimmed to remove variations associated with process and frequency. This process is fully automated on-chip.

The Synthesizer programming fractional and integer words is via the standard serial interface with separate registers for TX & RX. The channel resolution is 3Hz and 25kHz for Tx and Rx synthesizers, respectively.

Reference Path

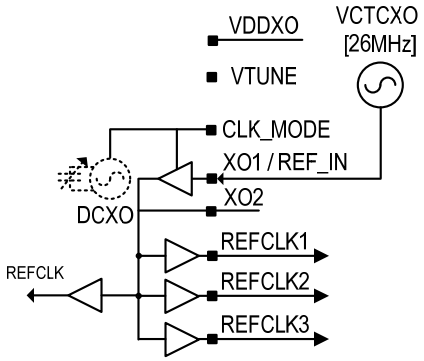

Figure 11: Reference Path

The MT6162 requires the standard frequency of 26 MHz as a reference input. Either this can be from an external VCTCXO, or on-chip DCXO circuit with AFC tuning and external crystal oscillator. The 26 MHz is internally buffered and distributed to the respective blocks, such as the synthesizer PFDs. The MT6162 provides three buffered outputs; one of them will go mainly to the digital baseband on-chip PLL system use to generate the clocks for Rx ADCs and Tx DACs. The additional buffers are available for driving auxiliary IC's such as connectivity solutions. The output buffers can be disabled via the serial interface.

Supply	Usage	Regulator Type	Voltage	Voltage Tolerance	Iave / Imax
VINT	Serial interface control logic	Switching	1.8V	±125mV	6mA/10mA
VDDXO	Regulated supply for VCXO/DCXO	Linear	2.8V	±100mV	3.5mA/5mA
VDD_18	Regulated Supply for IC	Switching	1.825V	±75mV	100mA/140mA
VDD_28a/b	Regulated supply for IC	Linear	2.85V	±100mV	53mA/85mA

VDD_28a and VDD_28b should be shorted together on the PCB (there is no internal connection)

Table 18 Power Supply Configuration

Supply	Usage	Connection	Nom O/P Voltage
VSUP1	Receiver Supply (low noise blocks) Regulated from VDD_18	External Decoupling Capacitor Cnom=1µF	1.65V
VSUP2a/ b	Transmitter Supply (low noise blocks). Regulated from VDD_18	External Decoupling Capacitor Cnom=1µF	1.65V
VSUP3	Transmit SupplyRegulated from VDD_28a/b	External Decoupling Capacitor Cnom=1µF	2.5V

VSUP2a and VSUP2b should be shorted together on the PCB (there is no internal connection)

Table 19 Internal Supplies Configuration

SERIAL INTERFACE

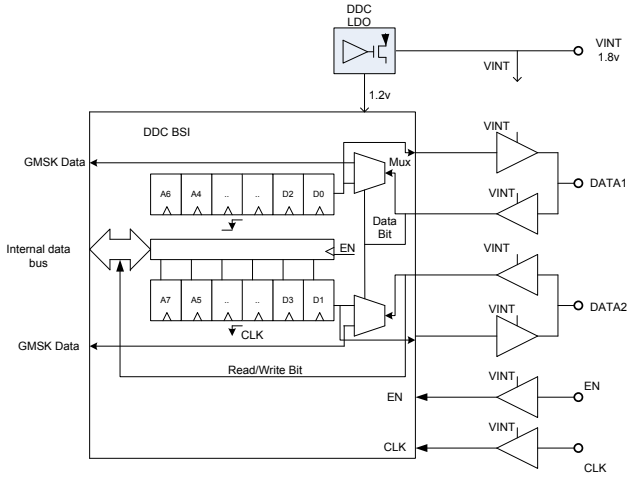

Figure 12. Serial Interface

The MT6162 uses a 4-wire bidirectional interface (BSI) for all communications with the baseband processor: writing control words, sending data to the DFM engine and reading back from the power detector. The serial interface contains four lines: Clock (CLK), two Bidirectional data (DATA1 & DATA2), and an active high chip select (EN) lines. The serial interface supports both write and read access protocols. Hardware details are described in the data sheet.

The types of words supported are:

a) Write (Control)
b) Read including Read request
c) DFM word (GMSK Data)

Serial port Write Control words are a fixed length of 30 bits over two data lines. The first 2 bits are mode selection for the BSI; The next 8 bits are address and the final 20 bits are data. DFM Data only contains 2 mode and 14 data bits; no address bits are required (Figure 5). DATA is sampled on the rising edge of CLK. The MSB of write and read words are transferred first; LSB last. The Read data is transferred out on the falling edge of the BSI clock.

The MT6162 Mode word formats are shown in Table 20:

Data	Read	Type of word
0	0	BSI Write word
0	1	BSI Read word
1	0	DFM (GMSK Data)

Table 20: Word Formats for MT6162 Serial Interface

APPLICATIONS

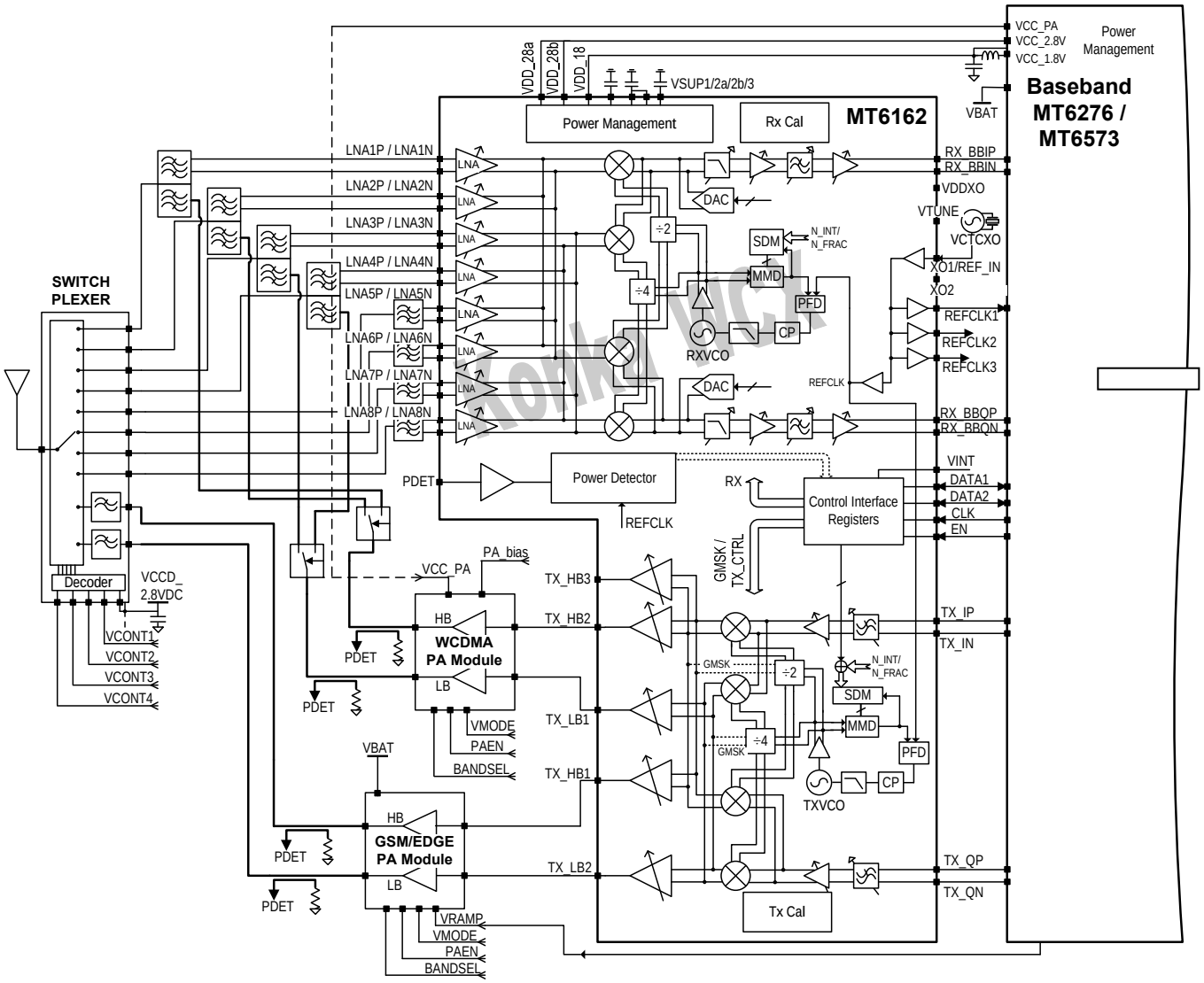

Figure 13: Multi-Band Multi-Mode Platform.

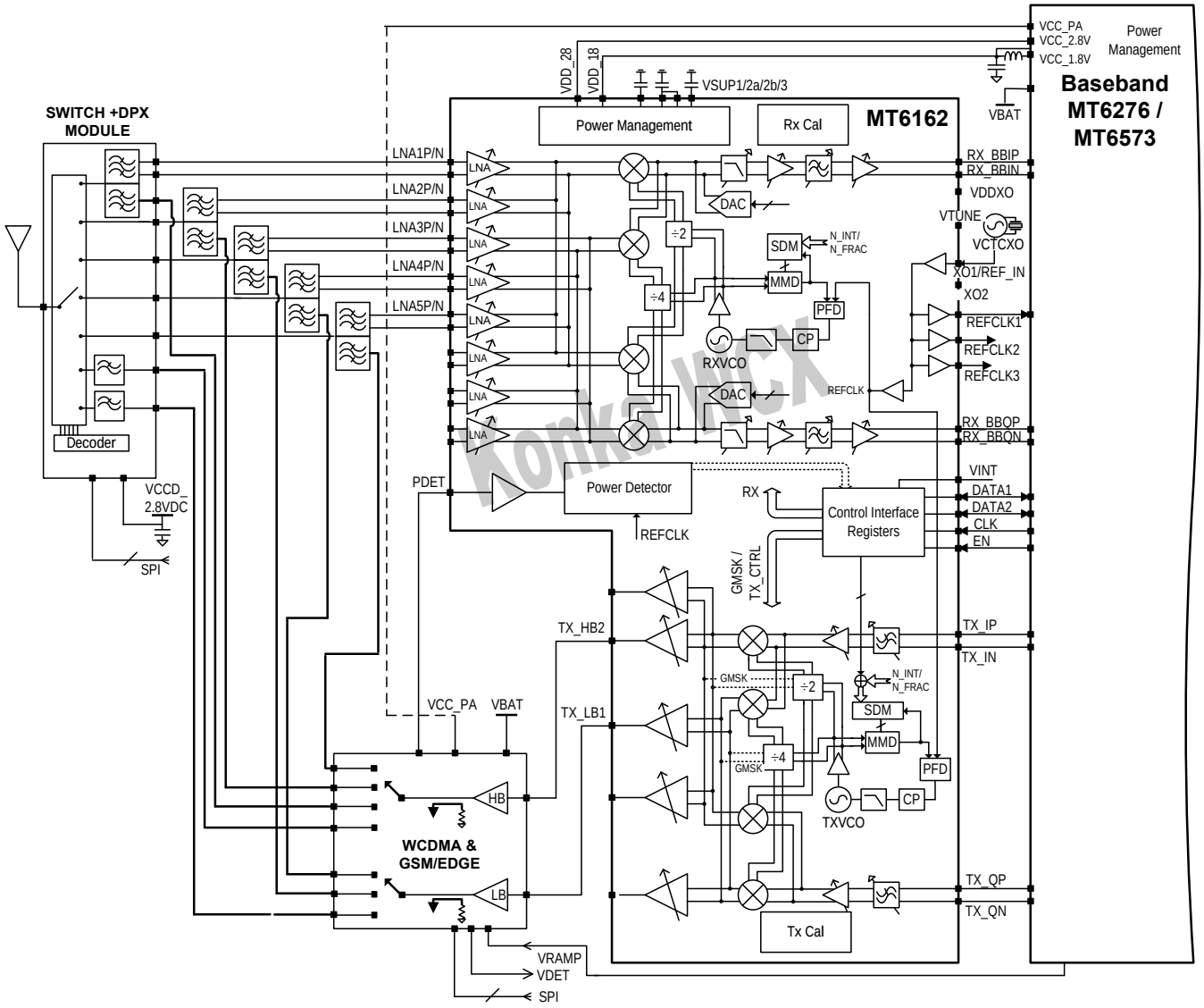

Figure 14: Multi-Band Multi-Mode platform, with MMMB PA configuration.

OUTLINE DIMENSIONS

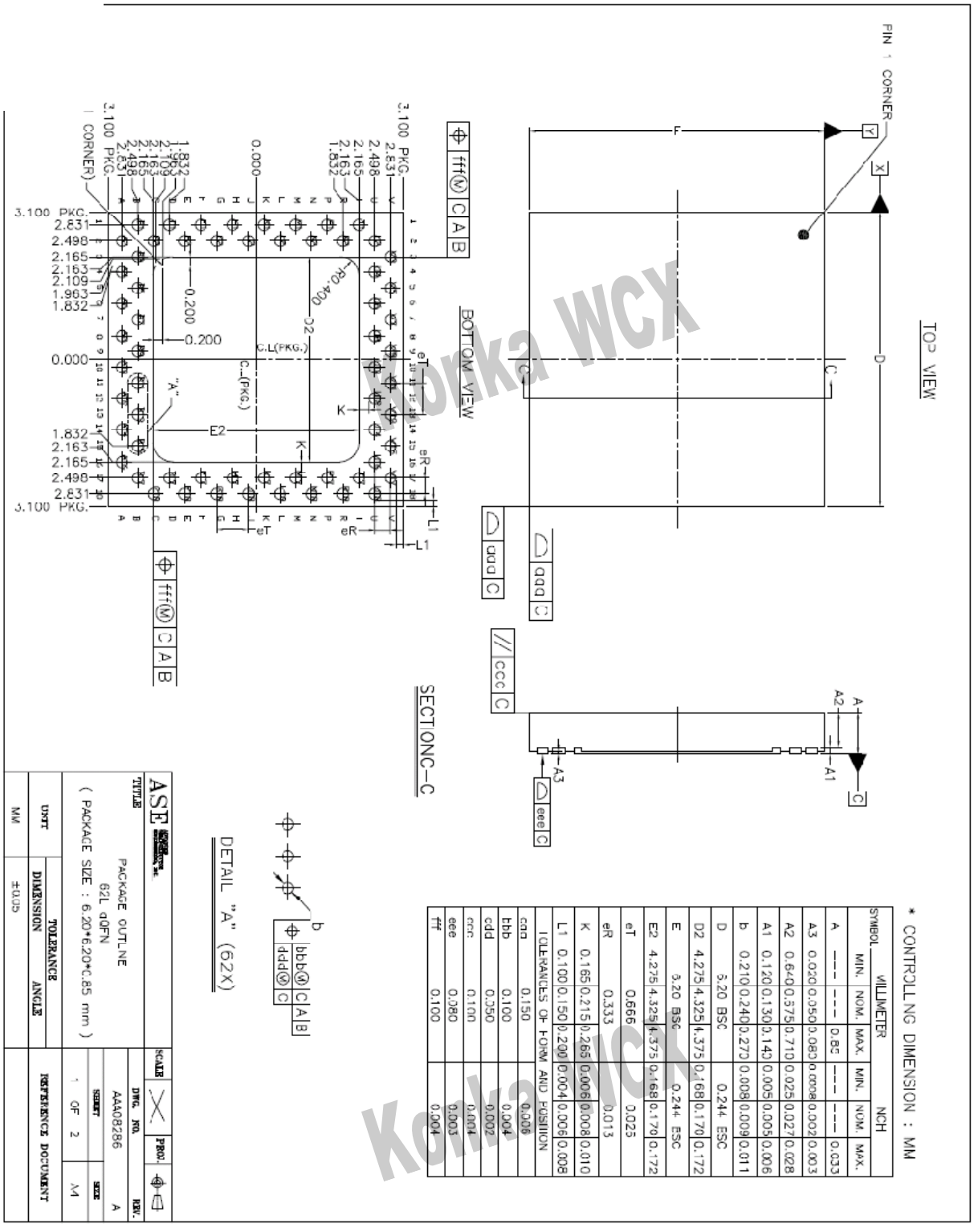

Figure 15.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
MT6162	-30 ºC to +85 ºC	aQFN (6.2x6.2mm^2)	-L Lead Free

REVISION HISTORY

Revision	Date	Silicon	Description
Pro – 1.0	12th Oct 2009	Rev 0.x	Initial review Document.
Pro – 1.1	June 02, 2010		- Based on 'Othello_H_Test_List-Ver1.1.xls - Taking into account feedback from TM on v1.0 document
Pro – 1.2	Sept 30th, 2010		Sept. 30th datasheet review
Pro – 1.3	Feb 14th, 2011	ES2	To be released to customers
Pro-1.4	Mar 17th, 2011	ES2	Corrected POD (Package Outline drawing)
Pro-1.5	Mar 20th, 2011	ES2	Removed unwanted references