MT6166 RF System Technical Brief

Version:	0.1
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Editor:	Chih-Chun Tang

1 Introduction

1.1 Overview

The MT6166 is a RF transceiver targeted at high speed 2G/3G-FDD/TDD multi-mode smart phone and tablet computers implanted in 40nm CMOS. The RF transceiver function is fully integrated. This document briefly introduces the RF macros in MT6166.

1.2 Key features

- Full multi-mode RF solution (GGE/WCDMA/TDSCDMA) through to 3GPP Release 8 (HSPA+)
  - *21.1Mbps peak DL (Cat. 24: 64QAM)*
  - *11.5Mbps peak UL (Cat. 7: 16QAM)*
  - *SAW-less Quad-band support in GGE mode (GSM850/900/1800/1900)*
  - *3G-FDD bands support: Band 1,2,5,8.*
  - *3G-TDSCDMA bands support: Band 34,39,40.*

- Direct Conversion (3G), Two Point Modulation (TPM) for GMSK and Small Signal Polar for 8-PSK
  - No external SAW filters required for transmitter (WCDMA//GGE)
  - Dedicated power detection circuits for power control over specific power range

- Hybrid Direct-Conversion (3G) / Low-IF (GGE, DC-HSDPA) receiver
  - *No external SAW filters required for receiver (GGE)*

- Low supply current & operation directly from DC-DC converter

- 26MHz internal DCXO or external VCTCXO operation (with integrated AFC DAC)
  - Three low noise additional Clock Drivers for clocking connectivity / peripheral IC's
  - Ultra Low power 32KHz mode

- Support RF Calibration features for key Rx and Tx specifications (Image rejection, LO feedthrough, DC offset)

- Temperature Measurement sub-system

2 Block Diagram and Application Diagram

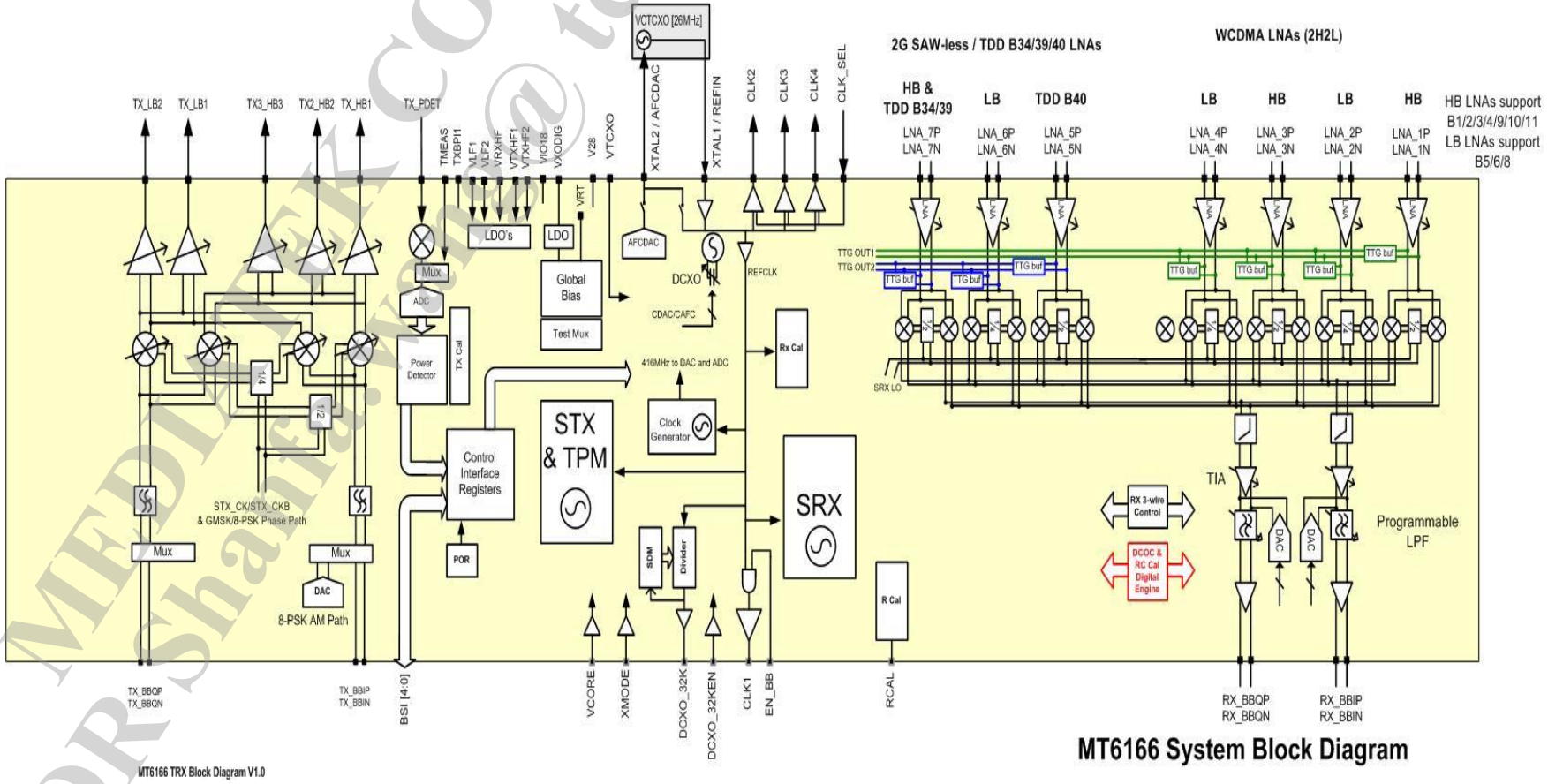


Figure 1: RFSYS Block Diagram

MT6166 System Block Diagram

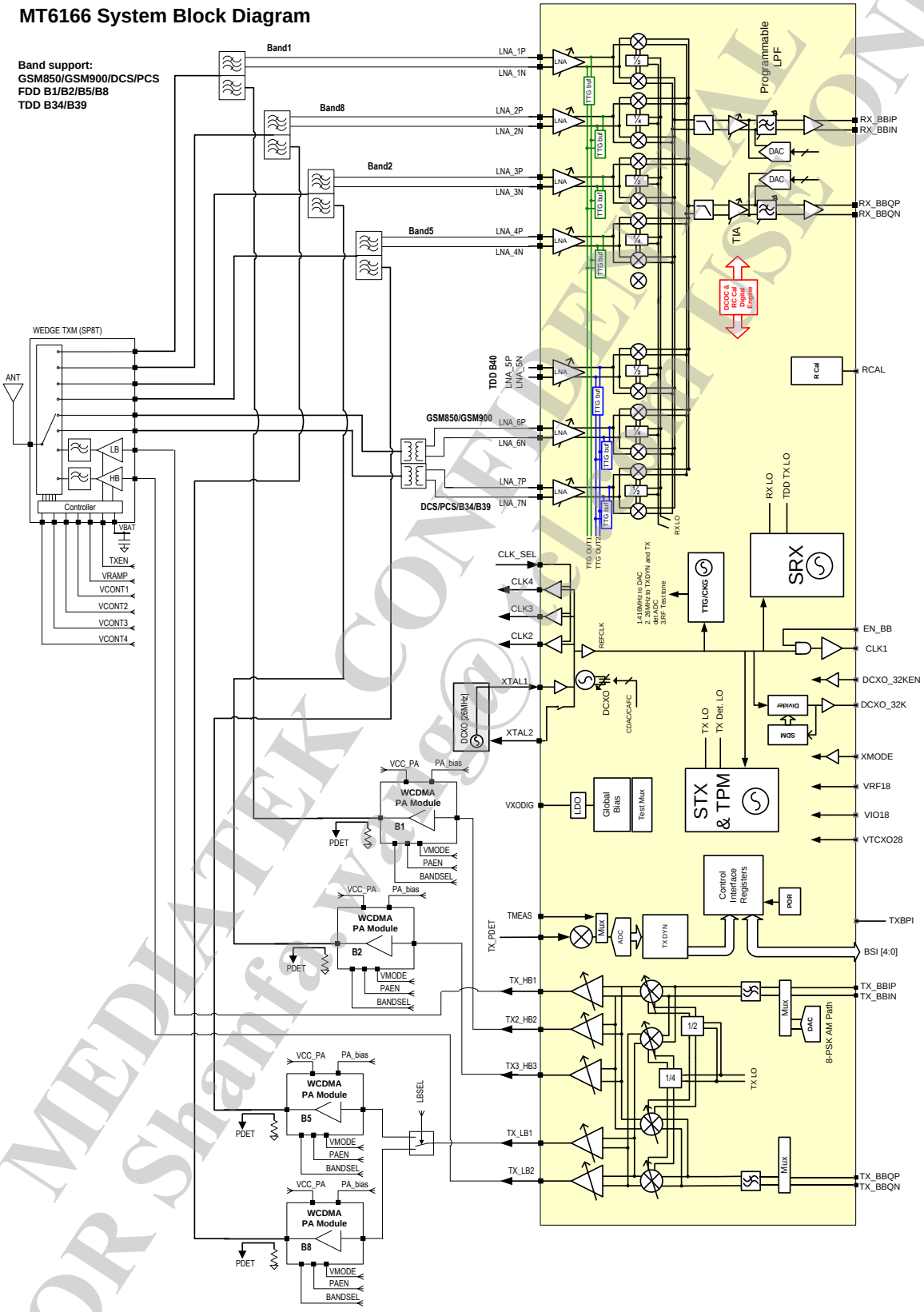


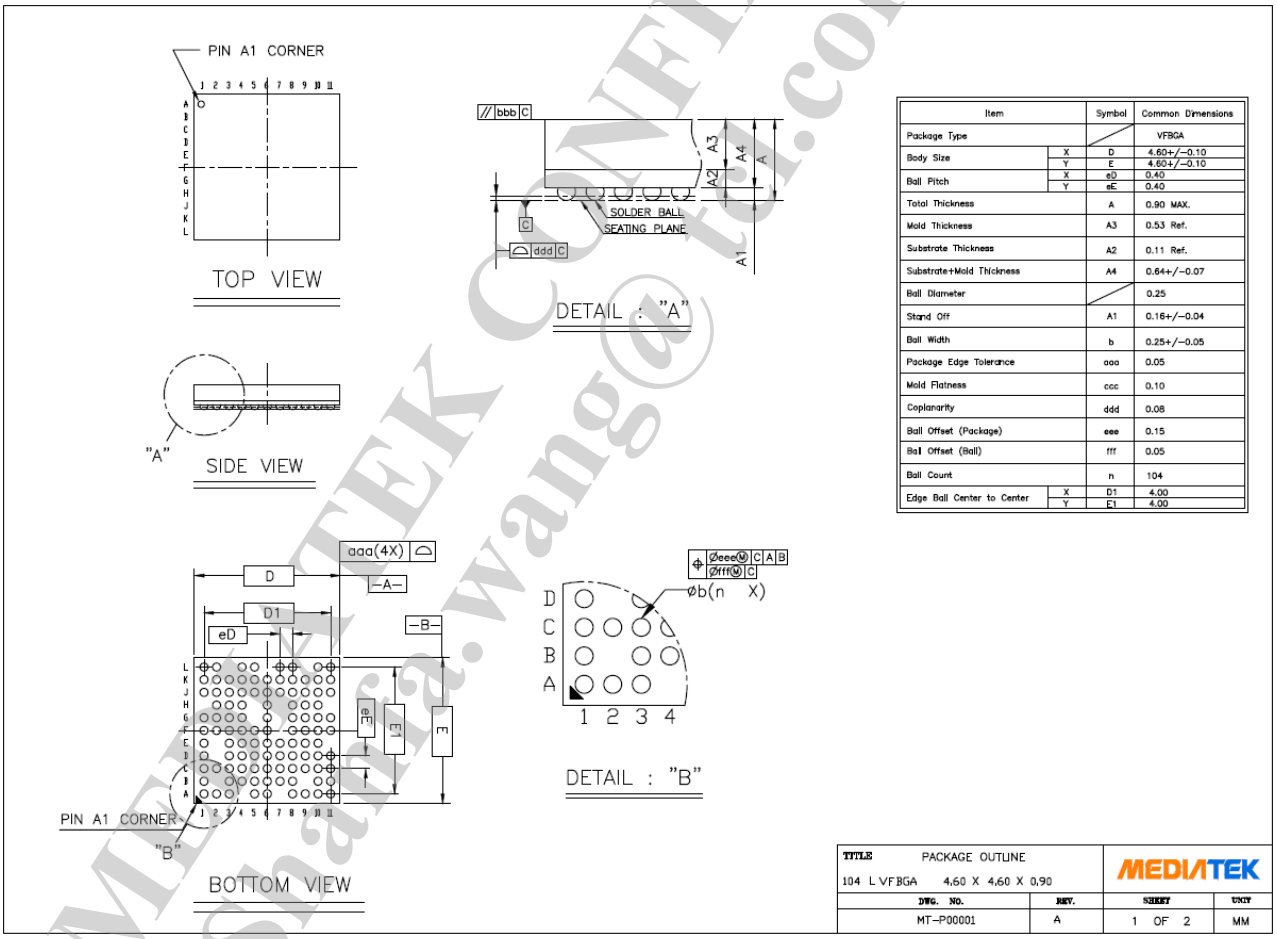
Figure 2 : Applications Diagram

3 General Specifications

3.1 Packaging

Wirebond TFBGA is currently considered for this product.

Parameter	Single die
Die thickness	6mil
Bond Wire Diameter [Cu]	0.7mil
Body Size	4.6x4.6mm
Ball Spacing	0.4mm
Ball number	11x11



Item		Symbol	Common Dimensions
Package Type			VFBGA
Body Size	X	D	4.60+/-0.10
	Y	E	4.60+/-0.10
Ball Pitch	X	eD	0.40
	Y	eE	0.40
Total Thickness		A	0.90 MAX.
Mold Thickness		A3	0.53 Ref.
Substrate Thickness		A2	0.11 Ref.
Substrate+Mold Thickness		A4	0.64+/-0.07
Ball Diameter			0.25
Stand Off		A1	0.16+/-0.04
Ball Width		b	0.25+/-0.05
Package Edge Tolerance		aaa	0.05
Mold Flatness		ccc	0.10
Coplanarity		ddd	0.08
Ball Offset (Package)		eee	0.15
Ball Offset (Ball)		fff	0.05
Ball Count		n	104
Edge Ball Center to Center	X	D1	4.00
	Y	E1	4.00

3.2 RF I/O List

Category	Ball Name			Description
	Name	I/O	GPIO/RF Pin	
RF I/O	HB_RXP	I	RF	2G RX HB/TDD B34/39 input
	HB_RXN	I	RF	2G RX HB/TDD B34/39 input
	LB_RXP	I	RF	2G RX LB input
	LB_RXN	I	RF	2G RX LB input
	RFIN_B1	I	RF	3G band 1 RX input
	RFIP_B1	I	RF	3G band 1 RX input
	RFIN_B5	I	RF	3G band 5 RX input
	RFIP_B5	I	RF	3G band 5 RX input
	RFIN_B2	I	RF	3G band 2 RX input
	RFIP_B2	I	RF	3G band 2 RX input
	RFIN_B8	I	RF	3G band 8 RX input
	RFIP_B8	I	RF	3G band 8 RX input
	B40_RXP	I	RF	TDSCDMA Band 40 RX input
	B40_RXN	I	RF	TDSCDMA Band 40 RX input
	2GHB_TX	O	RF	2G HB TX output
	3GH1_TX	O	RF	3G HB TX output 1
	3GH2_TX	O	RF	3G HB TX output 2
	3GL5_TX	O	RF	3G LB TX output
	2GLB_TX	O	RF	2G LB TX output
	DET	I	RF	TX detection path input
BB I/O	3GTX_IP	I	RF	TX I+ input from 3G DAC
	3GTX_IN	I	RF	TX I- input from 3G DAC
	3GTX_QP	I	RF	TX Q+ input from 3G DAC
	3GTX_QN	I	RF	TX Q- input from 3G DAC
	RX_IP	O	RF	RX I+ ouput to 2G/3G ADC
	RX_IN	O	RF	RX I- ouput to 2G/3G ADC
	RX_QP	O	RF	RX Q+ ouput to 2G/3G ADC
	RX_QN	O	RF	RX Q- ouput to 2G/3G ADC
	TMEAS	I	RF	External temperature measurement input
	TXBPI	O	GPIO	3G TX DCOC sign bit
BSI Interface	BSI_CLK/SCAN_CLK	I	GPIO	3-wire CLK / ATPG CLK
	BSI_EN/SCAN_EN	I	GPIO	3-wire enable / ATPG enable

	BSI_DATA0/SCAN_IN	IO	GPIO	3-wire data/2G data / ATPG input
	BSI_DATA1/SCAN_OUT	IO	GPIO	3-wire data/2G data / ATPG output
	BSI_DATA2	IO	GPIO	3-wire data/2G data
TCVCXO/DCXO	XTAL1	I	RF	XO input
	XTAL2/AFCDAC	IO	RF	XO input or AFCDAC voltage output
	XO4	O	RF	26MHz output clock 4 (PMIC/Audio)
	XO3	O	RF	Sine-26MHz output clock 3 (ATV/NFC)
	XO2	O	RF	26MHz output clock 2 (CON)
	XO1	O	RF	26MHz output clock 1 (BB/AP)
	XMODE	I	RF	DCXO(=1)/VCTCXO(=0) selection.
	CLK_SEL	I	RF	XO output buffer (for co-clock) enable
	32K_EN	I	RF	32KHz function enable (with 32KHz XO, EN=0; without 32KHz XO, EN=1)
	OUT32K	O	RF	32KHz output
	EN_BB	I	RF	Enable 26MHz clock buffer to DBB. Also to be the enable of global static macro.
Test / RCAL Ports	TST1	O	RF	Test output 1
	TST2	O	RF	Test output 2
	RCAL	O	RF	R-calibration
VCO Mon	RXVCO_MON	O	RF	Monitor port for RFVCO.
	TXVCO_MON	O	RF	Monitor port for TX VCO.
Voltage Supply /GND	DETGND	GND	RF	For TX Pdet GND (50-ohm R GND)
	VRXHF	VDD	RF	1.8V RX power supply1 (VRF18)
	AVDD_VIO18	VDD	RF	1.8V DC-DC power supply (=VGPIO, only for GPIO supply)
	VXODIG	VDD	RF	For DCXO digital and GS supply, connect to VTCXO28 with 32k-removal, connect to VIO18 for normal operation. (=VIO18 in original plan)
	VTCXO28	VDD	RF	2.8V LDO XO power supply and

				BG
	VRXLF	VDD	RF	1.8V RX power supply2 (VRF18) and TTG/CKG
	VTXLF	VDD	RF	1.8V TX power supply 2 (VRF18)
	VTXHF	VDD	RF	1.8V TX power supply 1 (VRF18)
	V28	VDD	RF	For ESD and TX some blocks supply

3.3 Ball Assignment

	1	2	3	4	5	6	7	8	9	10	11	
A	B40_RXP	3GB1_RXP	3GB1_RXN		3GB2_RXP	3GB8_RXP		3GH1_TX	3GH2_TX	3GL5_TX	2GLB_TX	A
B	B40_RXN		3GB5_RXP	3GB5_RXN	3GB2_RXN	3GB8_RXN	GND	2GHB_TX		GND	VTXHF	B
C	LB_RXP	GND	GND	GND	GND	GND	GND	GND	GND	GND	TMEAS	C
D	LB_RXN		GND	GND	GND	GND	GND	GND	GND	DETGND	DET	D
E	HB_RXP		GND	GND	GND	GND	GND	GND	GND	V28		E
F	HB_RXN	VRXHF	GND	GND	GND	GND		BSI_DATA0	GND	3GTX_QP	3GTX_QN	F
G	32K_EN	RFVCO_MON	GND	GND		BSI_EN		BSI_DATA2	GND	3GTX_IP	3GTX_IN	G
H		XTAL2	GND	GND		BSI_CLK		BSI_DATA1	GND	TXBPI		H
J	XTAL1	GND	GND	GND	GND	GND	GND	GND	GND	RCAL	VTXLF	J
K	VTCXO28	CLK_SEL	XO2	XO4	OUT32K	AVDD_VIO18	VXODIG	RX_IN	RX_QN	RX_QP	TST2	K
L	EN_BB	XO3		XO1	XMODE		VRXLF	RX_IP		TST1	TXVCO_MON	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 3 Bond Out

3.4 Operating Conditions

Within the operating range the IC operates as per the functional description.

Parameter	Conditions	Min	Nom	Max	Unit
Supply VIO18	Normal functional modes	1.7	1.8	1.9	V
Linear Supply VTCXO28		2.7	2.8	2.9	V
Supply VXODIG	Normal function mode	Connects to VIO18			
Supply VXODIG	32K-less mode	Connects to VTCXO28			
Supply VXODIG	ATPG mode – LDO's bypassed in this mode	1.1	1.2	1.4	V
Ambient Temperature	Note 1	-40		85	ºC
Junction Temperature	Functional – see section [3.9]	-40		125	ºC
Receiver Front End					
RX input frequency range	See Receiver Section for detailed frequency ranges				
Rx required amplitude balance	All Rx input pairs	-1		+1	dB
Rx required phase balance	All Rx input pairs	-10		+10	deg
Transmitter					
Tx Frequency Range	See Transmitter Section for detailed frequency ranges				
Tx O/P VSWR	All Phases ZL = 50Ω			2:1	
Reference Clock Input (VCTCXO)					
Reference Clock Frequency			26.0		MHz
Reference Clock Input Voltage Swing	AC coupled at input pin	700		1500	mVpp
Duty Cycle		40		60	%
Phase Noise – note 2	@ F_{offset} = 100Hz		<-103	-100	dBc/Hz
	@ F_{offset} = 1KHz		<-133	-130	dBc/Hz
	@ F_{offset} = 10KHz		<-147	-144	dBc/Hz
	@ F_{offset} = 100KHz		<-149	-146	dBc/Hz
Harmonic Content	HD2 @ 52MHz			-8	dBc
	HD3 @ 78MHz			-10	dBc
	HD4 @ 104MHz			-20	dBc
Start-up time	|Δf|<1ppm to >90% of final amplitude			3	ms
Crystal Requirements					

2 Crystal types are supported (Crystal #1 3225 body size / Crystal #2 2520 body size)					
Nominal Load Capacitance	Crystal #1		7.5		pF
	Crystal #2		7.0		pF
Initial Frequency error				±10	Ppm
ESR				30	Ω
Drive level				100	μW
Pull ability	Crystal #1	-10%	32	+10%	ppm/pF
	Crystal #2	-10%	27	+10%	ppm/pF

Note 1

The supportable ambient temperature range will depend on the thermal impedance of the package used and the exact operational state as well as the end application thermal design (housing, PCB etc).

Junction temperature is a more reliable indication of the actual operational range.

Note 2

The input clock requirement specified is defined to meet receiver and transmitter phase noise requirements e.g. IC EVM specification. Certain connectivity requirements may require better specifications than this. The clock source (non DCXO mode) can either be an external VCTCXO/VCXO module or alternatively another transceiver clock buffer when considering multiple transceiver applications.

n

4 Reference Clock Specification

The Reference Clock sub-system is shown in the figure below.

This integrates a core 26MHz XTAL oscillator (DCXO), AFCDAC and a 32KHz low power mode. Also all the clock buffers external and internal are integrated in this system.

The mode of operation (internal DCXO or external VCTCXO) is selected via the input XMODE from the baseband with the following function

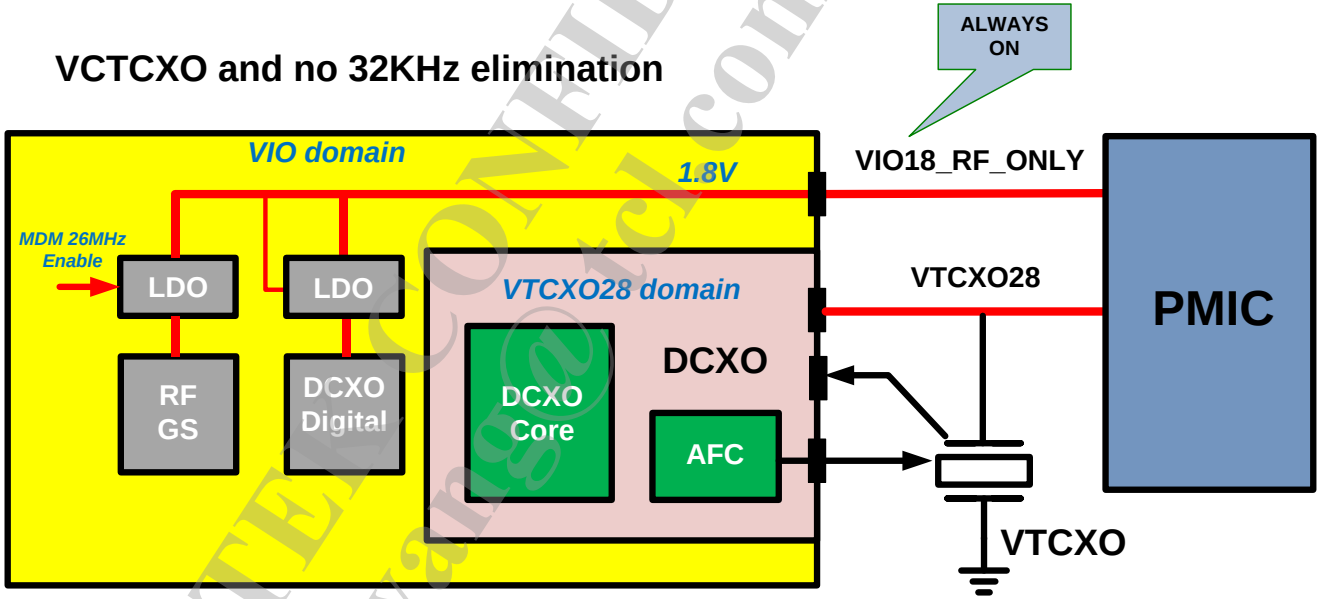
CLK_MODE	Mode
LOW	External CLK (VCTCXO)
HIGH	DCXO

In Crystal mode the XTAL is connected directly between XO1 and XO2.

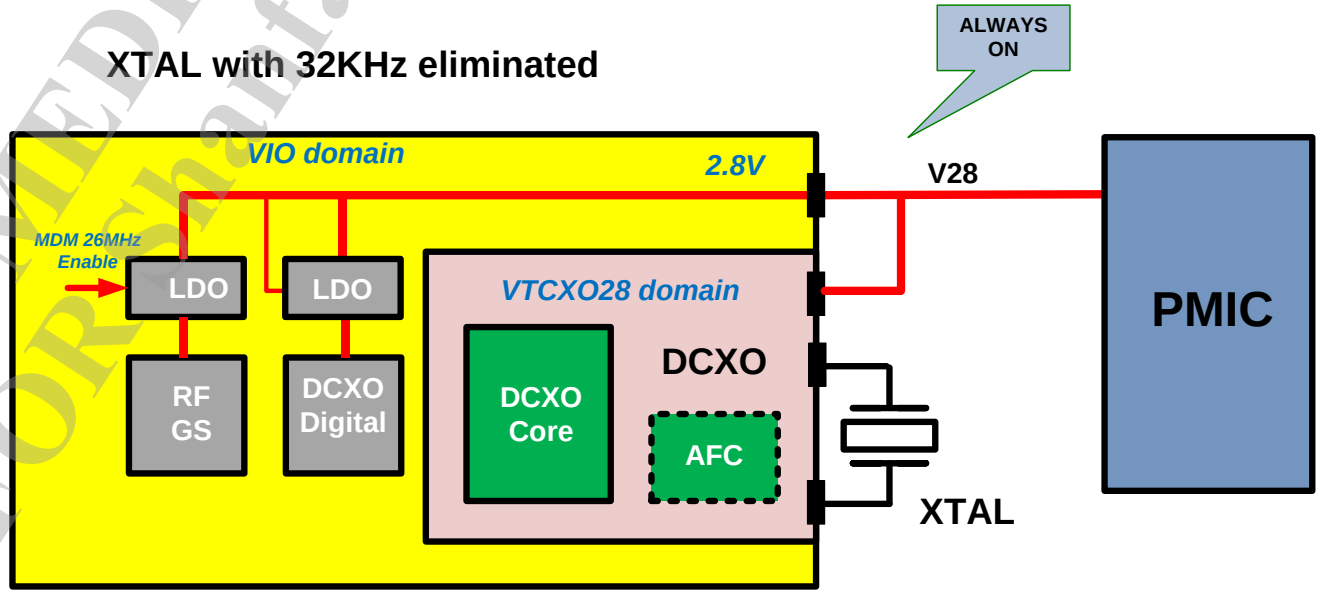
In VCTCXO mode XO2 pin is reconfigured to be the AFCDAC output and XO1 the VCTCXO clock input pin.

Since the state of XMODE is latched into the module then the baseband configuration can take place using a pin state “trapping” scheme on power up if desired.

VCTCXO and no 32KHz elimination



XTAL with 32KHz eliminated



4.1 External Clock Buffers

Our plan for 26MHz external clock buffer are
CLK1 – to Baseband
CLK2 – to WCN
CLK3 – ATV/NFC
CLK4 – Audio

Following is MT6166 DCXO control table.

Case	XMODE	DCXO32K_EN	CLK_SEL	EN_26M_BB	32K Clk out	CLK1 (MD/AP)	CLK2 (WCN)	CLK3 (ATV)	CLK4 (Audio)	Condition
1	0	X , no 32k less	0	0	Off	Off	Off	Off	Off	VCTCXO mode
2	0	X , no 32k less	0	1	Off	26M out	Off	Off	Off	
3	0	X , no 32k less	1	0	Off	Off	26M out	26M out	26M out	
4	0	X , no 32k less	1	1	Off	26M out	26M out	26M out	26M out	
5	1	0	0	0	Off	Off	Off	Off	Off	DCXO/OFF
6	1	0	0	1	Off	26M out	Off	Off	Off	DCXO/HPM#1
7	1	0	1	0	Off	Off	26M out	26M out	26M out	DCXO/HPM#1
8	1	0	1	1	Off	26M out	26M out	26M out	26M out	DCXO/HPM#1
9	1	1	0	0	On	Off	Off	Off	Off	DCXO/LPM
10	1	1	0	1	On	26M out	Off	Off	Off	DCXO/HPM
11	1	1	1	0	On	Off	26M out	26M out	26M out	DCXO/HPM
12	1	1	1	1	On	26M out	26M out	26M out	26M out	DCXO/HPM

4.2 32KHz Mode

In low power mode a 32KHz clock is produced by using a fractional-N divider (1st order Sigma Delta Modulated) to replace the normal 32KHz XTAL (watchdog). In this mode the CDAC and CAFC capacitance is minimized so that the XTAL core can operate from a significantly reduced bias current).

4.3 Reference Clock Supply Current

The DCXO clock system has a large number of modes. The approximate current breakdown is shown below for typical conditions. This does not include the AFCDAC for VCTCXO mode.

Mode	Current Breakdown	Total Current
LPM (Low Power Mode) for 32KHz operation	100µA	100µA
FPM (Full Power Mode) for 26MHz operation including baseband clock buffer	1mA	1mA
Delta current for Global Static Clock Buffer	75µA	75µA
Delta Current TTG Clock Buffer	100µA	100µA
Delta Current CLKG Clock Buffer	225µA	225µA
Delta Current STX Clock Buffer	225µA	225µA
Delta Current SRX Clock Buffer	250µA	250µA
Total Current FPM+CLKG+STX+SRX	1mA+0.225mA+0.225mA+0.25mA	1.7mA
External Clock Buffer Cload=20pF	1mA	1mA
FPM + 3x external clock buffer + CLKG+STX+SRX+TTG+GS	1mA+0.225mA+0.225mA+0.075mA +0.1mA+0.25mA+3mA	4.875mA

5 High Frequency Clock Generation

5.1 Clock Generator (CLKG)

This is an integer-N PLL that generates the 416MHz clocks for The TX DAC and Rx ADC. This operates at 26MHz (16x26MHz=416MHz) and as well as the 416MHz clocks certain 26MHz clocks are produced for synchronization e.g. TX Dynamic clock 26MHz from the feedback path so as to be synchronized to the 416MHz clocks. Also the 26MHz clock for the Tx ADC (power detector) is produced from this block.

5.2 Calibration Test Tone Generator (TTG)

This is a PLL used to generate a test tone for certain calibration modes.

1. Feedback to receiver inputs for image rejection calibration
2. Feedback to power detector pin (PDET) to us as a calibration tone for receiver gain calibration

6 Transmitter

Transmitter consists of 5 output ports. TX_LB2 and TX_HB1 ports are multi-mode ports which can support 2G or 3G depending on application circuits on the phone. Typ. maximum TX output power is >0dBm. Overall TX gain dynamic range is 78dB in RF and 8dB in BB. The power detection circuits are also included for better power accuracy over power region of PA gain mode change. In order to ensure power detection accuracy, the PCB trace to DET pin should not be put too close to TX output signal traces.

6.1 Tx Driver Mapping and Block Diagram

Tx Output Port Mapping

MT6166 TX Output Port Name	GSM850/900	FDD B5/B6/B8	Notes
3GL5_TX		✓	3G Path only
2GLB_TX	✓	✓	2G Path or 3G Path or Multimode Path

MT6166 TX Output Port Name	GSM1800/1900	FDD B1/B2/B3/B4 TDD B34/B39/B40	Notes
2GHB_TX	✓	✓	2G Path or 3G Path or Multimode Path or TDD Reuse Path
3GH1_TX		✓	3G FDD or TDD Path
3GH2_TX		✓	3G FDD or TDD Path

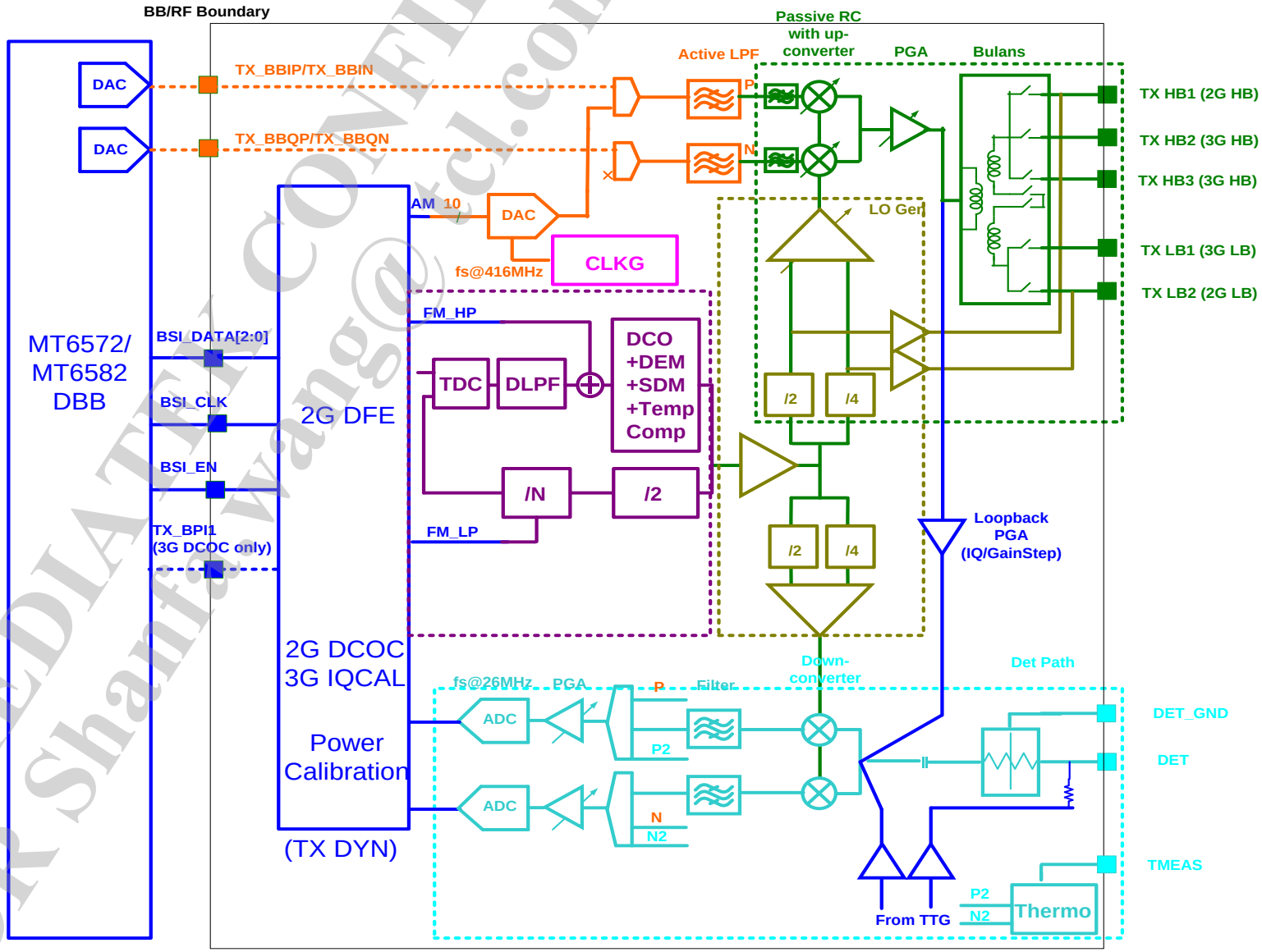
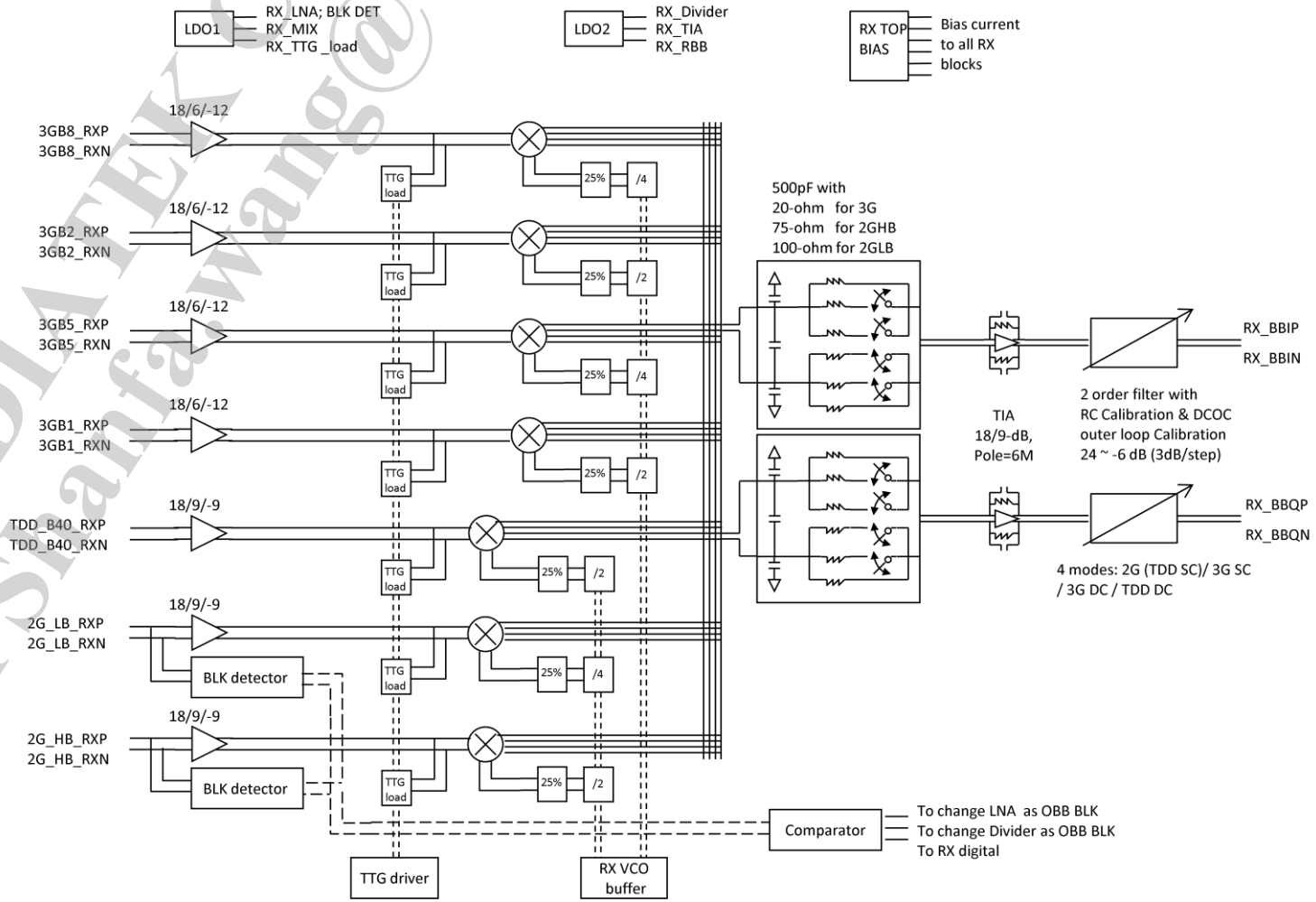


Figure 4 : Tx Block Diagram

7 Receiver Specification

The receiver circuits are all regulated by the internal LDOs.
The direct conversion/LIF receiver contains all active circuits for the complete receiver chain supporting single-cell (SC)/dual-cell (DC) 3G WCDMA, 3G TDSCDMA and 2G GSM/GPRS/EDGE (GGE) mode reception. The path contains a total of 7 LNAs (Low Noise Amplifier). The first 4 LNAs support 3G Band1/2/3/4/5/6/8/9; the fifth LNA supports TDD B40; the last 2 LNAs support GGE low band (GSM850/900) and GGE high band (DCS1800/PCS1900). GGE high band LNA also supports TDD B33/B34/B39.

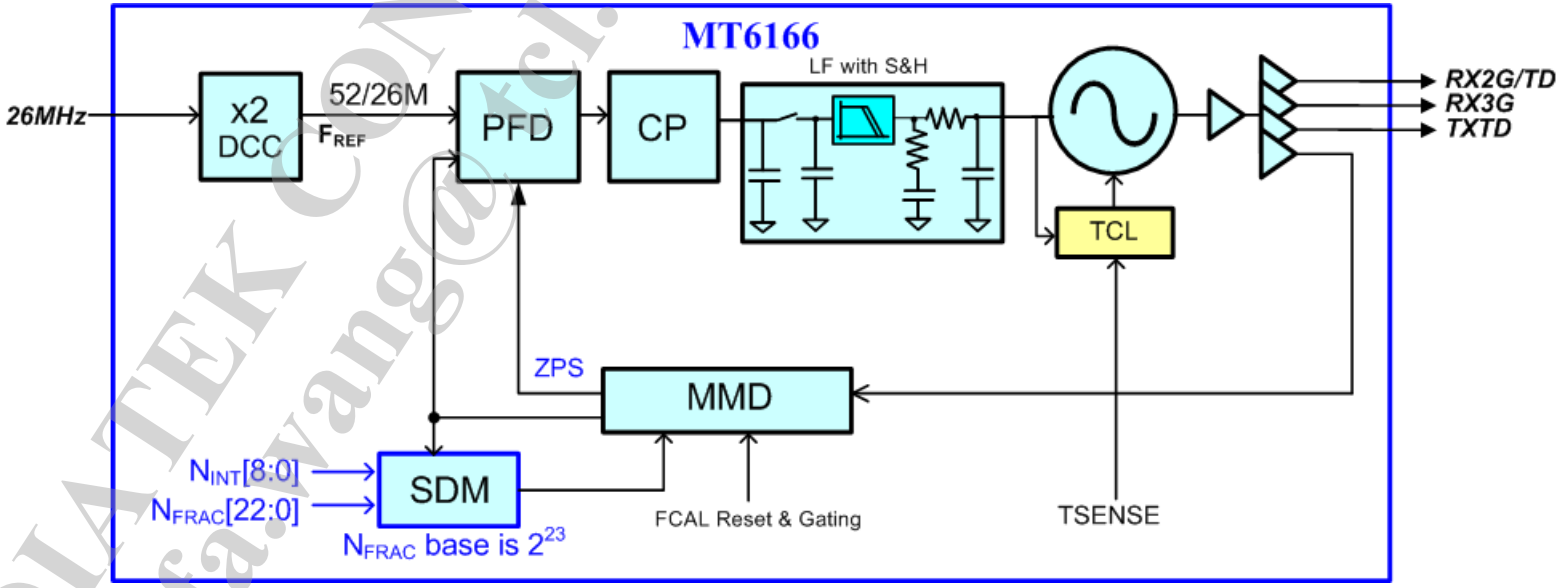


The receiver can also be used in platforms which support for dual-talk operations. In dual-talk applications, the first 4 LNAs also support TDD B33/B34 and 2G bands through co-banding. As listed in the table, there are 8 scenarios for single-talk and dual-talk applications. 3-wire control is used to choose one of these scenarios for normal operation.

			Sawless for single; Saw for dual			Duplexer			
Scenario	Mode	ST/DT	2G LB LNA	2G HB/ TDD B34&39 LNA	TDD B40 LNA	3G B1 LNA	3G B2 LNA	3G B5 LNA	3G B8 LNA
1	2G	single talk	GSM850/900 T1	DCS/PCS T1					
2	2G	dual talk 2G+2G	GSM850 T1_1	DCS T1_1			PCS T1_2		GSM900 T1_2
3	WCDMA	single talk	GSM850/900 T1	DCS/PCS T1		3G B1 T3	3G B2 T3	3G B5 T3	3G B8 T3
4	WCDMA	dual talk 2G+3G	GSM850 T1_1	DCS T1_1		3G B1 T3	3G B2 T3	3G B5 T3	GSM900 T1_2 3G B8 T3
5	TDSCDMA	single talk	GSM850/900 T1	DCS/PCS/TDD T1 B34&39 T2	TDD B40 T2				
6	TDSCDMA	dual talk 2G+TD	GSM850 T1_1	DCS T1_1 TDD B39 T2	TDD B40 T2	TDD B34 T2_1	PCS T1_2		GSM900 T1_2
7	WGT	single talk	GSM850/900 T1	DCS/PCS T1 TDD B34&39 T2	TDD B40 T2	3G B1 T3	3G B2 T3	3G B5 T3	3G B8 T3
8	WGT	dual talk Any one of the 2 combo 3G+2G, 2G+TD	GSM850 T1_1	DCS T1_1	TDD B40 T2	3G B1 T3	PCS T1_2 3G B2 T3	3G B5 T3	GSM900 T1_2 3G B8 T3

All LNAs have balanced inputs and are fully integrated. The quadrature LO signals are generated by a divide-by-2 divider for high band (HB) LNAs and a divide-by-4 divider for the low band (LB) LNAs. The RF signal is down converted by high/low band quadrature direct-down-conversion mixers. The analog baseband filter is a low pass filter with programmable transfer function and gain controls. Besides, it contains an RC-calibration circuit, and a DC Offset Cancellation circuit (DCOC). The low-pass filter is configured as a 2nd-order Butterworth filter for 3G FDD SC, 3G FDD DC, TDD DC and GGE modes. Receiver power ON/OFF sequence, LNA/band selection, total receiver gain including LNA, Mixer and analog baseband and DCOC timing are controlled by digital circuits. In addition, IQ calibration is done by injecting an offset frequency test tone generated by the test tone generator (TTG) into the RX mixer. Additional on-the-fly IQ imbalance tracking may be added in the DBB without changing the receiver design. The timing and control of this calibration scheme are also controlled by L1 software and digital circuitry.

8 Rx Synthesizer Specification



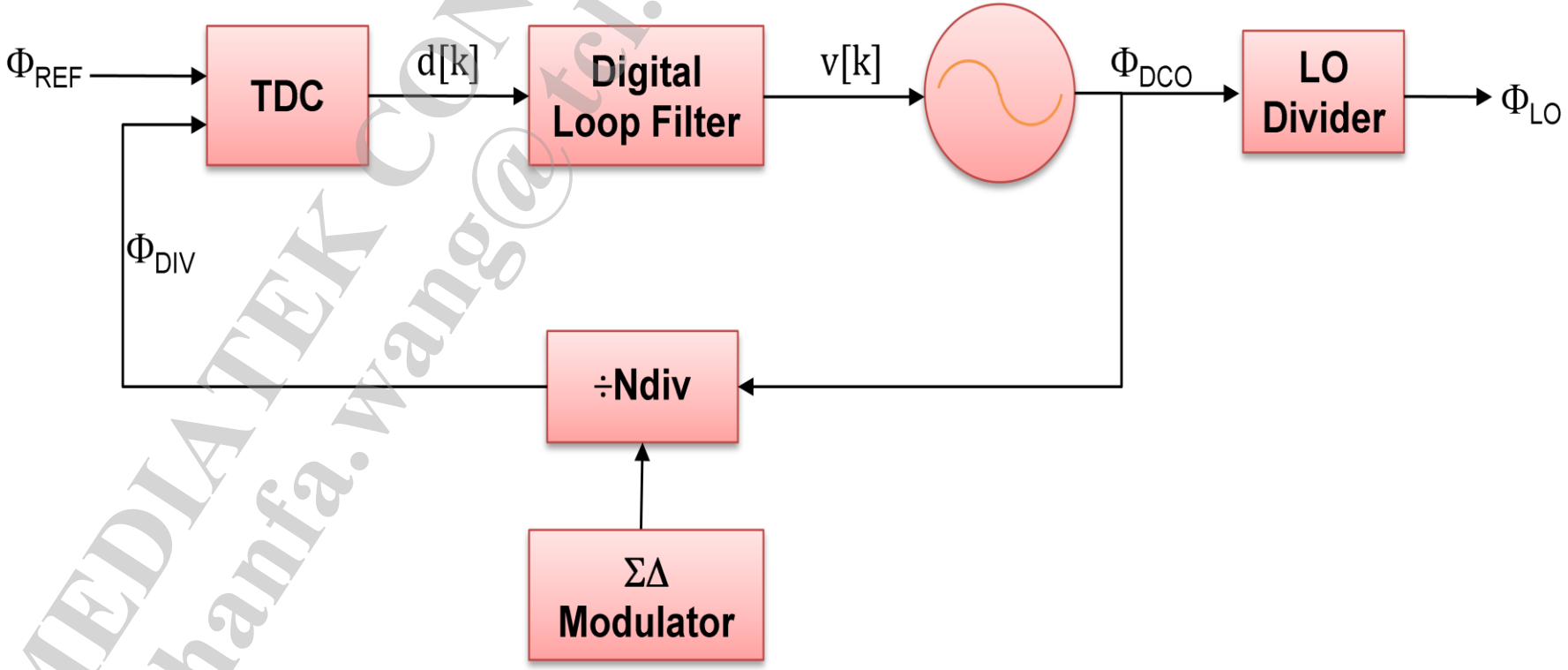
SRX uses analog PLL architecture.
Reference doubler is used to improve integrated phase noise (IPN). A fast duty-cycle calibration is used to correct 26M duty error.

FBDIV is simple MMD with zero-phase-start to speed up locking time.
A mash-I-I-I SDM with dithering is used to generate fractional part control MMD.

Multi-modes VCO include Temperature-Compensation-Loop (TCL) to against ~140° temperature drifting.

The SRX can generate 4xLO for 1GHz LB and 2xLO for 2GHz HB. It provides LO to 2G-RX, FDD-RX, TDD-T/RX.

9 Tx Synthesizer Specification



Above block diagram shows the TX synthesizer architecture. ADPLL architecture is used here for frequency modulation. It is similar to conventional PLL except charge pump is replaced by TDC and we used digital loop filter instead of analog one.

The ADPLL input clock is 26MHz and output clock is 2*LO (for TX HB) or 4*LO (for TX LB). As conventional PLL, a MESH 1-1-1 modulator is used for fractional part of frequency synthesis.

The TX synthesizer supports 2G TX GMSK/8PSK Phase modulation part and 3G FDD TX LO part and with temperature compensation loop to sustain ~140 degree temperature drift .

10 Digital Control Interfaces

10.1 Introduction

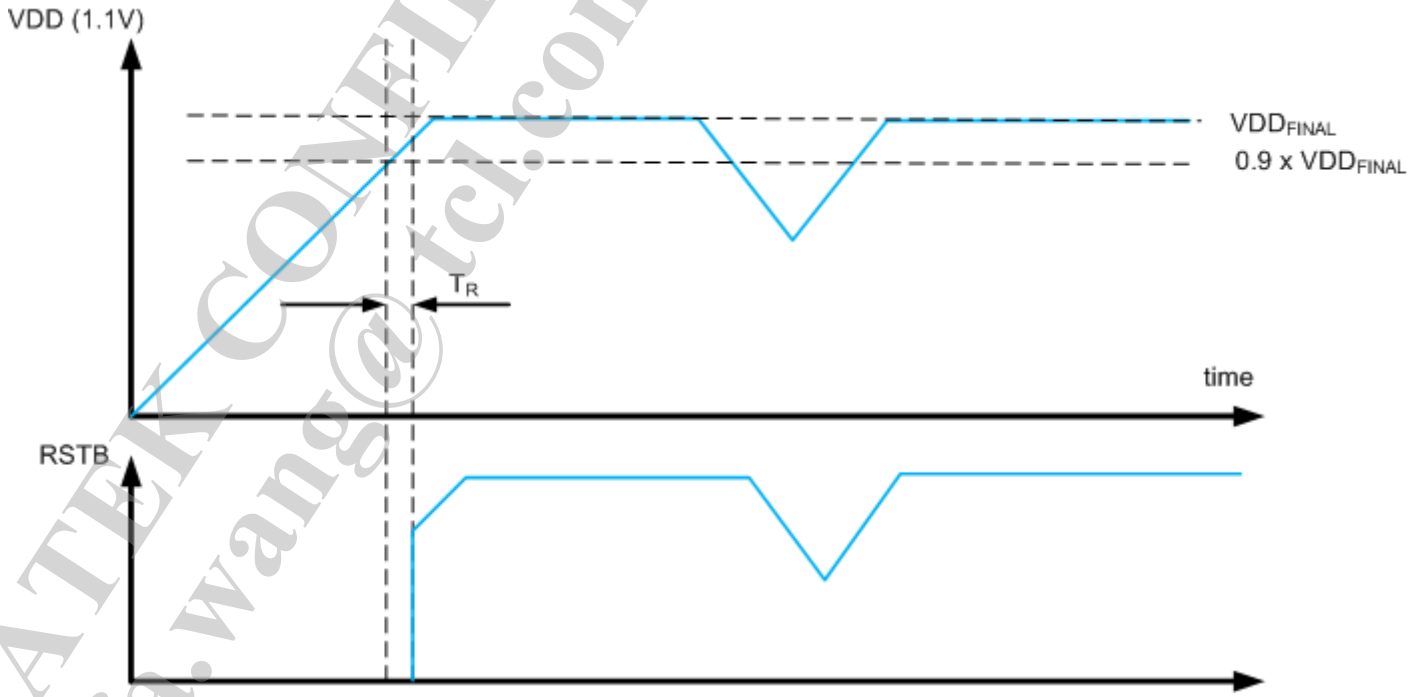
RFSYS is programmed through 5 BSI GPIO PADs. Both write and read operations are supported and 5 wires are used (3 bi-direction data pins, one clock pin, and one enable pin). All BSI interfaces are through VIO18 domain.

10.2 Power-On Reset

The chip includes two Power-On Reset (POR) operating from the static domain LDO's on the VXODIG domain. These operate on the DCXO_DIGITAL and GLOBAL_STATIC digital blocks from the 1.1V supply domain directly derived from VXODIG via LDO's. The designs are identical and since VXODIG is an "always-on" supply then a simplified implementation can be used - specifically there should not be situation where the VXODIG supply can drop after the internal LDO is enabled. The important point then is that the reset needs to be active for sufficiently long that the power supply has stabilized but short enough that the domain is available for BSI programming when requested.

In the case of the DCXO POR the LDO is directly enabled from the VXODIG supply. In the case of the GS LDO VXODIG is always present (in normal mode) and the LDO for this domain is enabled from the baseband (26MHz clock enabled from MT6583).

The operation is shown in the Figure below.

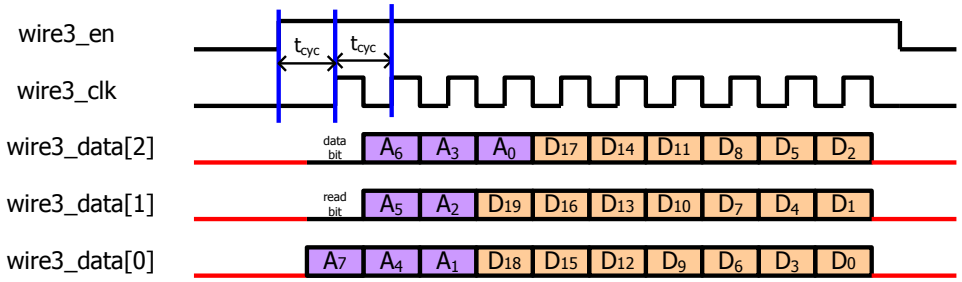


10.3 BSI Clock Frequency

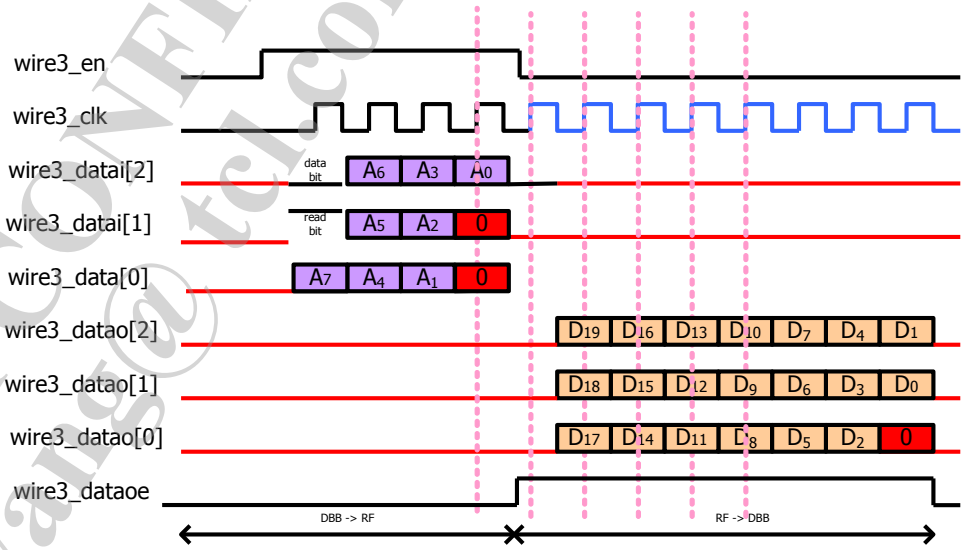
The BSI Clock is designed to operate at a maximum frequency of 61.44 MHz, switching down to 30.72 MHz during the read back phase of a read operation.

The BSI clock has nominally a 50% duty cycle (< 40:60 should be guaranteed by the baseband clock generator).

10.4 BSI Operation



Timing Diagram of Write Operation



Timing Diagram of Read Operation