MT6167 RF System Datasheet

Version:	1.1
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Editor:	Chi-Yao Yu

Detailed Document Revision History

Revision	Section	Date	Editor	Description of Changes
0.0		10/September/2012	CYYu	Initial released version
0.0	13.5	10/September/2012	CH.Shen	Modify some undefined numbers.
0.0	11.1 11.3	10/September/2012	Hsinhua	Remove spur spec @78MHz. Update some performances.
0.0	4.2.1 12.1 12.2.1 12.3.2	11/September/2012	Amos	Update current consumption and remove the unused table
0.1		14/September/2012	CYYu	Update DCXO, SRX, RX, STX, and TOP current tables
0.1	3.4 4.2	18/October/2012	CYYu	Update ESD level and current consumption table
1.0		23/October/2012	CYYu	Formal released version

1 Introduction

1.1 Overview

The MT6167 is an RF transceiver targeted at high speed 3G smart phone and tablet computers implemented in 40nm CMOS. The RF transceiver function is fully integrated. This document described the performance targets for the RF macro to be embedded in the overall product.

1.2 Key features

- Full multi-mode RF solution (GGE/WCDMA) through to 3GPP Release 8 (HSPA+)
  - *42.2Mbps peak DL (Cat. 24: 64QAM, Dual-Cell HSDPA)*
  - *11.5Mbps peak UL (Cat. 7: 16QAM)*
  - *Supports receiver diversity (RxD)*
  - *Quad-band support in GGE mode (GSM850/900/1800/1900)*
  - *3G bands support: Band I –VI , VIII-XI (including Softbank, JPN), XIX*

- Direct Conversion (3G), Two Point Modulation (TPM) for GMSK and Small Signal Polar for 8-PSK
  - No external SAW filters required for transmitter (WCDMA//GGE)
  - Dedicated power detection circuits for 3G TX power control over specific power range

- Hybrid Direct-Conversion (3G) / Low-IF (GGE, DC-HSDPA) receiver
  - *No external SAW filters required for receive (WCDMA/HSDPA)*
  - *Flexible support for a variety of bands configuration (5 Rx & 3 RxD)*
    - *Quad-band Rx GGE co-banded with 4 Rx WCDMA/HSDPA/DC-HSPA bands II,III,V,VIII*
    - *Additional Rx input for other 3G bands*

  Three RxD inputs can cover up to five bands through external band diplexing

- Low supply current & operation directly from DC-DC converter

- 26MHz internal DCXO or external VCTCXO operation (with integrated AFC DAC)
  - Three low noise additional Clock Drivers for clocking connectivity / peripheral IC's
  - Ultra Low power 32KHz mode

- Support RF Calibration features for key Rx and Tx specifications (Image rejection, LO feed through, DC offset)

- Temperature Measurement sub-system

2 Block Diagram and Application Diagram

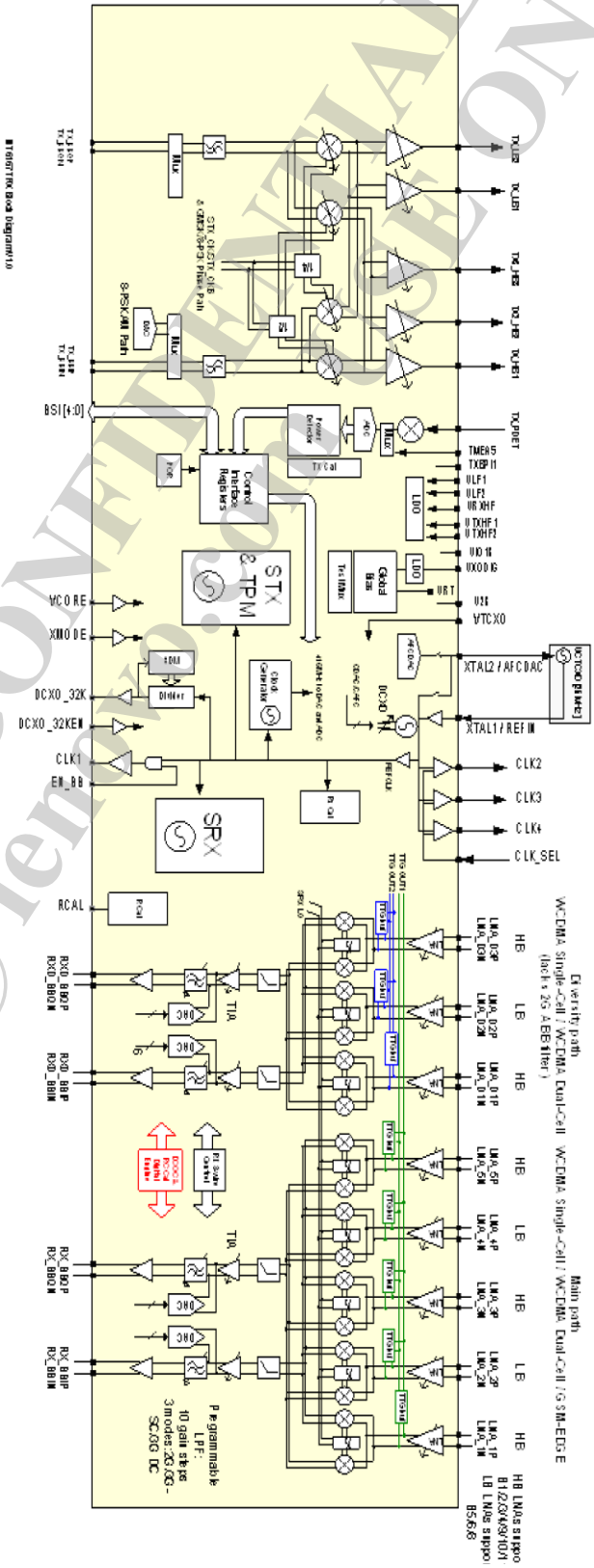


Figure 1: RFSYS Block Diagram

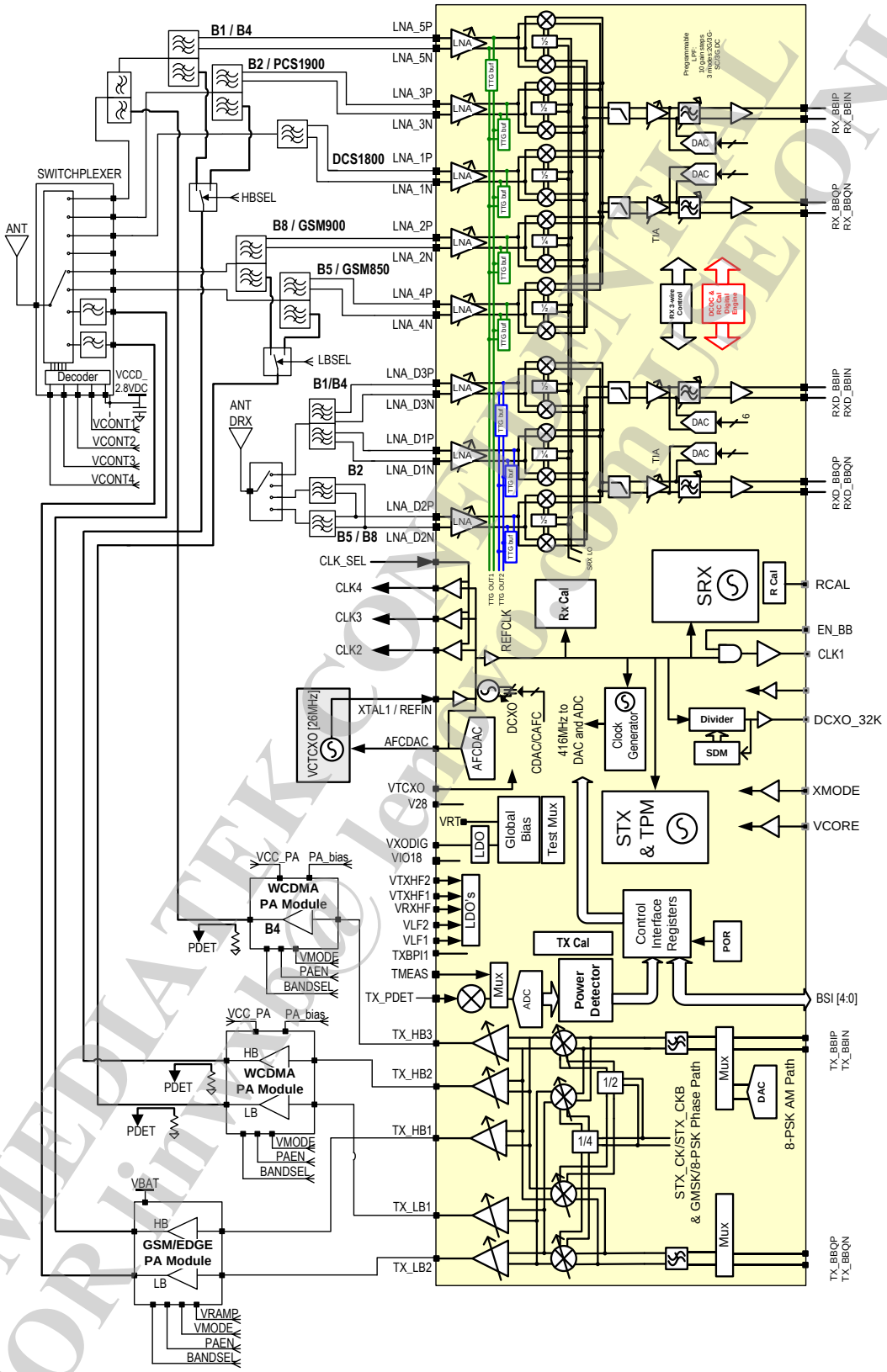


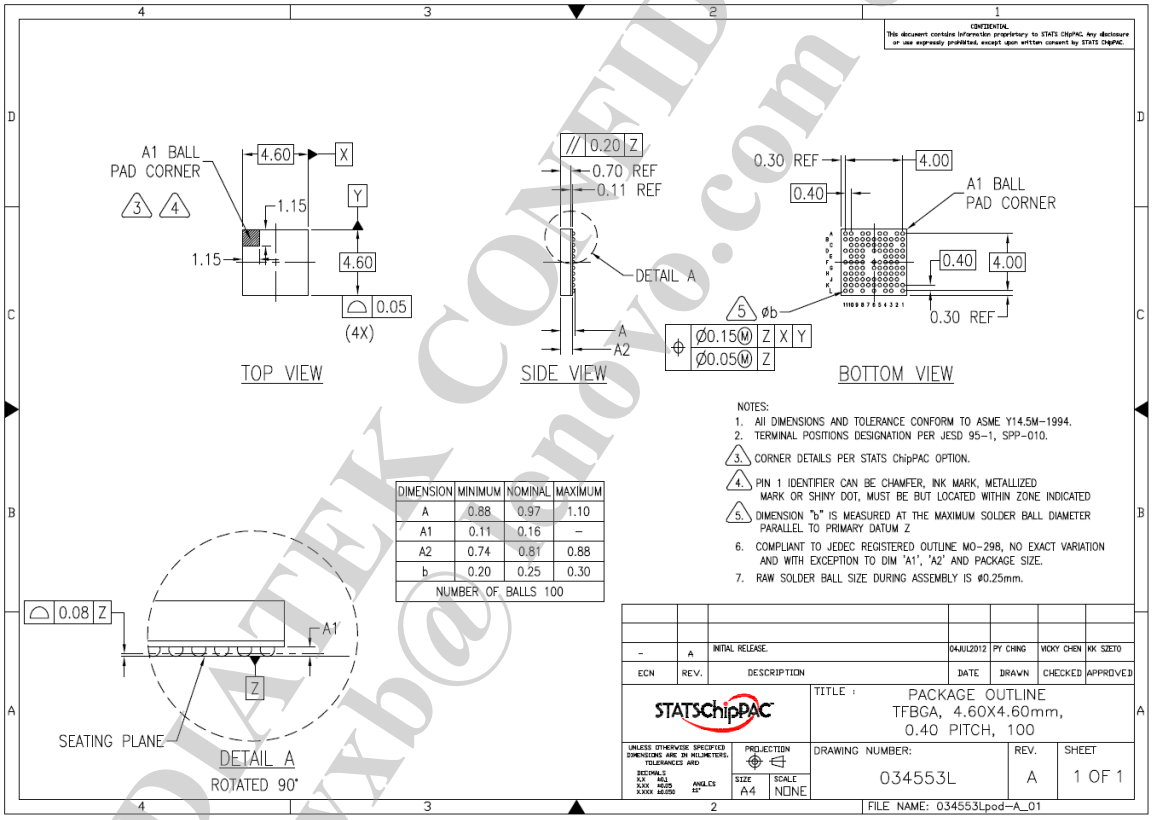
Figure 2 : Applications Diagram

3 General Specifications

3.1 Packaging

Wirebond TFBGA is currently considered for this product.

Parameter	Single die
Body Size	4.6x4.6mm
Ball Spacing	0.4mm
Ball number	11x11



3.2 RF I/O List

Category	PAD Name	Ball Name	Description	ESD/Supply	Comments
RF I/O	PAD_LNA_1P	LNA_1P	RX input (3G/2G HB)	[-]	ESD is GND protection only
	PAD_LNA_1N	LNA_1N	RX input (3G/2G HB)	[-]	ESD is GND protection only
	PAD_LNA_2P	LNA_2P	RX input (3G/2G LB)	[-]	ESD is GND protection only
	PAD_LNA_2N	LNA_2N	RX input (3G/2G LB)	[-]	ESD is GND protection only
	PAD_LNA_3P	LNA_3P	RX input (3G/2G HB)	[-]	ESD is GND protection only
	PAD_LNA_3N	LNA_3N	RX input (3G/2G HB)	[-]	ESD is GND protection only
	PAD_LNA_4P	LNA_4P	RX input (3G/2G LB)	[-]	ESD is GND protection only
	PAD_LNA_4N	LNA_4N	RX input (3G/2G LB)	[-]	ESD is GND protection only
	PAD_LNA_5P	LNA_5P	RX input (3G/2G HB)	[-]	ESD is GND protection only
	PAD_LNA_5N	LNA_5N	RX input (3G/2G HB)	[-]	ESD is GND protection only
	PAD_LNA_D1P	LNA_D1P	RX diversity input (3G HB)	[-]	ESD is GND protection only
	PAD_LNA_D1N	LNA_D1N	RX diversity input (3G HB)	[-]	ESD is GND protection only
	PAD_LNA_D2P	LNA_D2P	RX diversity input (3G LB)	[-]	ESD is GND protection only
	PAD_LNA_D2N	LNA_D2N	RX diversity input (3G LB)	[-]	ESD is GND protection only
	PAD_LNA_D3P	LNA_D3P	RX diversity input (3G HB)	[-]	ESD is GND protection only
	PAD_LNA_D3N	LNA_D3N	RX diversity input (3G HB)	[-]	ESD is GND protection only
	PAD_TX_HB1	TX_HB1	TX output (3G/2G HB)	AVDD28_ESD	
	PAD_TX_HB2	TX_HB2	TX output (3G/2G HB)	AVDD28_ESD	
	PAD_TX_HB3	TX_HB3	TX output (3G/2G HB)	AVDD28_ESD	
	PAD_TX_LB1	TX_LB1	TX output (3G/2G LB)	AVDD28_ESD	
	PAD_TX_LB2	TX_LB2	TX output (3G/2G LB)	AVDD28_ESD	
	PAD_TX_PDET	TX_PDET	TX detection path input	AVDD28_ESD	
BB I/O	PAD_RX_BBIP	RX_BBIP	Analog RX output (main I path)	AVDD18_RXHF	
	PAD_RX_BBIN	RX_BBIN	Analog RX output (main I path)	AVDD18_RXHF	
	PAD_RX_BBQP	RX_BBQP	Analog RX output (main Q path)	AVDD18_RXHF	
	PAD_RX_BBQN	RX_BBQN	Analog RX output (main Q path)	AVDD18_RXHF	
	PAD_RXD_BBIP	RXD_BBIP	Analog RX output (diversity I path)	AVDD18_RXHF	
	PAD_RXD_BBIN	RXD_BBIN	Analog RX output (diversity I path)	AVDD18_RXHF	
	PAD_RXD_BBQP	RXD_BBQP	Analog RX output (diversity Q path)	AVDD18_RXHF	
	PAD_RXD_BBQN	RXD_BBQN	Analog RX output (diversity Q path)	AVDD18_RXHF	
	PAD_TX_BBIP	TX_BBIP	3G BB TX input (I path)	AVDD28_ESD	
	PAD_TX_BBIN	TX_BBIN	3G BB TX input (I path)	AVDD28_ESD	
	PAD_TX_BBQP	TX_BBQP	3G BB TX input (Q path)	AVDD28_ESD	
	PAD_TX_BBQN	TX_BBQN	3G BB TX input (Q path)	AVDD28_ESD	
	PAD_TMEAS	TMEAS	Connect to external thermal resistor to detect temparature	AVDD28_ESD	
	PAD_TXBPI	TXBPI	TX calibration digital signal	AVDD18_TXHF	GPIO (AVDD18_TXHF)
BSI Interface	PAD_BSI_EN	BSI_EN	BSI enable	AVDD18_IO	GPIO (AVDD18_IO)

	PAD_BSI_CK	BSI_CK	BSI clock	AVDD18_IO	GPIO (AVDD18_IO)
	PAD_BSI_DATA0	BSI_DATA0	BSI input/output data	AVDD18_IO	GPIO (AVDD18_IO)
	PAD_BSI_DATA1	BSI_DATA1	BSI input/output data	AVDD18_IO	GPIO (AVDD18_IO)
	PAD_BSI_DATA2	BSI_DATA2	BSI input/output data	AVDD18_IO	GPIO (AVDD18_IO)
TCVCXO/DCXO	PAD_XTAL1	XTAL1	XO input	AVDD28_VTCXO	Also input clock for VCTCXO application
	PAD_XTAL2	XTAL2	XO input	AVDD28_VTCXO	Also AFCDAC o/p for VCTCXO application
	PAD_CLK1	CLK1	DCXO buffer 1 output for baseband chip	AVDD28_VTCXO	
	PAD_CLK2	CLK2	DCXO buffer 2 output for external connectivity chip	AVDD28_VTCXO	
	PAD_CLK3	CLK3	DCXO buffer 3 output for external connectivity chip	AVDD28_VTCXO	
	PAD_CLK4	CLK4	DCXO buffer 4 output for audio	AVDD28_VTCXO	
	PAD_XMODE	XMODE	Select DCXO (1) or TCVCXO (0)	AVDD18_VXODIG	
	PAD_CLK_SEL	CLK_SEL	Enable DCXO buffer 2 to 4	AVDD18_IO	
	PAD_DCXO_32KEN	DCXO_32KEN	Enable DCXO 32K output	AVDD28_VTCXO	
	PAD_DCXO_32K	DCXO_32K	DCXO 32-KHz output buffer	AVDD28_VTCXO	
	PAD_EN_BB	EN_BB	Enable DCXO buffer 1	AVDD18_IO	
Test Ports	PAD_TST1	TST1	Test pin 1	AVDD18_RXHF	
	PAD_TST2	TST2	Test pin 2	AVDD28_VTCXO	
Voltage Supply	AVSS18_DET	DET_GND	GND for TX detection path	AVDD28_ESD	Connect to AVSS18_RF on the package
	AVSS18_TXO	TXO_GND	GND for TX output balun	AVDD28_ESD	Connect to AVSS18_RF on the package
	AVDD18_RXHF	VRXHF	VDD for RX FE	[-]	
	AVDD18_IO	VIO18	VDD for digital LDOs and GPIO	[-]	
	AVDD18_VXODIG	VXODIG	VDD for DCXO/GS digital macros	[-]	
	AVDD28_VTCXO28	VTCXO28	VDD for DCXO and analog BGs	[-]	
	AVDD18_RXLF	VLF1	VDD for SRX low frequency part/TTG/CKG	AVDD28_VTCXO	
	AVDD18_TXLF	VLF2	VDD for TX low frequency part	AVDD28_ESD	
	AVDD18_TXHF	VTXHF	VDD for TX RF part	AVDD28_ESD	
	AVDD28_ESD	V28	VDD for ESD ring	[-]	
GND	AVSS18_RF	GND	Global GND	[-]	
RCAL	PAD_RCAL	RCAL	Connect to external resistor for resistor calibration	AVDD28_ESD	

3.3 Ball Assignment

	1	2	3	4	5	6	7	8	9	10	11	
A	TX_HB2	TX_HB3		VTXHF	TMEAS		TX_BBQP	TX_BBIP		DCXO_32KEN	DCXO_32K	A
B	TX_HB1	TX_LB1	TX_LB2	RCAL	DET	V28	TX_BBQN	TX_BBIN	VLF2	EN_BB	TST2	B
C	TXO_GND		TXO_GND	GND	DET_GND	GND	GND	GND	GND	VLF1		C
D	LNA_1N	GND	GND	GND	GND	TXBPI1		BSI_EN	GND	CLK4	CLK1	D
E	LNA_1P	LNA_2N	GND	GND				BSI_CK	GND	CLK2		E
F		LNA_2P	GND	GND	GND	GND		BSI_DATA0	GND	CLK3	XTAL2	F
G	LNA_3N	LNA_3P	GND	GND	GND	GND		BSI_DATA1	GND	XTAL1		G
H	LNA_4N	LNA_4P	GND	GND	GND			BSI_DATA2	GND	XMODE	VTCXO28	H
J		LNA_5P	GND	GND	GND	GND	GND	GND	GND	VXODIG	CLK_SEL	J
K	LNA_5N	LNA_D1N	LNA_D2N	LNA_D3N	VRXHF	RX_BBQN	RX_BBIN	TST1	RXD_BBIN	RXD_BBIP	VIO18	K
L	LNA_D1P		LNA_D2P	LNA_D3P		RX_BBQP		RX_BBIP		RXD_BBQN	RXD_BBQP	L
	1	2	3	4	5	6	7	8	9	10	11	

	I/O pin for RF/analog signal
	Differential RF Pins
	Differential RF Pins
	VDD Pins
	Ground Pins
	Digital or static Pins
	Removed Pins

Figure 3 Ball Map

3.4 Absolute Maximum Ratings

Parameter	Conditions	Min	Max	Unit	notes
Supply VTCXO28		-0.3	3.3	V	
Supply VIO18		-0.3	2.0	V	
Supply VXODIG		[-]	[-]	V	1. Connects to VIO18 in normal case 2. Connects to VTCXO28 in 32K-less case 3. In ATPG mode, it connects to an independent supply with 1.4-V maximum voltage
Supply VRF18		-0.3	2.0	V	
Junction Temperature			125	°C	
ESD Protection	HBM – analog and digital I/O	±2000		V	
	HBM – RF I/O	±2000		V	PDET, Rx inputs, Tx outputs
	FICDM – analog and digital I/O	±250		V	target - no current corporate requirement
	FICDM– RF I/O	±250		V	PDET, Rx inputs, Tx outputs target - no current corporate requirement
	MM – analog and digital I/O	±200		V	
	MM – RF I/O	±100		V	PDET, Rx inputs, Tx outputs

Notes

1. No DC input should be directly applied to the Rx inputs. Matching network should either be a series capacitor/inductor or shunt inductor (RXn/RXnB)
2. Tx Output is DC shorted to ground internally no DC should be applied under any circumstances (AC coupling required for those PA's with DC at the input)

3.5 Operating Conditions

Within the operating range the IC operates as per the functional description.

Parameter	Conditions	Min	Nom	Max	Unit
Supply VIO18		1.7	1.8	1.9	V
SMPS Supply VRF18		1.75	1.825	1.9	V
Linear Supply VTCXO28		2.7	2.8	2.9	V
Supply VXODIG	Normal function mode	Connects to VIO18			
Supply VXODIG	32K-less mode	Connects to VTCXO28			
Supply VXODIG	ATPG mode – LDO's bypassed in this mode	1.1	1.2	1.4	V
Receiver Front End					
RX input frequency range	See Receiver Section for detailed frequency ranges				
Rx required amplitude balance	All Rx input pairs	-1		+1	dB
Rx required phase balance	All Rx input pairs	-10		+10	deg
Transmitter					
Tx Frequency Range	See Transmitter Section for detailed frequency ranges				
Tx O/P VSWR	All Phases ZL = 50Ω			2:1	
Clock Buffers					
CLK1, CLK2,CLK3 Load (Rload||Cload) to GND	Cload	See section [7.3]			pF
	Rload				kΩ
Reference Clock Input (VCTCXO)					
Reference Clock Frequency			26.0		MHz
Reference Clock Input Voltage Swing	AC coupled at input pin	700		1500	mVpp
Duty Cycle		40		60	%
Phase Noise – note 2	@ F_{offset} = 100Hz		<-103	-100	dBc/Hz
	@ F_{offset} = 1KHz		<-133	-130	dBc/Hz
	@ F_{offset} = 10KHz		<-147	-144	dBc/Hz
	@ F_{offset} = 100KHz		<-149	-146	dBc/Hz
Harmonic Content	HD2 @ 52MHz			-8	dBc
	HD3 @ 78MHz			-10	dBc
	HD4 @ 104MHz			-20	dBc
Start-up time	|Δf|<1ppm to >90% of final amplitude			3	ms
Crystal Requirements					
2 Crystal types are supported (Crystal #1 3225 body size / Crystal #2 2520 body size)					
Nominal Load Capacitance	Crystal #1		7.5		pF
	Crystal #2		7.0		pF
Initial Frequency error				±10	Ppm
ESR				30	Ω
Drive level				100	µW
Pullability	Crystal #1	-10%	32	+10%	ppm/pF
	Crystal #2	-10%	27	+10%	ppm/pF

Note 1

The supportable ambient temperature range will depend on the thermal impedance of the package used and the exact operational state as well as the end application thermal design (housing, PCB etc).

Junction temperature is a more reliable indication of the actual operational range.

Note 2

The input clock requirement specified is defined to meet receiver and transmitter phase noise requirements e.g. IC EVM specification. Certain connectivity requirements may require better specifications than this. See clock buffer in section [7]. The clock source (non DCXO mode) can either be an external VCTCXO/VCXO module or alternatively another transceiver clock buffer when considering multiple transceiver applications.

4 Supply Specification

4.1 External Power Supplies & Interfaces

The RFSYS macro operates from four power supplies.

Supply Name	Usage	Regulator Type	Output Voltage
VTCXO28	Regulated supply for VCTCXO/DCXO	Linear	2.8V
VRF18	Regulated supply for all major sub-systems	Switching	1.825V
VIO18	Always-on supply for interface and register retention	Switching	1.8V
*VXODIG	Connects to VIO18 in normal mode and VTCXO28 in 32K-less mode	Linear or Switching	1.8V / 2.8V

* Since VXODIG is connected to VIO18 or VTCXO28, its current is merged to VIO18 or VTCXO28 in this section

4.2 Total Power Dissipation Specification and Budget

To simplify ease of comparison these are shown as the equivalent current, I_{BAT}, drawn from V_{BAT} when the IC is used in the system. Due to the use of a dc-dc converter in the system this is not the same as the IC current. The dc-dc converter supplying VIO18/VRF18 is assumed to have 85% efficiency and operates from a nominal Vbat ~ 3.6V. Therefore the equivalent battery current can be calculated as

$$I_{BAT} = Idd(VTCXO28) + Idd(VIO18) \times \frac{1.8V}{3.6V} \times \frac{1}{0.85} + Idd(VRF18) \times \frac{1.825V}{3.6V} \times \frac{1}{0.85}$$

4.2.1 Total Power Dissipation Specification

Following table shows the mode definition for current benchmarking and comparison.

Mode	VIO18	VTCXO	VXODIG	VRF18	EM_BB	DYN_EN	MODE[3:0]	Notes
Power off	OFF	OFF	OFF	OFF	0	0	0000	All RF circuits are off
Power off (32K-less)	OFF	ON	ON	OFF	0	0	0000	DCXO and DCXO digital are on
Deep sleep	ON	OFF	OFF	OFF	0	0	0000	DCXO digital is on
Deep sleep (32K-less)	ON	ON	ON	OFF	0	0	0000	DCXO and DCXO digital are on
Deep sleep (26M co-clock)	ON	ON	ON	OFF	0	0	0000	DCXO and DCXO digital are on
Phone standby	ON	ON	ON	OFF	1	0	0000	DCXO, DCXO digital, and global static digital are on
Sleep	ON	ON	ON	ON	1	1	0000	All blocks have power except analog/RF blocks
Active	ON	ON	ON	ON	1	1	Not 0000	Program required mode

Below is the total battery current measured when the chip is operating in the mode described using the recommended register settings. For ease of comparison and benchmarking it is assumed no peripheral clock buffers are enabled (except 26MHz co-clock case in the deep sleep mode).

Mode	Conditions	I_{VIO18}		I_{VTCXO}		I_{VRF18}		I_{BAT}		Unit
		Nom	Max	Nom	Max	Nom	Max	Nom	Max	
Deep Sleep (normal)	VIO18 only present, no other supplies, no 26MHz clock request	10.5	16	0	0	0	0	6.2	9.4	µA
Deep Sleep (32K-less)	DCXO enabled in the 32KHz low power mode	0	0	130		0	0	130		µA

Deep Sleep (26MHz co-clock)	DCXO and peripheral clock buffers are enabled	52	80	1100		0	0	1131		µA
Standby	DCXO and Global Static have Power. VRF18 not present	0.18	0.3	1.25		0	0	1.36		mA
Sleep	All power present (VIO18, VTCXO28, VRF18) but Rx / Tx not enabled	0.18	0.3	1.5		0.3		1.78		mA
RX ON	WCDMA mode SC / no Rx-D / LNA mid-gain	0.18	0.3	2		46		29.54		mA
	WCDMA mode DC / Rx-D / LNA high gain	0.18	0.3	2		87.5		54.29		mA
	WCDMA mode SC / Rx-D / LNA high gain	0.18	0.3	2		86.5		53.69		mA
	GSM/EDGE mode / LNA high gain	0.18	0.3	2		53		33.72		mA
TX ON	WCDMA mode @ Pout=Pmin	0.18	0.3	2		42		27		mA
	WCDMA mode @ Pout=0dBm	0.18	0.3	2		82		52		mA
	GMSK Mode	0.18	0.3	2		50		32		mA
	8-PSK Mode @ Pout=-4dBm	0.18	0.3	2		77		49		mA

5 Global Biasing

5.1 Biasing Overview

RFSYS has a global Band Gap reference that is used to generate a variety of different current references that are then distributed to different sub-systems.

Four types of biasing are provided

1. VBG/RI : temperature compensated current referred to an on-chip poly-p+ resistor (RI)
2. VPTAT/RI : PTAT current referred to an on-chip poly-p+ resistor (RI)
3. VBG/RT : temperature compensated current calibrated to an external resistor (RT)
4. VPTAT/RT : PTAT current calibrated to an external resistor (RT)

5.2 'VBG/RI' Reference Currents

Parameter	Conditions	Min	Nom	Max	Unit
Supply Voltage		2.65	2.8	2.95	V
Current Consumption	Core 'VBG/R' Current Reference Circuit.		420		µA

5.3 'VPTAT/RI' Reference Currents

Parameter	Conditions	Min	Nom	Max	Unit
Supply Voltage		2.65	2.8	2.95	V
Current Consumption	Core 'PTAT' Current Reference Circuit.		110		µA

5.4 Band-Gap Reference Voltage

An LDO Band-Gap Reference Voltage is typically generated, remotely, at a 12kΩ grounded resistor & from a 100µA 'V_{BG}/R' reference current.
The generated bandgap voltage can be trimmed by a 4 bit code that is programmed via the BSI at power up under L1 control.

Parameter	Conditions	Min	Nom	Max	Unit
Band-Gap Reference Voltage	Reference Trim Code: RSEL[3:0]=0b1000	1.10	1.20	1.30	V
Nominal Voltage Trim			12		mV/lsb

5.5 VBG/RT and VPTAT/RT

RFSYS contains a calibration block that is used to calibrate an on-chip resistor against an accurate off chip resistor (1%).

Specifically a 5 bit scaling code is generated via a successive approximation algorithm that is the required code that scales an on chip generated VBG/RI current dumped into an accurate off chip resistor to equal that of a non scaled VBG/RI current dumped into an on-chip resistor (proportional to RI).

The scheme is shown in the Figure below.

In more precise terms

$$I_{INT} = \frac{V_{BG}}{R_I}$$

$$I_{EXT} = \frac{V_{BG}}{R_I} \cdot (1+\alpha)$$

$$\alpha \text{ set by SAR\_CODE}$$

$$\text{SAR sets } V_{INT} = V_{EXT} \therefore$$

$$(1+\alpha) \cdot R_{EXT} = R_I$$

$$\frac{R_I}{R_{EXT}} = 1+\alpha$$

And for the specific implementation

$$1+\alpha = \frac{3}{4} + \frac{SC}{64} \quad SC = SAR\_CODE(0..31)$$

This can tune resistor variation of -25% (low) to +20% (high) with ~1.6% resolution.

The on-chip resistor calibration is performed during power-on phase. The result of running the calibration engine is available in Global_Static and is read back from BSI to the baseband chip after calibration. Each time when MT6167 is from deep-sleep mode to standby mode, the resistor calibration results are written to Global_Static from the baseband chip, and applied in active mode.

The RFSYS global bias generator includes currents scaled by the same factor as above i.e. [¾+code/64]. Both VBG and VPTAT versions are used and the scaling can be set independently. It is intended that these programmed values are derived from the calibrated code available.

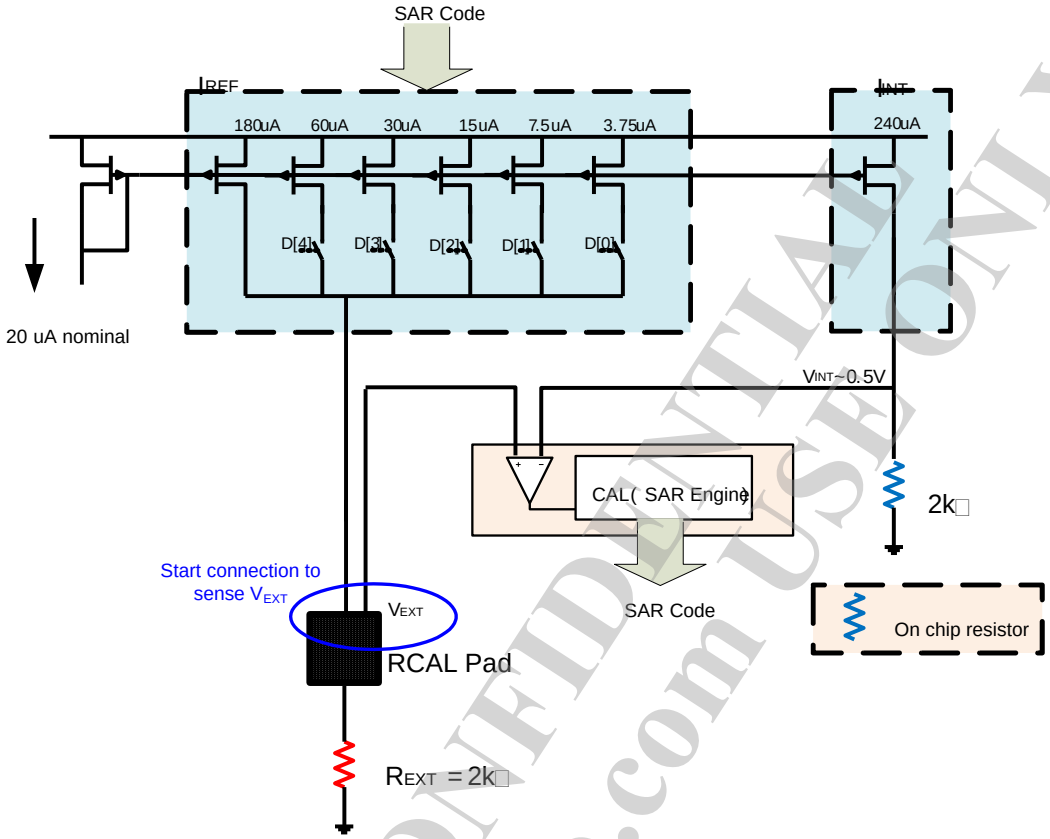


Figure 4 RCAL Function

6 LDO's and Level Shift Biasing

Each power sub domain of RFSYS is regulated from a low dropout regulator for correct supply conditioning. These are customized for each individual requirement e.g. noise, reverse isolation (high frequency leakage), DC accuracy, DC load requirement, and PSSR etc. The overall power plan is shown in Figure 5.

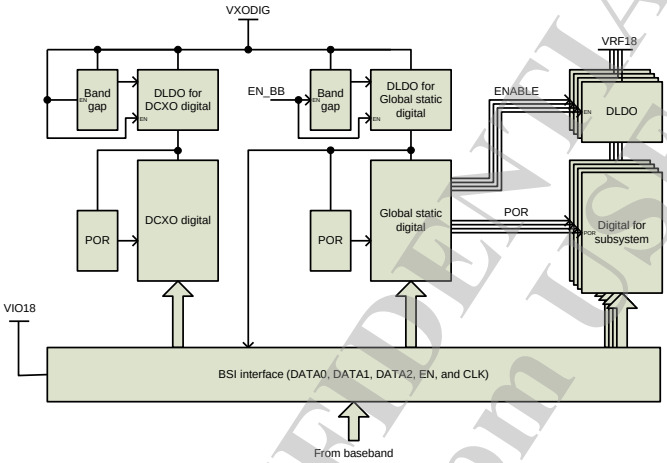


Figure 5 Overall Power Plan

6.1 Static Digital Domains

These are designed for very low power with good reverse isolation and have internal references. They are powered from VXODIG and are designed to also operate up to 2.8V.

6.1.1 DCXO_DIGITAL Domain

It is always on when VXODIG is present.

Parameter	Conditions	Min	Nom	Max	Unit
Nominal Output Voltage	Including supply variations	0.95	1.1	1.25	V
Supply drop Under Load	Supply drop under after digital block becomes active			300	mV
Load Current			0.2	1.0	mA
Ground Current – 1	Normal mode – includes reference generator			10	µA
Ground Current – 2	Scan Mode (high current)		0.5	>1	µA
PSSR	DC-100KHz	20			dB
Start up Time	After VIO18 > VIO18(final)-0.1V			25	µs

The LDO has various programmable modes including

(a) Programmable O/P voltage

Control Signal	Output Voltage [V]
TOP_DCXOLDO_VS=0	1.2 (default)
TOP_DCXOLDO_VS=1	1.0
TOP_DCXOLDO_VS=2	1.1
TOP_DCXOLDO_VS=3	1.3

The 1.2V default is recommended at power-up for design margin with a plan that the 1.1V setting can be used once performance is verified (via the initialization configuration).

(b) Scan Mode

Since when the digital is ATPG (Scan) mode the power consumption is significantly higher. Rather than increasing the LDO capacitor a mode is provided that bypasses the pass device.

6.1.2 GLOBAL_STATIC Domain

It is enabled when 26MHz is requested by the baseband.

Parameter	Conditions	Min	Nom	Max	Unit
Nominal Output Voltage	Including load and supply variations	0.95	1.1	1.25	V
Supply drop Under Load	Supply drop under after digital block becomes active			300	mV
Load Current			0.45		mA
Ground Current - 1	Normal load – includes reference generator			30	uA
Ground Current – 2	Scan Mode (high current)		1.4		uA
PSSR	DC-100KHz	20			dB
Start up Time	After Enable			25	us

The same programmable modes are supported as for the DCXO_DIGITAL Static LDO with the same voltage selection and power up values.

6.2 Level Shift Biasing

The power supplies for the receiver side of the level shifters are derived from VIO18 (always on) and is designed to provide a quiet filtered reference that prevents the propagation of digital noise from the low frequency to high frequency domain. The level shifters typically operate from two supplies: one for the input stage that has a DC voltage similar to the driving side (1.1V) allowing single ended DC coupling and then an output side supply that allows level shifting to a higher voltage.

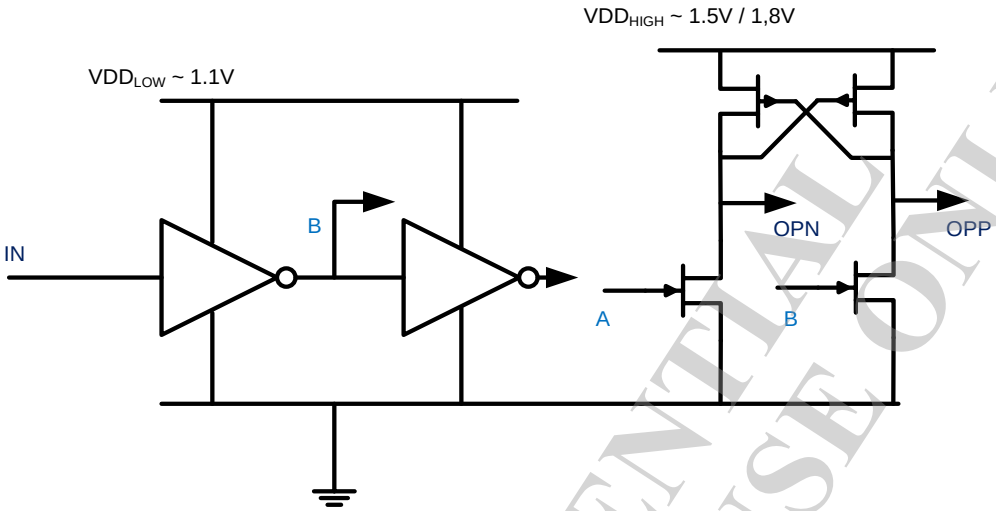


Figure 6 Level Shifter Scheme

The scheme is shown below

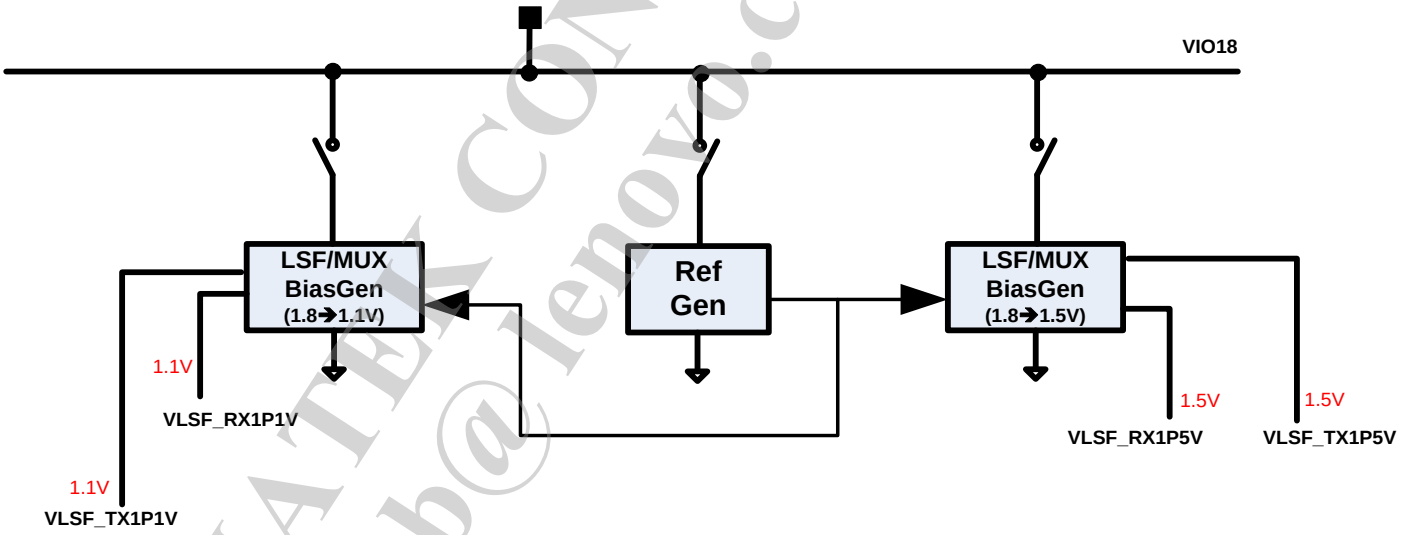


Figure 7 Level Shifter Biasing

The 1.1V generator for the DCXO uses a simple potential divider and follower from the clean VTCXO28 supply.

The 1.1V and 1.5V share a common 1.1V reference followed by a non-inverting amplifier to scale the voltage. Secondary outputs are produced by just having a replica of the amplifier output stage. Target current for each branch is in the ~uA range.

Reference Generator

Parameter	Conditions	Min	Nom	Max	Unit
Output Voltage		0.95	1.1	1.25	V
Ground Current	No load – includes reference generator			5	µA

7 Reference Clock Specification

MT6167 RF system integrates a core 26MHz XTAL oscillator (DCXO), AFCDAC and a 32KHz low power mode. Also all the clock buffers external and internal are integrated in this system.

The mode of operation (internal DCXO or external VCTCXO) is selected via the input XMODE from the baseband with the following function

CLK_MODE	Mode
LOW	External CLK (VCTCXO)
HIGH	DCXO

In Crystal mode the XTAL is connected directly between XO1 and XO2.

In VCTCXO mode XO2 pin is reconfigured to be the AFCDAC output and XO1 the VCTCXO clock input pin.

Since the state of XMODE is latched into the module then the baseband configuration can take place using a pin state “trapping” scheme on power up if desired.

7.1 DCXO Specification

Parameter	Test condition	title	Unit	Min	Nom	Max
Supply current in sleep (Core+one buffer for baseband)	VCTCXO=2.8V; output differential current 75uA$_{single,p-p}$ to BB	$I_{dcxo,sleep}$	mA		2	
Supply current in TRX (Core+ buffers for baseband, 3-wire, SX)	VCTCXO=2.8V; output differential current 75uA$_{single,p-p}$ to BB	$I_{dcxo,trx}$	mA			3
Supply current for other systems (each extra buffer)	VCTCXO=2.8V; loading refer to Table3	$I_{dcxo,buf}$	mA			1.5
Leakage current	ENdcxo(hardware) = 0V	$I_{leakage}$	uA			1
Center operating frequency	Internal resonant; crystal definition in Section [3.6]	F_{dcxo}	MHz		26	
Duty cycle	Square wave in high driving mode		%	45	50	55
Static range	CapID coding 0 ~ 255 at middle AFC coding. Nominal crystal TS definition in Section [3.6]	R_{static}	ppm		±50	
	At middle CAFC code. Minimum crystal TS definition in Section [3.6]. Smallest amount of negative range from 26MHz as -15% capacitor corner.		ppm	17		
	At mid CAFC code. Minimum crystal TS definition in Section [3.6]. Smallest amount of negative range from 26MHz		ppm	32		
	At middle CAFC coding. Minimum crystal TS definition in Section [3.6]. Smallest amount of positive range from 26MHz as +15% capacitor corner		ppm	17		
	At mid CAFC code. Minimum crystal TS definition in Section [3.6]. Smallest amount of positive range from 26MHz		ppm	32		
CapID bits	CDAC		bit		8	

Dynamic range	CAFC coding 0 ~ 8191 at mid CapID. Nominal crystal TS definition in Section [3.6].	$R_{dynamic}$	ppm		±30	
	Mid CAFC code and tune CapID to target frequency if FL has ±10ppm error. Minimum crystal TS definition in Section [3.6]. As -15% capacitor corner		ppm	±15		
	Mid CAFC code and tune CapID to target frequency if FL has ±10ppm error. Minimum crystal TS definition in Section [3.6].		+- ppm	18		
CAFC bits			bit		13	
CAFC tuning step	Average AFC frequency step , for the CAPID that is closest to 26MHz		ppm		0.007	
CAFC tuning step frequency linearity	No need Linearity Calibration to save time. Cafc at middle and tune CapID to target frequency if FL has +-10ppm error.		%		50	60
CAFC tuning step spike	for all adjacent CAFC coding, especially as capacitor array changes rows or columns	D	LSB	0		1 AFC LSB range
CAFC Slope Curve	CAFC coding 0 ~ 8191 for all CapID				smooth and Monotonic	
CAFC settling time	CAFC coding changes 2000 at one time. Delta f < 1ppm.	T_{settle}	us		150	200
Crystal input pins	Specific foundries		pin		2	
Crystal size					Both 2520&3225	

7.2 Reference Input Buffer Specification (XO1/REFIN)

The input conditions are given in section [3.5].

Parameter	Conditions	Min	Nom	Max	Unit
Input Impedance – Rp	Rp || Cp @ 26MHz	0.8	1		kΩ
Input Impedance – Cp	Rp || Cp @ 26MHz		10	12	pF

This pin should be AC coupled when used with an external clock source.

7.3 Reference Output Buffer(s) Specification

There are 3 reference clock output buffers driving out from the chip. They can be used as reference clock for other chips and application.

External DC block is assumed on all buffer outputs. All buffers are identical designs.

Parameter	Conditions	Min	Nom	Max	Unit
Buffer output Swing	Square wave @ Zload= Cp || Rp	700		1200	mVp-p
Zload (Rp||Cp)	Rp	3			kΩ
	Cp			30	pF
Duty Cycle		40		60	%
Rise / Fall Time	10% to 90% of signal swing @ Cload=30pF [normal drive mode]			6.5	ns
Buffer output harmonic rejection	2^{nd} harmonic			-22	dBc
	3^{rd} harmonic			-10	dBc
	4^{th} harmonic			-30	dBc
SSB phase noise	1Hz offset [30pF load, normal drive mode]		< -55	-50	dBc/Hz

	5Hz offset [30pF load, normal drive mode]		< -78	-73	dBc/Hz
	10Hz offset [30pF load, normal drive mode]		< -85	-80	dBc/Hz
	100Hz offset [30pF load, normal drive mode]		< -110	-105	dBc/Hz
	1kHz offset [30pF load, normal drive mode]		< -138	-131	dBc/Hz
	10kHz offset [30pF load, normal drive mode]		< -147	-145	dBc/Hz
	100KHz offset [30pF load, normal drive mode]		< -153	-150	dBc/Hz
Current Consumption	Zload = 20pF (each buffer)		1.0		mA
Phase Push	due to any mode change, measured over a 10µs window			0.2	deg-peak
Frequency Push	Due to any mode change e.g. other clock buffer switching			0.02	ppm
Output rms Phase Jitter	100Hz-5MHz			1.3	ps-rms

7.4 32KHz Mode

In low power mode a 32KHz clock is produced by using a fractional-N divider (1st order Sigma Delta Modulated) to replace the normal 32KHz XTAL (watchdog). In this mode the CDAC and CAFC capacitance is minimized so that the XTAL core can operate from a significantly reduced bias current).

Parameter	Conditions	Min	Nom	Max	Unit
Frequency			32768		Hz
DCXO Current Consumption	Low Power Mode With all capacitors switched off and auto-amplitude calibration is on		~200		µA
Duty Cycle				80	%
Settling Time				2	ms
Sustaining time after Battery Remove	External capacitor 10µF			300	µs
Frequency variation	After system calibration			±2	ppm
	Over temperature -25degC to 75degC			15	ppm
	Uncalibrated – total variation			200	ppm

7.5 AFCDAC

Includes voltage reference generator

Parameter	Description / Condition	Min	Typ	Max	Unit
FS – sampling rate	Event driven DAC => updated when new value written via BSI to DCXO_DIGITAL			1.0833	MSPS

Parameter	Description / Condition	Min	Typ	Max	Unit
	- Typically update rate is much slower				
Resolution			13		bit
Settling time	Full code jump, and 99% settling after RC filter			1000	µsec
	70 code jump, and 99% settling after RC filter			166	µsec
	6 code jump, and 99% settling after RC filter			48	µsec
Power down glitch	The overshoot while power down (after output cap 1nF)			10	mV
Full Scale Range	Maximum Output Voltage (0x3FF)	2.35			V
	Minimum Output Voltage (0x000)			0.4	V
	Range (GAINSEL=0) – centered on nominal 1.4V	1.9	2.0	2.1	V
Cp	Load Capacitance		1	10	nF
PSRR	All conditions DC-100KHz	43			dB
DNL	code 0 ~ 8191, after RC filter, output voltage 0.35~2.45V (GAINSEL= 0)	-1		+1	LSB
INL	code 0 ~ 8191, after RC filter, output voltage 0.35~2.45V (GAINSEL = 0)	-32		+32	LSB
O/P Noise	Full Scale Output @ 1Hz			21.5	µV /√Hz
	Full Scale Output @ 10Hz			6.5	µV /√Hz
	Full Scale Output @ 100Hz			2.0	µV /√Hz
	Full Scale Output @ 1KHz			0.5	µV /√Hz
	Full Scale Output @ 10KHz			0.2	µV /√Hz
	Full Scale Output @100KHz			0.1	µV /√Hz
AVDD	Analog Power Supply	2.7	2.8	2.9	V
Supply current	Power-up		500		µA
	Power-Down, 85degC			1	µA

8 High Frequency Clock Generation

8.1 Clock Generator (CLKG)

This is an integer-N PLL that generates the 416MHz clocks for The TX DAC. It operates at 26MHz (16x26MHz=416MHz) and as well as the 416MHz clocks. Certain 26MHz clocks are produced for synchronization e.g. TX Dynamic clock 26MHz from the feedback path so as to be synchronized to the 416MHz clocks. Also, the 26MHz clock for the Tx ADC (power detector) is produced from this block.

Parameter	Conditions	Min	Nom	Max	Unit
Current Consumption	Excluding Clock Buffers		1.7		mA
Settling Time				50	µs
Reference Spur @ 26MHz	Referenced to 416MHz O/P clock			-71	dBc
RMS Cycle-to-Cycle jitter				3	ps
RMS Period Jitter				50	ps
RF supply current leakage	@1GHz – guaranteed by in built supply filter			1	µA
	@2GHz – guaranteed by in built supply filter			500	nA
	@4GHz – guaranteed by in built supply filter			250	nA

8.2 Calibration Test Tone Generator (TTG)

This is a PLL used to generate a test tone for certain calibration modes.

1. Feedback to receiver inputs for image rejection calibration
2. Feedback to power detector pin (PDET) to us as a calibration tone for receiver gain calibration

The TTG is implemented as a fractional-N PLL clocked from a 26MHz reference clock

Parameter	Conditions	Min	Nom	Max	Unit
Current Consumption	Excluding Clock Buffers @ 2170MHz		3.4		mA
Frequency Range		1427.9		2170	MHz
Settling Time				50	µs
Frequency accuracy				1	KHz
Reference Spur @ 2MHz				-65	dBc
SSB Phase Noise @ 2MHz				<-90	dBc/Hz
RF supply current leakage	@1GHz – guaranteed by in built supply filter			1	µA
	@2GHz – guaranteed by in built supply filter			500	nA
	@4GHz – guaranteed by in built supply filter			250	nA

9 Transmitter

All transmitter characteristics are listed in this section. Typical specifications are for mid-band channel frequency, and under typical operating conditions. Min/Max specifications are for extreme operating voltage and temperature conditions.
Fig. 8 (will be updated with a simplified figure later.)

9.1 Tx Driver Mapping and Block Diagram

Tx Mapping

Orion-FDD Name	Tx_OP	GSM850/900	B5/B6/B8	Notes
2GLB1	TX_LB1		✓	3G Path
2GLB2	TX_LB2	✓		2G Path

Orion-FDD Name	Tx_OP	GSM1800/1900	B1/B2/B3/B4/B11	Notes
2GHB1	TX_HB1	✓		2G Path
3GHB1	TX_HB2		✓	3G Path (use for B11)
3GHB2	TX_HB3		✓	3G Path

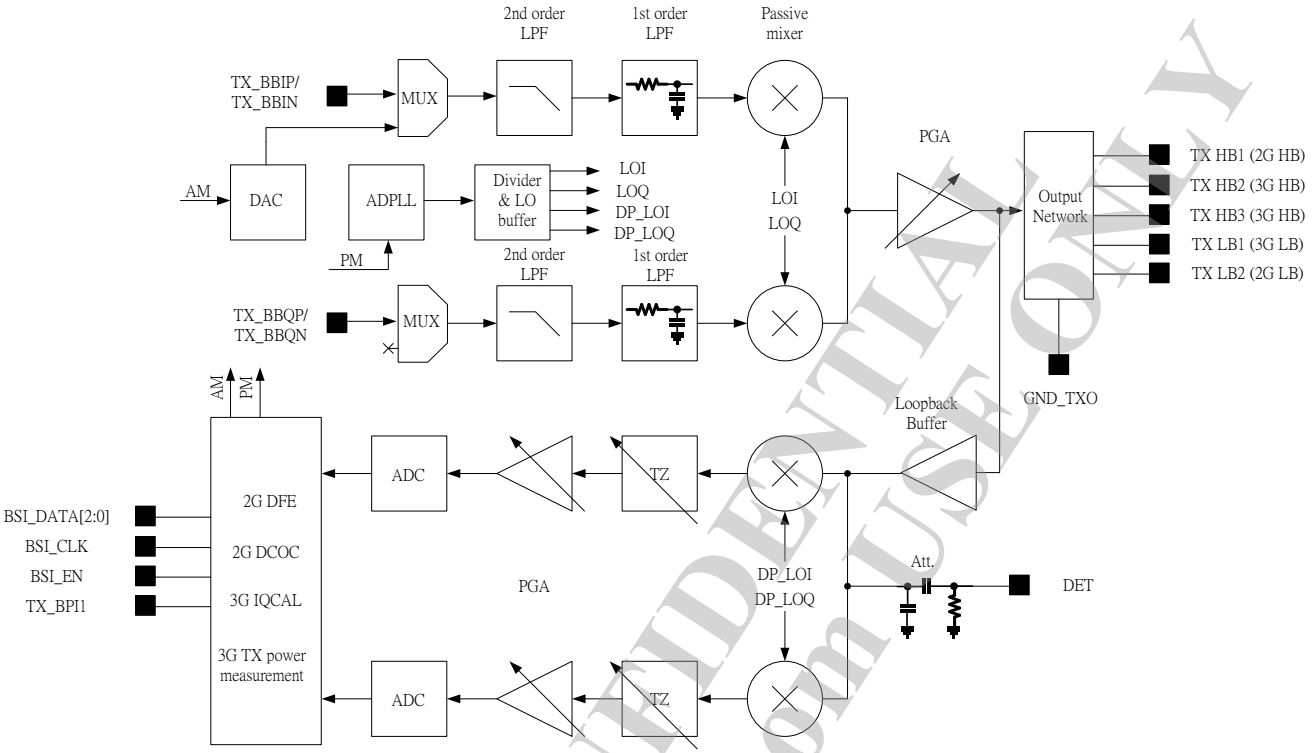


Figure 8 : Tx Block Diagram

9.2 3G Transmitter Chain Performance Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
3G Transmitter Output						
Output Return Loss	S_{22}		-10		dB	50Ω load
Max Output Power (R99)	P_{max}	2			dBm	
Min Output Power (R99)	P_{min}			-70	dBm	
Max Output Power (R6 16QAM)	P_{max}	-1.5			dBm	
Min Output Power (R6 16QAM)	P_{min}			-66.5	dBm	
RF Output Frequency Response	ΔP		±0.2		dB	±5MHz offset
ACLR1 (R99)			-46		dB	
ACLR2 (R99)			-70		dB	
RMS EVM (R99)			2.5		%	
Peak EVM (R99)			9		%	
ACLR1 (R6 16QAM)			-50		dB	
ACLR2 (R6 16QAM)			-68		dB	
RMS EVM (R6 16QAM)			2.5		%	
Peak EVM (R6 16QAM)			12		%	
Spectrum Emission Mask			-60		dBc	
Carrier Leakage			-40		dBc	After calibration with BB
Sideband Suppression			-40		dBc	After calibration with BB
Harmonic Emissions						
2^{nd} harmonic			-45		dBc	
3^{rd} harmonic			-20		dBc	
4^{th} harmonic			-45		dBc	
Noise Emissions						
Band I, noise in RX			-162		dBc/Hz	at Pout=0dBm
Band II, noise in RX			-160		dBc/Hz	at Pout=0dBm
Band V, noise in RX			-161		dBc/Hz	at Pout=0dBm
Band VIII, noise in RX			-161		dBc/Hz	at Pout=0dBm

9.3 2G Transmitter Chain Performance Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
2G Transmitter Output						
Output Return Loss	S_{22}		-10		dB	50Ω load
Max Output Power, LB (GMSK)	P_{max}	1	3	5	dBm	
Max Output Power, HB (GMSK)	P_{max}	0.5	2.5	4.5	dBm	

Max Output Power, LB (8PSK)	P_{max}	-2			dBm	
Max Output Power, HB (8PSK)	P_{max}	0			dBm	
Min Output Power (8PSK)	P_{min}		-44		dBm	
ORFS 400k, LB (GMSK)	$ORFS_{400k}$		-69		dBc	
ORFS 400k, HB (GMSK)	$ORFS_{400k}$		-66		dBc	
ORFS 400k, LB (8PSK)	$ORFS_{400k}$		-66		dBc	
ORFS 400k, HB (8PSK)	$ORFS_{400k}$		-65		dBc	
Modulation accuracy (GMSK)						
RMS phase error, LB	Φ_{RMS}		0.5		deg	
RMS phase error, HB	Φ_{RMS}		0.9		deg	
PEAK phase error, LB	Φ_{Peak}		2.5		deg	
PEAK phase error, HB	Φ_{Peak}		4.5		deg	
Modulation accuracy (8PSK)						
RMS EVM, LB	EVM_{RMS}		1.8		%	
RMS EVM, HB	EVM_{RMS}		2.1		%	
Peak EVM, LB	EVM_{Pk}		8		%	
Peak EVM, HB	EVM_{Pk}		14		%	
Origin offset suppression	OOS		-40		dB	
Sideband suppression			-45		dB	
Noise Emissions (GMSK)						
20MHz offset, LB			-168		dBc/Hz	
32MHz offset, LB			-170		dBc/Hz	
20MHz offset, HB			-164		dBc/Hz	
32MHz offset, HB			-165		dBc/Hz	
Noise Emissions (8PSK)						
20MHz offset, LB			-157		dBc/Hz	at Pout=-4dBm
32MHz offset, LB			-158		dBc/Hz	
68MHz offset, LB			-160		dBc/Hz	For G700 RX band noise
20MHz offset, HB			-156		dBc/Hz	
32MHz offset, HB			-157		dBc/Hz	
Harmonic Emissions						
2^{nd} harmonic			-25		dBc	
3^{rd} harmonic			-10		dBc	
4^{th} harmonic			-25		dBc	

9.4 Transmitter Power Control Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Power detector						
RF Input Frequency	F_{det}	824		1980	MHz	
Input Return Loss	S_{11}		-10		dB	Ref. impedance 50Ω
Maximum Input Signal	$P_{det,max}$			0	dBm	
Minimum Input Signal	$P_{det,min}$	-40			dBm	
Measurement Accuracy		-0.3		0.3	dB	
Measurement Time			16		us	

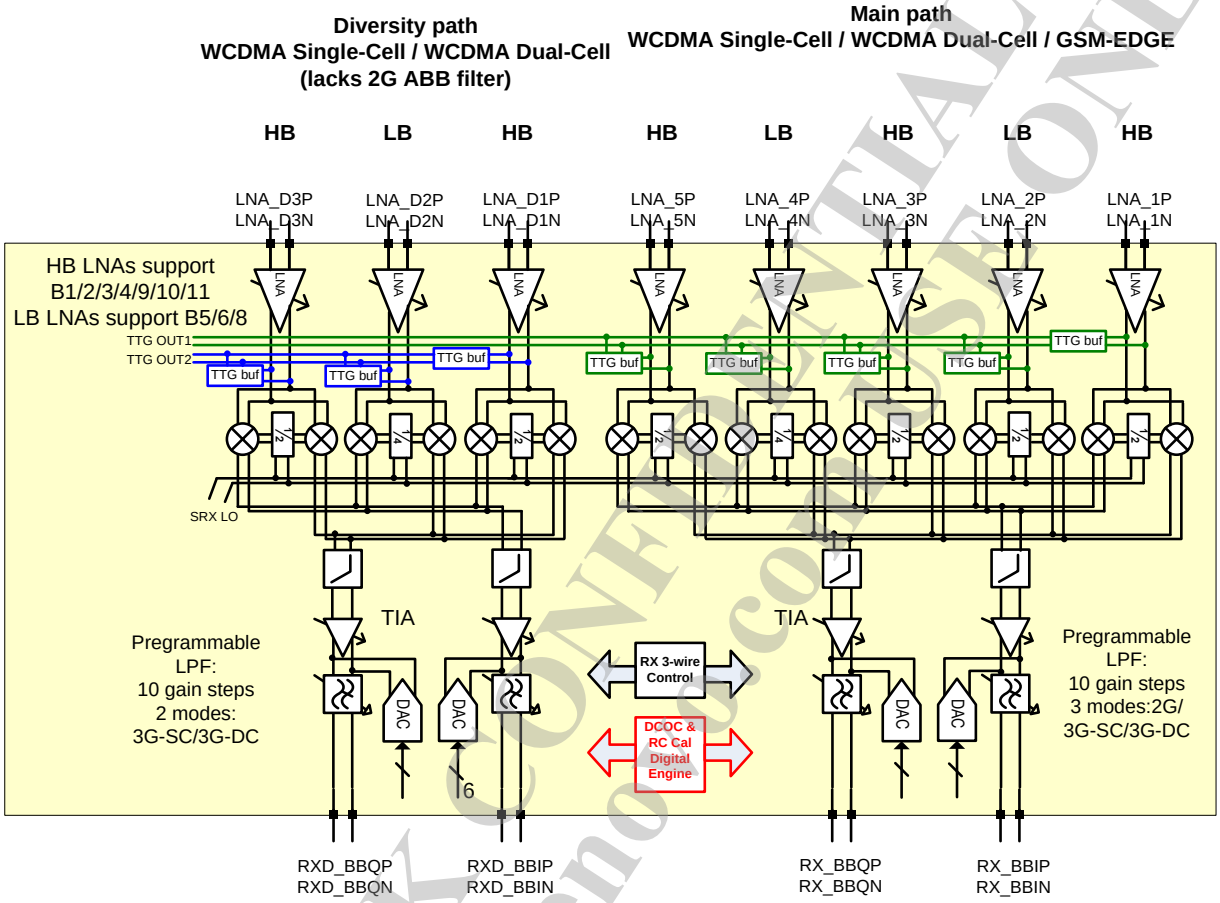
10 Transmit Synthesizer (STX)

10.1 Overall Specifications

Parameter	Conditions	Min	Nom	Max	Unit
Frequency		2856		3960	MHz
Frequency with margin	4.7% margin at fmax and 15% margin at fmin	2429		4146	MHz
Reference Frequency			26		MHz
Channel Resolution	23 bit SDM		3.1		Hz
Frequency error in GGE TX/RX Mode (Type-II)	Synthesizer only		0.01	-	ppm
3-dB Bandwidth in all Modes	Nominal conditions across all frequency	76		159	kHz
Total Integrated Phase Noise in Synthesizer Mode	1KHz to 10MHz, measured at 2GHz LO			0.54	deg
Spot Phase Noise @400KHz in GGE TX HB	Synthesizer + DCO, measured at the HB LO		-123	-121	dBc/Hz
Spot Phase Noise @20MHz in GGE TX LB	Synthesizer + DCO, measured at the DCO frequency, NTC1			-156	dBc/Hz
Spot Phase Noise @32MHz in GGE TX LB	Synthesizer + DCO, measured at the DCO frequency, NTC1			-160	dBc/Hz
Spot Phase Noise @48MHz in 3G B11 (HB)	Synthesizer + DCO, measured at the DCO frequency, NTC1			-164	dBc/Hz
Spot Phase Noise @45MHz in 3G B5/B6/B8 (LB)	Synthesizer + DCO, measured at the DCO frequency, NTC1			-159	dBc/Hz
Spot Phase Noise @80MHz in 3G B2 (HB)	Synthesizer + DCO, measured at the DCO frequency, NTC1			-165	dBc/Hz
Spot Phase Noise @95MHz in 3G B3/B9 (HB)	Synthesizer + DCO, measured at the DCO frequency, NTC1			-167	dBc/Hz
Spot Phase Noise @190MHz in 3G B1 (HB)	Synthesizer + DCO, measured at the DCO frequency, NTC1			-168	dBc/Hz
Spur @400KHz in GGE mode	Measured at the HB LO		--80	-65	dBc
Spur @26MHz in any Mode	Measured at the VCO frequency		Take exception		dBc
Locking time in GGE Mode	Include CLKG power-up (50uS), sub-band(32uS), and Kdco calibration(92uS)			170	uS
Locking time in 3G Mode	Include CLKG power-up (50uS), sub-band calibration(32uS), and settling (46uS)			113	uS
Current consumption GGE Mode (LB)	Including DCO/TDC/MMD/DIG LDO's, SX buffer, and TX LO driver		28.6		mA
Current consumption GGE Mode (HB)	Including DCO/TDC/MMD/DIG LDO's, SX buffer, and TX LO driver		31		mA

Current consumption 3G Mode (exclude B11)	Including DCO/TDC/MMD/DIG LDO's, SX buffer, and TX LO driver		25		mA
Current consumption 3G Mode (B11)	Including DCO/TDC/MMD/DIG LDO's, SX buffer, and TX LO driver		28.6		mA

11 Receiver Specification



The receiver operates in 3 basic modes

1. Direct Conversion (single carrier “SC” WCDMA)
2. Low-IF 2.5MHz nominal (dual cell “DC” WCDMA)
3. Low IF 26MHz*4*10/(96*64) ~ 169.27083kHz (GGE)

Furthermore for SC and DC mode both single receiver and diversity receiver modes are supported. No GGE mode filter setting is supported on the diversity path.

11.1 Receiver Timing Specifications

Parameter	Conditions	Min	Nom	Max	Unit
Settling time for combined gain and DC offset DAC change	Synchronous update of gain and DAC codes			5	µs
Filter RC calibration time	Automatic calibration with 104MHz clock frequency		22	32	µs

Note 1: Excluding frequency synthesizer.

11.2 Receiver Front-End

11.2.1 Target Specification

Parameter	Conditions	Min	Nom	Max	Unit
Differential Input Impedance			100		Ω
Differential Input Return Loss	Note 1	-10			dB
Input Frequency	For all bands	728		2170	MHz
Voltage gain	Maximum. Note 2		33		dB
	Mid. Note 2		21		dB
	Minimum. Note 2		3		dB
	LNA in Off state, mixer active		-7		dB
3 dB cut-off frequency	All modes. Note 3		6		MHz
Noise Figure	Notes 1, 4, 6; max gain; RXFE only		1.9	2.2	dB
	Notes 1, 5, 6; max gain; RXFE only		1.9	2.2	dB
	Notes 1, [4 or 5], 7; max gain				dB
Input IP3	±10MHz and ±20MHz offset, WCDMA	-11	-8		dBm
	±3.5MHz and ±6.5MHz offset, WCDMA, max gain	-11	-8		dBm
	±3.5MHz and ±6.5MHz offset, WCDMA, med gain	-4	-2.5		dBm
	±3.5MHz and ±6.5MHz offset, WCDMA, low gain	10	13		dBm
	-80MHz and -160MHz offset, WCDMA. Note1	-6	-5		dBm
	-95MHz and -190MHz offset, WCDMA. Note 1	-6	-5		dBm
	-45MHz and -90MHz offset, WCDMA. Note 1	-9	-7.5		dBm
	GMSK w Tx blocker, med gain, band V	-5	-4		dBm
	GMSK w Tx blocker, max gain, band V	-9.5	-8.5		dBm
	±0.8MHz and ±1.6MHz offset, GGE, max gain	-10	-8		dBm
Input IP2 (No calibration, nor digital compensation)	WCDMA, Tx offset, bands I, VIII	49	60		dBm
	WCDMA, Tx offset, bands II, V	49	60		dBm
	±4.5MHz and ±5.5MHz offset, WCDMA, low gain	50	75		dBm
	±14.5MHz and ±15.5MHz offset, WCDMA, max gain	40	55		dBm
	GGE mode, AM test.	25	40		dBm
Supply voltage		1.45	1.5	1.6	V
Current consumption	From 1.5 V supply, max. gain. Note9		34		mA

Note 1: Source/Reference impedance: 100 Ω
Note 2: From the chip pins and driven from a 100 Ω source
Note 3: TIA bandwidth variation after calibration
Note 4: Noise averaged over WCDMA channel.
Note 5: Noise averaged over GGE channel.
Note 6: No blockers.
Note 7: With blockers, including, in WCDMA mode, the own transmit signal.
Note 8: Includes LNA, mixer, LO divide-by-2 and buffers, TIA
Note 9: Includes RX LDO, LNA, LO divide-by-2 (or divide-by-4), 25% duty-cycle generation and buffers, TIA

11.2.2 Receiver Front End Mapping

LNA # in path 1	High / Low	Config #1	Config #2	Config #3
1	H	Band 2 / 1900		
2	L	Band 5 / 850		
3	H	Band 1 / 4		
4	L	Band 8 / 900		
5	H	1800		

LNA # in path 2	High / Low	Config #1	Config #2	Config #3
1	H	Band 1 / 4		
2	L	Band 5 / 8		
3	H	Band 2		

12 Rx Synthesizer Specification

Parameter	Conditions/comment	Min	Nom	Max	Unit
Synthesizer Frequency		2951.8		4340	MHz
Reference Frequency			26		MHz
Channel Resolution	Measured at VCO frequency			±25	Hz
3-dB Closed-Loop Bandwidth in GGE Mode	Nominal conditions and 3980MHz VCO frequency		130		kHz
3-dB Closed-Loop Bandwidth in 3G Mode	Nominal conditions and 4340MHz VCO frequency		130		kHz
Total Integrated Phase Noise in GGE	200Hz to 10MHz		0.35	0.45	deg-rms
Total Integrated Phase Noise in 3G	1KHz to 10MHz		0.35	0.45	deg-rms
Spot Phase Noise @400KHz in GGE	Synthesizer + VCO, Measured at the VCO frequency		-113	-111.5	dBc/Hz
Spur @61KHz / @122KHz in GGE mode	Measured at the 2GHz LO		-67	-65	dBc
Spur @400KHz / @600KHz in GGE mode	Measured at the 2GHz LO		-80		dBc
Spur @340KHz in GGE mode	Measured at the 2GHz LO		-80		dBc
Spur @26MHz in any Mode	Measured at the VCO frequency		-95		dBc
Spur @78MHz in any Mode	Measured at the VCO frequency		-95		dBc
Frequency gap left after VCO sub-band cal.	Used to calculate lock time. Across all bands.			10	MHz
Lock Time in GGE mode	Includes Sub-band cal, but not LDO power-up.Phase Error < 2.5deg		110	140	µs
Lock Time in 3G Mode	Includes Sub-band cal, but not LDO power-up. Phase Error < 5 deg		90	120	µs
Temperature drift absorbable after lock in Band XI	Maximum temperature drift before Synthesizer looses lock and needs to be re-locked	115			degC
Temperature drift absorbable after lock in all bands exept band XI	Maximum temperature drift before Synthesizer looses lock and needs to be re-locked	150			degC

13 Digital Control Interfaces

13.1 Introduction

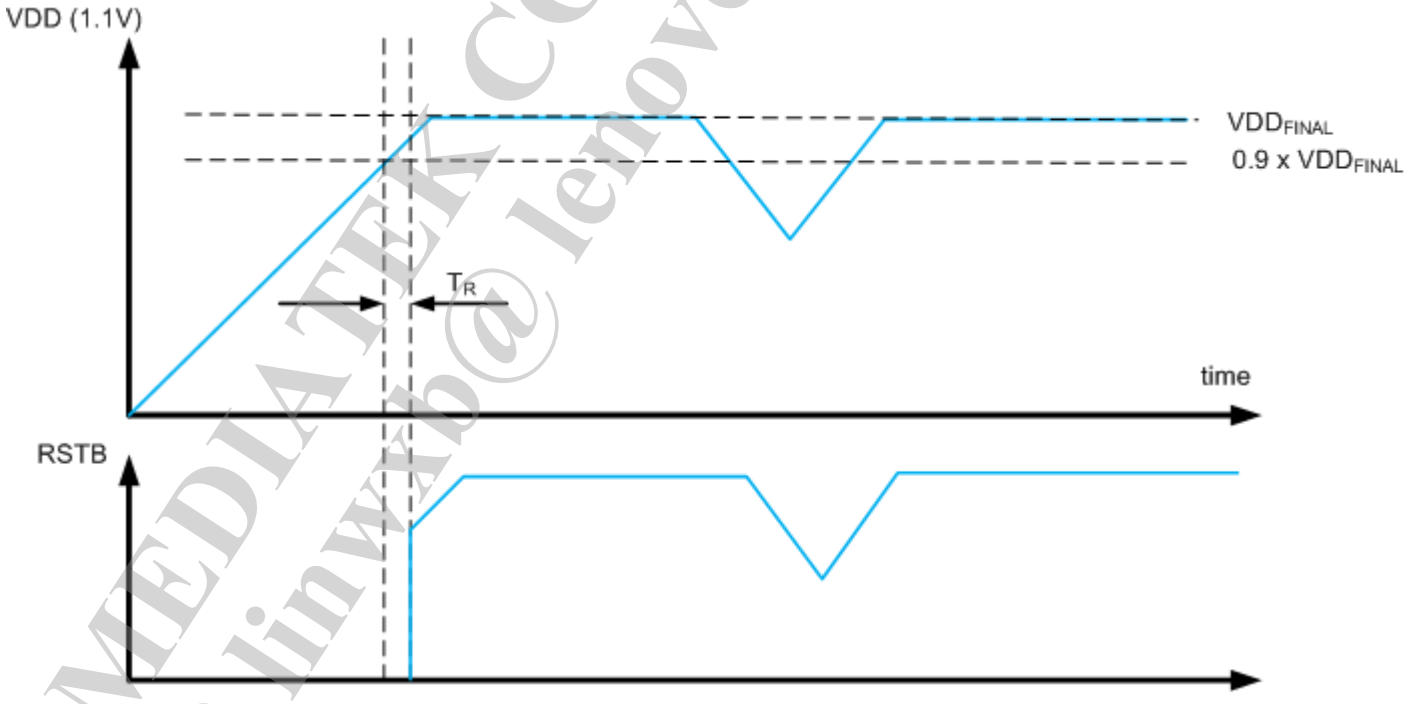
RFSYS is programmed through 5 BSI GPIO PADs. Both write and read operations are supported and 5 wires are used (3 bi-direction data pins, one clock pin, and one enable pin). All BSI interfaces are through VIO18 domain.

13.2 Power-On Reset

The chip includes two Power-On Reset (POR) operating from the static domain LDO's on the VXODIG domain. These operate on the DCXO_DIGITAL and GLOBAL_STATIC digital blocks from the 1.1V supply domain directly derived from VXODIG via LDO's. The designs are identical and since VXODIG is an "always-on" supply then a simplified implementation can be used - specifically there should not be situation where the VXODIG supply can drop after the internal LDO is enabled. The important point then is that the reset needs to be active for sufficiently long that the power supply has stabilized but short enough that the domain is available for BSI programming when requested.

In the case of the DCXO POR the LDO is directly enabled from the VXODIG supply. In the case of the GS LDO VXODIG is always present (in normal mode) and the LDO for this domain is enabled from the baseband.

The operation is shown in the Figure below.



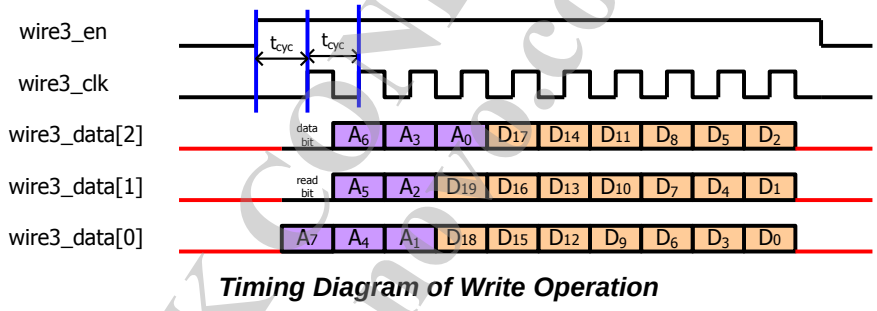
Parameter	Conditions	Min	Nom	Max	Unit	Notes
Reset Active Time T_R	Over range of full VIO18 ramp times	5		200	µs	
VDD		0.8	1.1	1.25	V	

Trigger Point V_{TH}			0.9 x VDD		V	
Idd Quiescent current				<100	nA	

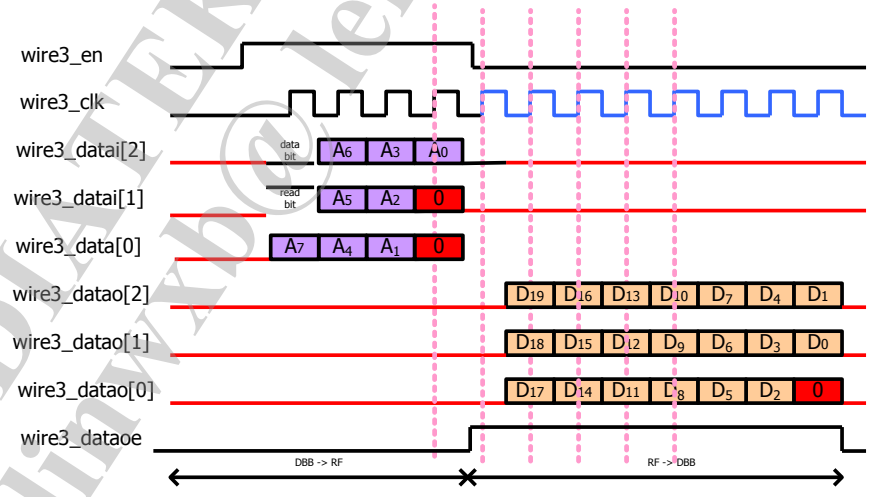
13.3 BSI Interface

The BSI Clock is designed to operate at a maximum frequency of 61.44 MHz, switching down to 30.72 MHz during the read back phase of a read operation.

The BSI clock has nominally a 50% duty cycle (< 40:60 should be guaranteed by the baseband clock generator). Following figure shows the timing diagram of write and read operations via BSI interface.



Timing Diagram of Write Operation



Timing Diagram of Read Operation