MT6250D GSM/GPRS/EDGE-RX SOC Processor Technical Brief

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Preface

Acronyms for register types

R/W	For both read and write access
RO	Read only
RC	Read only. After the register bank is read, every bit that is HIGH(1) will be cleared to LOW(0) automatically.
WO	Write only
W1S	Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be set to 1. Data bits that are LOW(0) have no effects on the corresponding bit.
W1C	Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be cleared to 0. Data bits that are LOW(0) have no effects on the corresponding bit.

1 System Overview

MT6250D is a monolithic chip integrating leading edge power management unit, analog baseband and radio circuitry based on the low-power CMOS process.

MT6250D is a feature-rich and extremely powerful single-chip solution for high-end GSM/GPRS and EDGE-Rx capability. Based on the 32-bit ARM7EJ-S™ RISC processor, MT6250D's superb processing power, along with high bandwidth architecture and dedicated hardware support, provides a platform for high-performance GPRS/EDGE-Rx Class 12 MODEM application and leading-edge multimedia applications.

MT6250D also features:

- A highly integrated Bluetooth transceiver which is fully compliant with Bluetooth specification v3.0.
- A FM receiver supporting both audio broadcast de-modulation and RDS/RBDS data decoding.

Typical application diagram is shown in Figure 1.

Platform

MT6250D is capable of running the ARM7EJ-S™ RISC processor at up to 260MHz, which provides the best trade-off between system performance and power consumption.

For large amounts of data transfer, high-performance DMA (Direct Memory Access) with hardware flow control is implemented, which greatly enhances the data movement speed while reducing the MCU processing load.

Targeted as a media-rich platform for mobile applications, MT6250D also provides hardware security digital rights management for copyright protection. For further safeguard and to protect the manufacturer's development investment, hardware flash content protection is provided to prevent unauthorized porting of the software load.

Multimedia

The MT6250D multimedia subsystem provides conventional parallel interface and 2-bit serial interface for CMOS sensors. The camera resolution is up to 2M pixels. The built-in Hybrid Motion JPEG Encoder hardware enables real-time capture of high-resolution images and recorder of video format such as MPEG-4 or Motion JPEG with smooth quality. The software-based codec can also be used to process various video types. Besides, MT6250D provides fancy UI capabilities through its hardware 2D accelerator. The 2D accelerator performs high-speed linear transformations with filtering. To take advantage of the high MCU performance, GIF and PNG decoders are implemented by the software.

In addition, MT6250D is implemented with a high-performance audio synthesis technology, as well as a high-quality audio amplifier to provide superior audio experiences.

Connectivity and storage

MT6250D supports UART, USB 1.1 FS/LS , SDIO, HIF interface and MMC/SD storage systems. These interfaces provide MT6250D users with the highest level of flexibility in implementing high-end solutions.

To achieve a complete user interface, MT6250D also brings together all the necessary peripheral blocks for a multimedia GSM/GPRS/EDGE-RX phone. The peripheral blocks include the keypad scanner with the capability to detect multiple key presses, SIM controller, real-time clock, PWM, serial/parallel LCD controller and general-purpose programmable I/Os.

Audio

Using a highly integrated mixed-signal audio front-end, the MT6250D architecture provides easy audio interfacing with direct connection to the audio transducers. The audio interface integrates A/D converters for voice band, as well as high-resolution stereo D/A converters for both audio and voice band.

MT6250D supports AMR codec to adaptively optimize the quality of speech and audio. Moreover, HE-AAC codec is implemented to deliver CD-quality audio at low bit rates.

In addition, a 850mW class-AB amplifier is also embedded to save the BOM cost of adopting external amplifiers.

GSM/GPRS/EDGE-Rx radio

MT6250D integrates a mixed-signal baseband front-end in order to provide a well-organized radio interface with flexibility for efficient customization. The front-end contains gain and offset calibration mechanisms and filters with programmable coefficients for comprehensive compatibility control on RF modules. MT6250D achieves outstanding MODEM performance by utilizing a highly dynamic range ADC in the RF downlink path.

MT6250D embeds a high-performance and completely integrated SAW-less RF transceiver for multi-band GSM cellular system. In this RF transceiver, a quad-band receiving feature with high sensitivity is supported utilizing two RF differential receivers and a fully integrated channel filter. With ultra-high dynamic range, the SAW filters on the receiving path can be removed for BOM cost reduction. In addition, the minimum component count is guaranteed by realizing a highly integrated transmitter, low-spur frequency synthesizer and a Digitally-Controlled Crystal Oscillator (DCXO).

Bluetooth radio

MT6250D offers a highly integrated Bluetooth radio and baseband processor. Only a minimum of external components are required. MT6250D provides superior sensitivity and class 1 output power and thus ensures the quality of the connection with a wide range of Bluetooth devices.

MT6250D is fully compliant with Bluetooth v3.0 and offers enhanced data rates of up to 3Mbps. It also provides the coexistence protocol with 802.11 system.

MT6250D supports rich Bluetooth profiles, enabling diversified applications that are widely used on the handset with excellent interoperability.

FM radio

The FM radio subsystem provides a completely integrated FM Rx receiver supporting 87.5 ~ 108MHz FM bands with 50kHz tuning step. It also performs fast channel seek/scan algorithm to validate 200 carrier frequencies in 6 seconds. In addition to receiving FM audio broadcasting, the digital RDS/RBDS data system is supported as well. The integrated FM transceiver utilizes state-of-the-art digital demodulation/modulation techniques to achieve excellent performance.

In order to achieve high SINAD, good sensitivity and excellent noise suppression, the FM receiver adopts adaptive demodulation scheme to optimize Rx system performance in all ranges of signal quality by reference of a very sophisticated channel quality index (CQI). When the received signal quality is poor, the design not only enhances the ACI rejection capability but also uses a very ingenious skill to soft mute annoying noise so as to provide good perception quality.

The FM radio subsystem supports both long antenna, which is usually an earphone, and auto-calibrated short antenna, which is usually a FPC short antenna or shared antenna with GSM for different application scenarios.

Debugging function

The JTAG interface enables in-circuit debugging of the software program with the ARM7EJ-S™ core. With this standardized debugging interface, MT6250D provides developers with a wide set of options in choosing ARM development kits from different third party vendors.

Power management

A power management is embedded in MT6250D to provide rich features a high-end feature phone supports, including Li-ion battery charger, high performance and low quiescent current LDOs, and drivers for LED and backlight.

MT6250D offers various low-power features to help reduce the system power consumption. MT6250D is also fabricated in an advanced low-power CMOS process, hence providing an overall ultra-low leakage solution.

Package

The MT6250D device is offered in a 9.8mm×9.6mm, 233-ball, 0.5mm pitch, TFBGA package.

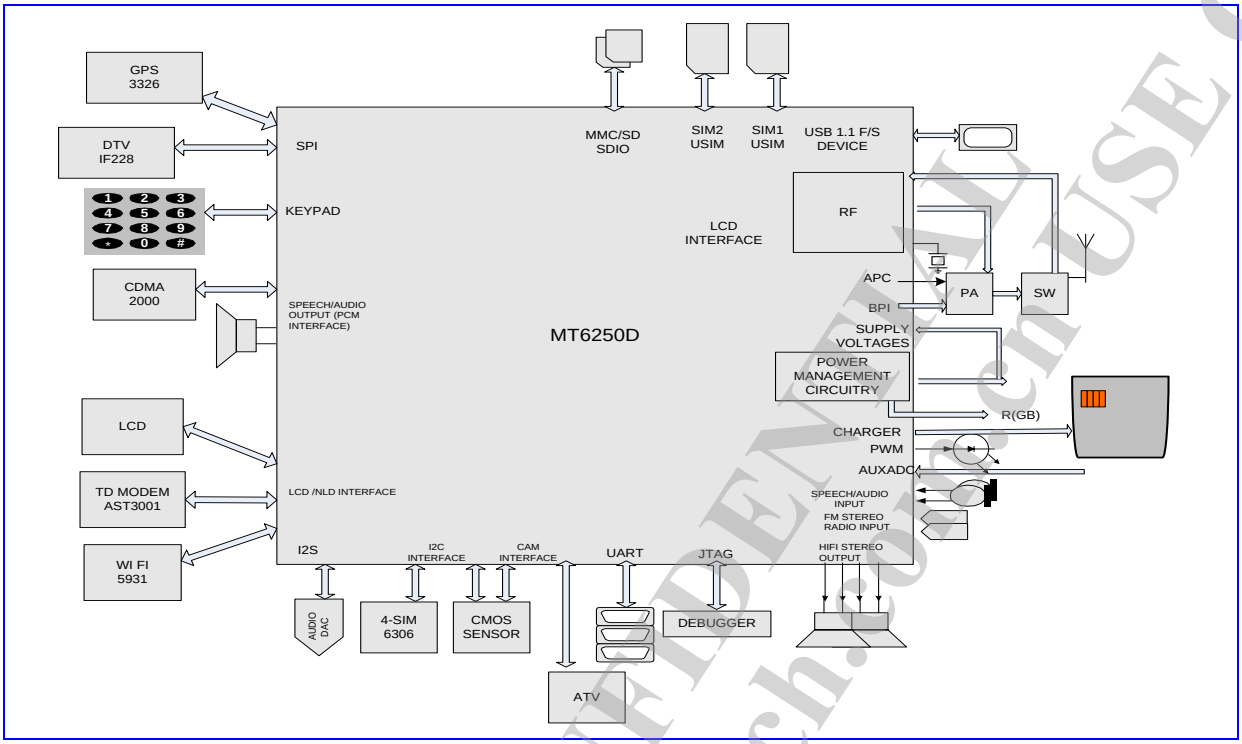


Figure 1. Typical application of MT6250D

1.1 Platform Features

General

- Integrated voice-band, audio-band and base-band analog front-end
- Integrated full-featured power management unit

MCU subsystem

- ARM7EJ-S™ 32-bit RISC processor
- Java hardware acceleration for fast Java-based games and applets
- Operating frequency: Max. 260MHz with dynamic clock gating
- High-performance multi-layer AHB bus
- Dedicated DMA bus with 17 DMA channels
- On-chip boot ROM for factory flash programming
- Watchdog timer for system crash recovery
- 4 sets of general-purpose timers
- Circuit switch data coprocessor
- Division coprocessor

User interfaces

- 8-row × 8-column and 5-row x 5-column keypad controller with hardware scanner
- Supports multiple key presses for gaming
- Dual SIM/USIM controller with hardware T = 0/T = 1 protocol control
- Real-time clock (RTC) operating with a low-quiescent-current power supply
- General-purpose I/Os (GPIOs) available for auxiliary applications
- 1 sets of Pulse Width Modulation (PWM) output
- 13 external interrupt lines
- 1 external channel auxiliary 10-bit A/D converter

Security

- Supports security key and chip random ID

Connectivity

- 3 UARTs with hardware flow control and supports baud rate up to 921,600 bps
- FS/LS USB 1.1 device controller
- Multimedia card, secure digital Memory Card, host controller with flexible I/O voltage power
- Supports SDIO interface for SDIO peripherals as well as WIFI connectivity
- DAI/PCM and I2S interface for audio applications
- I2C master interface for peripheral management including image sensors
- SPI master interface for peripheral management including digital TV chips

Power management

- Li-ion battery charger
- 16 LDOs for the power supply of memory card, camera, Bluetooth, RF, SIM card and other diversified usage
- 4 open-drain output switches to supply/control the LED
- LDO type vibrator
- One NMOS switch to control keypad LED
- Thermal overload protection
- Under-voltage lock-out protection
- Over-voltage protection
- Different levels of power-down modes with sophisticated software control enables excellent power saving performance.

Test and debugging

- Built-in digital and analog loop back modes for both audio and baseband front-end
- DAI port complies with GSM Rec.11.10.
- JTAG port for debugging embedded MCU

1.2 MODEM Features

Radio interface and baseband front-end

- Digital PM data path with baseband front-end
- High dynamic range delta-sigma ADC converts the downlink analog I and Q signals to digital baseband.
- 10-bit D/A converter for Automatic Power Control (APC)
- Programmable radio Rx filter with adaptive gain control
- Dedicated Rx filter for FB acquisition
- 4-pin Baseband Parallel Interface (BPI) with programmable driving strength
- Supports multi-band

Voice and modem CODEC

- Dial tone generation
- Voice memo
- Noise reduction
- Echo suppression
- Advanced sidetone oscillation reduction
- Digital sidetone generator with programmable gain
- Two programmable acoustic compensation filters
- GSM quad vocoders for adaptive multirate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
- GSM channel coding, equalization and A5/1, A5/2 and A5/3 ciphering
- GPRS GEA1, GEA2 and GEA3 ciphering
- Programmable GSM/GPRS/EDGE-Rx modem
- Packet switched data with CS1/CS2/CS3/CS4 coding schemes
- GSM circuit switch data
- GPRS/EDGE-Rx Class 12
- Supports SAIC (single antenna interference cancellation) technology
- Supports VAMOS(Voice services over Adaptive Multi-user channels on One Slot) technology in R9 spec.

Voice interface and voice front-end

- Two microphone inputs share one low-noise amplifier with programmable gain and Automatic Gain Control (AGC) mechanisms
- Voice power amplifier with programmable gain
- 2nd order Sigma-Delta A/D converter for voice uplink path
- Shares D/A converter with audio playback path
- Supports full-duplex hands-free operation
- Compliant with GSM 03.50

1.3 GSM/GPRS/EDGE RF Features

Receiver

- Quad band differential input LNAs
- Quadrature RF mixers
- Fully integrated channel filter
- High dynamic range ADC
- 24dB PGA gain with 6dB gain step

Transmitter

- Transmitter outputs support quad bands.
- Highly precise and low noise RF transmitter for GSM/GPRS applications

Frequency synthesizer

- Programmable fractional-N synthesizer
- Integrated wide range RFVCO
- Integrated loop filter
- Fast settling time suitable for multi-slot GPRS/EDGE-Rx applications

Digitally-Controlled Crystal Oscillator (DCXO)

- Two-pin 26MHz crystal oscillator
- On-chip programmable capacitor array for coarse-tuning
- On-chip programmable capacitor array for fine-tuning
- Low power mode supports 32K crystal removal

1.4 Multimedia Features

LCD/TD-modem/WiFi interface

- Dedicated parallel interface supports 3 external devices with 8-bit for TD-modem/WiFi interface and 8-/9-bit for parallel LCD interface.

LCD controller

- Supports simultaneous connection to 2 parallel and 2 serial LCD modules
- LCM formats supported: RGB332, RGB444, RGB565, RGB666, RGB888
- Supports LCD module with maximum resolution up to 480x320
- Per pixel alpha channel
- True color engine
- Supports hardware display rotation
- Capable of combining display memories with up to 4 blending layers

Camera interface

- YUV422 format image input
- Capable of processing image of size up to 0.3M pixels (Mediatek serial interface) and 2M pixels (w/o compression)

JPEG decoder

- Baseline JPEG decoding
- Supports various YUV formats, DC/AC Huffman tables and quantization tables

JPEG encoder

- Hybrid motion JPEG encoder for video encoding
- ISO/IEC 10918-1 JPEG baseline mode
- ISO/IEC 10918-2 compliance
- Supports YUV420 and grayscale formats
- Supports EXIF/JFIF
- Standard DC and AC Huffman tables
- Provides 5 levels of encode quality
- Supports zeros shutter delay

Image data processing

- Supports 4x digital zoom
- High throughput hardware scaler. Capable of tailoring an image to an arbitrary size.
- Horizontal scaling with bilinear interpolation
- Vertical scaling with bilinear interpolation
- YUV and RGB color space conversion
- RGB/YCbCr format thumbnail output

MPEG-4/H.263 CODEC

- Hybrid MPEG4 encoder
- Software-based MPEG4 decoder
- ISO/IEC 14496-2 simple profile:
- Decode @ level 0/1/2/3
- Encode @ level 0
- ISO/IEC 14496-2 advanced simple profile:
- Decode @ level 0/1/2/3
- ITU-T H.263 profile 0 @ level 40
- Supports visual tools for decoder: I-VOP, P-VOP, B-VOP, AC/DC prediction, 4-MV, unrestricted MV, error resilience, short header, global motion compensation, method 1/2 quantization, quarter-pel motion compensation.
- Error resilience for decoder: Slice resynchronization, data partitioning, reversible VLC
- Supports visual tools for encoder: I-VOP, P-VOP, Half-Pel, DC prediction, unrestricted MV, short header

H.264

- ISO/IEC 14496-10 baseline profile:
- Decode @ level 1

2D accelerator

- Supports 32-bpp ARGB8888, 24-bpp RGB888, 16-bpp RGB565, 24-bpp ARGB6666.
- 4 layers overlay with individual color format, window size, source key, constant alpha and rotation
- Rectangle fill with constant
- BitBlt: Capable with 7 rotation types

- Alpha blending with 7 rotation types, per-pixel alpha and pre-multiplied alpha
- Font drawing: Normal font and anti-aliasing font
- Linear transformation: Supports perspective transform, truncate/nearest/bi-linear sample filter.

Audio CODEC

- Supports HE-AAC codec decoding
- Supports AAC codec decoding
- Wavetable synthesis with up to 64 tones
- Advanced wavetable synthesizer capable of generating simulated stereo
- Wavetable including GM full set of 128 instruments and 47 sets of percussions
- PCM playback and record
- Digital audio playback

Audio interface and audio front-end

- Supports I2S interface
- High-resolution D/A converters for stereo audio playback
- Voice band A/D converter with digital MIC input support
- Stereo to mono conversion

1.5 Bluetooth Features

Radio features

- Fully compliant with Bluetooth specification 3.0 + EDR
- Low out-of-band spurious emissions support simultaneous operation with GPS and GSM/GPRS worldwide radio systems
- Low-IF architecture with high degree of linearity and high order channel filter
- Integrated T/R switch and Balun
- Fully integrated PA provides 10dBm output power
- -95dBm sensitivity with excellent interference rejection performance
- Hardware AGC dynamically adjusts receiver performance in changing environments

Baseband features

- Up to 4 simultaneous active ACL links
- Up to 1 simultaneous SCO or eSCO link with CVSD coding
- Supports eSCO
- Scatternet support: Up to 4 piconets simultaneously with background inquiry/page scan
- Supports sniff mode
- AFH and PTA collaborative support for WLAN/BT coexistence
- Idle mode and sleep mode enables ultra-low power consumption.
- Supports PCM interface and built-in programmable transcoders for linear voice with re-transmission
- Built-in hardware modem engine for access code correlation, header error correction, forward error correction, CRC, whitening and encryption
- Channel quality driven data rate adaptation
- Channel assessment for AFH

Platform features

- Embedded processor for Bluetooth protocol stack with built-in memory system
- Fully verified ROM based system with code patch for feature enhancement

1.6 FM Features

- 87.5-108MHz worldwide FM bands with 50kHz tuning step
- Supports RDS/RBDS radio data system
- Supports long/short antenna
- 30ms seek time per channel, and 6sec search time for all channels
- Superior stereo noise reduction
- Supports 32.768kHz clock as reference clock
- Soft mute volume control
- Supports short antenna, auto calibration for different FM channels
- 58dB SINAD with 22.5kHz FM deviation
- 3dBuVemf FM RX sensitivity with superior interference rejection
- 20dBuVemf RDS sensitivity (dev: 2kHz)
- More than 55dBc rejection capability against -200kHz ACI

1.7 General Descriptions

Figure 2 is the block diagram of MT6250D. Based on a multi-processor architecture, MT6250D integrates an ARM7EJ-S™ core, the main processor running high-level GSM/EDGE-Rx protocol software as well as multimedia applications, single digital signal processor core, which manages the low-level MODEM and advanced audio functions, an embedded processor running Bluetooth baseband and link control protocol and the Bluetooth radio control.

MT6250D consists of the following subsystems:

- Microcontroller Unit (MCU) subsystem: Includes an ARM7EJ-S™ RISC processor and its accompanying memory management and interrupt handling logics
- Digital Signal Processor (DSP) subsystem: Includes a DSP and its accompanying memory, memory controller and interrupt controller
- MCU/DSP interface: Junction at which the MCU and the DSP exchange hardware and software information
- Microcontroller peripherals: Include all user interface modules and RF control interface modules
- Microcontroller coprocessors: Run computing-intensive processes in place of the microcontroller
- DSP peripherals: Hardware accelerators for GSM/GPRS/EDGE-Rx channel codec
- Multimedia subsystem: Integrates several advanced accelerators to support multimedia applications
- Voice front-end: Data path for converting analog speech to and from digital speech
- Audio front-end: Data path for converting stereo audio from an audio source
- Baseband front-end: Data path for converting a digital signal to and from an analog signal from the RF modules
- Timing generator: Generates the control signals related to the TDMA frame timing
- Power, reset and clock subsystem: Manage the power, reset and clock distribution inside MT6250D.
- Bluetooth subsystem: Includes an embedded processor with embedded ROM/RAM system, baseband processor, and a high-performance radio block
- Power management unit: Self-contained power supply source which also controls the charging and system startup circuitry.

Details of the individual subsystems and blocks are described in the following chapters.

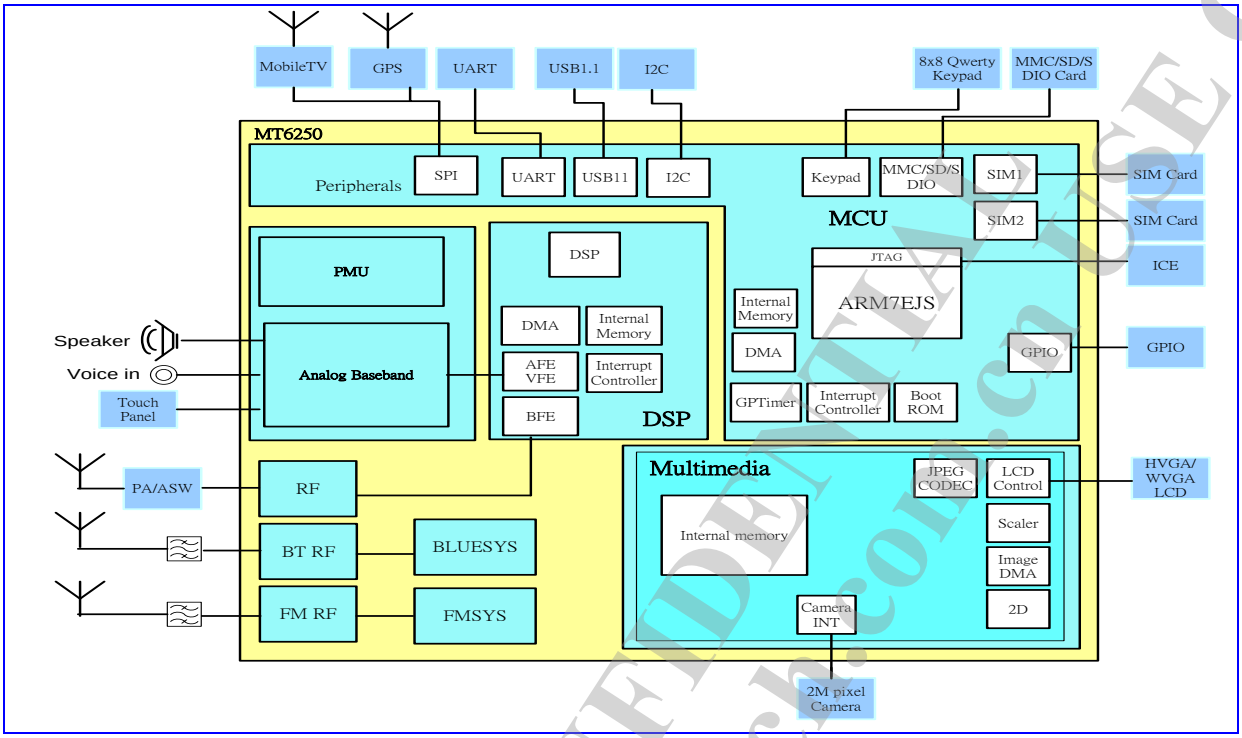


Figure 2. MT6250D block diagram

2 Product Descriptions

2.1 Pin Description

2.1.1 Ball Diagram

For MT6250D, an TFBGA 9.8mm*9.6mm, 233-ball, 0.5mm pitch package is offered. Pin-outs and the top view are illustrated in Figure 3 for this package.

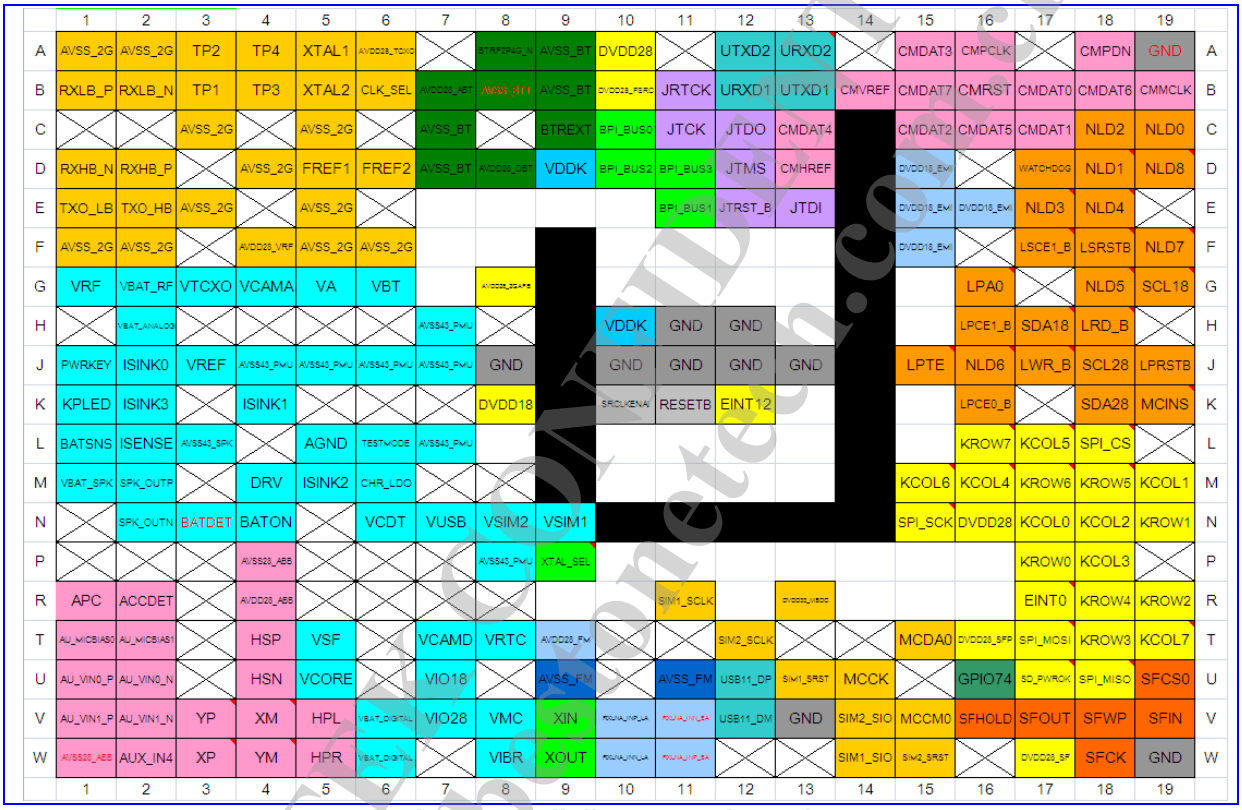


Figure 3. Ball diagram and top view

2.1.2 Pin Coordination

Pin#	Net name	Pin#	Net name	Pin#	Net name
A1	AVSS_2G	F19	NLD7	N7	VUSB
A10	DVDD28	F2	AVSS_2G	N8	VSIM2
A12	UTXD2	F4	AVDD28_VRF	N9	VSIM1
A13	URXD2	F5	AVSS_2G	P17	KROW0
A15	CMDAT3	F6	AVSS_2G	P18	KCOL3
A16	CMPCLK	G1	VRF	P4	AVSS28_ABB
A18	CMPDN	G16	LPA0	P8	AVSS43_PMU
A19	GND	G18	NLD5	P9	XTAL_SEL
A2	AVSS_2G	G19	SCL18	R1	APC
A3	TP2	G2	VBAT_RF	R11	SIM1_SCLK

Pin#	Net name	Pin#	Net name	Pin#	Net name
A4	TP4	G3	VTCXO	R13	DVDD33_MSDC
A5	XTAL1	G4	VCAMA	R17	EINT0
A6	AVDD28_TCXO	G5	VA	R18	KROW4
A8	BTRF2P4G_N	G6	VBT	R19	KROW2
A9	AVSS_BT	G8	AVDD28_2GAFE	R2	ACCDET
B1	RXLB_P	H10	VDDK	R4	AVDD28_ABB
B10	DVDD28_FSRC	H11	GND	T1	AU_MICBIAS0
B11	JRTCK	H12	GND	T12	SIM2_SCLK
B12	URXD1	H16	LPCE1_B	T15	MCDA0
B13	UTXD1	H17	SDA18	T16	DVDD28_SFP
B14	CMVREF	H18	LRD_B	T17	SPI_MOSI
B15	CMDAT7	H2	VBAT_ANALOG	T18	KROW3
B16	CMRST	H7	AVSS43_PMU	T19	KCOL7
B17	CMDAT0	J1	PWRKEY	T2	AU_MICBIAS1
B18	CMDAT6	J10	GND	T4	HSP
B19	CMMCLK	J11	GND	T5	VSF
B2	RXLB_N	J12	GND	T7	VCAMD
B3	TP1	J13	GND	T8	VRTC
B4	TP3	J15	LPTE	T9	AVDD28_FM
B5	XTAL2	J16	NLD6	U1	AU_VIN0_P
B6	CLK_SEL	J17	LWR_B	U11	AVSS_FM
B7	AVDD28_ABT	J18	SCL28	U12	USB11_DP
B8	AVSS_BT1	J19	LPRSTB	U13	SIM1_SRST
B9	AVSS_BT	J2	ISINK0	U14	MCCK
C10	BPI_BUS0	J3	VREF	U16	GPIO74
C11	JTCK	J4	AVSS43_PMU	U17	SD_PWROK
C12	JTDO	J5	AVSS43_PMU	U18	SPI_MISO
C13	CMDAT4	J6	AVSS43_PMU	U19	SFCS0
C15	CMDAT2	J7	AVSS43_PMU	U2	AU_VIN0_N
C16	CMDAT5	J8	GND	U4	HSN
C17	CMDAT1	K1	KPLED	U5	VCORE
C18	NLD2	K10	SRCLKENAI	U7	VIO18
C19	NLD0	K11	RESETB	U9	AVSS_FM
C3	AVSS_2G	K12	EINT12	V1	AU_VIN1_P
C5	AVSS_2G	K16	LPCE0_B	V10	RXLNA_INP_LA
C7	AVSS_BT	K18	SDA28	V11	RXLNA_INN_SA
C9	BTREXT	K19	MCINS	V12	USB11_DM
D1	RXHB_N	K2	ISINK3	V13	GND
D10	BPI_BUS2	K4	ISINK1	V14	SIM2_SIO
D11	BPI_BUS3	K8	DVDD18	V15	MCCM0
D12	JTMS	L1	BATSNS	V16	SFHOLD
D13	CMHREF	L16	KROW7	V17	SFOUT
D15	DVDD18_EMI	L17	KCOL5	V18	SFWP
D17	WATCHDOG	L18	SPI_CS	V19	SFIN
D18	NLD1	L2	ISENSE	V2	AU_VIN1_N
D19	NLD8	L3	AVSS43_SPK	V3	YP

Pin#	Net name	Pin#	Net name	Pin#	Net name
D2	RXHB_P	L5	AGND	V4	XM
D4	AVSS_2G	L6	TESTMODE	V5	HPL
D5	FREF1	L7	AVSS43_PMU	V6	VBAT_DIGITAL
D6	FREF2	M1	VBAT_SPK	V7	VIO28
D7	AVSS_BT	M15	KCOL6	V8	VMC
D8	AVDD28_DBT	M16	KCOL4	V9	XIN
D9	VDDK	M17	KROW6	W1	AVSS28_ABB
E1	TXO_LB	M18	KROW5	W10	RXLNA_INN_LA
E11	BPI_BUS1	M19	KCOL1	W11	RXLNA_INP_SA
E12	JTRST_B	M2	SPK_OUTP	W14	SIM1_SIO
E13	JTDI	M4	DRV	W15	SIM2_SRST
E15	DVDD18_EMI	M5	ISINK2	W17	DVDD28_SF
E16	DVDD18_EMI	M6	CHR_LDO	W18	SFCK
E17	NLD3	N15	SPI_SCK	W19	GND
E18	NLD4	N16	DVDD28	W2	AUX_IN4
E2	TXO_HB	N17	KCOL0	W3	XP
E3	AVSS_2G	N18	KCOL2	W4	YM
E5	AVSS_2G	N19	KROW1	W5	HPR
F1	AVSS_2G	N2	SPK_OUTN	W6	VBAT_DIGITAL
F15	DVDD18_EMI	N3	BATDET	W8	VIBR
F17	LSCE1_B	N4	BATON	W9	XOUT
F18	LSRSTB	N6	VCDT		

Table 1. Pin coordinates

2.1.3 Detailed Pin Description

Abbreviation	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-direction
DI	Digital input
DO	Digital output
DIO	Digital bi-direction
P	Power
G	Ground

Table 2. Acronym for pin types

Pin name	Type	Description	Power domain
System			
GPIO74	DIO	Reserved	DVDD28_SFP
RESETB	DIO	System reset	DVDD18

Pin name	Type	Description	Power domain
SRCLKENAI	DIO	26MHz clock request by external devices	DVDD18
RF control circuitry			
BPI_BUS0	DIO	RF hard-wire control bus bit 0	DVDD28
BPI_BUS1	DIO	RF hard-wire control bus bit 1	DVDD28
BPI_BUS2	DIO	RF hard-wire control bus bit 2	DVDD28
BPI_BUS3	DIO	RF hard-wire control bus bit 3	DVDD28
UART interface			
URXD1	DIO	UART1 receive data	DVDD28
UTXD1	DIO	UART1 transmit data	DVDD28
URXD2	DIO	UART2 receive data	DVDD28
UTXD2	DIO	UART2 transmit data	DVDD28
JTAG interface			
JTMS	DIO	JTAG test port mode switch	DVDD28
JTDI	DIO	JTAG test port data input	DVDD28
JTCK	DIO	JTAG test port clock input	DVDD28
JTRST_B	DIO	JTAG test port reset input	DVDD28
JRTCK	DIO	JTAG test port returned clock output	DVDD28
JTDO	DIO	JTAG test port data output	DVDD28
External interrupt			
EINT0	DIO	External interrupt 0	DVDD28
EINT12	DIO	External interrupt 12	DVDD18
Keypad interface			
KCOL0	DIO	Keypad column 0	DVDD28
KCOL1	DIO	Keypad column 1	DVDD28
KCOL2	DIO	Keypad column 2	DVDD28
KCOL3	DIO	Keypad column 3	DVDD28
KCOL4	DIO	Keypad column 4	DVDD28
KCOL5	DIO	Keypad column 5	DVDD28
KCOL6	DIO	Keypad column 6	DVDD28
KCOL7	DIO	Keypad column 7	DVDD28
KROW0	DIO	Keypad row 0	DVDD28
KROW1	DIO	Keypad row 1	DVDD28
KROW2	DIO	Keypad row 2	DVDD28
KROW3	DIO	Keypad row 3	DVDD28
KROW4	DIO	Keypad row 4	DVDD28
KROW5	DIO	Keypad row 5	DVDD28
KROW6	DIO	Keypad row 6	DVDD28
KROW7	DIO	Keypad row 7	DVDD28
Camera interface			
CMRST	DIO	CMOS sensor reset signal output	DVDD28

Pin name	Type	Description	Power domain
CMPDN	DIO	CMOS sensor power down control	DVDD28
CMVREF	DIO	CMOS sensor vertical reference signal input	DVDD28
CMHREF	DIO	CMOS sensor horizontal reference signal input	DVDD28
CMDAT0	DIO	CMOS sensor data input 0	DVDD28
CMDAT1	DIO	CMOS sensor data input 1	DVDD28
CMDAT2	DIO	CMOS sensor data input 2	DVDD28
CMDAT3	DIO	CMOS sensor data input 3	DVDD28
CMDAT4	DIO	CMOS sensor data input 4	DVDD28
CMDAT5	DIO	CMOS sensor data input 5	DVDD28
CMDAT6	DIO	CMOS sensor data input 6	DVDD28
CMDAT7	DIO	CMOS sensor data input 7	DVDD28
CMPCLK	DIO	CMOS sensor master clock output	DVDD28
CMMCLK	DIO	CMOS sensor master clock output	DVDD28
MS/SD card interface			
MCINS	DIO	SD card detect Input	DVDD18_EMI
MCDA0	DIO	SD serial data IO 0/memory stick serial data IO	DVDD33_MSDC
MCCK	DIO	SD serial clock/memory stick serial clock	DVDD33_MSDC
MCCM0	DIO	SD command output/memory stick bus state output	DVDD33_MSDC
SD_PWROK	DIO	For SD card general-purpose IO	DVDD33_MSDC
SIM card interface			
SIM1_SIO	DIO	SIM1 data input/outputs	VSIM1
SIM1_SRST	DIO	SIM1 card reset output	VSIM1
SIM1_SCLK	DIO	SIM1 card clock output	VSIM1
SIM2_SIO	DIO	SIM2 data input/outputs	VSIM2
SIM2_SRST	DIO	SIM2 card reset output	VSIM2
SIM2_SCLK	DIO	SIM2 card clock output	VSIM2
I2C interface			
SCL28	DIO	I2C clock 2.8v power domain	DVDD28
SDA28	DIO	I2C data 2.8v power domain	DVDD28
SCL18	DIO	I2C clock 1.8v power domain	DVDD18_EMI
SDA18	DIO	I2C data 1.8v power domain	DVDD18_EMI
LCD interface			
LSRSTB	DIO	Serial display interface reset signal	DVDD18_EMI
LSCE1_B	DIO	Serial display interface chip select 1 output	DVDD18_EMI
LPCE1_B	DIO	Parallel display interface chip select 1 output	DVDD18_EMI

Pin name	Type	Description	Power domain
LPCE0_B	DIO	Parallel display interface chip select 0 output	DVDD18_EMI
LPTE	DIO	Parallel display interface tearing effect	DVDD18_EMI
LPRSTB	DIO	Parallel display interface reset signal	DVDD18_EMI
LRD_B	DIO	Parallel display interface read strobe	DVDD18_EMI
LPA0	DIO	Parallel display interface address output	DVDD18_EMI
LWR_B	DIO	Parallel display interface write strobe	DVDD18_EMI
NLD8	DIO	Parallel LCD data 8	DVDD18_EMI
NLD7	DIO	Parallel LCD data 7	DVDD18_EMI
NLD6	DIO	Parallel LCD data 6	DVDD18_EMI
NLD5	DIO	Parallel LCD data 5	DVDD18_EMI
NLD4	DIO	Parallel LCD data 4	DVDD18_EMI
NLD3	DIO	Parallel LCD data 3	DVDD18_EMI
NLD2	DIO	Parallel LCD data 2	DVDD18_EMI
NLD1	DIO	Parallel LCD data 1	DVDD18_EMI
NLD0	DIO	Parallel LCD data 0	DVDD18_EMI
Serial port interface			
SPI_MOSI	DIO	Data signal from master output to slave input	DVDD28
SPI_MISO	DIO	Data signal from slave output to master input	DVDD28
SPI_SCK	DIO	Bit serial clock	DVDD28
SPI_CS	DIO	Low-active chip select signal	DVDD28
Watchdog reset			
WATCHDOG	DIO	Reset external memory device	DVDD18_EMI
General purpose I/O interface			
SFCS0	DIO	General purpose Input/Output 81	DVDD28_SFP
SFIN	DIO	General purpose Input/Output 82	DVDD28_SFP
SFOUT	DIO	General purpose Input/Output 83	DVDD28_SFP
SFSHOLD	DIO	General purpose Input/Output 84	DVDD28_SFP
SFWP	DIO	General purpose Input/Output 85	DVDD28_SFP
SFCK	DIO	General purpose Input/Output 86	DVDD28_SFP
FM			
RXLNA_INN_LA	AI	FM input from long antenna	AVDD28_FM
RXLNA_INP_LA	AI	FM input from long antenna	AVDD28_FM
RXLNA_INN_SA	AI	FM input from short antenna	AVDD28_FM
RXLNA_INP_SA	AI	FM input from short antenna	AVDD28_FM
Bluetooth			
BTRF2P4G_N	AIO	Bluetooth RF single-ended input	-
BTREXT	AIO	Bluetooth external reference resistor	-
2G RF			

Pin name	Type	Description	Power domain
RXHB_P	AIO	Differential RF input for highband Rx (DCS/PCS)	-
RXHB_N	AIO	Differential RF input for highband Rx (DCS/PCS)	-
RXLB_P	AIO	Differential RF input for lowband Rx (GSM900/GSM850)	-
RXLB_N	AIO	Differential RF input for lowband Rx (GSM900/GSM850)	-
TXO_HB	AIO	RF output for highband Tx (DCS/PCS)	-
TXO_LB	AIO	RF output pin for lowband Tx (GSM900/GSM850)	-
FREF1	AIO	DCXO reference clock output	-
FREF2	AIO	DCXO reference clock output	
XTAL1	AIO	Input 1 for DCXO crystal	-
XTAL2	AIO	Input 2 for DCXO crystal	-
TP1	AIO	Test pin 1	-
TP2	AIO	Test pin 2	-
TP3	AIO	Test pin 3	-
TP4	AIO	Test pin 4	-
CLK_SEL	AIO	DCXO mode selection	-
USB			
USB11_DM	AIO	D- data Input/Output	-
USB11_DP	AIO	D+ data Input/Output	-
Analog baseband			
HPR	AIO	Audio head phone output (R channel)	AVDD28_ABB
HPL	AIO	Audio head phone output (L channel)	AVDD28_ABB
HSP	AIO	Voice handset output (positive)	AVDD28_ABB
HSN	AIO	Voice handset output (negative)	AVDD28_ABB
AU_VIN0_P	AIO	Microphone 0 input (positive)	AVDD28_ABB
AU_VIN0_N	AIO	Microphone 0 input (negative)	AVDD28_ABB
AU_VIN1_P	AIO	Microphone 1 input (positive)	AVDD28_ABB
AU_VIN1_N	AIO	Microphone 1 input (negative)	AVDD28_ABB
AUX_IN4	AIO	Auxiliary ADC input	AVDD28_ABB
SPK_OUTP	AIO	Speaker positive output	AVDD28_ABB
SPK_OUTN	AIO	Speaker negative output	AVDD28_ABB
APC	AIO	Automatic power control DAC output	AVDD28_ABB
XP	AIO	Touch panel X-axis positive input	AVDD28_ABB
XM	AIO	Touch panel X-axis negative input	AVDD28_ABB
YP	AIO	Touch panel Y-axis positive input	AVDD28_ABB
YM	AIO	Touch panel Y-axis negative input	AVDD28_ABB
AU_MICBIAS0	AIO	Microphone bias source 0	AVDD28_ABB
AU_MICBIAS1	AIO	Microphone bias source 1	AVDD28_ABB
ACCDET	AIO	Accessory detection	AVDD28_ABB

Pin name	Type	Description	Power domain
Real-time clock			
XIN	AIO	Input pin for 32K crystal	VRTC
XOUT	AIO	Input pin for 32K crystal	VRTC
XTAL_SEL	DIO	Pin option for external 32K crystal	VRTC
Power management unit			
VA	AIO	LDO output for ABB - VA	VBAT_ANALOG
VBT	AIO	LDO output for BTRF - VBT	VBAT_RF
VCAMA	AIO	LDO output for sensor – VCAMA	VBAT_ANALOG
VCAMD	AIO	LDO output for sensor - VCAMD	VBAT_DIGITAL
VIBR	AIO	LDO output for vibrator - VIBR	VBAT_DIGITAL
VIO18	AIO	LDO output for 1.8V power - VIO18	VBAT_DIGITAL
VIO28	AIO	LDO output for 2.8V power - VIO28	VBAT_DIGITAL
VMC	AIO	LDO output for memory card - VMC	VBAT_DIGITAL
VSF	AIO	LDO output - VSF	VBAT_DIGITAL
VRF	AIO	LDO output for GSMRF - VRF	VBAT_DIGITAL
VRTC	AIO	LDO output for RTC - VRTC	VBAT_DIGITAL
VSIM1	AIO	LDO output for 1st SIM - VSIM	VBAT_DIGITAL
VSIM2	AIO	LDO output for 2nd SIM - VSIM2	VBAT_DIGITAL
VTCXO	AIO	LDO output for DCXO - VTCXO	VBAT_ANALOG
VUSB	AIO	LDO output for USB - VUSB	VBAT_DIGITAL
VCORE	AIO	LDO output for core circuit - Vcore	VBAT_DIGITAL
VREF	AIO	Band gap reference	BATSNS
VCDT	AIO	Charger-In level sense pin	BATSNS
DRV	AIO	IDAC current output open-drain pin	BATSNS
BATON	AIO	Battery Pack, NTC connected pin	BATSNS
ISENSE	AIO	Top node of current sensing 0.2ohm Rsense resistor	BATSNS
CHR_LDO	AIO	2.8V shunt-regulator output	BATSNS
BATDET	AIO	Battery detection pin	BATSNS
ISINK0	AIO	Backlight driver channel 0	VBAT_SPK
ISINK1	AIO	Backlight driver channel 1	VBAT_SPK
ISINK2	AIO	Backlight driver channel 2	VBAT_SPK
ISINK3	AIO	Backlight driver channel 3	VBAT_SPK
KPLED	AIO	Keypad led driver	VBAT_SPK
TESTMODE	AIO	Test mode	BATSNS
PWRKEY	AIO	PWR key	BATSNS
Analog power			
AVDD28_FM	P	FM power	-
AVDD28_VRF	P	2.8V power supply for 2G RF	-
AVDD28_TCXO	P	2.8V power supply for 2G TCXO	-
AVDD28_2GAFE	P	2.8V power supply for 2G AFE	-

Pin name	Type	Description	Power domain
AVDD28_ABB	P	ABB 2.8V power	-
AVDD28_DBT	P	2.8V power supply for DBT	-
AVDD28_ABT	P	2.8V power supply for ABT	-
VBAT_RF	P	RF LDOs used battery voltage input	-
VBAT_DIGITAL	P	Digital LDOs used battery voltage input	-
VBAT_ANALOG	P	Analog LDOs used battery voltage input	-
VBAT_SPK	P	VBAT input for loud speaker driver	-
BATSNS	P	Battery node of battery pack	-
Analog ground			
AVSS28_ABB	G	ABB 2.8V ground	-
AVSS_BT	G	BT ground	-
AVSS_BT1	G	BT1 ground	-
AVSS_2G	G	2G RF ground	-
AVSS_FM	G	FM ground	-
AVSS43_PMU	G	PMU ground	-
AVSS43_SPK	G	SPK ground	-
AGND	G	GND for VREF	-
Digital power			
DVDD28	P	2.8V power supply for digital macros in transceiver	-
DVDD18	P	1.8V power supply for digital macros in transceiver	-
DVDD28_FSRC	P	E-FUSE blowing power control	-
DVDD33_MSDC	P	3.3V memory card power	-
DVDD18_EMI	P	1.8V EMI IO power	-
DVDD28_SF	P	2.8V IO power	-
DVDD28_SFP	P	2.8V IO power	-
VDDK	P	1.2V core power	
Digital ground			
GND	G	Ground	-

Table 3. PIN function description and power domain

Abbreviation	Description
I	Input
LO	Low output
HO	High output
XO	Low or high output
PU	Pull-up
PD	Pull-down
-	No PU/PD
0~N	Aux. function number

Abbreviation	Description
X	Delicate function pin

Table 4. Acronym for state of pins

Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
System						
GPIO74	I	1	PU	DIOH2/DIOL2	No need	IO Type2
RESETB	O	1	-	DIOH6/DIOL6	No need	IO Type6
SRCLKENAI	I	7	PD	DIOH6/DIOL6	No need	IO Type6
RF control circuitry						
BPI_BUS0	O	1	-	DIOH1/DIOL1	No need	IO Type1
BPI_BUS1	O	1	-	DIOH1/DIOL1	No need	IO Type1
BPI_BUS2	O	1	-	DIOH1/DIOL1	No need	IO Type1
BPI_BUS3	O	1	-	DIOH1/DIOL1	No need	IO Type1
UART interface						
URXD1	I	1	PU	DIOH3/DIOL3	No need	IO Type3
UTXD1	O	1	-	DIOH1/DIOL1	No need	IO Type1
URXD2	I	7	PD	DIOH1/DIOL1	No need	IO Type1
UTXD2	I	7	PD	DIOH1/DIOL1	No need	IO Type1
JTAG interface						
JTMS	I	1	PU	DIOH1/DIOL1	No need	IO Type1
JTDI	I	1	PU	DIOH1/DIOL1	No need	IO Type1
JTCK	I	1	PU	DIOH1/DIOL1	No need	IO Type1
JTRST_B	I	1	PD	DIOH1/DIOL1	No need	IO Type1
JRTCK	O	1	-	DIOH1/DIOL1	No need	IO Type1
JTDO	O	1	-	DIOH1/DIOL1	No need	IO Type1
External interrupt						
EINT0	I	7	PD	DIOH1/DIOL1	No need	IO Type1
EINT12	I	7	PD	DIOH6/DIOL6	No need	IO Type6
Keypad Interface						
KCOL0	I	0	PU	DIOH4/DIOL4	No need	IO Type4
KCOL1	I	7	PD	DIOH4/DIOL4	No need	IO Type4
KCOL2	I	7	PD	DIOH4/DIOL4	No need	IO Type4
KCOL3	I	7	PD	DIOH4/DIOL4	No need	IO Type4
KCOL4	I	7	PD	DIOH4/DIOL4	No need	IO Type4
KCOL5	I	7	PD	DIOH1/DIOL1	No need	IO Type1
KCOL6	I	7	PD	DIOH3/DIOL3	No need	IO Type3

[1] The column "State" of "Reset" shows the pin state during reset. (Input, High Output, Low Output, etc)

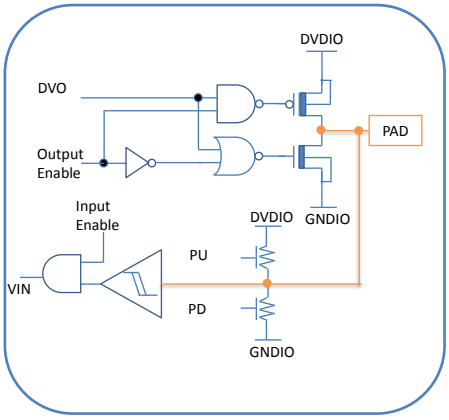
[2] The column "Aux" for "Reset" means the default aux function number, shown in the table "Pin Multiplexing, Capability and Settings".

[3] The column "PU/PD" for "Reset" means if there is internal pull-up or pull-down when the pin is input in the reset state.

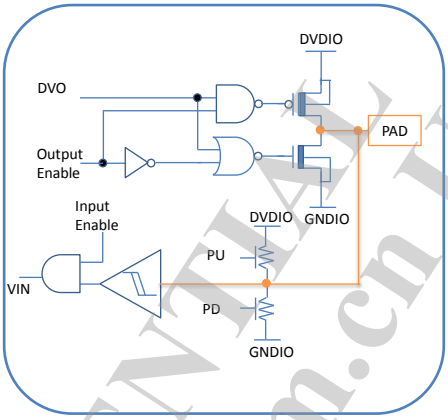
Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
KCOL7	I	7	PD	DIOH3/DIOL3	No need	IO Type3
KROW0	O	0	-	DIOH5/DIOL5	No need	IO Type5
KROW1	I	7	PD	DIOH5/DIOL5	No need	IO Type5
KROW2	I	7	PD	DIOH5/DIOL5	No need	IO Type5
KROW3	I	7	PD	DIOH5/DIOL5	No need	IO Type5
KROW4	I	7	PD	DIOH5/DIOL5	No need	IO Type5
KROW5	I	7	PD	DIOH1/DIOL1	No need	IO Type1
KROW6	I	7	PD	DIOH3/DIOL3	No need	IO Type3
KROW7	I	7	PD	DIOH1/DIOL1	No need	IO Type1
Camera interface						
CMRST	I	0	PD	DIOH1/DIOL1	No need	IO Type1
CMPDN	I	0	-	DIOH1/DIOL1	No need	IO Type1
CMVREF	I	7	PD	DIOH1/DIOL1	No need	IO Type1
GMHREF	I	7	PD	DIOH1/DIOL1	No need	IO Type1
CMDAT0	I	7	PD	DIOH1/DIOL1	No need	IO Type1
CMDAT1	I	7	PD	DIOH1/DIOL1	No need	IO Type1
CMDAT2	I	7	PD	DIOH1/DIOL1	No need	IO Type1
CMDAT3	I	7	PD	DIOH1/DIOL1	No need	IO Type1
CMDAT4	I	7	PD	DIOH1/DIOL1	No need	IO Type1
CMDAT5	I	7	PD	DIOH1/DIOL1	No need	IO Type1
CMDAT6	I	7	PD	DIOH1/DIOL1	No need	IO Type1
CMDAT7	I	7	PD	DIOH1/DIOL1	No need	IO Type1
CMPCLK	I	7	PD	DIOH1/DIOL1	No need	IO Type1
CMMCLK	I	7	PD	DIOH1/DIOL1	No need	IO Type1
MS/SD card interface						
MCINS	I	7	PD	DIOH2/DIOL2	No need	IO Type2
SD_PWROK	I	7	PD	DIOH2/DIOL2	No need	IO Type2
MCDA0	I	0	PD	DIOH3/DIOL3	No need	IO Type3
MCCM	I	0	PD	DIOH3/DIOL3	No need	IO Type3
MCMM0	I	0	PD	DIOH3/DIOL3	No need	IO Type3
I2C interface						
SCL28	I	7	PD	DIOH1/DIOL1	No need	IO Type1
SDA28	I	7	PD	DIOH1/DIOL1	No need	IO Type1
SCL18	I	7	PD	DIOH2/DIOL2	No need	IO Type2
SDA18	I	7	PD	DIOH2/DIOL2	No need	IO Type2
LCD interface						
LSRSTB	I	7	PD	DIOH2/DIOL2	No need	IO Type2
LSCE1B	I	0	PU	DIOH2/DIOL2	No need	IO Type2
LPCE0B	O	1	-	DIOH2/DIOL2	No need	IO Type2
LPCE1B	O	1	-	DIOH2/DIOL2	No need	IO Type2
LPTE	I	7	PD	DIOH2/DIOL2	No need	IO Type2

Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
LPRSTB	I	7	PD	DIOH2/DIOL2	No need	IO Type2
LRD_B	I	7	PD	DIOH2/DIOL2	No need	IO Type2
LPAD0	I	7	PD	DIOH2/DIOL2	No need	IO Type2
LWR_B	I	7	PD	DIOH2/DIOL2	No need	IO Type2
NLD8	I	7	PD	DIOH2/DIOL2	No need	IO Type2
NLD7	I	7	PD	DIOH2/DIOL2	No need	IO Type2
NLD6	I	7	PD	DIOH2/DIOL2	No need	IO Type2
NLD5	I	7	PD	DIOH2/DIOL2	No need	IO Type2
NLD4	I	7	PD	DIOH2/DIOL2	No need	IO Type2
NLD3	I	7	PD	DIOH2/DIOL2	No need	IO Type2
NLD2	I	7	PD	DIOH2/DIOL2	No need	IO Type2
NLD1	I	7	PD	DIOH2/DIOL2	No need	IO Type2
NLD0	I	7	PD	DIOH2/DIOL2	No need	IO Type2
Serial port interface						
SPI_MOSI	I	7	PD	DIOH1/DIOL1	No need	IO Type1
SPI_MISO	I	7	PD	DIOH1/DIOL1	No need	IO Type1
SPI_SCK	I	7	PD	DIOH1/DIOL1	No need	IO Type1
SPI_SCS	I	7	PD	DIOH1/DIOL1	No need	IO Type1
Watchdog reset						
WATCHDOG	O	1	-	DIOH1/DIOL1	No need	IO Type1
General purpose I/O interface						
SFCS0	I	7	PD	DIOH2/DIOL2	No need	IO Type2
SFIN	I	7	PD	DIOH2/DIOL2	No need	IO Type2
SFOUT	I	7	PD	DIOH2/DIOL2	No need	IO Type2
SFSHOLD	I	7	PD	DIOH2/DIOL2	No need	IO Type2
SFWP	I	7	PD	DIOH2/DIOL2	No need	IO Type2
SFCK	I	7	PD	DIOH2/DIOL2	No need	IO Type2

Table 5. State of pins



IO tyep1



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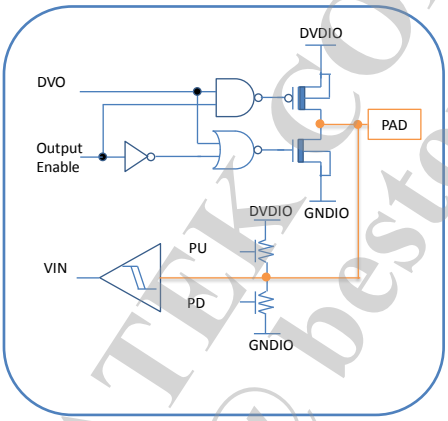

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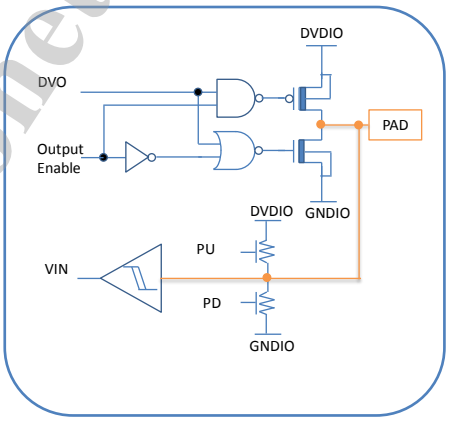

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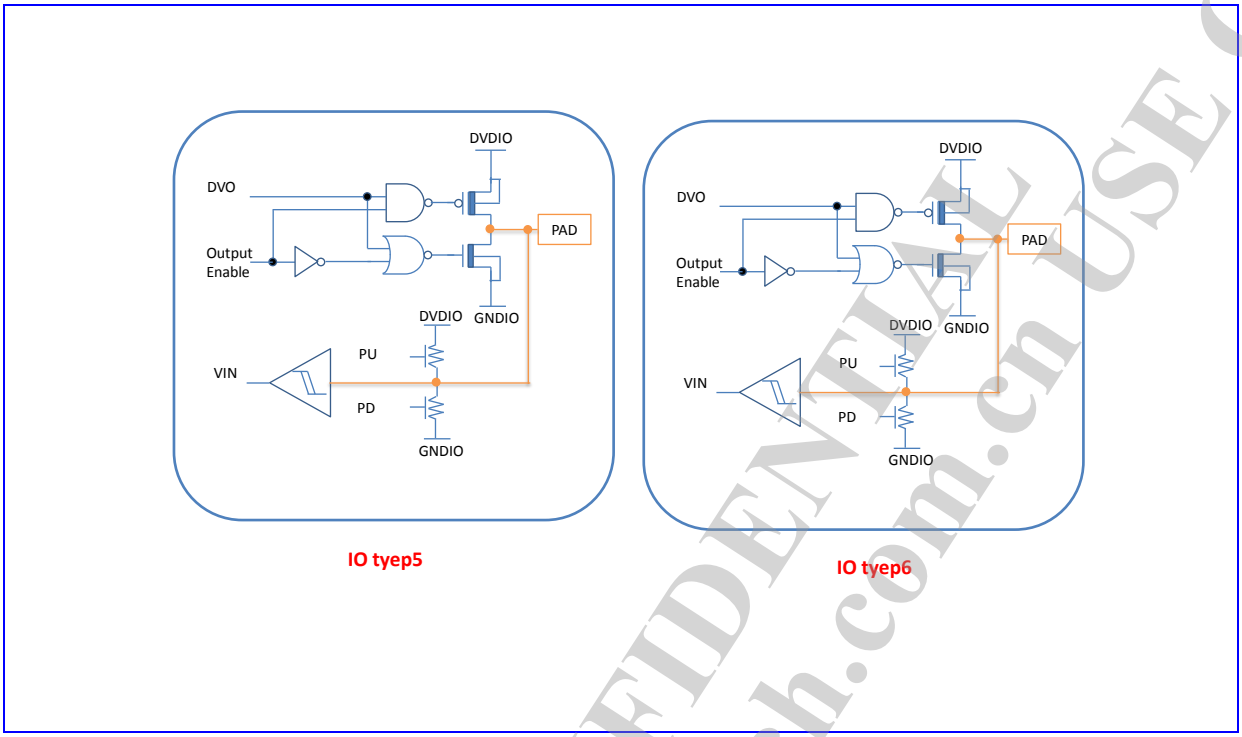


Figure 4. IO types in state of pins

2.1.4 Pin Multiplexing, Capability and Settings

Abbreviation	Description
PU	Pull-up, not controllable
PD	Pull-down, not controllable
CU	Pull-up, controllable
CD	Pull-down, controllable
X	Cannot pull-up or pull-down

Table 6. Acronym for pull-up and pull-down types

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
SPI_MOSI	0	GPIO0	IO	CU, CD	4, 8, 12, 16mA	0
	1	CLKO0	O	-	4, 8, 12, 16mA	0
	3	EDICK	O	-	4, 8, 12, 16mA	0
	4	SPIMOSI0	O	-	4, 8, 12, 16mA	0
	5	U3RXD	I	CU, CD	4, 8, 12, 16mA	0
	6	PWM	O	-	4, 8, 12, 16mA	0
	7	EGND0	I	PD	4, 8, 12, 16mA	0
SCL28	0	GPIO1	IO	CU, CD	4, 8, 12, 16mA	0
	1	SCL	IO	CU, CD	4, 8, 12, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	4	SPISCK0	O	-	4, 8, 12, 16mA	0
	7	EGND1	I	PD	4, 8, 12, 16mA	0
SDA28	0	GPIO2	IO	CU, CD	4, 8, 12, 16mA	0
	1	SDA	IO	CU, CD	4, 8, 12, 16mA	0
	4	SPICS0	O	-	4, 8, 12, 16mA	0
	7	EGND2	I	CU, CD	4, 8, 12, 16mA	0
KCOL7	0	GPIO3	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL7	IO	CU, CD	4, 8, 12, 16mA	0
	2	EDICK	O	-	4, 8, 12, 16mA	0
	5	MCDA1	IO	CU, CD	4, 8, 12, 16mA	0
	6	LSA0DA10	O	-	4, 8, 12, 16mA	0
	7	EGND3	I	PD	4, 8, 12, 16mA	0
KCOL6	0	GPIO4	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL6	IO	CU, CD	4, 8, 12, 16mA	0
	2	U1RXD	I	PU	4, 8, 12, 16mA	0
	3	CLKO5	O	-	4, 8, 12, 16mA	0
	4	WIFITOBT	I	CU, CD	4, 8, 12, 16mA	0
	5	MCDA2	IO	CU, CD	4, 8, 12, 16mA	0
	7	EGND4	I	PD	4, 8, 12, 16mA	0
KCOL5	0	GPIO5	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL5	IO	CU, CD	4, 8, 12, 16mA	0
	2	EDI2CK	O	-	4, 8, 12, 16mA	0
	5	EINT2	I	CU, CD	4, 8, 12, 16mA	0
	7	EGND5	I	PD	4, 8, 12, 16mA	0
KCLO4	0	GPIO6	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL4	IO	CU, CD	4, 8, 12, 16mA	0
	3	U3CTS	I	CU, CD	4, 8, 12, 16mA	0
	7	EGND6	I	PD	4, 8, 12, 16mA	0
KCOL3	0	GPIO7	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL3	IO	CU, CD	4, 8, 12, 16mA	0
	2	DAIPCMIN	I	CU, CD	4, 8, 12, 16mA	0
	7	EGND7	I	PD	4, 8, 12, 16mA	0
KCOL2	0	GPIO8	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL2	IO	CU, CD	4, 8, 12, 16mA	0
	2	DAICLK	O	-	4, 8, 12, 16mA	0
	7	EGND8	I	PD	4, 8, 12, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
KCOL1	0	GPIO9	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL1	IO	CU, CD	4, 8, 12, 16mA	0
	2	SPIMOSI1	O	-	4, 8, 12, 16mA	0
	7	EGND9	I	PD	4, 8, 12, 16mA	0
KCOL0	0	GPIO10	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCLO0	IO	CU, CD	4, 8, 12, 16mA	0
KROW7	0	GPIO11	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW7	IO	CU, CD	4, 8, 12, 16mA	0
	2	EINT3	I	CU, CD	4, 8, 12, 16mA	0
	4	EDIDAT	IO	CU, CD	4, 8, 12, 16mA	0
	5	MCDA3	IO	CU, CD	4, 8, 12, 16mA	0
	6	CLKO1	O	-	4, 8, 12, 16mA	0
	7	EGND10	I	PD	4, 8, 12, 16mA	0
KROW6	0	GPIO12	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW6	IO	CU, CD	4, 8, 12, 16mA	0
	2	EDI2WS	O	CU, CD	4, 8, 12, 16mA	0
	3	WIFITOBT	I	CU, CD	4, 8, 12, 16mA	0
	4	SPIMISO0	I	CU, CD	4, 8, 12, 16mA	0
	7	EGND11	I	PD	4, 8, 12, 16mA	0
KROW5	0	GPIO13	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW5	IO	CU, CD	4, 8, 12, 16mA	0
	2	U1TXD	O	-	4, 8, 12, 16mA	0
	3	EDI2DAT	O	-	4, 8, 12, 16mA	0
	4	SRCLKENA	O	-	4, 8, 12, 16mA	0
	7	EGND12	I	PD	4, 8, 12, 16mA	0
KROW4	0	GPIO14	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW4	IO	CU, CD	4, 8, 12, 16mA	0
	2	DAIPCMOUT	O	-	4, 8, 12, 16mA	0
	7	EGND13	I	CU, CD	4, 8, 12, 16mA	0
KROW3	0	GPIO15	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW3	IO	CU, CD	4, 8, 12, 16mA	0
	2	LSA0DA11	O	-	4, 8, 12, 16mA	0
	3	DAISYNC	O	-	4, 8, 12, 16mA	0
	7	EGND14	I	PD	4, 8, 12, 16mA	0
KROW2	0	GPIO16	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW2	IO	CU, CD	4, 8, 12, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	2	LSCK0	O	-	4, 8, 12, 16mA	0
	5	LSDI0	I	CU, CD	4, 8, 12, 16mA	0
	7	EGND15	I	PD	4, 8, 12, 16mA	0
KROW1	0	GPIO17	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW1	IO	CU, CD	4, 8, 12, 16mA	0
	2	LSDA00	IO	PU, CD	4, 8, 12, 16mA	0
	3	U1CTS	I	CU, CD	4, 8, 12, 16mA	0
	4	DAIRST	I	CU, CD	4, 8, 12, 16mA	0
	7	EGND16	I	PD	4, 8, 12, 16mA	0
KROW0	0	GPIO18	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW0	IO	CU, CD	4, 8, 12, 16mA	0
	2	LSDI0	I	CU, CD	4, 8, 12, 16mA	0
	4	CLKO6	O	-	4, 8, 12, 16mA	0
	5	LSCK0	O	-	4, 8, 12, 16mA	0
	7	EGND17	I	PD	4, 8, 12, 16mA	0
SPI_MOSI	0	GPIO19	IO	CU, CD	4, 8, 12, 16mA	0
	1	SPIMISO1	I	CU, CD	4, 8, 12, 16mA	0
	2	GPSFSYNC	O	-	4, 8, 12, 16mA	0
	3	LRSTB	O	-	4, 8, 12, 16mA	0
	4	DAIRST	I	CU, CD	4, 8, 12, 16mA	0
	7	EGND18	I	PD	4, 8, 12, 16mA	0
SPI_SCK	0	GPIO20	IO	CU, CD	4, 8, 12, 16mA	0
	1	SPISCK1	O	-	4, 8, 12, 16mA	0
	2	BPI_BUS5	O	-	4, 8, 12, 16mA	0
	7	EGND19	I	CU, CD	4, 8, 12, 16mA	0
SD_PWROK	0	GPIO21	IO	CU, CD	4, 8, 12, 16mA	0
	1	CLKO2	O	-	4, 8, 12, 16mA	0
	2	EDIWS	O	-	4, 8, 12, 16mA	0
	3	BPIBUS5	O	-	4, 8, 12, 16mA	0
	4	LSCK1	O	-	4, 8, 12, 16mA	0
	7	EGND20	I	PD	4, 8, 12, 16mA	0
SPI_CS	0	GPIO22	IO	CU, CD	4, 8, 12, 16mA	0
	1	SPICS1	O	-	4, 8, 12, 16mA	0
	2	BPIBUS4	O	-	4, 8, 12, 16mA	0
	7	EGND21	I	CU, CD	4, 8, 12, 16mA	0
URXD2	0	GPIO23	IO	CU, CD	4, 8, 12, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	1	U2RXD	I	CU, CD	4, 8, 12, 16mA	0
	2	BTPRI	IO	CU, CD	4, 8, 12, 16mA	0
	3	LSCE0B0	O	-	4, 8, 12, 16mA	0
	4	U1RTS	O	-	4, 8, 12, 16mA	0
	7	EGND22	I	PD	4, 8, 12, 16mA	0
UTXD2	0	GPIO24	IO	CU, CD	4, 8, 12, 16mA	0
	1	U2TXD	O	-	4, 8, 12, 16mA	0
	2	U3TXD	O	-	4, 8, 12, 16mA	0
	3	BPIBUS4	O	-	4, 8, 12, 16mA	0
	4	CLKO7	O	-	4, 8, 12, 16mA	0
	7	EGND23	I	PD	4, 8, 12, 16mA	0
URXD1	0	GPIO25	IO	CU, CD	4, 8, 12, 16mA	0
	1	U1RXD	I	PU	4, 8, 12, 16mA	0
	2	LSDI1	I	CU, CD	4, 8, 12, 16mA	0
	3	EINT11	I	CU, CD	4, 8, 12, 16mA	0
UTXD1	0	GPIO26	IO	CU, CD	4, 8, 12, 16mA	0
	1	U1TXD	O	-	4, 8, 12, 16mA	0
	2	U3CTS	I	CU, CD	4, 8, 12, 16mA	0
	3	LSDA01	IO	PU, CD	4, 8, 12, 16mA	0
SCL18	0	GPIO27	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	EINT4	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	2	DAICLK	O	-	2,4,6,8,10,12 ,14,16mA	0
	3	GPT_INT	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	4	SCL	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	5	NLD14	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
	7	EGND24	I	PD	2,4,6,8,10,12 ,14,16mA	0
SDA18	0	GPIO28	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	U3RTS	O	-	2,4,6,8,10,12 ,14,16mA	0
	2	SDA	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	3	NLD13	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
	4	U3TXD	O	-	2,4,6,8,10,12 ,14,16mA	0
	5	CMCSD1	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	6	EINT1	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	7	EGND25	I	PD	2,4,6,8,10,12 ,14,16mA	0
JTDO	1	JTDO	O	-	4, 8, 12, 16mA	0
JTMS	1	JTMS	I	PU	4, 8, 12, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
JTCK	1	JTCK	I	PU	4, 8, 12, 16mA	0
JTDI	1	JTDI	I	PU	4, 8, 12, 16mA	0
JTRST_B	1	JTRST_B	I	PD	4, 8, 12, 16mA	0
JRTCK	1	JRTCK	O	-	4, 8, 12, 16mA	0
MCINS	0	GPIO29	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	EINT5	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	2	DAIPCMOUT	O	-	2,4,6,8,10,12 ,14,16mA	0
	3	NLD12	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
	4	CMCSK	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	5	LSA0DA12	O	-	2,4,6,8,10,12 ,14,16mA	0
	6	LPTE1	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	7	EGND26	I	PD	4, 8, 12, 16mA	0
MCCK	0	GPIO30	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCCK	IO	CU, CD	4, 8, 12, 16mA	0
MCDA0	0	GPIO31	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCDA0	IO	CU, CD	4, 8, 12, 16mA	0
MCCM0	0	GPIO32	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCCM0	IO	CU, CD	4, 8, 12, 16mA	0
NLD8	0	GPIO33	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD8	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
	2	DAIPCMIN	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	3	CMMCLK	O	-	2,4,6,8,10,12 ,14,16mA	0
	4	EINT6	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	5	CMPDN	O	-	2,4,6,8,10,12 ,14,16mA	0
	6	LSDI2	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	7	EGND27	I	PD	2,4,6,8,10,12 ,14,16mA	0
NLD7	0	GPIO34	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD7	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
	2	EINT7	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	3	LPTE1	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	7	EGND28	I	PD	2,4,6,8,10,12 ,14,16mA	0
NLD6	0	GPIO35	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD6	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
	7	EGND29	I	PD	2,4,6,8,10,12 ,14,16mA	0
NLD5	0	GPIO36	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD5	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	7	EGND30	I	PD	2,4,6,8,10,12 ,14,16mA	0
NLD4	0	GPIO37	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD4	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
	7	EGND31	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
NLD3	0	GPIO38	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD3	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
	2	LSDI3	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	7	EGND32	I	PD	2,4,6,8,10,12 ,14,16mA	0
NLD2	0	GPIO39	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD2	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
	2	LSDA02	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
	7	EGND33	I	PD	2,4,6,8,10,12 ,14,16mA	0
NLD1	0	GPIO40	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD1	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
	2	LSA0DA13	O	-	2,4,6,8,10,12 ,14,16mA	0
	7	EGND34	I	PD	2,4,6,8,10,12 ,14,16mA	0
NLD0	0	GPIO41	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD0	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
	2	LSCK2	O	-	2,4,6,8,10,12 ,14,16mA	0
	7	EGND35	I	PD	2,4,6,8,10,12 ,14,16mA	0
LWR_B	0	GPIO42	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	LWRB	O	-	2,4,6,8,10,12 ,14,16mA	0
	7	EGND36	I	PD	2,4,6,8,10,12 ,14,16mA	0
LRD_B	0	GPIO43	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	LRDB	O	-	2,4,6,8,10,12 ,14,16mA	0
	7	EGND37	I	PD	2,4,6,8,10,12 ,14,16mA	0
LPA0	0	GPIO44	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	LPA0	O	-	2,4,6,8,10,12 ,14,16mA	0
	7	EGND38	I	PD	2,4,6,8,10,12 ,14,16mA	0
LPCE0_B	0	GPIO45	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	LPCE0B	O	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	2	LSCE0B1	O	CU, CD	2,4,6,8,10,12 ,14,16mA	0
LSCE1_B	0	GPIO46	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	LSCE1B	O	-	2,4,6,8,10,12 ,14,16mA	0
	2	DAISYNC	O	-	2,4,6,8,10,12 ,14,16mA	0
	3	SCL	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	4	NLD9	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	5	LPCE2B	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	6	LSA0DA14	O	-	2,4,6,8,10,12 ,14,16mA	0
	7	EGND39	I	PD	2,4,6,8,10,12 ,14,16mA	0
LPCE1_B	0	GPIO47	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	LPCE1B	O	-	2,4,6,8,10,12 ,14,16mA	0
	2	CMMCLK	O	-	2,4,6,8,10,12 ,14,16mA	0
	3	SDA	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	4	NLD10	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	5	CMPDN	O	-	2,4,6,8,10,12 ,14,16mA	0
	6	LPTE1	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
LSRSTB	0	GPIO48	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	LSRSTB	O	-	2,4,6,8,10,12 ,14,16mA	0
	2	CLKO3	O	-	2,4,6,8,10,12 ,14,16mA	0
	3	U3RXD	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	4	NLD11	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	5	CMCSD0	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	6	LSCK3	O	-	2,4,6,8,10,12 ,14,16mA	0
	7	EGND40	I	PD	2,4,6,8,10,12 ,14,16mA	0
WATCHDOG	0	GPIO49	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	WATCHDOG	O	-	2,4,6,8,10,12 ,14,16mA	0
	2	NLD15	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	3	CMCSK	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	4	CMCSD1	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	5	LSDA03	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
LPTE	0	GPIO50	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	LPTE1	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	2	CLKO4	O	-	2,4,6,8,10,12 ,14,16mA	0
	7	EGND41	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
LPRSTB	0	GPIO51	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	LPRSTB	O	-	2,4,6,8,10,12 ,14,16mA	0
	2	EINT8	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	3	LSCK4	O	-	2,4,6,8,10,12 ,14,16mA	0
	4	LPTE1	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	5	LPCE3B	O	-	2,4,6,8,10,12 ,14,16mA	0
	7	EGND42	I	PD	2,4,6,8,10,12 ,14,16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
CMDAT0	0	GPIO52	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMDAT0	I	CU, CD	4, 8, 12, 16mA	0
	2	CMCSD0	I	CU, CD	4, 8, 12, 16mA	0
	7	EGND43	I	PD	4, 8, 12, 16mA	0
CMDAT1	0	GPIO53	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMDAT1	I	CU, CD	4, 8, 12, 16mA	0
	2	CMCSD1	I	CU, CD	4, 8, 12, 16mA	0
	7	EGND44	I	PD	4, 8, 12, 16mA	0
CMDAT2	0	GPIO54	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMDAT2	I	CU, CD	4, 8, 12, 16mA	0
	2	SCL	IO	CU, CD	4, 8, 12, 16mA	0
	7	EGND45	I	PD	4, 8, 12, 16mA	0
CMDAT3	0	GPIO55	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMDAT3	I	CU, CD	4, 8, 12, 16mA	0
	2	LRSTB	O	-	4, 8, 12, 16mA	0
	3	DAIPCMIN	I	CU, CD	4, 8, 12, 16mA	0
	7	EGND46	I	PD	4, 8, 12, 16mA	0
CMDAT4	0	GPIO56	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMDAT4	I	CU, CD	4, 8, 12, 16mA	0
	2	LSA0DA15	O	-	4, 8, 12, 16mA	0
	3	DAICLK	O	-	4, 8, 12, 16mA	0
	4	U3RTS	O	-	4, 8, 12, 16mA	0
	7	EGND47	I	PD	4, 8, 12, 16mA	0
CMDAT5	0	GPIO57	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMDAT5	I	CU, CD	4, 8, 12, 16mA	0
	2	LSCK5	O	-	4, 8, 12, 16mA	0
	3	DAIPCMOUT	O	-	4, 8, 12, 16mA	0
	4	U2RXD	I	CU, CD	4, 8, 12, 16mA	0
	7	EGND48	I	PD	4, 8, 12, 16mA	0
CMDAT6	0	GPIO58	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMDAT6	I	CU, CD	4, 8, 12, 16mA	0
	2	LSDA04	IO	PU, CD	4, 8, 12, 16mA	0
	3	DAISYNC	O	-	4, 8, 12, 16mA	0
	4	U2TXD	O	-	4, 8, 12, 16mA	0
	7	EGND49	I	PD	4, 8, 12, 16mA	0
CMDAT7	0	GPIO59	IO	CU, CD	4, 8, 12, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	1	CMDAT7	I	CU, CD	4, 8, 12, 16mA	0
	2	U3CTS	I	CU, CD	4, 8, 12, 16mA	0
	3	PWM	O	-	4, 8, 12, 16mA	0
	7	EGND50	I	PD	4, 8, 12, 16mA	0
CMHREF	0	GPIO60	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMHREF	I	CU, CD	4, 8, 12, 16mA	0
	2	EINT9	I	CU, CD	4, 8, 12, 16mA	0
	3	U3RXD	I	CU, CD	4, 8, 12, 16mA	0
	7	EGND51	I	PD	4, 8, 12, 16mA	0
CMVREF	0	GPIO61	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMVREF	I	CU, CD	4, 8, 12, 16mA	0
	2	SDA	IO	CU, CD	4, 8, 12, 16mA	0
	7	EGND52	I	PD	4, 8, 12, 16mA	0
CMPDN	0	GPIO62	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMPDN	O	-	4, 8, 12, 16mA	0
	2	LSCE0B2	O	-	4, 8, 12, 16mA	0
	3	U3TXD	O	-	4, 8, 12, 16mA	0
CMMCLK	0	GPIO63	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMMCLK	O	-	4, 8, 12, 16mA	0
	7	EGND54	I	CU, CD	4, 8, 12, 16mA	0
CMPCLK	0	GPIO64	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMPCLK	I	CU, CD	4, 8, 12, 16mA	0
	2	CMCSK	I	CU, CD	4, 8, 12, 16mA	0
	7	EGND54	I	PD	4, 8, 12, 16mA	0
CMRST	0	GPIO65	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMRST	O	-	4, 8, 12, 16mA	0
	7	EGND55	I	PD	4, 8, 12, 16mA	0
EINT0	0	GPIO66	IO	CU, CD	4, 8, 12, 16mA	0
	1	EINT0	I	CU, CD	4, 8, 12, 16mA	0
	2	EDIDAT	IO	CU, CD	4, 8, 12, 16mA	0
	7	EGND56	I	PD	4, 8, 12, 16mA	0
BPI_BUS3	0	GPIO77	IO	CU, CD	4, 8, 12, 16mA	0
	1	BPIBUS3	O	-	4, 8, 12, 16mA	0
BPI_BUS2	0	GPIO78	IO	CU, CD	4, 8, 12, 16mA	0
	1	BPIBUS2	O	-	4, 8, 12, 16mA	0
BPI_BUS1	0	GPIO79	IO	CU, CD	4, 8, 12, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	1	BPIBUS1	O	-	4, 8, 12, 16mA	0
BPI_BUS0	0	GPIO80	IO	CU, CD	4, 8, 12, 16mA	0
	1	BPIBUS0	O	-	4, 8, 12, 16mA	0
SFSCK	1	GPIO81	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	7	EGND57	I	PD	2,4,6,8,10,12 ,14,16mA	0
SFSWP	1	GPIO82	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	7	EGND58	I	PD	2,4,6,8,10,12 ,14,16mA	0
SFSHOLD	1	GPIO83	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	7	EGND59	I	PD	2,4,6,8,10,12 ,14,16mA	0
SFCS0	1	GPIO84	O	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	7	EGND60	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
SFSIN	1	GPIO85	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	7	EGND61	I	PD	2,4,6,8,10,12 ,14,16mA	0
SFSOUT	1	GPIO86	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	7	EGND62	I	PD	2,4,6,8,10,12 ,14,16mA	0
SIM1_SIO	0	GPIO67	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIMSIO	IO	CU, CD	2, 4, 6, 8mA	0
	7	EGND63	I	PD	2, 4, 6, 8mA	0
SIM1_SRST	0	GPIO68	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIMSRST	IO	CU, CD	2, 4, 6, 8mA	0
	7	EGND64	I	PD	2, 4, 6, 8mA	0
SIM2_SIO	0	GPIO69	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIM2SIO	IO	CU, CD	2, 4, 6, 8mA	0
	7	EGND65	I	PD	2, 4, 6, 8mA	0
SIM1_SCLK	0	GPIO70	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIMSCLK	IO	CU, CD	2, 4, 6, 8mA	0
	7	EGND66	I	PD	2, 4, 6, 8mA	0
SIM2_SCLK	0	GPIO71	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIM2SCLK	IO	CU, CD	2, 4, 6, 8mA	0
	7	EGND67	I	PD	2, 4, 6, 8mA	0
SIM2_SRST	0	GPIO72	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIM2SRST	IO	CU, CD	2, 4, 6, 8mA	0
	7	EGND68	I	PD	2, 4, 6, 8mA	0
GPIO74	0	GPIO74	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	SFSCS1	O	-	2,4,6,8,10,12 ,14,16mA	0
	2	EINT10	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
SRCLKENAI	0	GPIO105	IO	CU, CD	4, 8, 12, 16mA	0
	1	SRCLKENAI	I	CU, CD	4, 8, 12, 16mA	0
	7	EGND69	I	PD	4, 8, 12, 16mA	0
RESETB	0	GPIO106	IO	CU, CD	4, 8, 12, 16mA	0
	1	RESETB	IO	CU, CD	4, 8, 12, 16mA	0
	7	EGND70	I	PD	4, 8, 12, 16mA	0
EINT12	0	GPIO107	IO	CU, CD	4, 8, 12, 16mA	0
	1	EINT12	I	CU, CD	4, 8, 12, 16mA	0
	7	EGND71	I	PD	4, 8, 12, 16mA	0

Table 7. Capability of PU/PD, driving and Schmitt trigger

2.2 Electrical Characteristics

2.2.1 Absolute Maximum Ratings

Symbol or pin name	Description	Min.	Max.	Unit
VBAT_DIGITAL	Digital used battery voltage input	-0.3	+4.3	V
VBAT_ANALOG	Analog used battery voltage input	-0.3	+4.3	V
VBAT_SPK	VBAT input for loud speaker driver	-0.3	+4.3	V
VBAT_RF	RF used battery voltage input	-0.3	+4.3	V
VUSB	LDO output for USB-VUSB	+3.0	+3.6	V
AVDD28_FM	2.8V power supply for FM	+2.52	+3.08	V
AVDD28_VRF	2.8V power supply for 2G RF	+2.52	+3.08	V
AVDD28_TCXO	2.8V power supply for 2G TCXO	+2.52	+3.08	V
AVDD28_2GAFE	2.8V power supply for 2G AFE	+2.52	+3.08	V
AVDD28_ABB	2.8V power supply for ABB	+2.52	+3.08	V
AVDD28_DBT	2.8V power supply for DBT	+2.52	+3.08	V
AVDD28_ABT	2.8V power supply for ABT	+2.52	+3.08	V
DVDD28	2.8V power supply for digital macros in transceiver	+2.52	+3.08	V
DVDD18	1.8V power supply for digital macros in transceiver	+1.62	+1.98	V
DVDD28_SF	2.8V IO power	+2.7	+3.6	V
	1.8V IO power	+1.7	+1.98	V
DVDD28_SFP	2.8V IO power	+2.7	+3.6	V
	1.8V IO power	+1.7	+1.98	V
DVDD33_MSDC	3.3V memory card power	+3.0	+3.6	V
DVDD18_EMI	1.8V EMI IO power	+1.62	+1.98	V

Symbol or pin name	Description	Min.	Max.	Unit
DVDD28_FSRC	E-FUSE blowing power control	+2.52	+3.08	V
VDDK	1.2v core power	+1.08	+1.32	V

Table 8. Absolute maximum ratings for power supply

Symbol or pin name	Description	Min.	Max.	Unit
VIN1	Digital input voltage for IO Type 1	-0.3	3.08	V
VIN2	Digital input voltage for IO Type 2	-0.3	3.08	V
VIN3	Digital input voltage for IO Type 3	-0.3	3.08	V
VIN4	Digital input voltage for IO Type 4	-0.3	3.08	V
VIN5	Digital input voltage for IO Type 5	-0.3	3.08	V
VIN6	Digital input voltage for IO Type 6	-0.3	3.08	V

Table 9. Absolute maximum ratings for voltage input

Symbol or pin name	Description	Min.	Max.	Unit
Tstg	Storage temperature	-55	125	^{o}C

Table 10. Absolute maximum ratings for storage temperature

2.2.2 Recommended Operating Conditions

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
VBAT_DIGITAL	Digital used battery voltage input	3.4	3.8	4.2	V
VBAT_ANALOG	Analog used battery voltage input	3.4	3.8	4.2	V
VBAT_SPK	VBAT input for loud speaker driver	3.4	3.8	4.2	V
VBAT_RF	RF used battery voltage input	3.4	3.8	4.2	V
VUSB	LDO output for USB-VUSB	3.0	3.3	3.6	V
AVDD28_FM	2.8V power supply for FM	2.6	2.8	3.0	V
AVDD28_VRF	2.8V power supply for 2G RF	2.65	2.8	2.95	V
AVDD28_TCXO	2.8V power supply for 2G TCXO	2.65	2.8	2.95	V
AVDD28_2GAFE	2.8V power supply for 2G AFE	2.65	2.8	2.95	V
AVDD28_ABB	2.8V power supply for ABB	2.6	2.8	3.0	V
AVDD28_DBT	2.8V power supply for DBT	2.6	2.8	3.0	V
AVDD28_ABT	2.8V power supply for ABT	2.6	2.8	3.0	V
DVDD28	2.8V power supply for digital macros in transceiver	2.7	2.8	2.9	V
DVDD18	1.8V power supply for digital macros in transceiver	1.62	1.8	1.98	V
DVDD28_SF	2.8V IO power	2.7	3.3	3.6	V
	1.8V IO power	1.7	1.8	1.98	

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
DVDD28_SFP	2.8V IO power	2.7	3.3	3.6	V
	1.8V IO power	1.7	1.8	1.98	
DVDD33_MSDC	3.3V memory card power	3.0	3.3	3.6	V
DVDD18_EMI	1.8V EMI IO power	1.62	1.8	1.98	V
DVDD28_FSRC	E-FUSE blowing powr control	2.7	2.8	3.08	V
VDDK	1.2v core power	1.08	1.2	1.32	VDDK

Table 11. Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
VIN1	Digital input voltage for IO Type 1	-0.3	-	DVDIO+0.3	V
VIN2	Digital input voltage for IO Type 2	-0.3	-	DVDIO+0.3	V
VIN3	Digital input voltage for IO Type 3	-0.3	-	DVDIO+0.3	V
VIN4	Digital input voltage for IO Type 4	-0.3	-	DVDIO+0.3	V
VIN5	Digital input voltage for IO Type 5	-0.3	-	DVDIO+0.3	V
VIN6	Digital input voltage for IO Type 6	-0.3	-	DVDIO+0.3	V

Table 12. Recommended operating conditions for voltage input

Symbol or pin name	Description	Min.	Typ	Max.	Unit
Tc	Operating temperature	-20	-	85	^{o}C

Table 13. Recommended operating conditions for operating temperature

2.2.3 Electrical Characteristics under Recommended Operating Conditions

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DIIH1	Digital high input current for IO Type 1	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN1 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN1 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1<VIN1<3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN1 < 2.1	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN1 < 2.1	-11.4	-	9.3	

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		PD enabled, DVDIO = 1.8V, 1.35 < VIN1 < 2.1	-0.8	-	35	
DIIL1	Digital low input current for IO Type 1	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN1 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN1 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN1 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN1 < 0.45	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN1 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN1 < 0.45	-9.3	-	11.4	
DIOH1	Digital high output current for IO Type 1	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-12	-	-	mA
DIOL1	Digital low output current for IO Type 1	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	12	mA
DRPU1	Digital I/O pull-up resistance for IO Type 1	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPD1	Digital I/O pull-down resistance for IO Type 1	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DVOH1	Digital output high voltage for IO Type 1	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL1	Digital output low voltage for IO Type 1	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V
DIIH2	Digital high input current for IO Type 2	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN2 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN2 < 3.1	-22.5	-	12.5	

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		PD enabled, DVDIO = 2.8V, 2.1 < VIN2 < 3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN2 < 2.1	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN2 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN2 < 2.1	-0.8	-	35	
DIIL2	Digital low input current for IO Type 2	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN2 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN2 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN2 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN2 < 0.45	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN2 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN2 < 0.45	-9.3	-	11.4	
DIOH2	Digital high output current for IO Type 2	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-12	-	-	mA
DIOL2	Digital low output current for IO Type 2	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	12	mA
DRPU2	Digital I/O pull-up resistance for IO Type 2	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPD2	Digital I/O pull-down resistance for IO Type 2	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DVOH2	Digital output high voltage for IO Type 2	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DVOL2	Digital output low voltage for IO Type 2	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V
DIIH3	Digital high input current for IO Type 3	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN3 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN3 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1 < VIN3 < 3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN3 < 2.1	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN3 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN3 < 2.1	-0.8	-	35	
DIIL3	Digital low input current for IO Type 3	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN3 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN3 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN3 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN3 < 0.45	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN3 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN3 < 0.45	-9.3	-	11.4	
DIOH3	Digital high output current for IO Type 3	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-12	-	-	mA
DIOL3	Digital low output current for IO Type 3	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		DVOL < 0.27V, DVDIO = 1.8V	-	-	12	mA
DRPU3	Digital I/O pull-up resistance for IO Type 3	DVDIO = 2.8V	10	47	100	kΩ
		DVDIO = 1.8V	10	47	100	kΩ
DRPD3	Digital I/O pull-down resistance for IO Type 3	DVDIO = 2.8V	10	47	100	kΩ
		DVDIO = 1.8V	10	47	100	kΩ
DVOH3	Digital output high voltage for IO Type 3	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL3	Digital output low voltage for IO Type 3	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V
DIIH4	Digital high input current for IO Type 4	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN4 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN4 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1 < VIN4 < 3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN4 < 2.1	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN4 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN4 < 2.1	-0.8	-	35	
DIIL4	Digital low input current for IO Type 4	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN4 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN4 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN4 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN4 < 0.45	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN4 < 0.45	-35	-	0.8	

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		PD enabled, DVDIO = 1.8V, -0.3 < VIN4 < 0.45	-9.3	-	11.4	
DIOH4	Digital high output current for IO Type 4	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-12	-	-	mA
DIOL4	Digital low output current for IO Type 4	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	12	mA
DRPU4	Digital I/O pull-up resistance for IO Type 4 (GPIO mode)	DVDIO = 2.8V	40	75	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPD4	Digital I/O pull-down resistance for IO Type 4 (GPIO mode)	DVDIO = 2.8V	40	75	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPU4 200K	Digital I/O pull-up resistance for IO Type 4 (Key PAD mode)	DVDIO = 2.8V	200	-	380	kΩ
DRPD4 200K	Digital I/O pull-down resistance for IO Type 4 (Key PAD mode)	DVDIO = 2.8V	200	-	380	kΩ
DVOH4	Digital output high voltage for IO Type 4	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL4	Digital output low voltage for IO Type 4	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V
DIIH5	Digital high input current for IO Type 5	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN5 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN5 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1 < VIN5 < 3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN5 < 2.1	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN5 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN5 < 2.1	-0.8	-	35	

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DIIL5	Digital low input current for IO Type 5	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN5 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN5 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN5 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN5 < 0.45	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN5 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN5 < 0.45	-9.3	-	11.4	
DIOH5	Digital high output current for IO Type 5	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-12	-	-	mA
DIOL5	Digital low output current for IO Type 5	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	12	mA
DRPU5	Digital I/O pull-up resistance for IO Type 5 (GPIO mode)	DVDIO = 2.8V	40	75	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPD5	Digital I/O pull-down resistance for IO Type 5 (GPIO mode)	DVDIO = 2.8V	40	75	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPU5 2K	Digital I/O pull-up resistance for IO Type 4 (Key PAD mode)	DVDIO = 2.8V	1	-	2	kΩ
DRPD5 2K	Digital I/O pull-down resistance for IO Type 4 (Key PAD mode)	DVDIO = 2.8V	1	-	2	kΩ
DVOH5	Digital output high voltage for IO Type 5	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL5	Digital output low voltage for IO Type 5	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V
DIIH6	Digital high input current for IO Type 6	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN6 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN6 < 3.1	-22.5	-	12.5	

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		PD enabled, DVDIO = 2.8V, 2.1<VIN6<3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN6 < 2.1	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN6 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN6 < 2.1	-0.8	-	35	
DIIL6	Digital low input current for IO Type 6	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN6 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN6 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO=2.8V, -0.3<VIN6<0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN6 < 0.45	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN6 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN6 < 0.45	-9.3	-	11.4	
DIOH6	Digital high output current for IO Type 6	DVOH > 2.38V, DVDIO = 2.8V	-8	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-6	-	-	mA
DIOL6	Digital low output current for IO Type 6	DVOL < 0.42V, DVDIO = 2.8V	-	-	8	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	6	mA
DRPU6	Digital I/O pull-up resistance for IO Type 6	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPD6	Digital I/O pull-down resistance for IO Type 6	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DVOH6	Digital output high voltage for IO Type 6	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL6	Digital output low voltage for IO Type 6	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V

Table 14. Electrical characteristics

2.3 System Configuration

2.3.1 Strapping Resistors

Pin name	Description	Trapping condition
CMPDN	Pull-up with 75K register	Power-on reset
CMRST	Pull-up with 75K register	Power-on reset/watchdog reset

Table 15. Strapping table

2.3.2 Mode Selection

Pin name	Description
XTAL_SEL	GND: Uses external 32K crystal as RTC clock source VRTC: Uses internal 32K as RTC clock source
CMPDN	GND: Use 1.8V device DVDD28: Use 3.0V device
KCOL0	GND: Boot ROM enter USB download mode DVDD28: Normal boot-up mode
CMRST	GND: Disables USB download sub-feature for supporting virtual 2 USB com port DVDD28: Enables USB download sub-feature for supporting virtual 2 USB com port

Table 16. Mode selection of chip

2.3.3 Constant Tied Pins

Pin name	Description
TESTMODE	Tie to GND

Table 17. Constant tied pin of chip

2.4 Power-on Sequence and Protection Logic

MT6250D provides 32K crystal removal feature. The XOSC32_ENB state tells if MT6250D provides this feature or not. VTCXO will be turned on at the same time with VRTC when XOSC32_ENB = 1. The power-on/off sequence controlled by “Control” and “Reset Generator” is shown as the figure below.

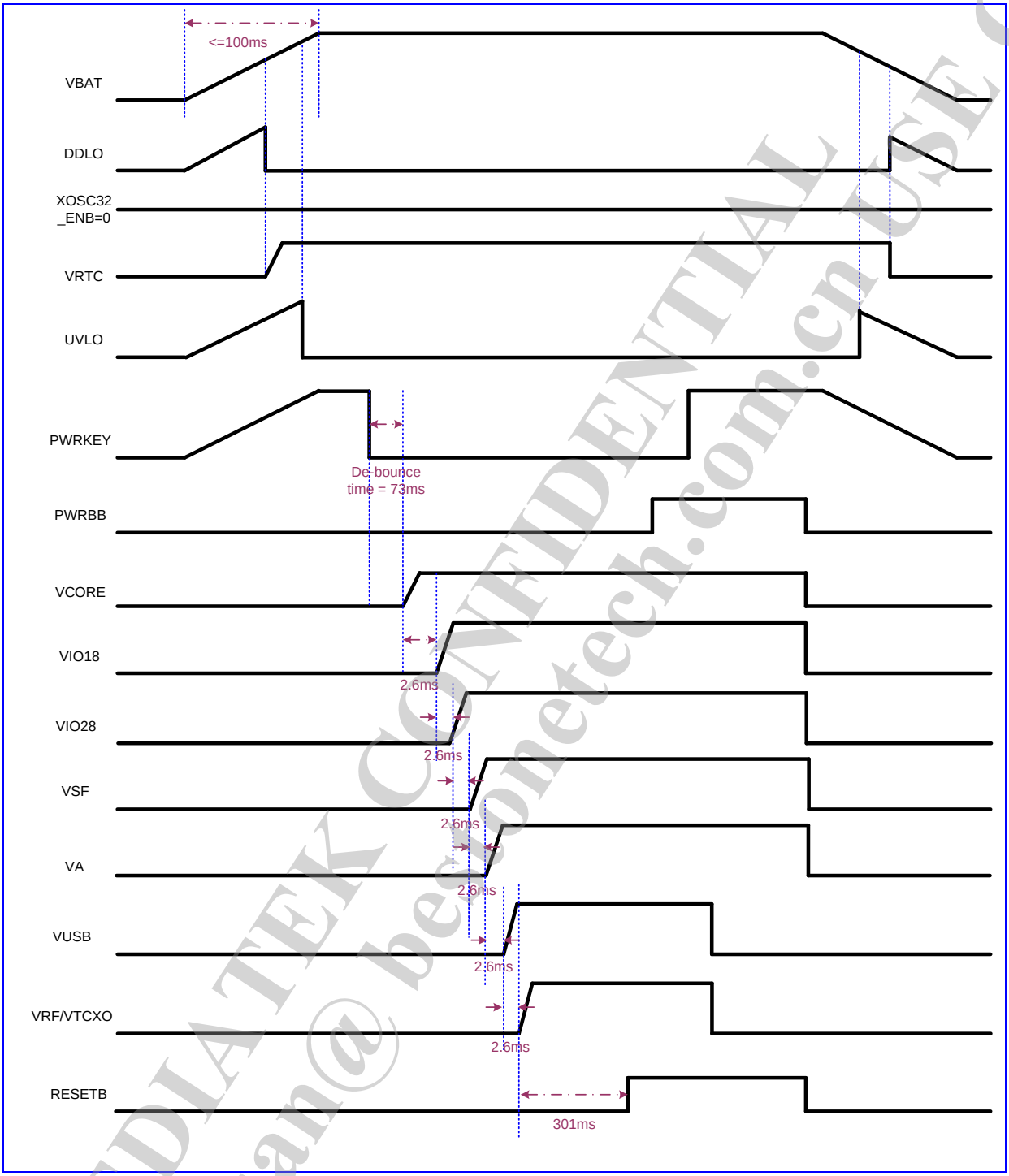


Figure 5. Power-on/off control sequence by pressing PWRKEY and XOSC32_ENB = 0

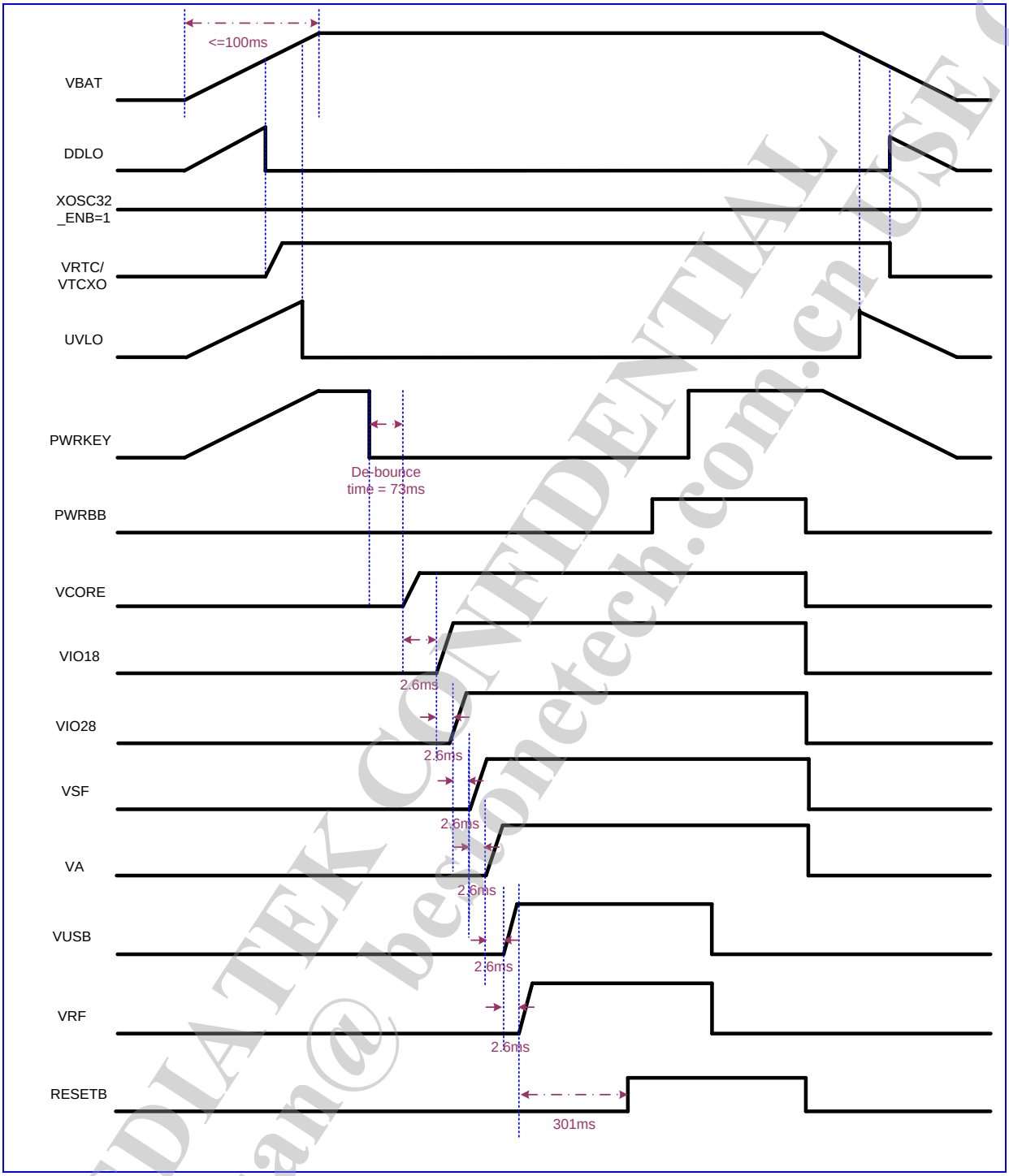


Figure 6. Power-on/off control sequence by pressing PWRKEY and XOSC32_ENB = 1

Note that each of the above figures only shows one power-on/off condition when XOSC32_ENB = 0 or XOSC32_ENB = 1. MT6250D handles the power-on and off of the handset. The following three methods can switch on the handset (when leaving UVLO): XOSC32_ENB = 0

1. Push PWRKEY (Pull the PWRKEY pin to the low level.)
   Pulling PWRKEY low is the typical way to turn on the handset. The turn-on sequence is VCORE → VIO18 → VIO28 → VSF → VA → VUSB → VRF/VTCXO

The supplies for the baseband are ready, and the system reset ends at the moment when the above LDOs are fully turned on to ensure correct timing and function. After that, the baseband will send the PWRBB signal back to the PMU for acknowledgement. To successfully power on the handset, PWRKEY should be kept low until PMU receives PWRBB from the baseband.

2. RTC module generates PWRBB to wake up the system.
   If the RTC module is scheduled to wake up the handset at a certain time, the PWRBB signal will be directly sent to the PMU. In this case, PWRBB will become high at specific moment and allow the PMU to be powered on as the sequence described above. This is called the RTC alarm.

3. Valid charger plug-in (CHRIN voltage is within the valid range.)
   The charger plug-in will also turn on the handset if the charger is valid (no OVP takes place). However, if the battery voltage is too low to power on the handset (UVLO state), the system will not be turned on by any of the three methods. In this case, the charger will charge the battery first and the handset will be powered on automatically as long as the battery voltage is high enough.

Under-voltage lockout (UVLO)

The UVLO state in the PMU prevents startup if the initial voltage of the main battery is below the 3.2V threshold. It ensures that the handset is powered on with the battery in good condition. The UVLO function is performed by a hysteretic comparator which ensures a smooth power-on sequence. In addition, when the battery voltage is getting lower, it will enter the UVLO state, and the PMU will be turned off by itself, except for VRTC LDO, to prevent further discharging. Once the PMU enters the UVLO state, it will draw low quiescent current. The RTC LDO will still be working until the DDLO disables it.

Deep discharge lockout (DDLO)

The PMU will enter the deep discharge lockout (DDLO) state when the battery voltage drops below 2.5V. In this state, the VRTC LDO will be shut down. Otherwise, it will draw very low quiescent current to prevent further discharging or damage to the cells.

Reset

The PMU contains a reset control circuit which takes effect at both power-up and power-down. The RESETB pin is held low in the beginning of power-up and returns to high after the pre-determined delay time. The delay time is controlled by a large counter which uses the clock from internal ring-oscillator. At power-off, the RESETB pin will return to low immediately without any delay.

Over-temperature protection

If the die temperature of PMU exceeds 150°C, the PMU will automatically disable all the LDOs except for VRTC. Once the over-temperature state is resolved, a new power-on sequence will be required to enable the LDOs.

2.5 Analog Baseband

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are some dedicated interfaces for data transfer. The common control interface

translates the APB bus write and read cycle for specific addresses related to analog front-end control. During the writing or reading of any of these control registers, there is a latency associated with the transfer of data to or from the analog front-end. Dedicated data interface of each analog block is implemented in the corresponding digital block. An analog block includes the following analog functions for the complete GSM/GPRS baseband signal processing:

1. RF control: DAC for automatic power control (APC) is included, and its output is provided to external RF power amplifier respectively.
2. Auxiliary ADC: Provides an ADC for the battery and other auxiliary analog functions monitoring
3. Audio mixed-signal block: Provides complete analog voice signal processing including microphone amplification, A/D conversion, D/A conversion, earphone driver, etc. Dedicated stereo D/A conversion and amplification for audio signals are also included.
4. Clock generation: Includes a clock squarer for shaping the system clock, and PLL providing clock signals to DSP, MCU and USB unit
5. XOSC32: A 32-kHz crystal oscillator circuit for RTC applications on analog blocks

2.5.1 APC-DAC

2.5.1.1 Block Description

APC-DAC is a 10-bit DAC with output buffer aiming at automatic power control. See the tables below for its analog pin assignment and functional specifications. It is an event-driven scheme for power saving purpose.

2.5.1.2 Functional Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
FS	Sampling rate			1.0833	MSPS
SINAD	Signal to noise and distortion ratio (10-kHz sine with 1.0V swing & 100-kHz BW)	47			dB
	99% settling time (full swing on maximal capacitance)			5	µS
	Output swing	0		AVDD	V
	Output capacitance		200	2200	pF
	Output resistance	0.47	10		KΩ
DNL	Differential nonlinearity for code 20 to 970		± 1		LSB
INL	Integral nonlinearity for code 20 to 970		± 1		LSB
DVDD	Digital power supply	1.1	1.2	1.3	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	-20		80	°C
	Current consumption Power-up Power-down		 400 1		 µA µA

Table 18. APC-DAC specifications

2.5.2 Auxiliary ADC

2.5.2.1 Block Description

The auxiliary ADC includes the following functional blocks:

1. Analog multiplexer: Selects signal from one of the seven auxiliary input pins. Real-world messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
2. 10-bit A/D converter: Converts the multiplexed input signal to 10-bit digital data.

Channel	Application	Input range [V]
0	BATSNS	3.2 ~ 4.2
1	ISENSE	3.2 ~ 4.2
2	VCDT	Decided by application circuit
3	BATON	0 ~ AVDD28
4	AUXIN4	0 ~ AVDD28
others	Internal use	N/A

2.5.2.2 Functional Specifications

The functional specifications of the auxiliary ADC are listed in the following table.

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
FC	Clock rate		1.08		MHz
FS	Sampling rate @ N-Bit		1.08/(N+1)		MSPS
	Input swing	0		AVDD	V
CIN	Input capacitance Unselected channel Selected channel			 50 4	 fF pF
RIN	Input resistance Unselected channel Selected channel	 400 1			 MΩ MΩ
	Clock latency		N+1		1/FC
DNL	Differential nonlinearity		± 1		LSB
INL	Integral nonlinearity		± 1		LSB
OE	Offset error		± 10		mV
FSE	Full swing error		± 10		mV
SINAD	Signal to noise and distortion ratio (10-kHz full swing input & 1.0833-MHz clock rate)		50		dB
DVDD	Digital power supply	1.1	1.2	1.3	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	-20		80	°C
	Current consumption				

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Power-up Power-down		280 1		µA µA

Table 19. Functional specifications of auxiliary ADC

2.5.3 Audio Mixed-Signal Blocks

2.5.3.1 Block Description

Audio mixed-signal blocks (AMB) integrate complete voice uplink/downlink and audio playback functions. As shown in the figure below, it includes three parts. The first consists of stereo audio DACs and audio amplifiers for audio playback. The second part is the voice downlink path, including voice-band DACs (right channel audio DAC) and voice amplifier, which produces voice signals to earphones or other auxiliary output devices. Amplifiers in the two blocks are equipped with multiplexers to accept signals from the internal audio/voice. The last part is the voice uplink path, which is the interface between the microphone (or other auxiliary input device) input and MT6250D DSP. A set of bias voltage is provided for the external electric microphone.

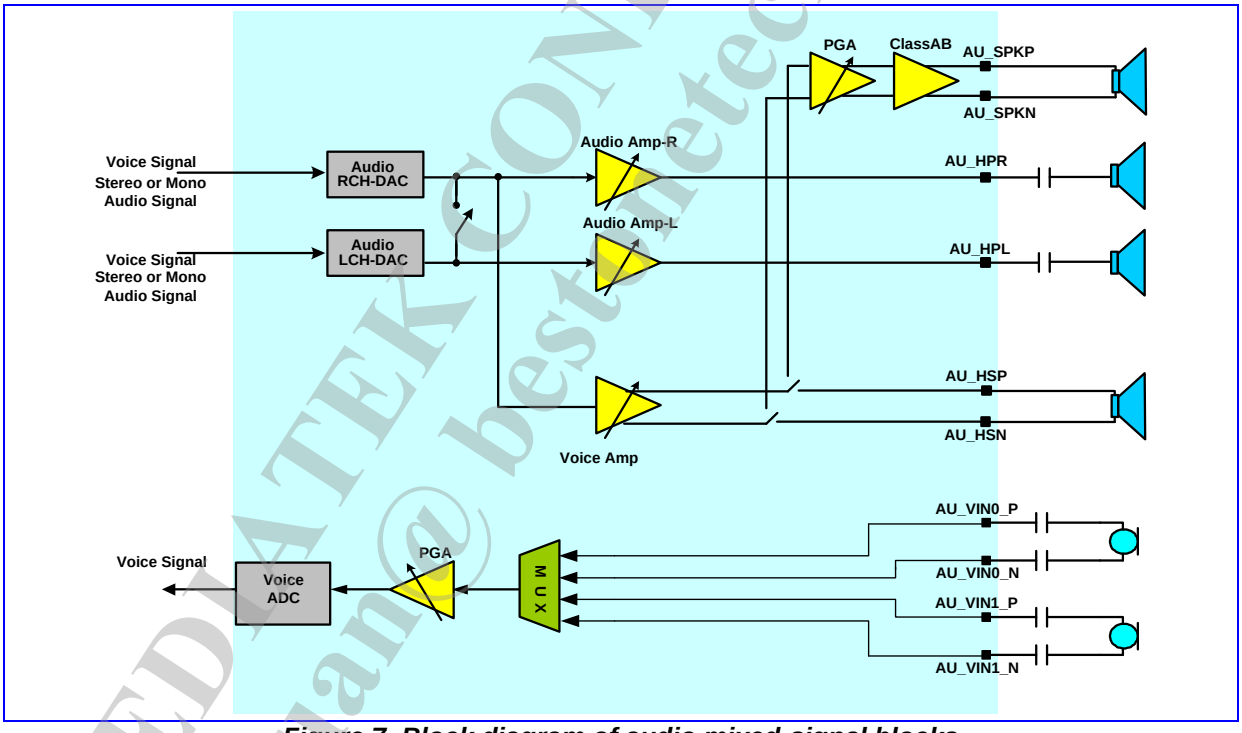


Figure 7. Block diagram of audio mixed-signal blocks

2.5.3.2 Functional Specifications

See the table below for the functional specifications of voice-band uplink/downlink blocks.

Symbol	Parameter	Min.	Typ.	Max.	Unit
FS	Sampling rate		6,500		kHz

Symbol	Parameter	Min.	Typ.	Max.	Unit
DVDD	Digital power supply	1.1	1.2	1.3	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	-20		80	°C
VMIC	Microphone biasing voltage		1.9	2.2	V
IMIC	Current draw from microphone bias pins			2	mA
Uplink path[4]					
IDC	Current consumption for one channel		1.5		mA
SINAD	Signal to noise and distortion ratio Input level: -40 dbm0 Input level: 0 dbm0	29	 69		 dB dB
RIN	Input impedance (differential)	13	20	27	KΩ
ICN	Idle channel noise			-67	dBm0
Downlink path					
IDC	Current consumption		4		mA
SINAD	Signal to noise and distortion ratio Input level: -40 dBm0 Input level: 0 dBm0	29	 69		 dB dB
RLOAD	Output resistor load (differential)	16	32		Ω
CLOAD	Output capacitor load			250	pF
ICN	Idle channel noise of transmit path			-67	dBm0
XT	Crosstalk level on transmit path			-66	dBm0

Table 20. Functional specifications of analog voice blocks

See the table below for the functional specifications of audio blocks.

Symbol	Parameter	Min.	Typ.	Max.	Unit
FCK	Clock frequency		6.5		MHz
Fs	Sampling rate	32	44.1	48	kHz
AVDD	Power supply	2.6	2.8	3.0	V
T	Operating temperature	-20		80	°C
IDC	Current consumption		4		mA
PSNR	Peak signal to noise ratio		88		dB
DR	Dynamic range		88		dB
VOUT	Output swing for 0dBFS input level @ -1dB headphone gain		0.78		Vrms
$VOUT_{MAX}$	Maximum output swing		2.4		Vpp
THD	Total harmonic distortion 10mW at 64Ω load			-70	dB

[4] For uplink-path, not all gain settings of VUPG meet the specifications listed in the table, especially for several the lowest gains. The minimum gain that meets the specifications is to be determined.

Symbol	Parameter	Min.	Typ.	Max.	Unit
RLOAD	Output resistor load (single-ended)	64			Ω
CLOAD	Output capacitor load			250	pF
XT	L-R channel cross talk	70			dB

Table 21. Functional specifications of analog audio blocks

2.5.4 32-kHz Crystal Oscillator

2.5.4.1 Block Description

The low-power 32-kHz crystal oscillator XOSC32 is designed to work with an external piezoelectric 32.768 kHz crystal and a load composed of two functional capacitors. See the figure below.

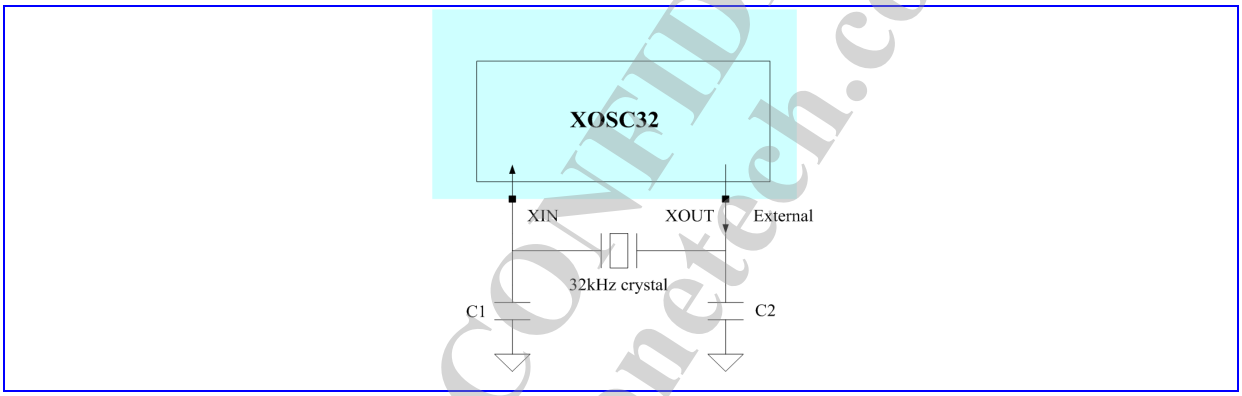


Figure 8. Block diagram of XOSC32

2.5.4.2 Functional Specifications

See the table below for the functional specifications of XOSC32.

Symbol	Parameter	Min.	Typ.	Max.	Unit
AVDDRTC	Analog power supply	1	2.8		V
Tosc	Start-up time			1	sec
Dcyc	Duty cycle	30	50	70	%
	Current consumption			5	μA
T	Operating temperature	-25		70	°C

Table 22. Functional specifications of XOSC32

See the table below for recommendations on crystal parameters to use with XOSC32.

Symbol	Parameter	Min.	Typ.	Max.	Unit
F	Frequency range		32,768		Hz

Symbol	Parameter	Min.	Typ.	Max.	Unit
GL	Drive level			1	uW
Δf/f	Frequency tolerance		± 20		ppm
ESR	Series resistance		50	70	KΩ
C0	Static capacitance		0.9		pF
CL	Load capacitance		12.5		pF

Table 23. Recommended parameters of 32kHz crystal

2.6 Power Management Unit Blocks

The power management unit (PMU) manages the power supply of the entire chip, such as baseband, processor, memory, SIM cards, camera, vibrator, etc. The digital part of PMU is integrated into the analog part (see the figure below). PMU includes the following analog functions for signal processing:

- LDO: Regulates battery voltage to lower voltage level
- Keypad LED driver (KPLED) and current sink (ISINK) switches: Sink current for keypad LED and LCM module.
- Start-up (STRUP): Generates power-on/off control sequence of start-up circuits
- Pulse charger (PCHR): Controls battery charging
- Class-AB audio amplifier: Supports high-power audio amplifier

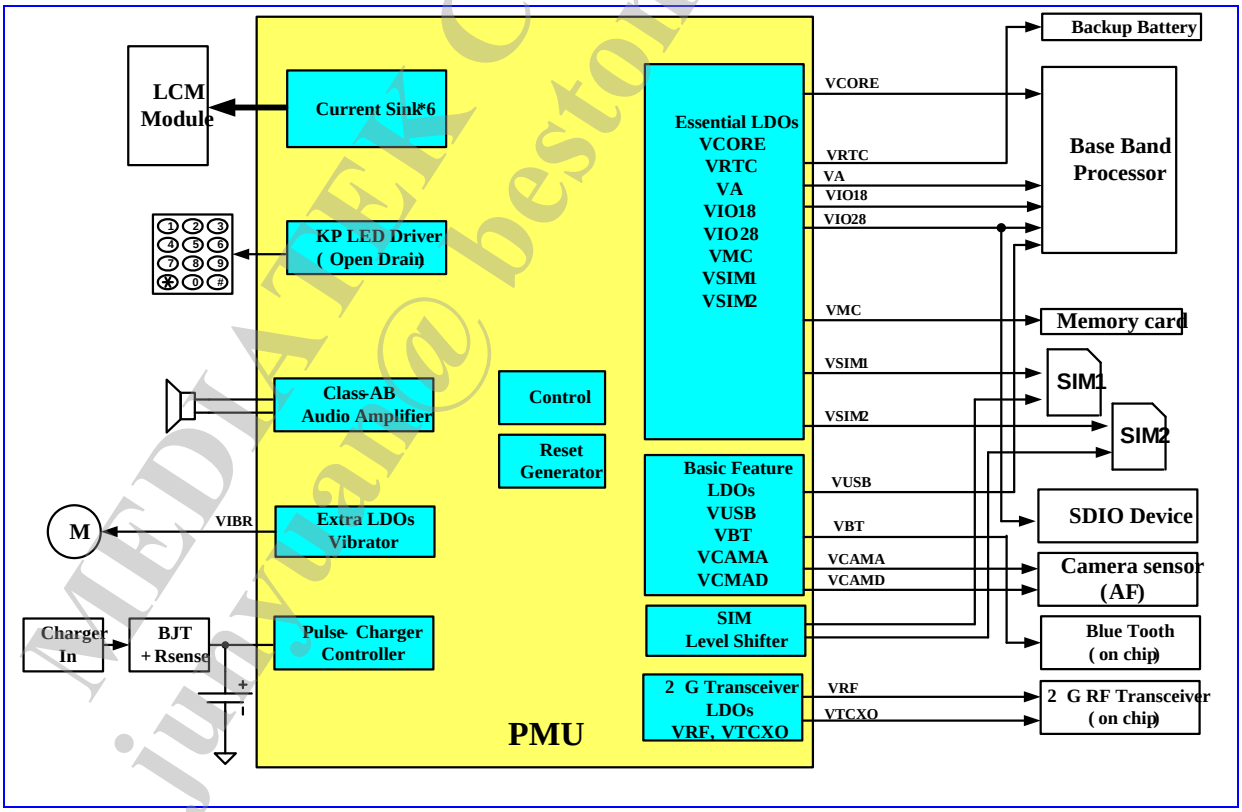


Figure 9. PMU system block diagram

2.6.1 LDO

PMU integrates 16 general low dropout regulators (LDO) optimized for their given functions by balancing the quiescent current, dropout voltage, line/load regulation, ripple rejection and output noise.

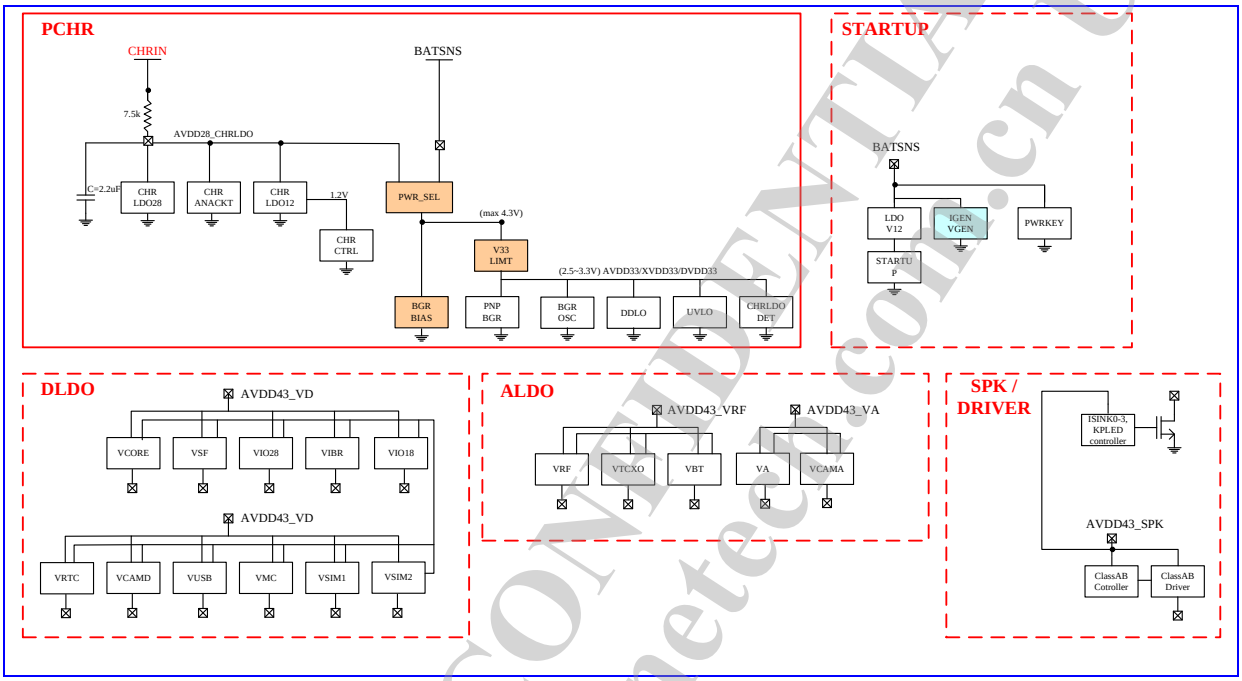


Figure 10. Power domain

2.6.1.1 LDO

A low-dropout regulator (LDO) is capable of maintaining its specified output voltage over a wide range of load current and input voltage, down to a very small difference between input and output voltages.

There are several features in the design of LDO, including discharge control, soft start and current limit. Before LDO is enabled, the output pin of LDO should be discharged first to avoid voltage accumulation on the capacitance. The soft-start limits inrush current and controls output-voltage rising time during the power-up. The current limit is the current protection to limit the LDO's output current and power dissipation.

There are three types of LDOs in PMU of MT6250D PMU. The analog LDO is optimized for low-frequency ripple rejection in order to reject the ripples coming from the burst of RF power amplifier. The digital IO LDO is a linear regulator optimized for very low quiescent current. The single-step RTC LDO is a linear regulator that can charge up a capacitor-type backup coin cell, which also supplies the RTC module even at the absence of the main battery. The single-step LDO features reverse current protection and is optimized for ultra-low quiescent current while sustaining the RTC function as long as possible.

2.6.1.1.1 Block Description

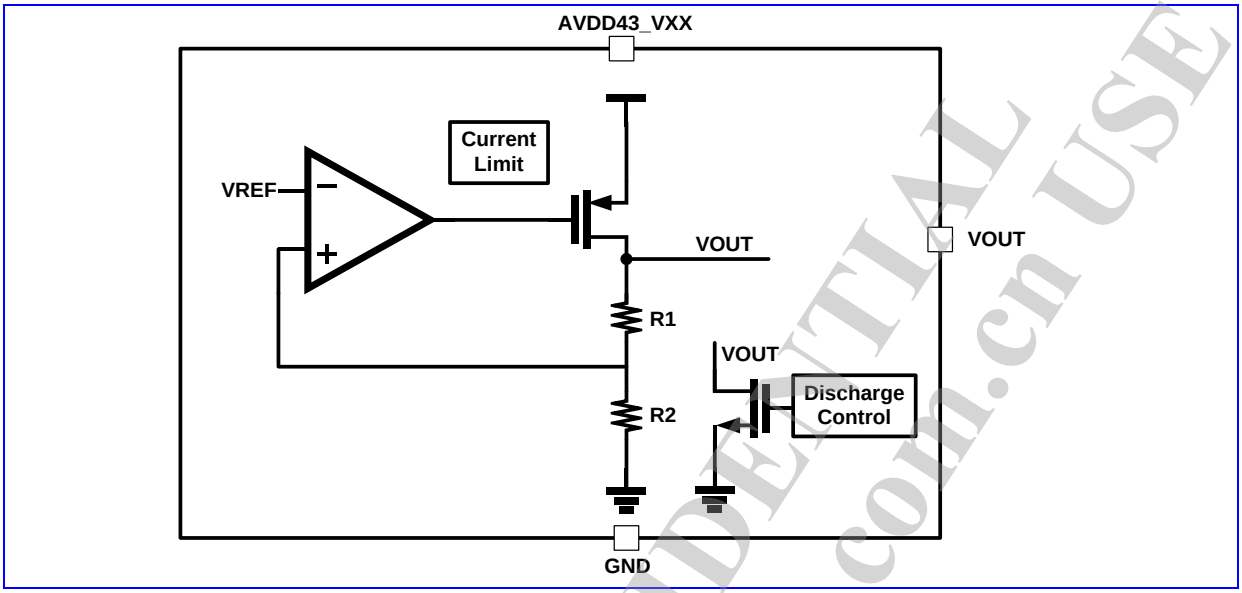


Figure 11. LDO block diagram

2.6.1.1.2 LDO Types

Type	LDO name	Vout (Volt)	Imax (mA)	Description
ALDO	VRF	2.8	150	RF chip
ALDO	VA	2.8	150	Analog baseband
ALDO	VTCXO	2.8	50	13/26 MHz reference clock
ALDO	VCAMA	1.5/1.8/2.5/2.8	150	Camera sensor
ALDO	VBT	2.8	50	Blue tooth
DLDO	VIO28	2.8	200	Digital IO
DLDO	VSIM	1.8/3.0	30	SIM card
DLDO	VSIM2	1.3/1.5/1.8/2.5/2.8/3.0/3.3	30	SIM card
DLDO	VUSB	3.3	50	USB
DLDO	VIO18	1.8	200	Digital IO
DLDO	VCORE	0.85~1.35	200	Digital baseband
DLDO	VCAMD	1.3/1.5/1.8/2.5/2.8/3.0/3.3	100	Camera Sensor
DLDO	VIBR	1.3/1.5/1.8/2.5/2.8/3.0/3.3	150	Vibrator
DLDO	VMC	1.6/1.8/2.8/3.0	200	Memory card
DLDO	VSF	1.86/3.3	100	General purpose LDO
RTCLDO	VRTC	2.8	2	Real-time clock

Table 24. LDO types and brief specifications

2.6.1.1.3 Functional Specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Load capacitor			1[5]		µF
	Current limit		1.2*Imax		5*Imax	mA
	Vout	Includes load regulation, line regulation, and temperature coefficient	Max. (-5%, -0.1V)		Max. (+5%, +0.1V)	V
	Transient response	Slew: 15mA/us	Max. (-5%, -0.1V)		Max. (+5%, +0.1V)	V
	Temperature coefficient				100	ppm/C
	PSRR	Iout < 0.5*Imax 10 < f < 3 kHz	65			dB
		Iout < 0.5*Imax 3K < f< 30 kHz	45			dB
	Output noise	With A-weighted filter			90	uVrms
	Quiescent current	Iout = 0		55		µA
	Turn-on overshoot	Iout = 0			Max. (+10%, +0.1V)	V
	Turn-on settling time	Iout = 0			240	µsec

Table 25. Analog LDO specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Load capacitor			1		µF
	Current limit		1.2*Imax		5*Imax	mA
	Vout	Includes load regulation, line regulation, and temperature coefficient	Max. (-5%, -0.1V)		Max. (+5%, +0.1V)	V
	Transient response	Slew: 15mA/us	Max. (-5%, -0.1V)		Max. (+5%, +0.1V)	V
	Temperature coefficient				100	ppm/C
	Quiescent current	Iout = 0		15		µA
	Turn-on overshoot	Iout = 0			Max. (+10%, +0.1V)	V
	Turn-on settling time	Iout = 0			240	µs

Table 26. Digital LDO specifications

[5] VRF loading capacitor typical value is 2.2uF. Other analog LDOs are 1uF.

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Load capacitor			1		µF
	Vout	Includes load regulation, line regulation, and temperature coefficient	2	2.8	3	V
	Temperature coefficient				100	ppm/C
	Quiescent current	Iout = 0		15		µA

Table 27. RTC LDO specification

2.6.2 ISINK and KPLED Switches

One built-in open-drain output switch drives the keypad LED (KPLED) in the handset. The switch is controlled by baseband with enabling registers. The switch of keypad LED can sink as much as 60mA current, and the output is high impedance when disabled. The value of the sink current decides the brightness of the LED.

Four current controlled open drain drivers (ISINK0 ~ 3) are also implemented to drive the LCM backlight module, and each channel provides 6-current-level steps up to 24mA.

2.6.2.1 Block Description

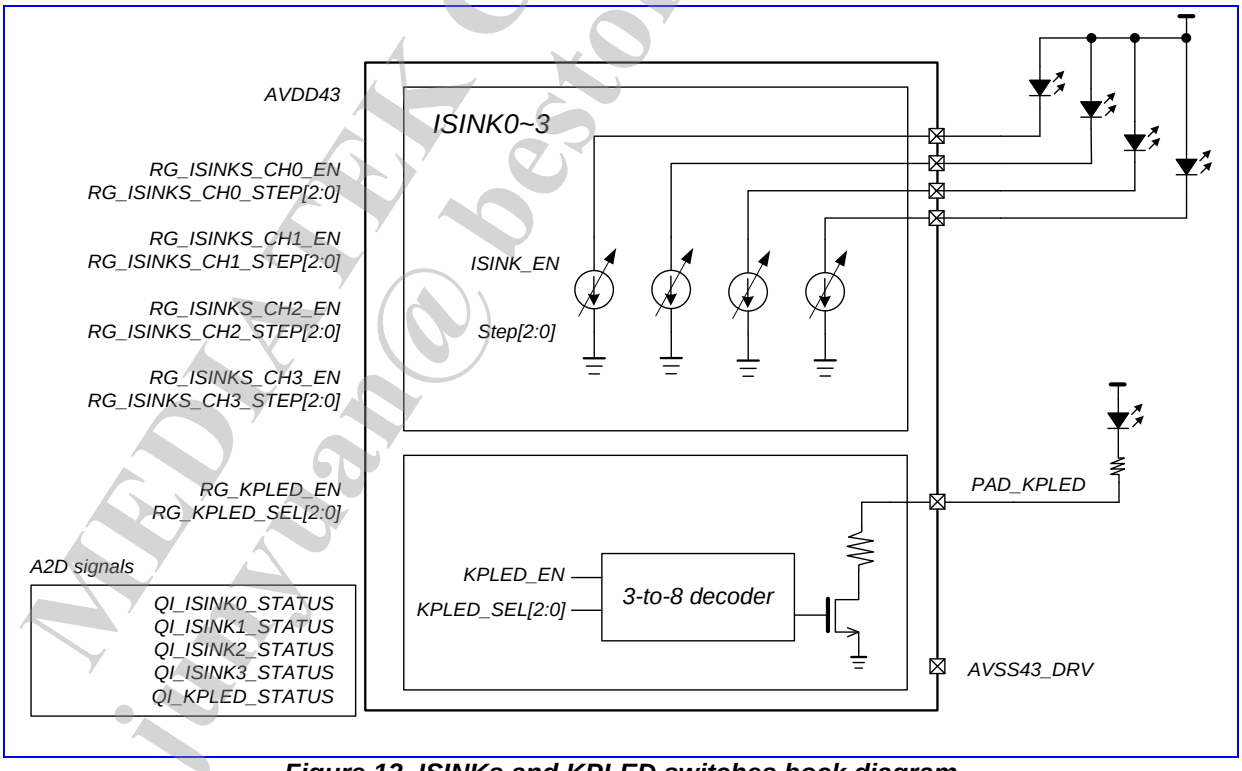


Figure 12. ISINKs and KPLED switches bock diagram

2.6.2.2 Functional Specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Sink current of keypad LED driver	Von > 0.5V, 100% dimming duty	60			mA
	Sink current of ISINK0 ~ 3	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 000		4		mA
	Sink current of ISINK0 ~ 3	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 001		8		mA
	Sink current of ISINK0 ~ 3	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 010		12		mA
	Sink current of ISINK0 ~ 3	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 011		16		mA
	Sink current of ISINK0 ~ 3	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 100		20		mA
	Sink current of ISINK0 ~ 3	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 101		24		mA
	Current mismatch between the 4 channels	Von > 0.15V, 100% dimming duty	-5		5	%

Table 28. ISINKs and KPLED switches specifications

2.6.3 STRUP

PMU handles the power-on and off of the handset. If the battery voltage is neither in the UVLO state (VBAT ≥ 3.4V) nor in the thermal condition, there are three methods to power on the handset system: pulling PWRKEY low (the user pushes PWRKEY), pulling PWRBB high (baseband BB_WakeUp) or valid charger plug-in.

According to different battery voltage (VBAT) and phone states, control signals and regulators will have different responses.

2.6.4 PCHR

The charger controller senses the charger input voltage from either a standard AC-DC adaptor or an USB charger. When the charger input voltage is within a pre-determined range, the charging process will be activated. This detector can resist higher input voltage than other parts of the PMU.

2.6.4.1 Block Description

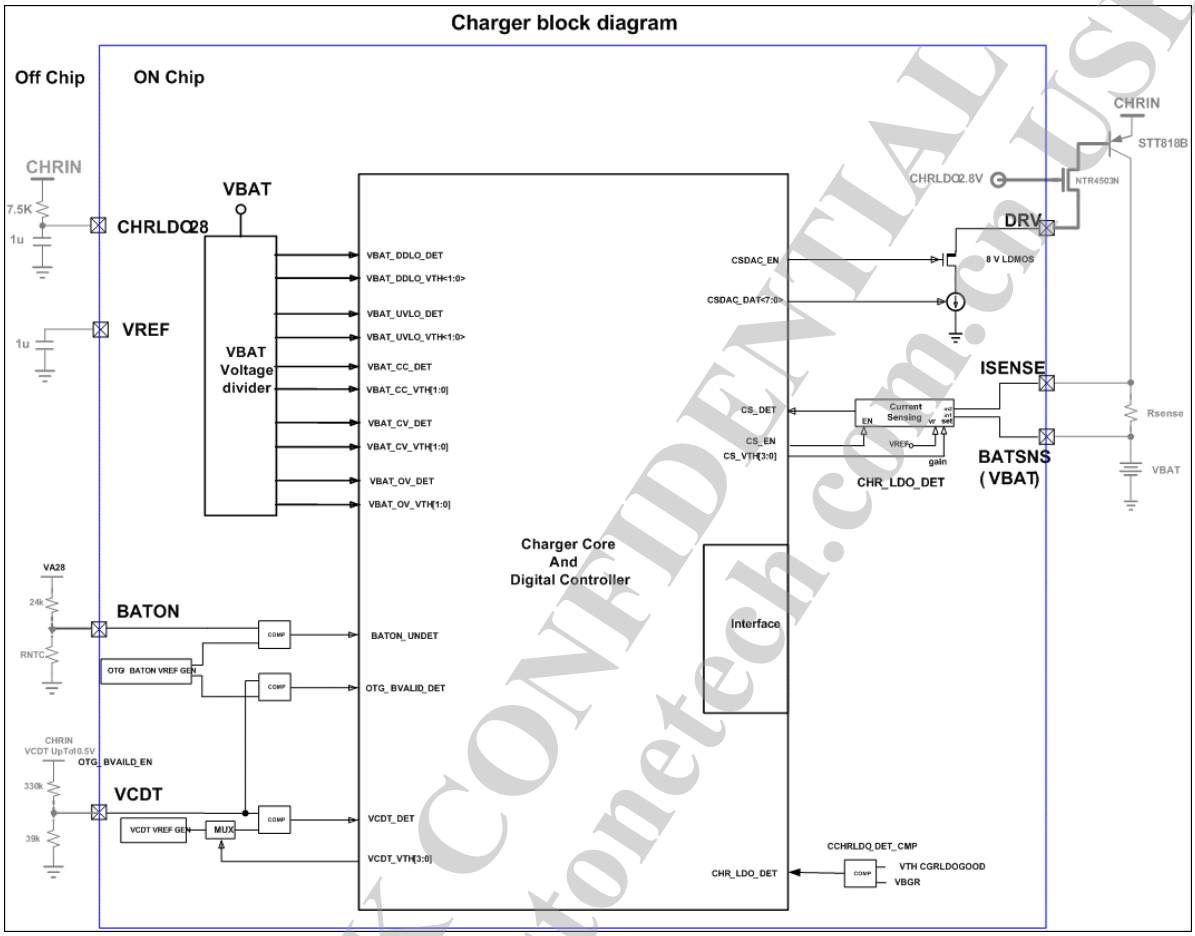


Figure 13. PCHR block diagram

2.6.4.1.1 Charger Detection

Whenever an invalid charging source is detected (> 7.0V), the charger detector stops the charging process immediately to avoid burning out the chip or even the phone. In addition, if the charger-in level is not high enough (< 4.3V), the charger will also be disabled to avoid improper charging behavior.

2.6.4.1.2 Charging Control

When the charger is active, the charger controller manages the charging phase according to the battery status. During the charging period, the battery voltage is constantly monitored. The battery charger supports pre-charge mode (VBAT < 3.2V, PMU power-off state), CC mode (constant current mode or fast charging mode at the range 3.2V < VBAT < 4.2V) and CV mode (constant voltage mode) to optimize the charging procedure for Li-ion battery. The charging states diagram is shown in the figure below.

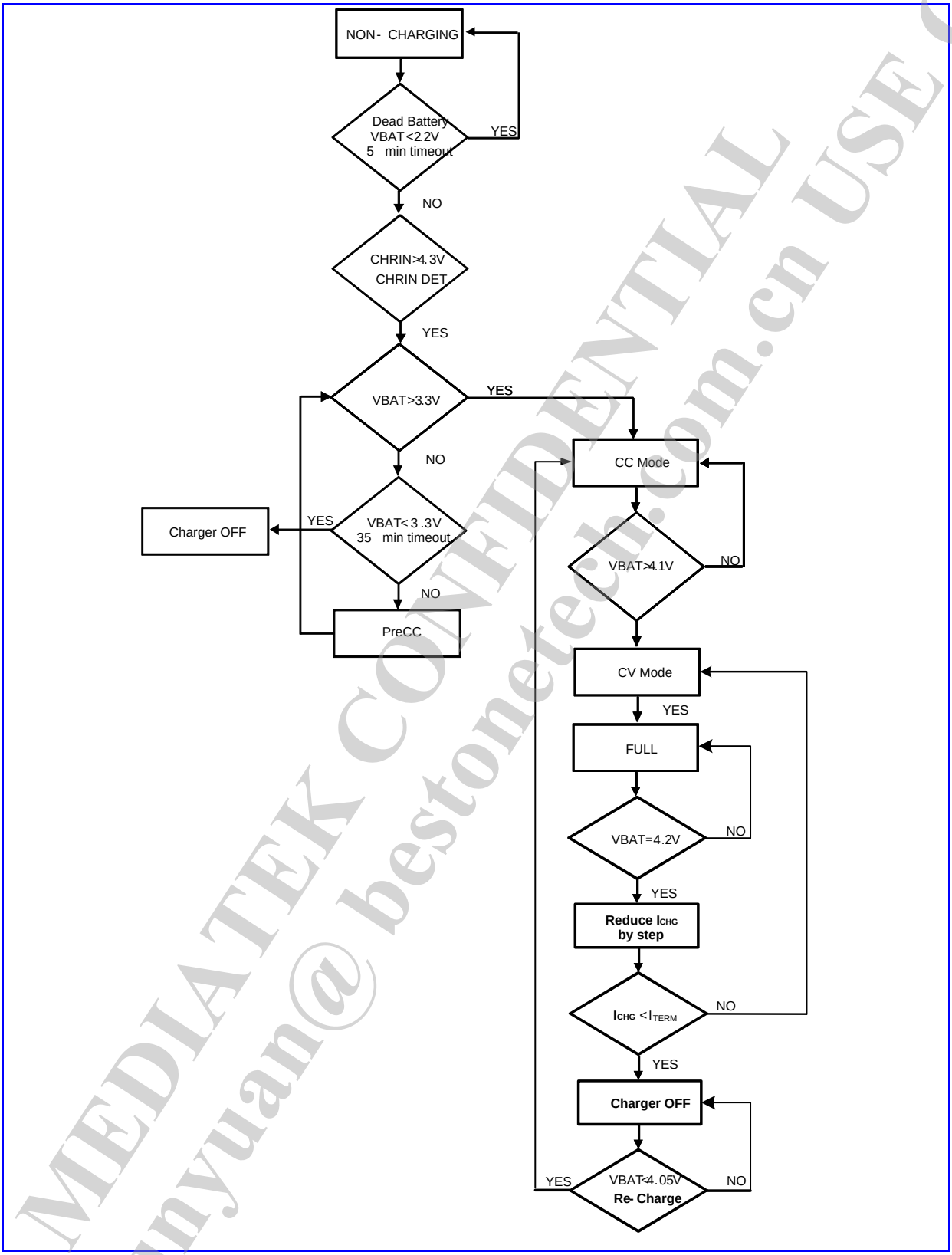


Figure 14. Charging states diagram

Pre-charge mode

When the battery voltage is in the UVLO state, the charger operates in the pre-charge mode. There are two steps in this mode. When the battery voltage is deeply discharged below 2.2V, PRECC0 trickle charging current will be applied to the battery.

The PRECC1 trickle charging current is about 550ms pulse 70mA current when VBAT is under 2.2V.

When the battery voltage exceeds 2.2V, called the PRECC2 stage, the closed-loop pre-charge is enabled. The voltage drop across the external RSENSE is kept around 40mV (AC charger) or 14mV (USB host). The closed-loop pre-charge current can be calculated:

$$I_{PRECC2,\,AC\ adapter} = \frac{V_{SENSE}}{Rsense} = \frac{40mV}{Rsense}$$

$$I_{PRECC2,\,USBHOST} = \frac{V_{SENSE}}{Rsense} = \frac{14mV}{Rsense}$$

Constant current mode

As the battery is charged up and over 3.4V, it can switch to the CC mode. (CHR_EN should be high) In the CC mode, several charging currents can be set by programming registers or the external RSENSE resistor. The charging current can be determined by CS_VTH/RSENSE, where CS_VTH is programmed by registers. For example, if RSENSE is selected as 0.2ohm, the CC mode charging current can be set from 70 to 800mA. It can accommodate the battery charger to various charger inputs with different current capabilities.

Constant voltage mode and over-voltage protection (OV)

While the battery voltage reaches about 4.2V, a constant voltage is used for charging. This is called the full-voltage charging mode or constant-voltage charging mode in correspondence to a linear charger. While the battery voltage actually reaches 4.2V, the charging current is gradually decreased step-by-step, the end-of-charging process starts. It may prolong the charging and detecting period for acquiring optimized full charging volume. The charging process is completed once the current reaches zero automatically and this mechanism is optimized for different battery

BC1.1 Dead-Battery Support of China Standard

MT6250D supports dead-battery condition from China standard (called BC1.1). The specification protects dead-battery charging by timer and trickle current. Once the battery voltage is below 2.2V, a period (TUNIT) of trickle current (IUNIT) will be applied to the battery.

If the battery voltage is still below 2.2V after applying trickle current, the charger will be disabled. On the other hand, if the battery voltage is raised to above 2.2V, the charger will enter the PRECC1 stage, and the charging current will be 70mA or 200mA depending on the type of charging port.

Under the condition of battery voltage from 2.2V to 3.3V, the charger will charge the battery with the PRECC1 current.

A dedicated 5mins (T1) timer will be timed out and disable the charger if the battery voltage is always below 2.7V under charging. Another 35mins (T2) timer will also be timed out and disable the charger if the battery voltage is always kept between 2.7V and 3.3V under charging.

The trickle current (IUNIT) and two dedicated timers protect the charging action if the battery is dead.

2.6.4.2 Functional Specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Charger detect-on range		4.3		7	V

Table 29. Charger detection specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	IUNIT with 500ms pulse	VBAT < 2.2V	28	56	84	mA
	Pre-charging current	VBAT < 2.2V (500ms pulse)	28	56	84	mA
		VBAT ≥ 2.2V (USB host)	$7/R_{sense}$	$14/R_{sense}$	$20/R_{sense}$	mA
		VBAT ≥ 2.2V (AC adapter < 7V)	$30/R_{sense}$	$40/R_{sense}$	$50/R_{sense}$	mA
		VBAT ≥ 2.2V (AC adapter > 7V)	$7/R_{sense}$	$14/R_{sense}$	$20/R_{sense}$	mA
	Pre-charging off threshold	CHR_EN = L		3.3		V
	Pre-charging off hysteresis			0.4		V

Table 30. Pre-charge specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	CC mode charging current (CS_VTH)	CS_VTH [2:0] = 000		$160/R_{sense}$		mA
		CS_VTH [2:0] = 001		$140/R_{sense}$		mA
		CS_VTH [2:0] = 010		$130/R_{sense}$		mA
		CS_VTH [2:0] = 011		$110/R_{sense}$		mA
		CS_VTH [2:0] = 100		$90/R_{sense}$		mA
		CS_VTH [2:0] = 101		$60/R_{sense}$		mA
		CS_VTH [2:0] = 110		$40/R_{sense}$		mA
		CS_VTH [2:0] = 111		$14/R_{sense}$		mA
	Current sensing resistor	RSENSE		0.2		ohm

Table 31. Constant current specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Charging complete threshold		4.15	4.2	4.25	V
	Battery over-voltage protection threshold (OV)			4.35		V

Table 32. Constant voltage and over-voltage protection specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
IUNIT	BC1.1 trickle current	VBAT < 2.2V		56	100	mA
IPRECC1 (USB host)	PRECC1 current	2.2 < VBAT < 3.3V		70	100	mA
IPRECC1 (AC adapter)	PRECC1 current	2.2 < VBAT < 3.3V		200	250	mA
T1	5 minute dedicated timer	2.2 < VBAT < 2.7V		5	7	min.
T2	35 minute dedicated timer	2.7 < VBAT < 3.3V		35	36	min.
TUNIT	BC1.1 trickle current period				1	sec.

Table 33. BC1.1 specifications

2.6.5 Class-AB Audio Amplifier

2.6.5.1 Block Description

MT6250D has built-in high efficiency class AB audio power amplifier, capable of delivering 1 watts of power to an 8 ohm BTL load with less than 10% distortion (THD+N) from a 4.2V battery supply. The speaker amplifier in MT6250D is integrated in PMU SOC. MT6250D class AB also supports 2-in-1 receivers.

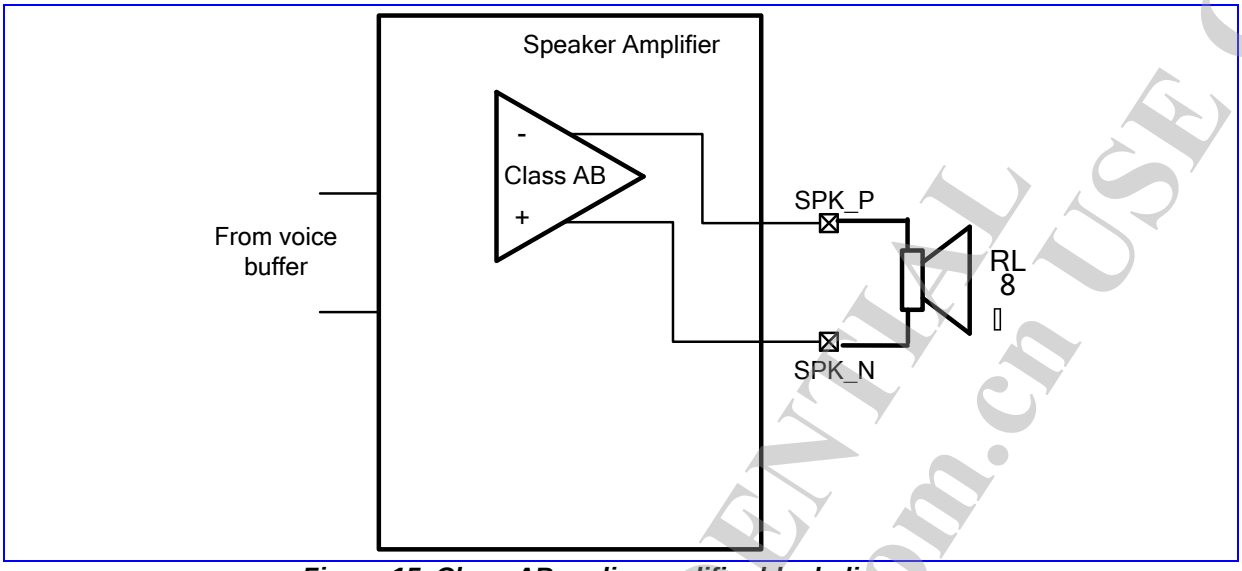


Figure 15. Class-AB audio amplifier block diagram

2.6.5.2 Functional Specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	RMS power@1% THD	8Ω load, VBAT = 4.2V		850		mW
	THD + N	1kHz, Po = 600mWrms, 4.2V		0.1		%
	PSRR	20Hz ~ 1kHz, diff. mode	60	85		dB
	Shutdown current	SPK_EN = SPK_OUTSTG_EN = 0		1		μA
	Quiescent power supply current	VBAT = 4.2V, no input		4		mA
	Gain adjustment	Audio speaker mode		6/12		dB
	Gain adjustment	Voice receiver mode		-6		dB
	Gain adjustment steps	Audio speaker mode		6		dB

Table 34. Class-AB audio amplifier specifications

2.7 GSM/GPRS/EDGE-Rx RF

2.7.1 General Description

2G RFSYS which is built in MT6250D SOC is a highly integrated RF transceiver for multi-band GSM, GPRS and EDGE-Rx cellular systems.

The features include:

Receiver

- Saw-less Rx
- Quadrature RF mixers
- Fully integrated channel filter
- High dynamic range ADC
- 24dB PGA gain with 6dB gain step

Transmitter

- High accurate transmitter modulator for GSM/GPRS application
- Built-in calibration of SX loop filter and loop gain

Frequency synthesizer

- Programmable fractional-N synthesizer
- Integrated wide range RFVCO
- Integrated loop filter
- Fast settling time suitable for multi-slot GSM/GPRS/EDGE-Rx applications

Digitally-Controlled Crystal Oscillator (DCXO)

- Two-pin 26 MHz crystal oscillator
- On-chip programmable capacitor array for coarse-tuning
- On-chip programmable capacitor array for fine-tuning
- Supports 32K XTAL-less operation

2.7.2 Functional Block Diagram

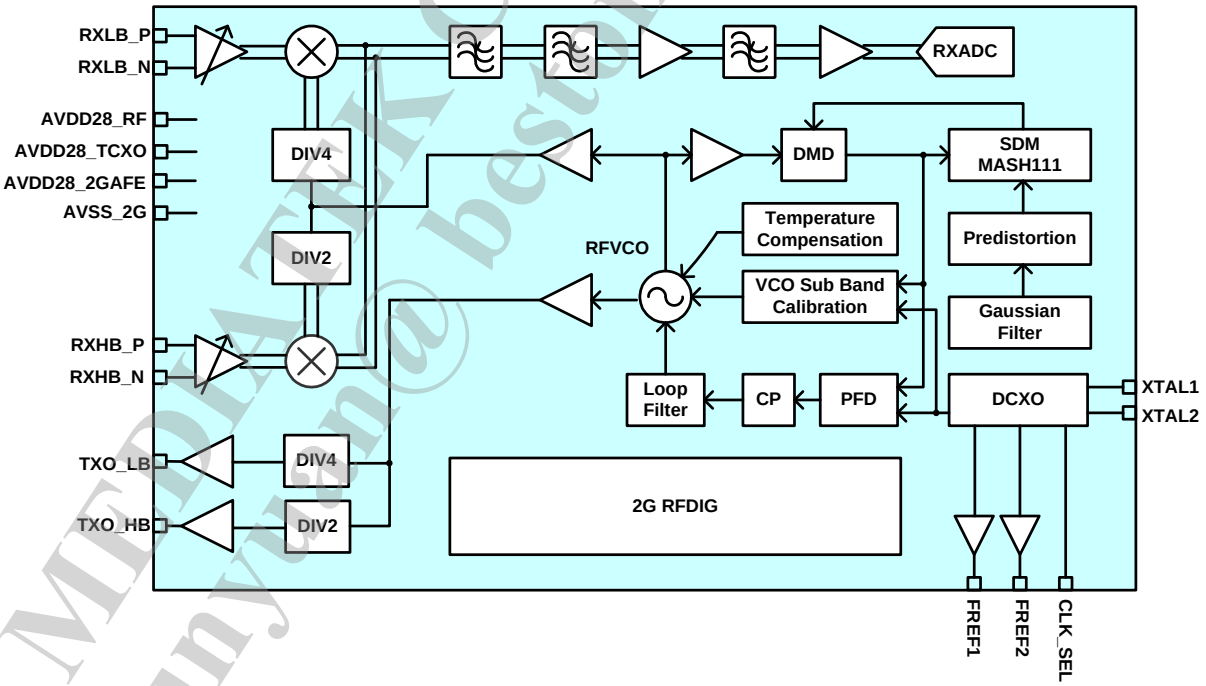


Figure 16. Diagram of MT6250D 2G RFSYS

2.7.3 Electrical Characteristics

RFSYS Mode	AVDD28_RF	AVDD28_TCXO	AVDD28_2GAFE	RFSYS Total	Unit
BCM_Deep Sleep (DCXO is off)	3	14	1	18	uA
BCM_Sleep (DCXO is on)	0.003	2.8	0.26	3.1	mA
Low power mode	3	88	1	92	uA
Full power mode	0.003	2.8	0.26	3.1	mA
RX (GSM850/EGSM)	53	8	5	66	mA
RX (DCS/PCS)	60	8	5	73	mA
TX (GSM850/EGSM)	46	10	2	58	mA
TX (DCS/PCS)	40	10	2	52	mA

Table 35. DC characteristics (TA = 25oC, VDD = 2.8V unless otherwise stated)

Item	Symbol	Band	Test condition	Min.	Typ.	Max.	Unit
Input frequency	F_{RX}	GSM850		869		894	MHz
		GSM900		925		960	MHz
		DCS1800		1,805		1,880	MHz
		PCS1900		1,930		1,990	MHz
Differential voltage gain 1	G_1	GSM850	LNA = High gain	54[1]	57		dB
		GSM900	PGA = Middle high gain	54[2]	57		dB
		DCS1800	LNA = High gain	53.5[3]	56.5		dB
		PCS1900	PGA = Middle high gain	53.5[4]	56.5		dB
Differential voltage gain 2	G_2	GSM850	LNA = Middle high gain		55.5		dB
		GSM900	PGA = Middle high gain		55.5		dB
		DCS1800	LNA = Middle high gain		53.5		dB
		PCS1900	PGA = Middle high gain		53.5		dB
Differential voltage gain 3	G_3	GSM850	LNA = Middle gain		51		dB
		GSM900	PGA = Middle high gain		51		dB
		DCS1800	LNA = Middle gain		50		dB
		PCS1900	PGA = Middle high gain		50		dB
Differential voltage gain 4	G_4	GSM850	LNA = Low gain		24		dB
		GSM900	PGA = Middle high gain		24		dB
		DCS1800	LNA = Low gain		24		dB

Item	Symbol	Band	Test condition	Min.	Typ.	Max.	Unit
		PCS1900	PGA = Middle high gain		24		dB
Noise figure at 25°C	NF_{25}	GSM850	G_1		2.5	4.5[1]	dB
		GSM900			2.5	4.5[2]	dB
		DCS1800			2.5	4.5[3]	dB
		PCS1900			2.5	4.5[4]	dB
Noise figure at 85°C	NF_{85}	GSM850	G_1		3.5		dB
		GSM900			3.5		dB
		DCS1800			3.5		dB
		PCS1900			3.5		dB
2nd-order input intercept point	IIP2	GSM850	G2	31[1]	43		dBm
		GSM900		31[2]	43		dBm
		DCS1800		31[3]	43		dBm
		PCS1900		31[4]	43		dBm
3rd-order input intercept point	IIP3	GSM850	G2	-14[1]	-3		dBm
		GSM900		-14[2]	-3		dBm
		DCS1800		-14[3]	-3		dBm
		PCS1900		-14[4]	-3		dBm
3rd-order input intercept point @ -20°C	$IIP3_{-20}$	GSM850	G2		-5		dBm
		GSM900			-5		dBm
		DCS1800			-5		dBm
		PCS1900			-5		dBm
Receiver S/N with 3MHz blocker	SN_{3M}	GSM850	G2 Blocker = rN wdBm	8[1]	14		dB
		GSM900		8[2]	14		dB
		DCS1800	G2 Blocker = rN wdBm	8[3]	14		dB
		PCS1900		8[4]	14		dB
Receiver S/N with OBB	SN_{OOB}	GSM850	G3 Blocker = 3dBm, offset 20MHz	6[5]	8		dB
		GSM900		6[5]	8		dB
		DCS1800	G3 Blocker = 3dBm, offset 80MHz	6[5]	8		dB
		PCS1900		6[5]	8		dB
Image rejection ratio	IRR	ALL	G1	32[1,2,3,4]	40		dB
Receiver channel response attenuation		ALL	@3MHz offset		20		dB
			@6MHz offset		35		dB
Receiver filtering 3-dB bandwidth		ALL	For all gain settings		900		kHz
PGA gain linearity		ALL	INL		0.2	1[5]	dBΩ
			DNL		0.1	0.5[5]	dBΩ
PGA gain step		ALL			6		dBΩ
PGA dynamic range		ALL			24		dBΩ

Item	Symbol	Band	Test condition	Min.	Typ.	Max.	Unit
I/Q common-mode output voltage		ALL	G1	1.1[5]	1.2	1.3[5]	V
Output static dc offset		ALL	G1		100	200	mV

Table 36. Rx AC characteristics (TA = 25oC, VDD = 2.8V unless otherwise stated)

Item	Symbol	Band	Test condition	Min.	Typ.	Max.	Unit
Frequency	F_{TX}	GSM850		824		849	MHz
		GSM900		880		915	MHz
		DCS1800		1,710		1,785	MHz
		PCS1900		1,850		1,910	MHz
RMS phase error	PE_{rms}	GSM850 GSM900			1	2.5[1,2]	degree
		DCS1800 PCS1900			1	2.5[3,4]	degree
Output modulation spectrum	ORFS	GSM850 GSM900	400kHz offset (RBW = 30kHz bandwidth)		-66	-64[1,2]	dBc
		DCS1800 PCS1900			-66	-64[3,4]	dBc
		GSM850 GSM900	1.8MHz offset (RBW = 30kHz bandwidth)			-75[5]	dBc
		DCS1800 PCS1900				-75[5]	dBc
Tx noise in Rx band		GSM850	20MHz offset		-165	-164[5]	dBc/Hz
			35MHz offset		-168	-167[5]	dBc/Hz
		GSM900	20MHz offset		-165	-164[5]	dBc/Hz
			35MHz offset		-168	-167[5]	dBc/Hz
		DCS1800	20MHz offset		-160	-156[5]	dBc/Hz
		PCS1900	20MHz offset		-160	-156[5]	dBc/Hz
Output power level	P_{out}	GSM850 GSM900	PA driver amplifier R_{load} = 50Ω	1[1,2]	3	6[1,2]	dBm
		DCS1800 PCS1900		1[3,4]	3	6[3,4]	dBm
Output 3rd harmonics		ALL	PA driver amplifier		-10		dBc

Table 37. Tx GMSK AC characteristics (TA = 25oC, VDD = 2.8V unless otherwise stated)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Frequency range	F_{range}		3,296		3,980	MHz
Reference frequency	F_{ref}			26		MHz

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Frequency step resolution	F_{res}			3		Hz
Phase noise	PN_{10k}	@ 10kHz offset		-83		dBc/Hz
	PN_{400k}	@ 400kHz offset		-116		dBc/Hz
	PN_{3M}	@ 3MHz offset		-136		dBc/Hz
Lock time of Rx burst	T_{lock_rx}	Frequency error < ± 0.1ppm		150	200[5]	us
Lock time of Tx burst	T_{lock_tx}	Frequency error < ± 0.1ppm		200	300[5]	us
Pushing figure		With internal RFVCO LDO		400		kHz/V

Table 38. SX AC characteristics (TA = 25oC, VDD = 2.8V unless otherwise stated)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Operating frequency	F_{ref}			26		MHz
Crystal C load	C_L			7.5		pF
Crystal tuning sensitivity	T_S		27.5	32.3		ppm/pF
Static range	SR	CDAC from 0 to 255	± 22	± 50		ppm
Dynamic range	DR	CAFC from 0 to 8191	36	50		ppm
AFC tuning step	$F_{res\text{-}AFC}$			0.006		ppm/DAC
AFC settling time	T_{AFC}	CAFC from 0 to 8191 CAFC from 8191 to 0 Frequency error < 0.1ppm		100	200[5]	us
Start-up time	T_{DCXO}	Frequency error < 1ppm Amplitude > 90 %			2[5]	ms
Pushing figure				0.2		ppm/V
Fref buffer output level	V_{Fref}	Max. loading = 19pF	0.8[5]			$V_{p\text{-}p}$
Fref buffer output phase noise		10kHz offset Jitter noise		-140		dBc/Hz

Table 39. DCXO AC characteristics (TA = 25oC, VDD = 2.8V unless otherwise stated)

[1, 2]: Tested at E-GSM Tx channel 0 and GSM850 Rx channel 190.
[3, 4]: Tested at PCS Tx channel 601 and DCS Rx channel 636.
[5]: Not subject to production test – verified by characterization and design.

2.8 Bluetooth

2.8.1 Block Description

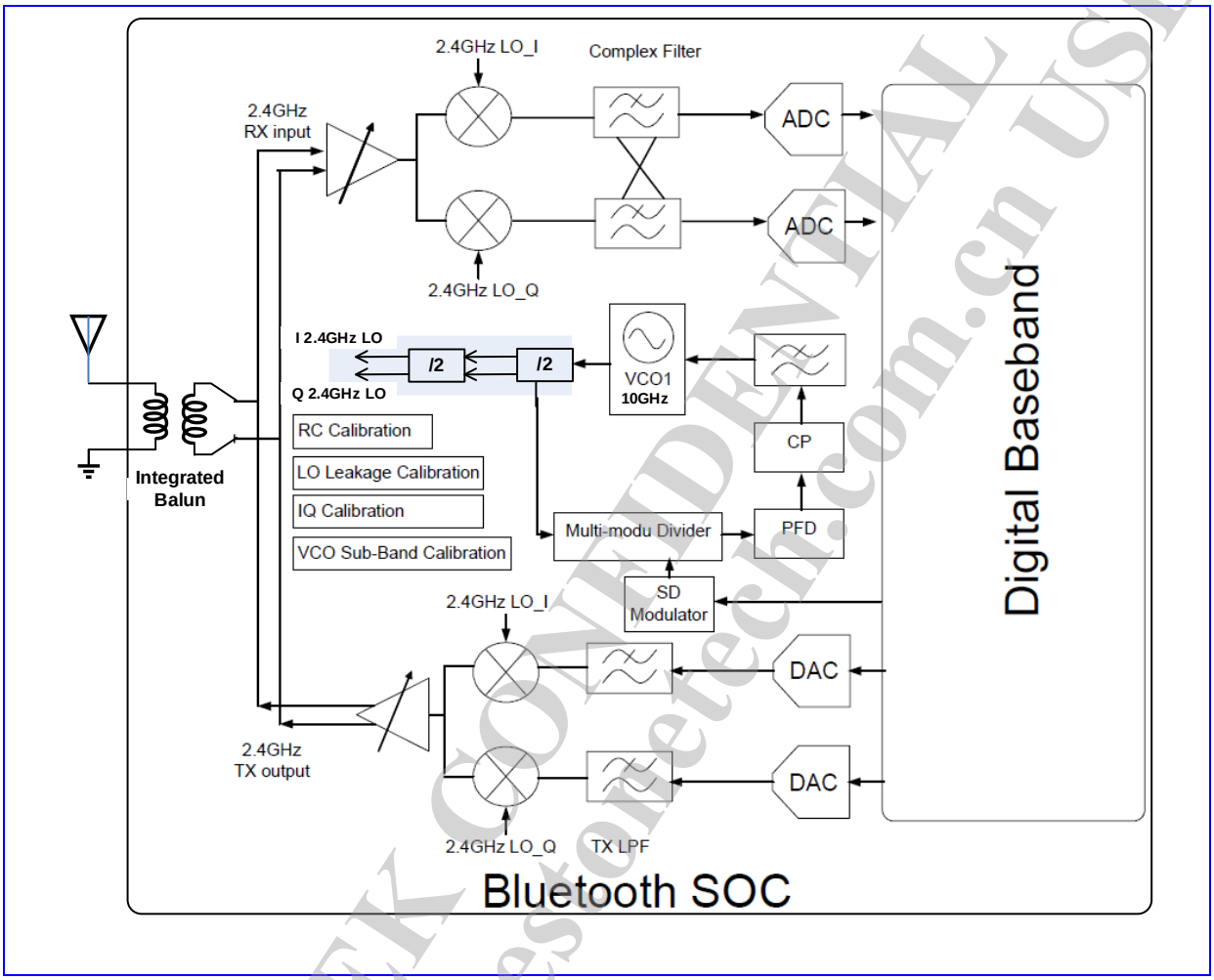


Figure 17. System diagram of Bluetooth RF transceiver

The Bluetooth RF subsystem contains a fully integrated transceiver.

For the Tx path, the baseband transmit data are digitally modulated in the baseband processor then up-converted to 2.4GHz RF channels through the DA converter, filter, IQ up-converter and power amplifier. The power amplifier is capable of transmitting 10dBm power for class-1.5 operation.

For the Rx path, MT6250D is a low IF receiver architecture. An image-reject mixer down-converts the RF signal to the IF with the LO from the synthesizer, which supports different clock frequencies as the reference clock. The mixer output is then converted to digital signal, down-converted to baseband for demodulation. A fast AGC enables the effective discovery of device within the dynamic range of the receiver.

MT6250D features self calibration schemes to compensate the process and temperature variation to maintain high performance. Those calibrations are performed automatically right after the system boot-up.

2.8.2 Functional Specifications

2.8.2.1 Basic Data Rate – Receiver Specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Frequency range		2,402	-	2,480	MHz
	Receiver sensitivity	BER < 0.1%	-	-95	-	dBm
	Max. detectable input power	BER < 0.1%	-	0	-	dBm
	C/I co-channel selectivity	BER < 0.1%	-	4	-	dB
	C/I 1MHz adj. channel selectivity	BER < 0.1%	-	-15	-	dB
	C/I 2MHz adj. channel selectivity	BER < 0.1%	-	-47.5	-	dB
	C/I ≥ 3MHz adj. channel selectivity	BER < 0.1%	-	-47.5	-	dB
	C/I image channel selectivity	BER < 0.1%	-	-27.5	-	dB
	C/I image 1MHz adj. channel selectivity	BER < 0.1%	-	-47.5	-	dB
	Out-of-band blocking	30 to 2,000MHz	-	10	-	dBm
		2,000 to 2,399MHz	-	-2	-	dBm
		2,498 to 3,000MHz	-	-3	-	dBm
		3,000MHz to 12.75GHz	-	10	-	dBm
	Intermodulation		-	-20	-	dBm

Table 40. Basic data rate – receiver specifications

2.8.2.2 Basic Data Rate – Transmitter Specification

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Frequency range		2,402	-	2,480	MHz
	Max. transmit power		-	10	-	dBm
	Gain step		-	4	-	dB
	Δf1avg (00001111)		140	158	175	kHz
	Δf2max (10101010)		115	145	-	kHz
	Δf1avg/Δf2avg		0.8	0.98	-	kHz
	Initial carrier frequency drift		-75	5	75	kHz
	Frequency drift	DH1	-25	9	25	kHz
		DH3	-40	10	40	kHz
		DH5	-40	10	40	kHz
	Max. drift rate		-	100	400	Hz/µs
	BW_{20dB} of Tx output spectrum		-	920	1,000	kHz
	In-band spurious emission	±2 MHz offset	-	-44	-	dBm
		±3 MHz offset	-	-48	-	dBm

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		> ±3 MHz offset	-	-48	-	dBm
	Out-of-band spurious emission	30 MHz to 1 GHz	-	-75	-	dBm
		1 to 12.75 GHz	-	-41	-	dBm
		1.8 to 1.9 GHz	-	-84	-	dBm
		5.15 to 5.3 GHz	-	-88	-	dBm

Table 41. Basic data rate – transmitter specifications

2.8.2.3 Enhanced Data Rate – Receiver Specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Frequency range		2,402	-	2,480	MHz
	Receiver sensitivity	π/4 DQPSK, BER < 0.01%	-	-95	-	dBm
		8PSK, BER < 0.01%	-	-88	-	dBm
	Max. detectable input power	π/4 DQPSK, BER < 0.01%	-	0	-	dBm
		8PSK, BER < 0.01%	-	0	-	dBm
	C/I co-channel selectivity	π/4 DQPSK, BER < 0.01%	-	8	-	dB
		8PSK, BER < 0.01%	-	14.5	-	dB
	C/I 1MHz adj. channel selectivity	π/4 DQPSK, BER < 0.01%	-	-13.5	-	dB
		8PSK, BER < 0.01%	-	-7.5	-	dB
	C/I 2MHz adj. channel selectivity	π/4 DQPSK, BER < 0.01%	-	-47.5	-	dB
		8PSK, BER < 0.01%	-	--41.5	-	dB
	C/I ≥ 3MHz adj. channel selectivity	π/4 DQPSK, BER < 0.01%	-	-50.5	-	dB
		8PSK, BER < 0.01%	-	-44.5	-	dB
	C/I image channel selectivity	π/4 DQPSK, BER < 0.01%	-	-30	-	dB
		8PSK, BER < 0.01%	-	-25	-	dB
	C/I image 1 MHz adj. channel selectivity	π/4 DQPSK, BER < 0.01%	-	-48.5	-	dB
		8PSK, BER < 0.01%	-	-44.5	-	dB

Table 42. Enhanced data rate – receiver specifications

2.8.2.4 Enhanced Data Rate – Transmitter Specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Frequency range		2,402	-	2,480	MHz
	Max. transmit power	π/4 DQPSK	-	8		dBm
		8PSK	-	8		dBm
	Relative transmit power	π/4 DQPSK	-	-1.7	-	dB
		8PSK	-	-1.7	-	dB
	Freq. stability ω_0	π/4 DQPSK	-	1.5	-	kHz

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		8PSK	-	1.5	-	kHz
	Freq. stability ω_1	π/4 DQPSK	-	3	-	kHz
		8PSK	-	3	-	kHz
	$\lvert \omega_0+\omega_1 \rvert$	π/4 DQPSK	-	2.8	-	kHz
		8PSK	-	2.8	-	kHz
	RMS DEVM	π/4 DQPSK	-	5.4	-	%
		8PSK	-	5.7	-	%
	99% DEVM	π/4 DQPSK	-	10	-	%
		8PSK	-	11	-	%
	Peak DEVM	π/4 DQPSK	-	18	-	%
		8PSK	-	18	-	%
	In-band spurious emission	π/4 DQPSK, ±1MHz offset	-	-40	-	dBm
		8PSK, ±1MHz offset	-	-40	-	dBm
		π/4 DQPSK, ±2MHz offset	-	-34	-	dBm
		8PSK, ±2MHz offset	-	-34	-	dBm
		π/4 DQPSK, ±3MHz offset	-	-42	-	dBm
		8PSK, ±3MHz offset	-	-42	-	dBm

Table 43. Enhanced data rate – transmitter specifications

Note: To meet the specifications, use a front-end band-pass filter.

2.9 FM RF

2.9.1 Block Descriptions

The connection between internal modules, as well as, external interfaces can be found in Figure 18. The FM receiver section incorporates the complete receiving path with wide tuning range. The FM baseband signal processor incorporates the digital demodulator and audio processing function which provides superior audio quality.

FM contains completely integrated FM audio receiver functions (RDS/RBDS may also be supported depending on the model number). The integrated receiver enables superior sensitivity, ACI performance and FM audio performances with minimum external BOM.

The FM subsystem supports either high-performance stereo analog line out or digital audio output.

For models supporting RDS/RBDS, large dedicated internal data buffers are allocated to reduce the frequency of the interrupt to the host, so that the receiving host can enter low-power states efficiently.

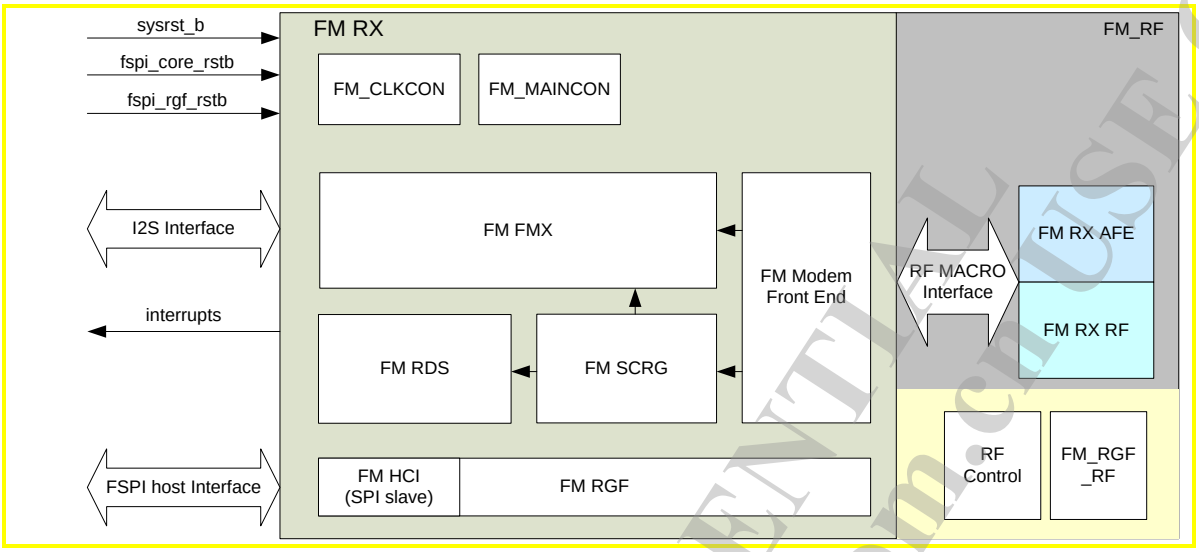


Figure 18. Block diagram of hardware top-level architecture

2.9.2 Functional Specifications

Operating mode	Current consumption	Unit
Idle	5	μA
FM receiver	10.5	mA

Table 44. FM receiver DC characteristics (TA = 25°C, VDD = 2.8V unless otherwise stated)

Unless otherwise stated, all receiver characteristics are applicable to both long and short antenna ports when operated under the recommended operating conditions. Typical specifications are for channel 98MHz, default register settings and under recommended operating conditions. The minimum and maximum specifications are for extreme operating voltage and temperature conditions, unless otherwise stated.

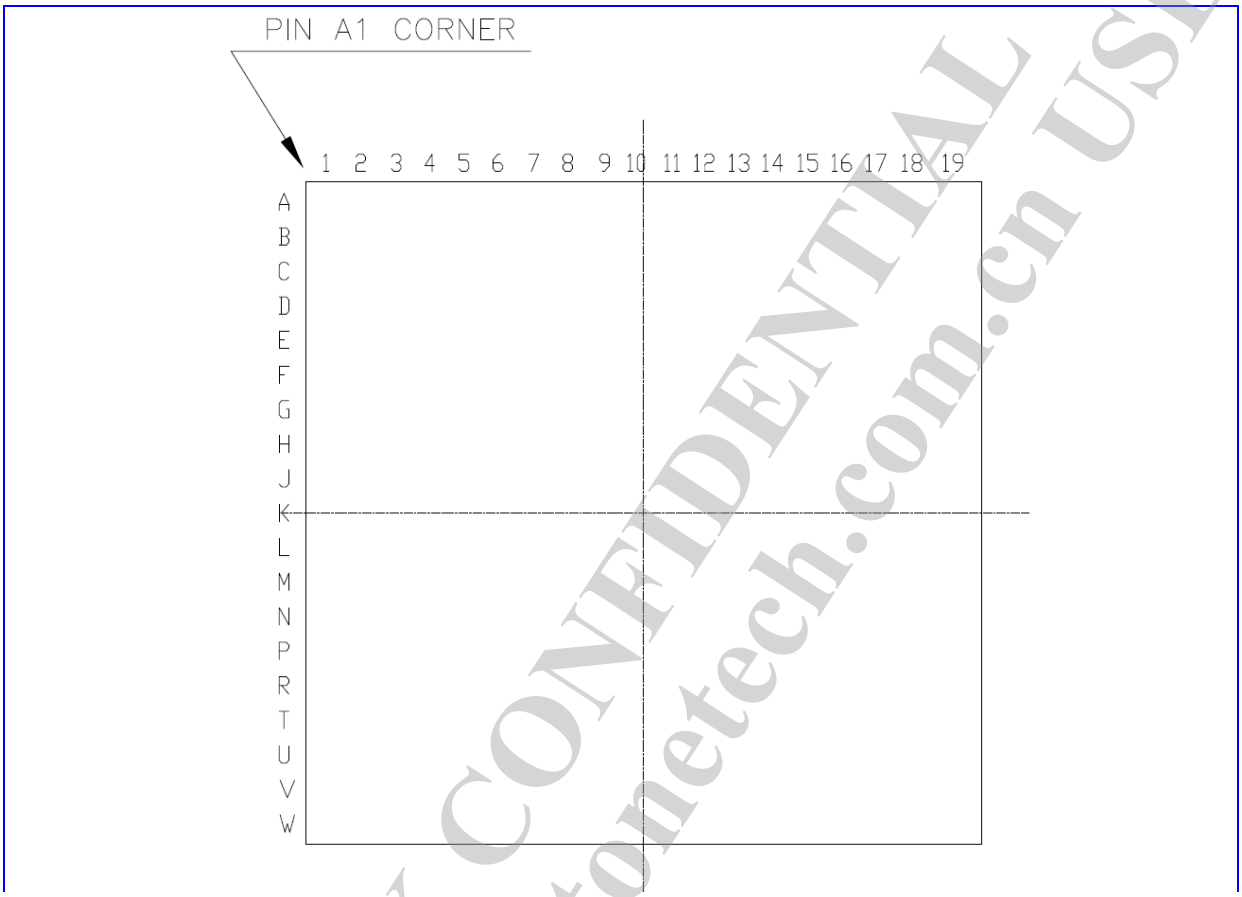
Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Input frequency range		87.5		108	MHz
	Sensitivity (long antenna)[1,3]	(S+N)/N = 26dB, unmatched		3		dBμVemf
		(S+N)/N = 26dB, matched		2		dBμVemf
	RDS sensitivity (long antenna)	Δf=2kHz, BLER < 5%, unmatched		19		dBμVemf
	Sensitivity (short antenna)[1,3]	(S+N)/N = 26dB, unmatched		4		dBμVemf
	RDS sensitivity (short antenna)	Δf = 2kHz, BLER < 5%, unmatched		20		dBμVemf
	LNA input resistance[4]			2.4k		Ohm
	LNA input capacitance[4]			8		pF

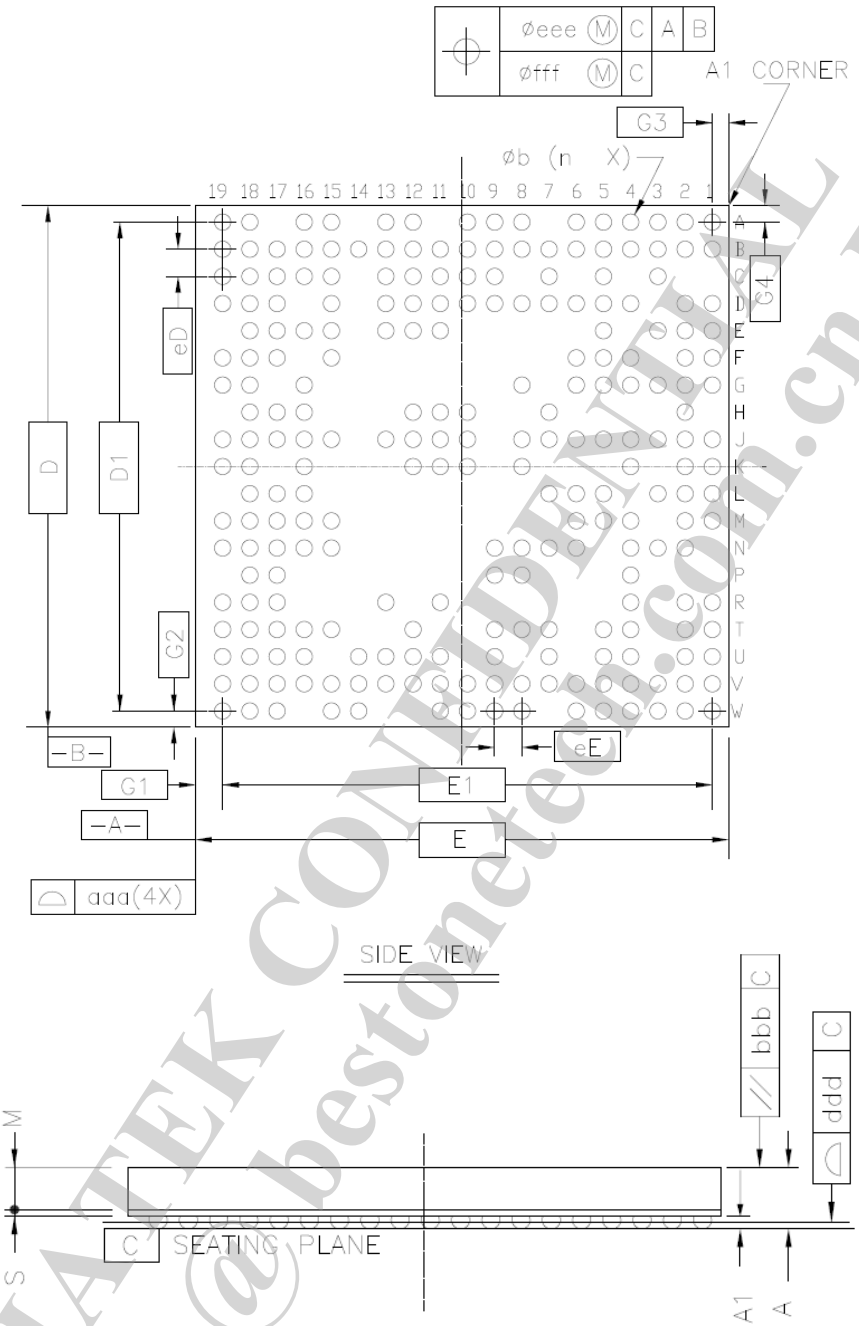
Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	AM suppression[1,4]	M = 0.3		60		dB
	Adjacent channel selectivity[1,4]	±200kHz		53		dB
	Alternate channel selectivity[1,4]	±400kHz		66		dB
	Spurious response rejection[4]	In-band		55		dB
	Maximum input level				117	dBμVemf
	Audio mono (S+N)/N[1,3,4]			58		dB
	Audio stereo (S+N)/N[2,3,4]			55		dB
	Audio stereo separation[4]	Δf = 75 kHz		35		dB
[1] Δf = 22.5kHz, fm = 1kHz, 75μs de-emphasis, mono, L = R						
[2] Δf = 22.5kHz, fm = 1kHz, 75s de-emphasis, stereo						
[3] A-weighting, BW = 300Hz to 15kHz						
[4] Vin = 60dBμVemf						
[5] Reference clock accuracy assumes ideal FM source. If the input FM source has less frequency error, then it is recommended to use a reference clock of accuracy within ±100ppm so as not to affect the channel scan quality.						

Table 45. FM receiver AC characteristics

2.10 Package Information

2.10.1 Package Outlines





		Symbol	Common Dimensions
Package :			TFBGA
Body Size:	X	E	9.800
	Y	D	9.600
Ball Pitch :	X	eE	0.500
	Y	eD	0.500
Total Thickness :		A	1.100 MAX.
Mold Thickness :		M	0.700 Ref.
Substrate Thickness :		S	0.110 Ref.
Ball Diameter :			0.300
Stand Off :		A1	0.160 ~ 0.260
Ball Width :		b	0.250 ~ 0.350
Package Edge Tolerance :		aaa	0.100
Mold Flatness :		bbb	0.100
Coplanarity:		ddd	0.080
Ball Offset (Package) :		eee	0.150
Ball Offset (Ball) :		fff	0.050
Ball Center TO Package Edge :		G1	0.500
		G2	0.300
		G3	0.300
		G4	0.300
Ball Count :		n	233
Edge Ball Center to Center :	X	E1	9.000
	Y	D1	9.000

Figure 19. Outlines and dimension of TFBGA 9.8mm*9.6mm, 233-ball, 0.5 mm pitch package

2.10.2 Thermal Operating Specifications

Symbol	Description	Value	Unit	Notes
	Thermal resistance from device junction to package case	45.3	C/W	
	Maximum package temperature	65	Deg C	
	Maximum power dissipation	1.328	W	

2.10.3 Lead-free Packaging

MT6250D is provided in a lead-free package and meets RoHS requirements

2.11 Ordering Information

2.11.1 Top Marking Definition

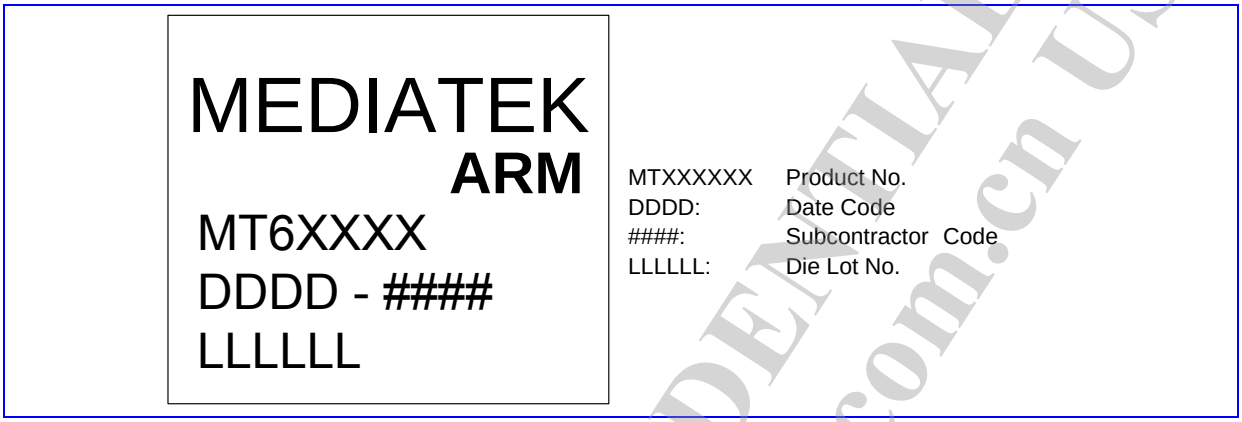


Figure 20. Mass production top marking of MT6250D

Part number	Package	Description
MT6250DA/BMB-PCU-H	TFBGA	9.8mm*9.6mm, 233-ball, 0.5 mm pitch package, non-security version