LPDDR5 SDRAM

MT62F512M32D2, MT62F1G32D4, MT62F2G32D8, MT62F512M64D4, MT62F1G64D8

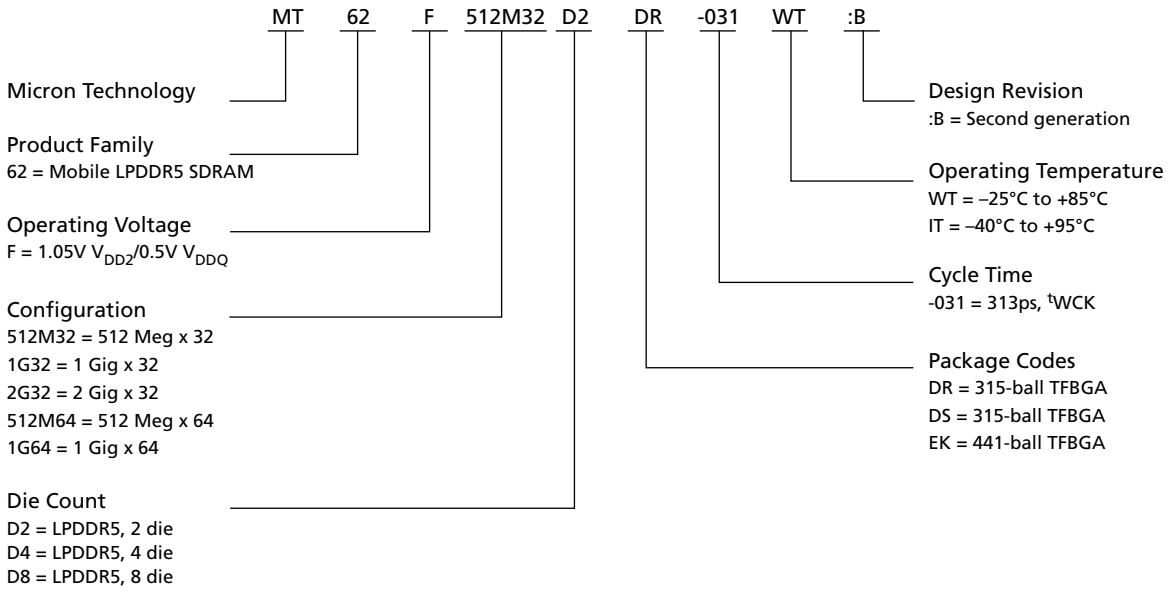
Features

- **Architecture**
  - 12.8 GB/s maximum bandwidth per channel
  - Frequency range: 800–5 MHz (data rate range per pin: 6400–40 Mb/s with WCK:CK = 4:1)
  - Selectable CKR (WCK:CK = 2:1 or 4:1)
- **LPDDR5 data interface**
  - Single x16 channel/die
  - Double-data-rate command/address entry
  - Differential command clocks (CK_t/CK_c) for high-speed operation
  - Differential data clocks (WCK_t/WCK_c)
  - Optional differential read strobe (RDQS_t/RDQS_c)
  - 16*n*-bit or 32*n*-bit prefetch architecture
  - 4KB page size with 8-bank (8B mode), 2KB page size with bank group (BG mode), or 16-bank (16B mode) operation
  - Command-selectable burst lengths (BL = 16 or 32) in bank group or 16-bank modes
  - Background ZQ calibration/command-based ZQ calibration
  - Optional link protection (link ECC)
  - Partial-array self refresh (PASR) and partial-array auto refresh (PAAR) with segment mask
- **Ultra-low-voltage core and I/O power supplies**
  - V_{DD1} = 1.70–1.95V; 1.8V NOM
  - V_{DD2H} = 1.01–1.12V; 1.05V NOM
  - V_{DD2L} = V_{DD2H} or 0.87–0.97V; 0.9V NOM
  - V_{DDQ} = 0.5V NOM or 0.3V NOM (ODT off)
- **I/O characteristics**
  - Interface-LVSTL 0.5/0.3
  - I/O type: Low-swing single-ended, V_{SS} terminated
  - V_{OH}-compensated output drive
  - Programmable V_{SS} on-die termination (ODT)
  - Non target ODT support
  - DVFSQ support
- **Low power features**
  - DVFSC: Dynamic voltage frequency scaling core
  - Single-ended CK, single-ended WCK and single-ended RDQS
  - Data copy
  - Write X

Options	Marking
• V_{DD1}/V_{DD2H}/V_{DD2L}/V_{DDQ} (ODTon)/(ODToff): 1.8V/1.05V/0.9V/0.5V/0.3V	F
• Array configuration	
– 512 Meg x 32 (2 channels x16 I/O)	512M32
– 1 Gig x 32 (2 channels x16 I/O)	1G32
– 2 Gig x 32 (2 channels x16 I/O)	2G32
– 512 Meg x 64 (4 channels x16 I/O)	512M64
– 1 Gig x 64 (4 channels x16 I/O)	1G64
• Device configuration	
– 512M16 × 2 die in package	D2
– 512M16 × 4 die in package	D4
– 512M16 × 8 die, 1024M8 × 8 die in package	D8
• FBGA "green" package	
– 315-ball TFBA (12.4mm × 15.0mm, seated height: 1.1mm MAX, Ø0.48SMD)	DR
– 315-ball TFBA (12.4mm × 15.0mm, seated height: 1.1mm MAX, Ø0.48SMD)	DS
– 441-ball TFBA (14.0mm × 14.0mm, seated height: 1.1mm MAX, Ø0.44SMD)	EK
• Speed grade, cycle time (^{t}WCK)	
– 6400 Mb/s	-031
• Operating temperature:	
– –25°C to +85°C	WT
– –40°C to +95°C	IT
• Revision	:B

Part Number Ordering Information

Figure 1: Part Number Chart



FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

LPDDR5/LPDDR5X Data Sheet List

For general LPDDR5/LPDDR5X specifications, please refer to the data sheets below.

- General LPDDR5/LPDDR5X Specifications 1: Mode Registers
- General LPDDR5/LPDDR5X Specifications 2: AC/DC and Interface Specifications
- General LPDDR5/LPDDR5X Specifications 3: Features and Functionalities

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General Notes

Throughout the data sheet, figures and text refer to DQs as DQ. DQ should be interpreted as any or all DQs collectively, unless specifically stated otherwise.

RDQS, CK, and WCK should be interpreted as RDQS_t, RDQS_c, CK_t, CK_c, and WCK_t, WCK_c respectively unless specifically stated otherwise. CA includes all CA pins used for a given density.

In timing diagrams, CMD is used as an indicator only. Actual signals occur on CA[6:0].

V_{REF} indicates $V_{REF(CA)}$ and $V_{REF(DQ)}$.

Complete functionality is described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

Device Configuration

Table 1: Die Organization in the Package (Dual Channel)

Die Organization	512M32 (16 Gb/package)	1G32 (32 Gb/package)	2G32 (64 Gb/package)
Channel A, rank 0	x16 mode × 1 die	x16 mode × 1 die	x8 mode × 2 die
Channel B, rank 0	x16 mode × 1 die	x16 mode × 1 die	x8 mode × 2 die
Channel A, rank 1	–	x16 mode × 1 die	x8 mode × 2 die
Channel B, rank 1	–	x16 mode × 1 die	x8 mode × 2 die

Notes: 1. Refer to the Package Block Diagram section in this data sheet.

Table 2: Die Organization in the Package (Quad Channel)

Die Organization	512M64 (32 Gb/package)	1G64 (64 Gb/package)
Channel A, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel B, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel C, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel D, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel A, rank 1	–	x16 mode × 1 die
Channel B, rank 1	–	x16 mode × 1 die
Channel C, rank 1	–	x16 mode × 1 die
Channel D, rank 1	–	x16 mode × 1 die

Notes: 1. Refer to the Package Block Diagram section in this data sheet.

Table 3: Die Addressing

Description	512M32 (16 Gb/package)/ 1G32 (32 Gb/package)/ 512M64 (32 Gb/package)/ 1G64 (64 Gb/package)			2G32 (64 Gb/package)		
Density per die	8Gb			8Gb		
Bits	8,589,934,592			8,589,934,592		
Bank mode	BG mode	16B mode	8B mode	BG mode	16B mode	8B mode
Configuration	32Mb × 16 DQ × 4 banks × 4BG	32Mb × 16 DQ × 16 banks	64Mb × 16 DQ × 8 banks	64Mb × 8DQ × 4 banks × 4BG	64Mb × 8DQ × 16 banks	128Mb × 8DQ × 8 banks
Number of banks	4	16	8	4	16	8
Number of bank groups	4	1	1	4	1	1
Array prefetch bits	256	256	512	128	128	256
Rows per bank	32,768			65,536		
Columns	64			64		
Page size (bytes)	2048	2048	4096	1024	1024	2048
Native burst length	16	16	32	16	16	32

Table 3: Die Addressing (Continued)

Description	512M32 (16 Gb/package)/ 1G32 (32 Gb/package)/ 512M64 (32 Gb/package)/ 1G64 (64 Gb/package)			2G32 (64 Gb/package)		
Number of I/Os	16			8		
Bank address	BA[1:0]	BA[3:0]	BA[2:0]	BA[1:0]	BA[3:0]	BA[2:0]
Bank group address	BG[1:0]	–	–	BG[1:0]	–	–
Row address	R[14:0]			R[15:0]		
Column address	C[5:0]			C[5:0]		
Burst address	B[3:0]	B[3:0]	B[4:0]	B[3:0]	B[3:0]	B[4:0]
Burst starting address boundary	128-bit			128-bit		

Notes: 1. Refer to the SDRAM Addressing section in General LPDDR5 Specifications 3.

Refresh Requirement Parameters

Table 4: Refresh Requirement Parameters

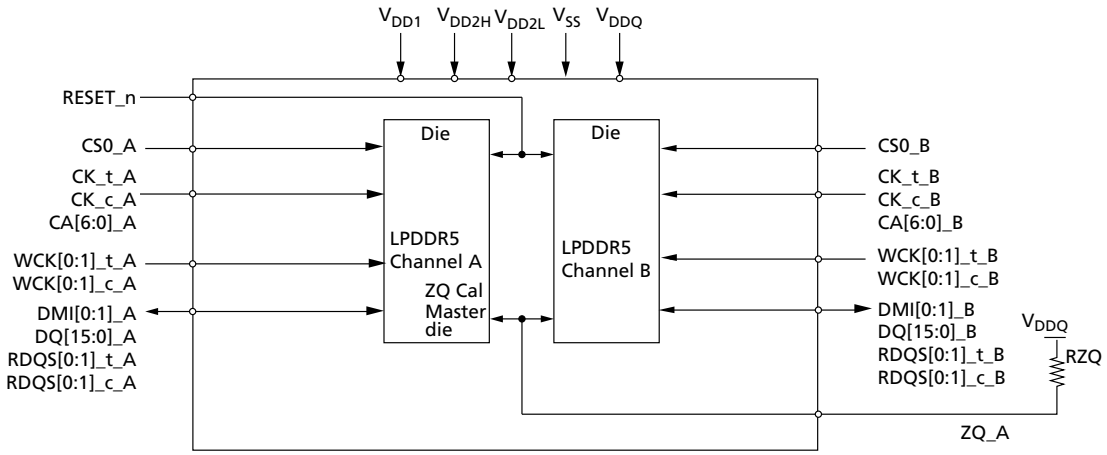
Parameter	Symbol	8Gb Die		Unit
		BG and 16B Mode	8B Mode	
REFRESH cycle time (all banks)	^{t}RFCab	210	210	ns
REFRESH cycle time (per bank)	^{t}RFCpb	120	120	ns
Per bank refresh to per bank refresh time (different bank)	^{t}PBR2PBR	90	90	ns
Per bank refresh to ACTIVATE command time (different bank)	^{t}PBR2ACT	7.5	10	ns

Notes: 1. This table only describes refresh parameters that are density dependent. Refer to Refresh Requirement section in General LPDDR5/LPDDR5X Specifications 3 for all refresh parameters.

Package Block Diagrams

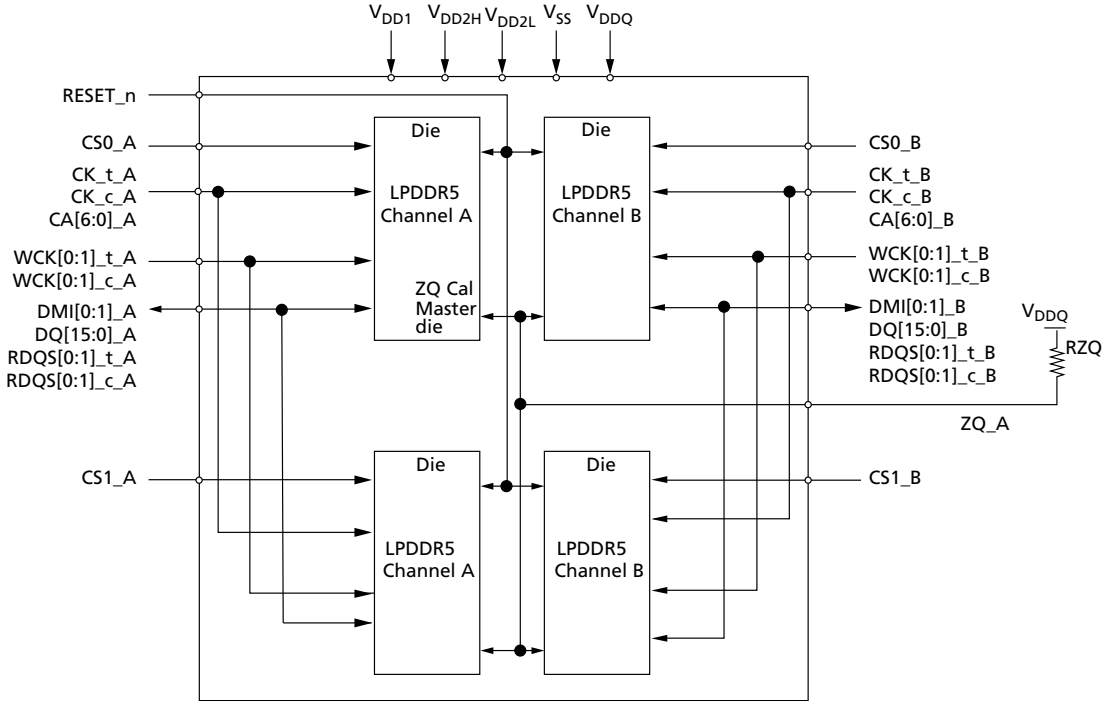
Dual Die, Dual Channel

Figure 2: Dual-Die, Dual-Channel Package Block Diagram



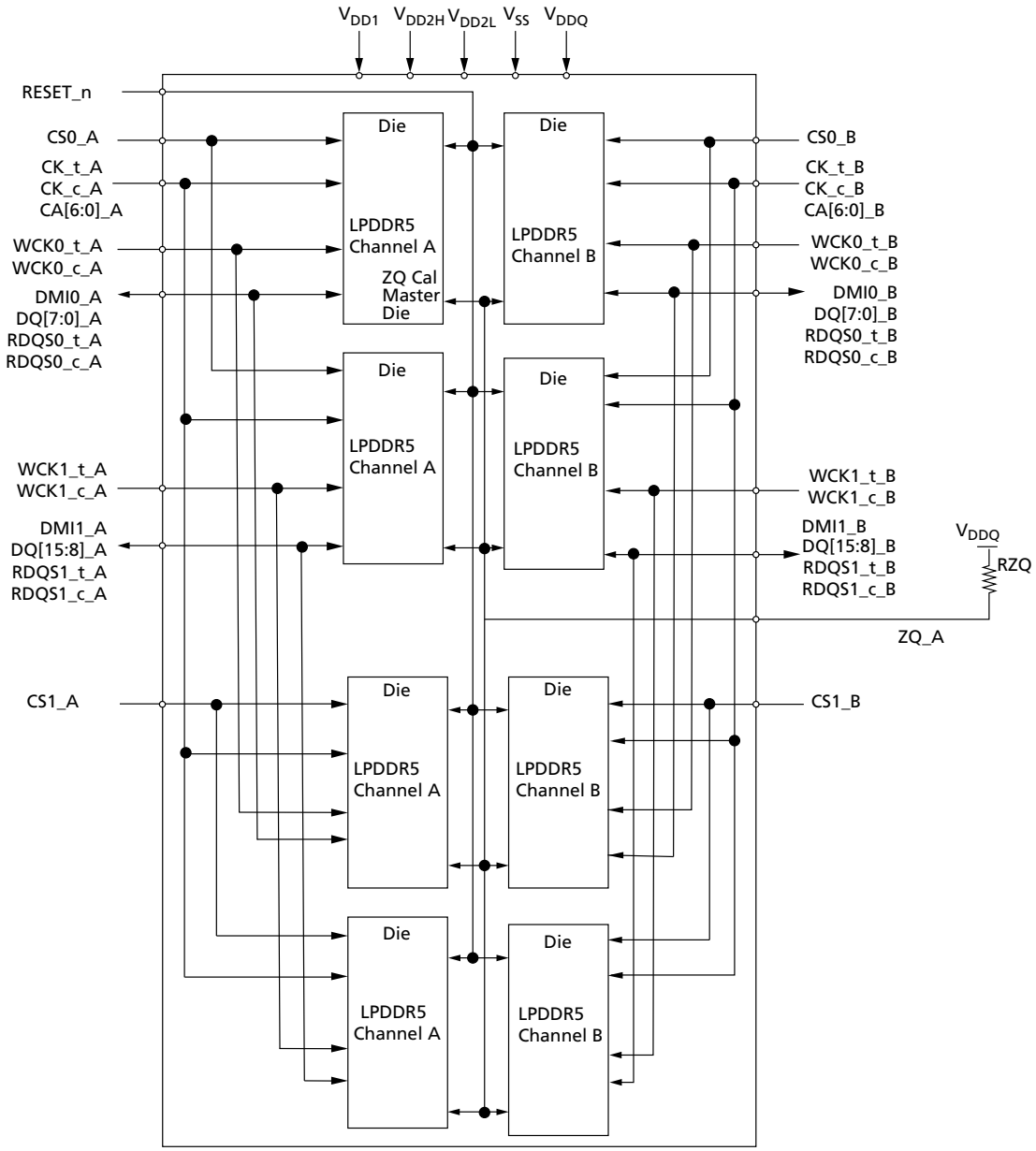
Quad Die, Dual Channel

Figure 3: Quad-Die, Dual-Channel Package Block Diagram



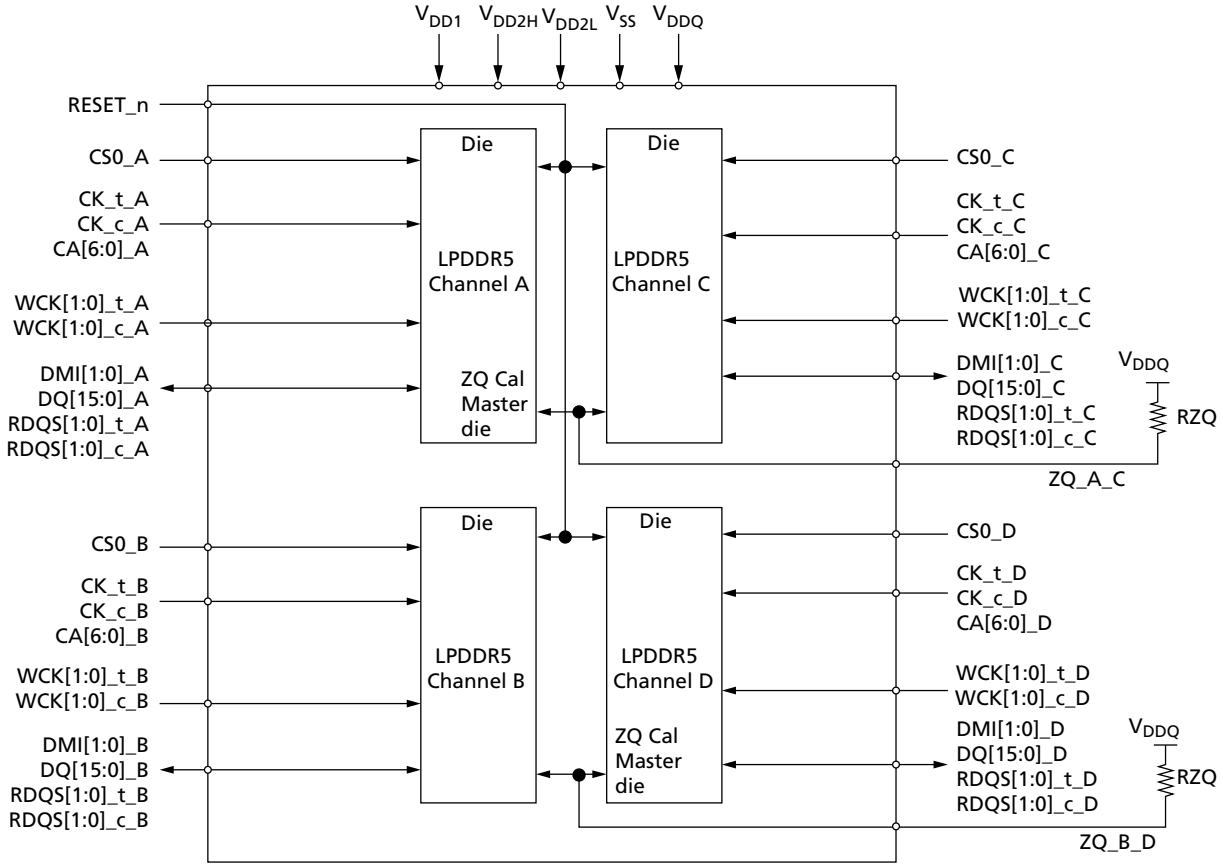
Eight Die, Dual Channel

Figure 4: Eight-Die, Dual-Channel Package Block Diagram



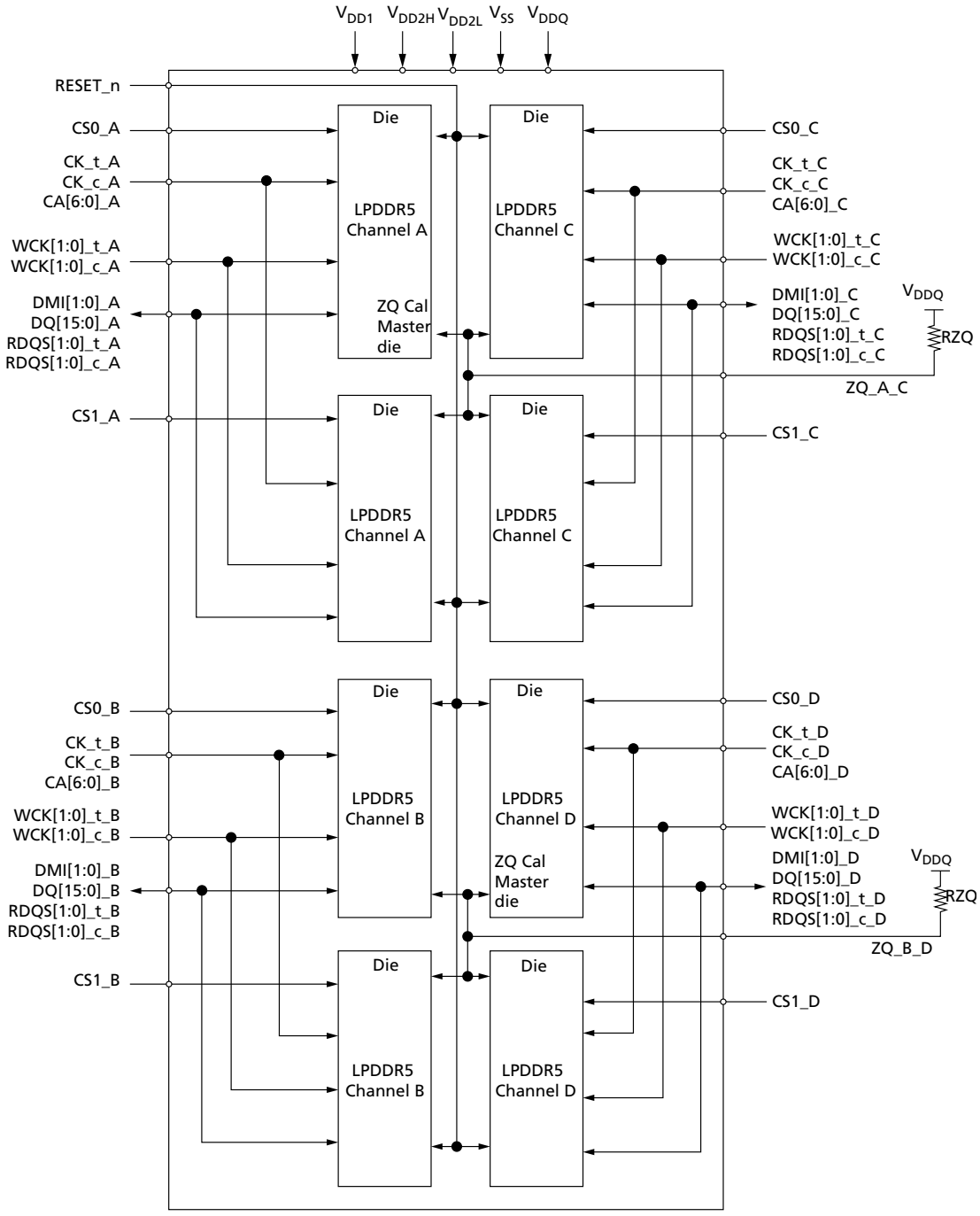
Quad Die, Quad Channel

Figure 5: Quad-Die, Quad-Channel Package Block Diagram



Eight Die, Quad Channel

Figure 6: Eight-Die, Quad-Channel Package Block Diagram

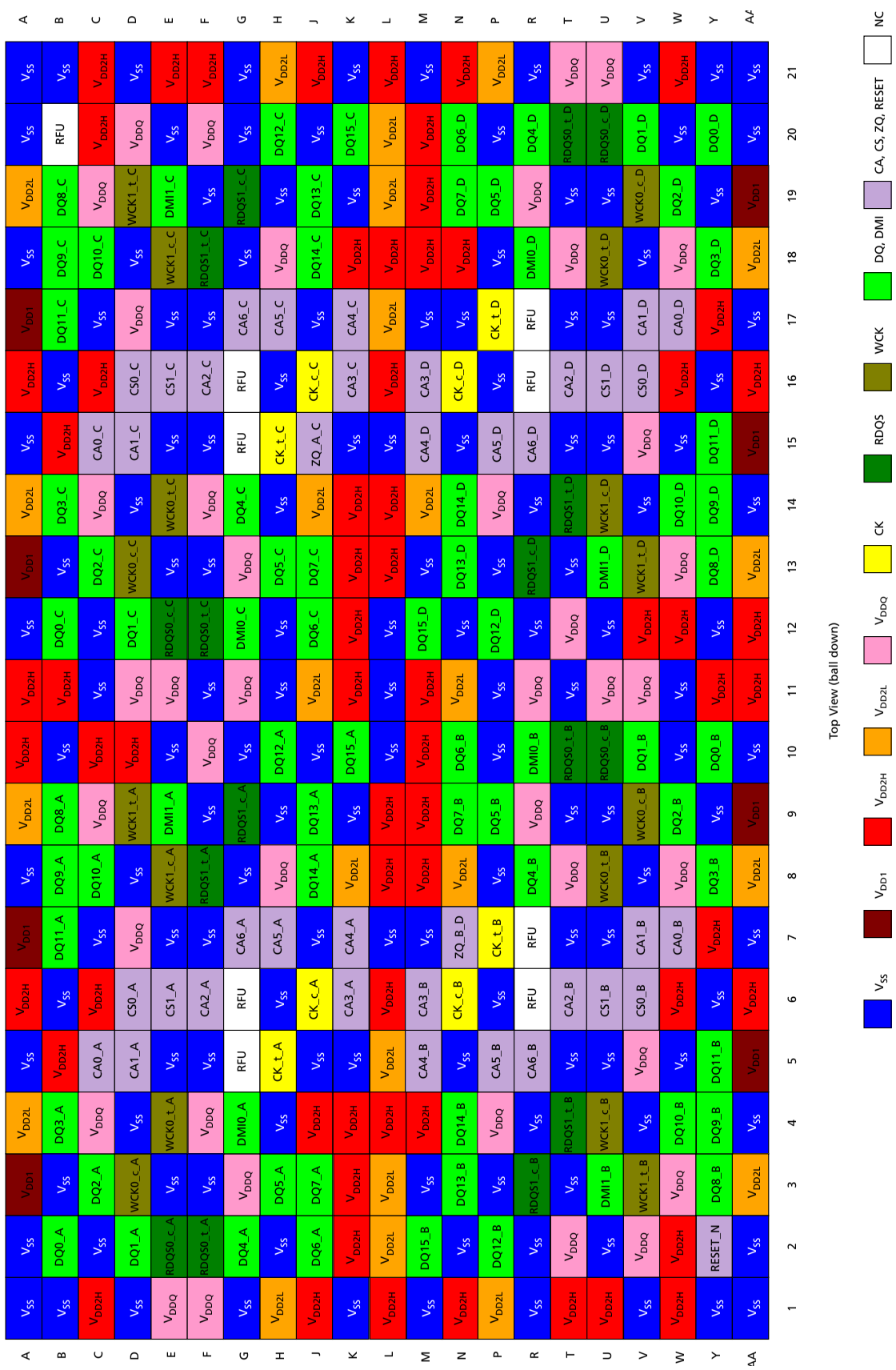


Ball Assignments and Descriptions

Table 5: 441-Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A:D] CK_c_[A:D]	Input	**Clock:** CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A:D], CS1_[A:D]	Input	**Chip select:** CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:D] become NC pins in a single-rank package.
CA[6:0]_[A:D]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A:D] WCK[1:0]_c_[A:D]	Input	**Data clock:** WCK_t and WCK_c are differential clock inputs used for WRITE data capture and READ data output.
DQ[15:0]_[A:D]	I/O	**Data input/output:** Bidirectional data bus.
RDQS[1:0]_t_[A:D] RDQS[1:0]_c_[A:D]	I/O Output	**Read data strobe:** RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A:D]	I/O	**Data mask inversion:** DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A_C, ZQ_B_D	Reference	**ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V_{DDQ} through a 240Ω ±1% resistor.
V_{DDQ}, V_{DD1}, V_{DD2H}, V_{DD2L}	Supply	**Power supplies:** Isolated on the die for improved noise immunity.
V_{SS}	Supply	**Ground reference:** Power supply ground reference.
RESET_n	Input	**Reset:** When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	**No connect:** Not internally connected.

Figure 7: 441-Ball Quad-Channel FBGA



Ball Assignments and Descriptions

Table 6: 315-Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A:B] CK_c_[A:B]	Input	**Clock:** CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A:B], CS1_[A:B]	Input	**Chip select:** CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:B] become NC pins in a single-rank package.
CA[6:0]_[A:B]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A:B] WCK[1:0]_c_[A:B]	Input	**Data clock:** WCK_t and WCK_c are differential clock inputs used for write data capture and read data output.
DQ[15:0]_[A:B]	I/O	**Data input/output:** Bidirectional data bus.
RDQS[1:0]_t_[A:B] RDQS[1:0]_c_[A:B]	I/O Output	**Read data strobe:** RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A:B]	I/O	**Data mask inversion:** DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A	Reference	**ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V_{DDQ} through a 240Ω ±1% resistor.
V_{DDQ}, V_{DD1}, V_{DD2H}, V_{DD2L}	Supply	**Power supplies:** Isolated on the die for improved noise immunity.
V_{SS}	Supply	**Ground reference:** Power supply ground reference.
RESET_n	Input	**Reset:** When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	**No connect:** Not internally connected.

Figure 8: 315-Ball Dual-Channel Discrete FBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	NC	NC	V_{DDQ}	DMI0_A	V_{SS}	V_{DD2L}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2L}	V_{SS}	DMI1_A	V_{DDQ}	NC	NC	A
B	NC	V_{DDQ}	RDQS0_t_A	V_{SS}	DQ4_A	V_{DD2L}	V_{DD2H}	V_{SS}	V_{DD2H}	V_{DD2L}	DQ12_A	V_{SS}	RDQS1_t_A	V_{DDQ}	NC	B
C	V_{DD1}	DQ1_A	V_{DDQ}	RDQS0_c_A	V_{SS}	DQ5_A	V_{DD2H}	V_{SS}	V_{DD2H}	DQ13_A	V_{SS}	RDQS1_c_A	V_{DDQ}	DQ9_A	V_{DD1}	C
D	DQ0_A	V_{SS}	DQ3_A	V_{DDQ}	WCK0_c_A	V_{SS}	V_{SS}	V_{DD2H}	V_{SS}	V_{SS}	WCK1_c_A	V_{DDQ}	DQ11_A	V_{SS}	DQ8_A	D
E	V_{SS}	DQ2_A	V_{SS}	WCK0_t_A	V_{DDQ}	DQ6_A	V_{DD2H}	V_{SS}	V_{DD2H}	DQ14_A	V_{DDQ}	WCK1_t_A	V_{SS}	DQ10_A	V_{SS}	E
F	V_{DDQ}	V_{SS}	V_{DDQ}	V_{DDQ}	DQ7_A	V_{DD2H}	V_{DD2H}	V_{SS}	V_{DD2H}	V_{DD2H}	DQ15_A	V_{DDQ}	V_{DDQ}	V_{SS}	V_{DDQ}	F
G	V_{DDQ}	V_{DDQ}	V_{SS}	CA0_A	V_{SS}	CS1_A	V_{SS}	CA2_A	V_{SS}	CA4_A	V_{SS}	CA6_A	V_{SS}	V_{DDQ}	V_{DDQ}	G
H	RESET_N	V_{DD2L}	V_{SS}	V_{SS}	CA1_A	V_{SS}	CS0_A	V_{SS}	CK_t_A	V_{SS}	CA3_A	V_{SS}	CA5_A	V_{DD2L}	ZQ_A	H
J	V_{SS}	V_{DD2L}	V_{SS}	RFU	V_{DD2H}	RFU	V_{SS}	V_{SS}	CK_c_A	V_{SS}	V_{DD2H}	V_{SS}	V_{SS}	V_{DD2L}	V_{SS}	J
K	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{SS}	V_{SS}	V_{SS}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	K
L	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	L
M	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{SS}	V_{SS}	V_{SS}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	M
N	V_{SS}	V_{DD2L}	V_{SS}	V_{SS}	V_{DD2H}	V_{SS}	CK_c_B	V_{SS}	V_{SS}	V_{SS}	V_{DD2H}	V_{SS}	V_{SS}	V_{DD2L}	V_{SS}	N
P	RFU	V_{DD2L}	CA5_B	V_{SS}	CA3_B	V_{SS}	CK_t_B	V_{SS}	CS0_B	V_{SS}	CA1_B	V_{SS}	V_{SS}	V_{DD2L}	RFU	P
R	V_{DDQ}	V_{DDQ}	V_{SS}	CA6_B	V_{SS}	CA4_B	V_{SS}	CA2_B	V_{SS}	CS1_B	V_{SS}	CA0_B	V_{SS}	V_{DDQ}	V_{DDQ}	R
T	V_{DDQ}	V_{SS}	V_{DDQ}	V_{DDQ}	DQ15_B	V_{DD2H}	V_{DD2H}	V_{SS}	V_{DD2H}	V_{DD2H}	DQ7_B	V_{DDQ}	V_{DDQ}	V_{SS}	V_{DDQ}	T
U	V_{SS}	DQ10_B	V_{SS}	WCK1_t_B	V_{DDQ}	DQ14_B	V_{DD2H}	V_{SS}	V_{DD2H}	DQ6_B	V_{DDQ}	WCK0_t_B	V_{SS}	DQ2_B	V_{SS}	U
V	DQ8_B	V_{SS}	DQ11_B	V_{DDQ}	WCK1_c_B	V_{SS}	V_{SS}	V_{DD2H}	V_{SS}	V_{SS}	WCK0_c_B	V_{DDQ}	DQ3_B	V_{SS}	DQ0_B	V
W	V_{DD1}	DQ9_B	V_{DDQ}	RDQS1_c_B	V_{SS}	DQ13_B	V_{DD2H}	V_{SS}	V_{DD2H}	DQ5_B	V_{SS}	RDQS0_c_B	V_{DDQ}	DQ1_B	V_{DD1}	W
Y	NC	V_{DDQ}	RDQS1_t_B	V_{SS}	DQ12_B	V_{DD2L}	V_{DD2H}	V_{SS}	V_{DD2H}	V_{DD2L}	DQ4_B	V_{SS}	RDQS0_t_B	V_{DDQ}	NC	Y
AA	NC	NC	V_{DDQ}	DMI1_B	V_{SS}	V_{DD2L}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2L}	V_{SS}	DMI0_B	V_{DDQ}	NC	NC	AA
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

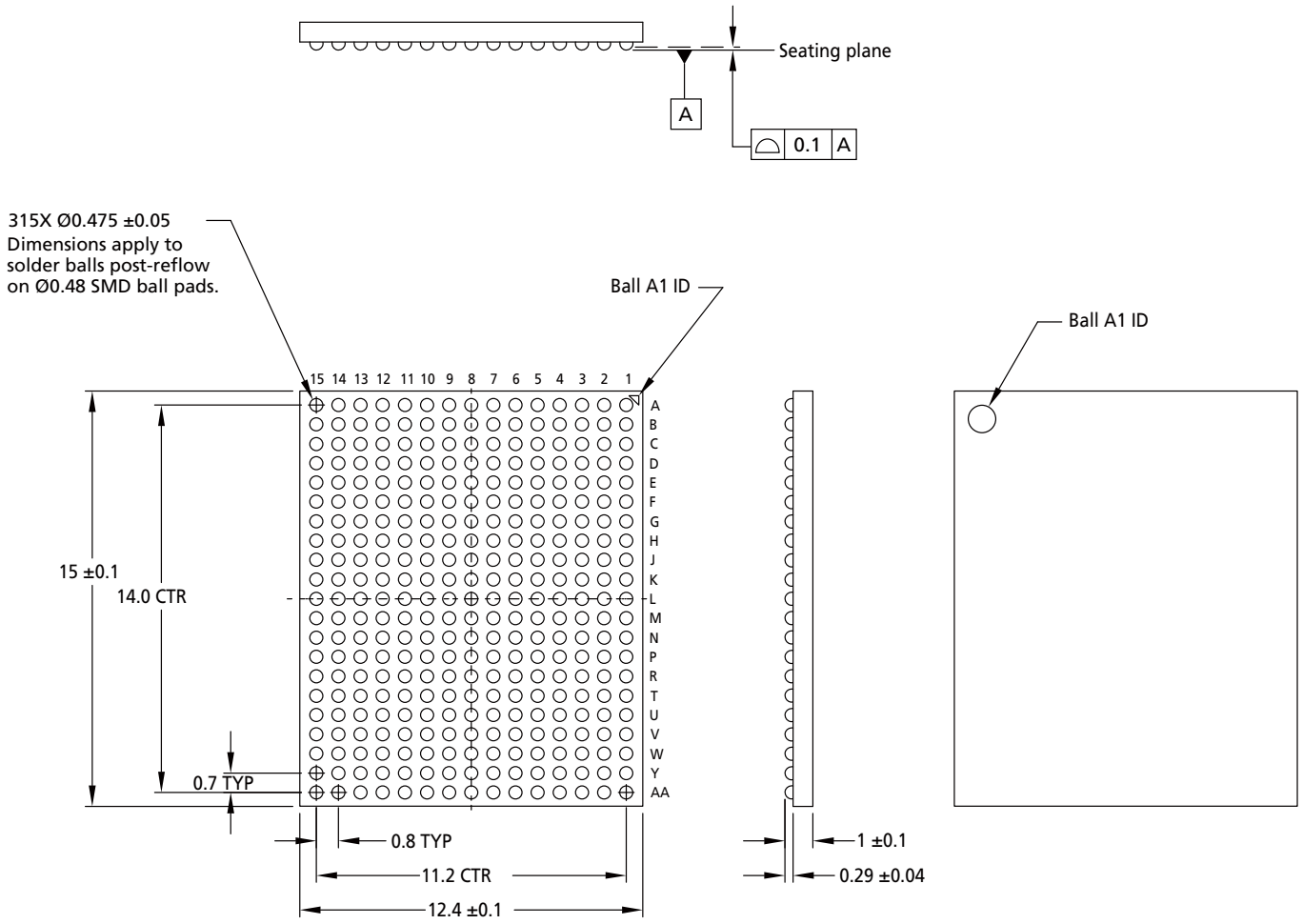
Top View (ball down)

VSS | V_{DD1} | V_{DD2H} | V_{DD2L} | V_{DDQ} | CK | RDQS | WCK | DQ,DMI | CA, CS, ZQ, RESET | NC, RFU

Package Dimensions

315-Ball Package (Package Code: DR)

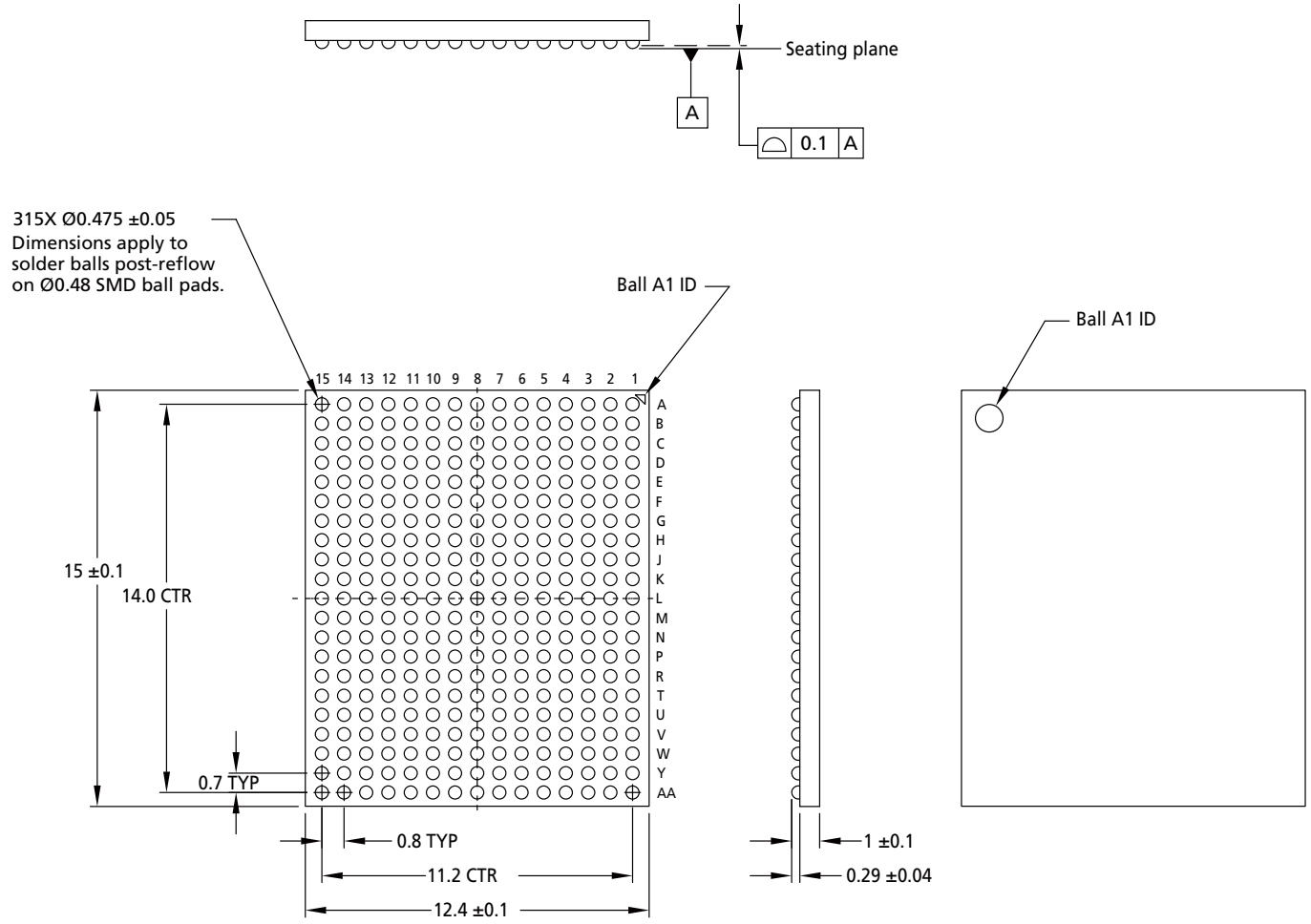
Figure 9: 315-Ball TFBGA – 12.4mm × 15mm (Package Code: DR)



Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SAC302 with NiAu pads (Sn-3Ag-0.2Cu)

315-Ball Package (Package Code: DS)

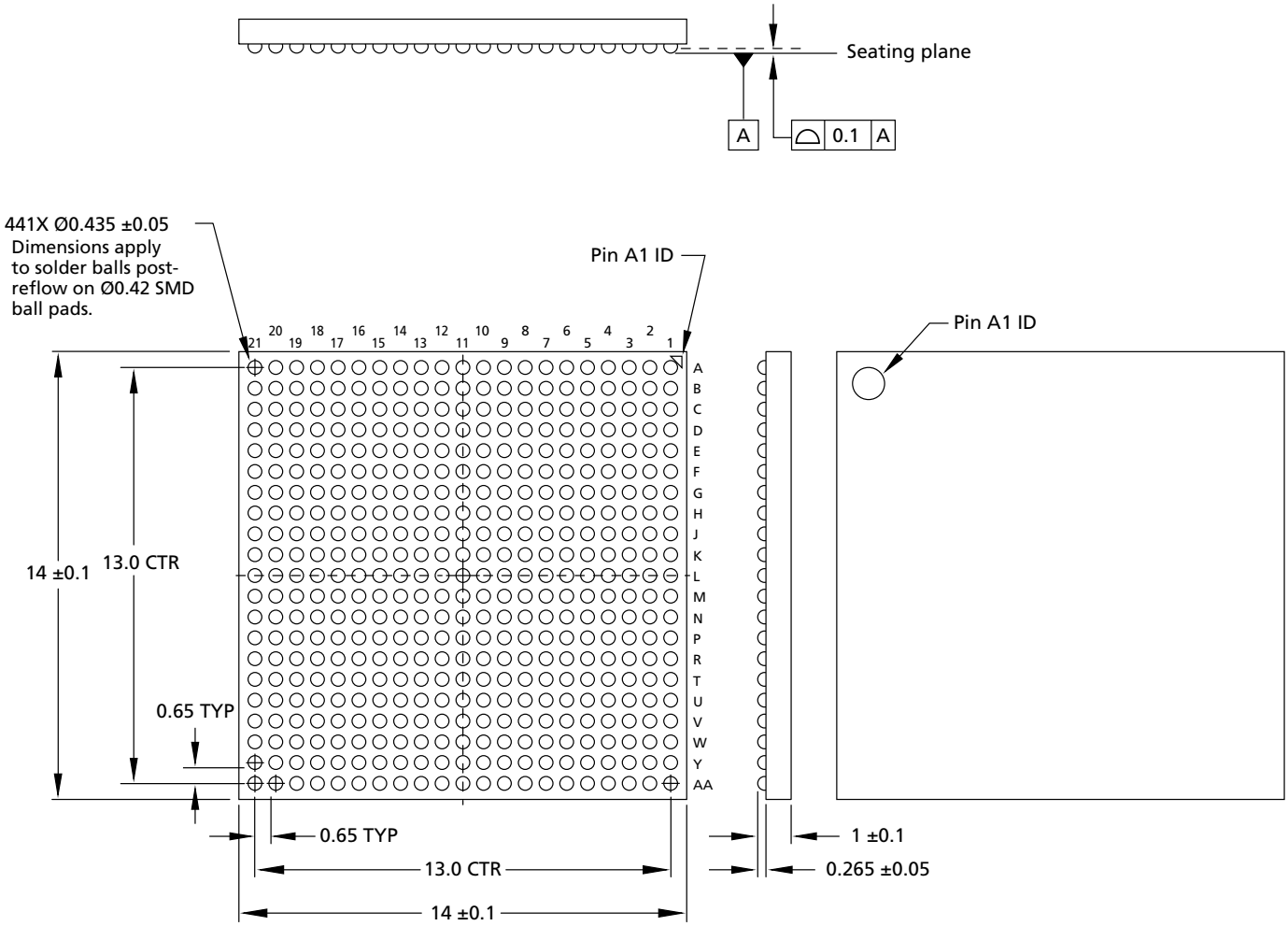
Figure 10: 315-Ball TFBGA – 12.4mm × 15mm (Package Code: DS)



Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SACQ with CuOSP pads (Sn-4Ag-0.5Cu-3Bi-0.05Ni)

441-Ball Package (Package Code: EK)

Figure 11: 441-Ball TFBGA – 14.0mm x 14.0mm (Package Code: EK)



Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SACQ with CuOSP pads (Sn- 4Ag-0.5Cu-3Bi-0.05Ni)

Product-Specific Mode Register Definition

Table 7: Mode Register Contents

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR0			Unified NT ODT behavior mode	DMI output behavior mode	Optimized refresh mode	Enhanced WCK always-on mode	Latency mode	NT ODT timing mode
	OP[0] = 1b: Device supports different NT ODT latency for DQ and RDQS							
	OP[1] = 0b: Device supports x16 mode latency 1b: Device supports byte mode latency							
	OP[2] = 1b: Device supports enhanced WCK always-on mode							
	OP[3] = 1b: Device supports optimized refresh mode							
	OP[4] = 1b: Device supports both DMI behavior mode 1 and 2 and mode selection							
	OP[5] = 1b: The NT ODT behavior follows the unified NT ODT behavior							
MR5	Manufacturer ID							
	1111 1111b : Micron							
MR6	Revision ID1							
	0000 0110b							
MR8	I/O width		Density					
	OP[7:6] = 00b: x16 OP[7:6] = 01b: x8		OP[5:2] = 0100b: 8Gb					
MR13						VRO		
	OP[2] = 0b: Normal operation (default) 1b: Output the $V_{REF(CA)}$ value on DQ7 and $V_{REF(DQ)}$ value on DQ6							
MR19			WCK2DQ OSC FM					
	OP[5] = 1b: WCK2DQ OSC FM supported							
MR21	WXS				ODTD-CSFS	WXFS	RDCFS	WDCFS
	OP[0] = 1b: WRITE DATA COPY function supported							
	OP[1] = 1b: READ DATA COPY function supported							
	OP[2] = 1b: WRITE X function supported							
	OP[3] = 1b: Device ODTD-CS is supported							
	OP[7] = 1b: Data to be written can be selected with 0 and 1							
MR22	RECC		WECC					
	OP[5:4] = 00b: Write link ECC disabled (default) 01b: Write link ECC enabled (See Note 3)							
	OP[7:6] = 00b: Read link ECC disabled (default) 01b: Read link ECC enabled (See Note 3)							
MR24	DFES							
	OP[7] = 1b: DFE is supported							

Table 7: Mode Register Contents (Continued)

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR26		**RDQSTFS**						
	OP[6] = 1b: Read/write-based RDQS_t TRAINING function supported							
MR27								**RFM**
	OP[0] = 0b: RFM not required							
MR43		**SBEC Rule**						
	OP[6] = 1b: Simultaneous SBE on each DQ byte and DMI are independently counted							

Notes: 1. The contents of mode registers described here reflect information specific to each die in these packages.
2. Refer to General LPDDR5 Specification 1 for mode registers not described here.
3. Write link ECC and read link ECC are supported.

I_{DD} Parameters

Refer to I_{DD} Specification Parameters and Test Conditions section in General LPDDR5 Specifications 2 for detailed conditions.

Table 8: I_{DD} Parameters – Single Die

V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V

Notes 1 and 2 apply to entire table.

Symbol	Supply	x8 Mode, 6400 Mb/s	Unit	Note
		WT		
I_{DD01}	V_{DD1}	2.40	mA	
I_{DD02H}	V_{DD2H}	27.00		
I_{DD02L}	V_{DD2L}	0.25		
I_{DD0Q}	V_{DDQ}	0.75		
I_{DD2P1}	V_{DD1}	1.20	mA	
I_{DD2P2H}	V_{DD2H}	1.80		
I_{DD2P2L}	V_{DD2L}	0.25		
I_{DD2PQ}	V_{DDQ}	0.75		
I_{DD2PS1}	V_{DD1}	1.20	mA	
$I_{DD2PS2H}$	V_{DD2H}	1.80		
$I_{DD2PS2L}$	V_{DD2L}	0.25		
I_{DD2PSQ}	V_{DDQ}	0.75		
I_{DD2N1}	V_{DD1}	1.20	mA	
I_{DD2N2H}	V_{DD2H}	16.00		
I_{DD2N2L}	V_{DD2L}	0.25		
I_{DD2NQ}	V_{DDQ}	0.75		
I_{DD2NS1}	V_{DD1}	1.20	mA	
$I_{DD2NS2H}$	V_{DD2H}	16.00		
$I_{DD2NS2L}$	V_{DD2L}	0.25		
I_{DD2NSQ}	V_{DDQ}	0.75		
I_{DD3P1}	V_{DD1}	1.30	mA	
I_{DD3P2H}	V_{DD2H}	4.80		
I_{DD3P2L}	V_{DD2L}	0.25		
I_{DD3PQ}	V_{DDQ}	0.75		

Symbol	Supply	x8 Mode, 6400 Mb/s	Unit	Note
		WT		
I_{DD3PS1}	V_{DD1}	1.30	mA	
$I_{DD3PS2H}$	V_{DD2H}	4.80		
$I_{DD3PS2L}$	V_{DD2L}	0.25		
I_{DD3PSQ}	V_{DDQ}	0.75		
I_{DD3N1}	V_{DD1}	1.60	mA	
I_{DD3N2H}	V_{DD2H}	23.00		
I_{DD3N2L}	V_{DD2L}	0.25		
I_{DD3NQ}	V_{DDQ}	0.75		
I_{DD3NS1}	V_{DD1}	1.60	mA	
$I_{DD3NS2H}$	V_{DD2H}	23.00		
$I_{DD3NS2L}$	V_{DD2L}	0.25		
I_{DD3NSQ}	V_{DDQ}	0.75		
I_{DD4R1}	V_{DD1}	5.90	mA	3, 4
I_{DD4R2H}	V_{DD2H}	227.00		
I_{DD4R2L}	V_{DD2L}	0.25		
I_{DD4RQ}	V_{DDQ}	52.90		
I_{DD4W1}	V_{DD1}	5.20	mA	3
I_{DD4W2H}	V_{DD2H}	180.00		
I_{DD4W2L}	V_{DD2L}	0.25		
I_{DD4WQ}	V_{DDQ}	0.75		
I_{DD51}	V_{DD1}	20.00	mA	
I_{DD52H}	V_{DD2H}	160.00		
I_{DD52L}	V_{DD2L}	0.25		
I_{DD5Q}	V_{DDQ}	0.75		
I_{DD5AB1}	V_{DD1}	2.20	mA	
$I_{DD5AB2H}$	V_{DD2H}	24.00		
$I_{DD5AB2L}$	V_{DD2L}	0.25		
I_{DD5ABQ}	V_{DDQ}	0.75		
I_{DD5PB1}	V_{DD1}	2.20	mA	
$I_{DD5PB2H}$	V_{DD2H}	24.00		
$I_{DD5PB2L}$	V_{DD2L}	0.25		
I_{DD5PBQ}	V_{DDQ}	0.75		

Notes: 1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.

2. BG mode. DVFSC and DVFSQ disabled.
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C

Table 9: I_{DD} Parameters – Single Die

V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V

Notes 1 and 2 apply to entire table.

Symbol	Supply	x16 Mode, 6400 Mb/s		Unit	Note
		WT	IT		
I_{DD01}	V_{DD1}	2.80	2.90	mA	
I_{DD02H}	V_{DD2H}	32.00	45.00		
I_{DD02L}	V_{DD2L}	0.25	0.25		
I_{DD0Q}	V_{DDQ}	0.75	0.75		
I_{DD2P1}	V_{DD1}	1.20	1.30	mA	
I_{DD2P2H}	V_{DD2H}	1.80	2.50		
I_{DD2P2L}	V_{DD2L}	0.25	0.25		
I_{DD2PQ}	V_{DDQ}	0.75	0.75		
I_{DD2PS1}	V_{DD1}	1.20	1.30	mA	
$I_{DD2PS2H}$	V_{DD2H}	1.80	2.50		
$I_{DD2PS2L}$	V_{DD2L}	0.25	0.25		
I_{DD2PSQ}	V_{DDQ}	0.75	0.75		
I_{DD2N1}	V_{DD1}	1.20	1.30	mA	
I_{DD2N2H}	V_{DD2H}	16.00	30.00		
I_{DD2N2L}	V_{DD2L}	0.25	0.25		
I_{DD2NQ}	V_{DDQ}	0.75	0.75		
I_{DD2NS1}	V_{DD1}	1.20	1.30	mA	
$I_{DD2NS2H}$	V_{DD2H}	16.00	30.00		
$I_{DD2NS2L}$	V_{DD2L}	0.25	0.25		
I_{DD2NSQ}	V_{DDQ}	0.75	0.75		
I_{DD3P1}	V_{DD1}	1.30	1.50	mA	
I_{DD3P2H}	V_{DD2H}	4.80	8.40		
I_{DD3P2L}	V_{DD2L}	0.25	0.25		
I_{DD3PQ}	V_{DDQ}	0.75	0.75		
I_{DD3PS1}	V_{DD1}	1.30	1.50	mA	
$I_{DD3PS2H}$	V_{DD2H}	4.80	8.40		
$I_{DD3PS2L}$	V_{DD2L}	0.25	0.25		
I_{DD3PSQ}	V_{DDQ}	0.75	0.75		

Symbol	Supply	x16 Mode, 6400 Mb/s		Unit	Note
		WT	IT		
I_{DD3N1}	V_{DD1}	1.60	1.90	mA	
I_{DD3N2H}	V_{DD2H}	23.00	39.00		
I_{DD3N2L}	V_{DD2L}	0.25	0.25		
I_{DD3NQ}	V_{DDQ}	0.75	0.75		
I_{DD3NS1}	V_{DD1}	1.60	1.90	mA	
$I_{DD3NS2H}$	V_{DD2H}	23.00	39.00		
$I_{DD3NS2L}$	V_{DD2L}	0.25	0.25		
I_{DD3NSQ}	V_{DDQ}	0.75	0.75		
I_{DD4R1}	V_{DD1}	7.10	7.20	mA	3, 4
I_{DD4R2H}	V_{DD2H}	360.00	372.00		
I_{DD4R2L}	V_{DD2L}	0.25	0.25		
I_{DD4RQ}	V_{DDQ}	105.78	106.00		
I_{DD4W1}	V_{DD1}	6.10	6.20	mA	3
I_{DD4W2H}	V_{DD2H}	280.00	310.00		
I_{DD4W2L}	V_{DD2L}	0.25	0.25		
I_{DD4WQ}	V_{DDQ}	0.75	0.75		
I_{DD51}	V_{DD1}	20.00	23.00	mA	
I_{DD52H}	V_{DD2H}	160.00	170.00		
I_{DD52L}	V_{DD2L}	0.25	0.25		
I_{DD5Q}	V_{DDQ}	0.75	0.75		
I_{DD5AB1}	V_{DD1}	2.20	2.20	mA	
$I_{DD5AB2H}$	V_{DD2H}	24.00	35.00		
$I_{DD5AB2L}$	V_{DD2L}	0.25	0.25		
I_{DD5ABQ}	V_{DDQ}	0.75	0.75		
I_{DD5PB1}	V_{DD1}	2.20	2.20	mA	
$I_{DD5PB2H}$	V_{DD2H}	24.00	35.00		
$I_{DD5PB2L}$	V_{DD2L}	0.25	0.25		
I_{DD5PBQ}	V_{DDQ}	0.75	0.75		

Notes: 1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. BG mode. DVFSC and DVFSQ disabled.
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C

Table 10: Full-Array Power-Down Self Refresh Current – Single Die

V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V

Temperature	Symbol	Supply	Value	Unit
25°C	I_{DD61}	V_{DD1}	0.25	mA
	I_{DD62H}	V_{DD2H}	0.60	
	I_{DD62L}	V_{DD2L}	0.01	
	I_{DD6Q}	V_{DDQ}	0.01	
85°C	I_{DD61}	V_{DD1}	2.00	
	I_{DD62H}	V_{DD2H}	5.30	
	I_{DD62L}	V_{DD2L}	0.25	
	I_{DD6Q}	V_{DDQ}	0.75	
95°C	I_{DD61}	V_{DD1}	3.60	
	I_{DD62H}	V_{DD2H}	14.50	
	I_{DD62L}	V_{DD2L}	0.25	
	I_{DD6Q}	V_{DDQ}	0.75	

Notes: 1. I_{DD6}25°C is the typical value in the distribution with nominal V_{DD} and a reference-only value. I_{DD6}85°C and I_{DD6}95°C are the maximum I_{DD} guaranteed value considering the worst-case conditions of process, temperature, and voltage.
2. DVFSC and DVFSQ disabled.

Revision History

Rev. A – 5/2021

- Initial release , CCM005-1974498342-68 y31m_embedded_lpddr5.pdf – Rev. D 01/2021 EN and CCM005-1974498342-69 315b_y31m_ddp_qdp_8dp_lpddr5.pdf – Rev. C 4/2021 EN

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006
208-368-4000, micron.com/support