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MT6500, MT6510

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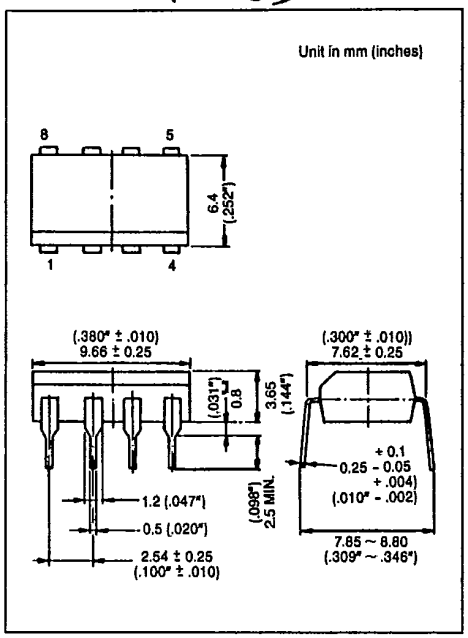


APPLICATIONS

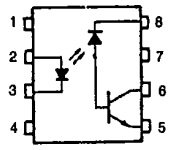
- DIGITAL LOGIC ISOLATION
- LINE RECEIVER FEEDBACK CONTROL
- POWER SUPPLY CONTROL
- SWITCHING POWER SUPPLY
- TRANSISTOR INVERTOR

Both the MT6500 and the MT6510 contain a high output emitting diode and a one chip photo diode transistor in an 8 lead dip package. The MT6500 has no internal base connection and is best suited for applications in noisy environmental conditions. The MT6510 contains an internal base connection and is used for analog applications or enable operation.

FEATURES

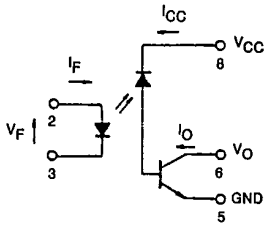
- Isolation Voltage : 5000V_{rms} Min.
- Switching Speed : t_{PHL}, t_{PLH}=0.5 μs (Typ.) (R_L=1.9kΩ)
- TTL Compatible

MT6500
PIN CONFIGURATIONS (TOP VIEW)

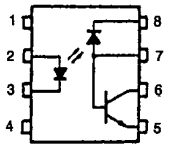


1. NC
2. ANODE
3. CATHODE
4. NC
5. EMITTER
6. COLLECTOR
7. NC
8. V_{CC}

SCHEMATIC

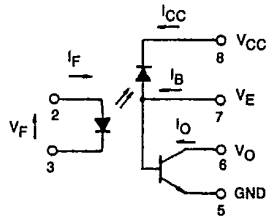


MT6510
PIN CONFIGURATIONS (TOP VIEW)



1. NC
2. ANODE
3. CATHODE
4. NC
5. EMITTER
6. COLLECTOR
7. BASE
8. V_{CC}

SCHEMATIC



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MAXIMUM RATINGS (Ta = 25°C)

	CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Forward Current	(Note 1)	I_F	25	mA
	Pulse Forward Current	(Note 2)	I_{FP}	50	mA
	Total Pulse Forward Current	(Note 3)	I_{FPT}	1	A
	Reverse Voltage		V_R	5	V
	Diode Power Dissipation	(Note 4)	P_D	45	mW
DETECTOR	Output Current		I_O	8	mA
	Peak Output Current		I_{OP}	16	mA
	MT6500		—	—	—
	MT6510 Emitter-Base Reverse Voltage		V_{EB}	5	V
	Supply Voltage		V_{CC}	-0.5 ~ 15	V
	Output Voltage		V_O	-0.5 ~ 15	V
	MT6500		—	—	—
	MT6510 Base Current		I_B	5	mA
	Output Power Dissipation	(Note 5)	P_o	100	mW
Operating Temperature Range			T_{opr}	-55 ~ 100	°C
Storage Temperature Range			T_{stg}	-55 ~ 125	°C
Isolation Voltage		(Note 6)	BV_S	5000	V_{rms}

Note 1: Derate 0.8mA above 70°C.

Note 2: 50% duty cycle, 1ms pulse width.
Derate 1.6mA/°C above 70°C.

Note 3: Pulse width 1μs, 300pps.

Note 4: Derate 0.9mW/°C above 70°C.

Note 5: Derate 2mW/°C above 70°C.

Note 6: R.H. = 40 ~ 60%, AC/1 min.

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ELECTRICAL CHARACTERISTICS (Ta=25°C)

	CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
LED	Forward Voltage	V_F	I_F=16mA	1.45	1.65	1.85	V
	Forward Voltage Temperature Coefficient	$\Delta V_F/\Delta Ta$	I_F=16mA	—	-2	—	mV/°C
	Reverse Current	I_R	V_R=5V	—	—	10	μA
	Capacitance Between Terminal	C_T	V_F=0, f=1MHz	—	60	—	pF
DETECTOR	High Level Output Current	I_{OH}(1)	I_F=0mA, V_{CC}=V_O=5.5V	—	3	500	nA
		I_{OH}(2)	I_F=0mA, V_{CC}=V_O=15V	—	—	5	μA
		I_{OH}	I_F=0mA, V_{CC}=V_O=15V,Ta=70°C	—	—	250	μA
	High Level Supply Voltage	I_{CCH}	I_F=0mA, V_{CC}=15V	—	0.01	1	μA
COUPLED	Current Transfer Ratio	I_O/I_F	I_F=16mA, V_{CC}=4.5V, V_O=0.4V, Ta=25°C	10	30	—	%
			rank: 0	19	30	—	
			Ta=0 ~ 70°C	5	—	—	
			rank: 0	15	—	—	
	Low Level Output Voltage	V_{OL}	I_F=16mA, V_{CC}=4.5V, I_O=1.1mA (rank 0:I_O=2.4mA)	—	—	0.4	V
	Isolation Resistance	R_S	R.H.=40~60%,V=1kV DC(Note 9)	—	10^{12}	—	Ω
	Capacitance Between Input to Output	C_S	V=0, f=1MHz	—	0.8	—	pF

SWITCHING CHARACTERISTICS (Ta=25°C, V_{CC}=5V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time (H→L)		t_{pHL}	I_F=0→16mA, V_{CC}=5V, R_L=4.1kΩ	—	0.3	0.8	μs
			(Note 7) rank 0:R_L=1.9kΩ	—	0.5	0.8	
Propagation Delay Time (L→H)		t_{pLH}	I_F=16→0mA, V_{CC}=5V, R_L=4.1kΩ	—	1.0	2.0	μs
			(Note 7) rank 0:R_L=1.9kΩ	—	0.6	1.2	
Common Mode Transient Immunity at Logic High Output	MT6500	CM_H	I_F=0mA, V_{CM}=200V_{p-p}	—	1500	—	V/μs
	MT6510		R_L=4.1kΩ, (Rank O:R_L=1.9kΩ) (Note 8)	—	400	—	
Common Mode Transient Immunity at Logic Low Output	MT6500	CM_L	I_F=16mA, V_{CM}=200V_{p-p}	—	-1500	—	V/μs
	MT6510		R_L=4.1kΩ, (Rank O:R_L=1.9kΩ) (Note 8)	—	-1000	—	

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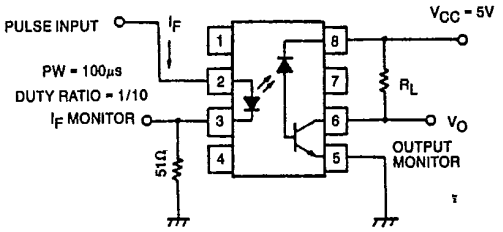
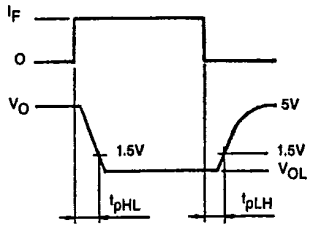
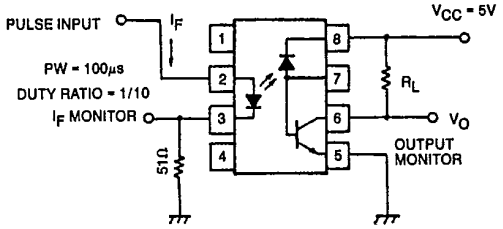
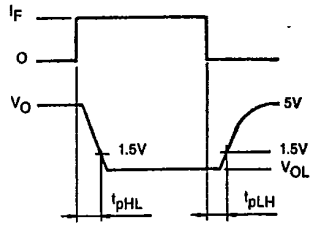
MT6500
Note 7. Switching Time Test Circuit





MT6510
Note 7. Switching Time Test Circuit





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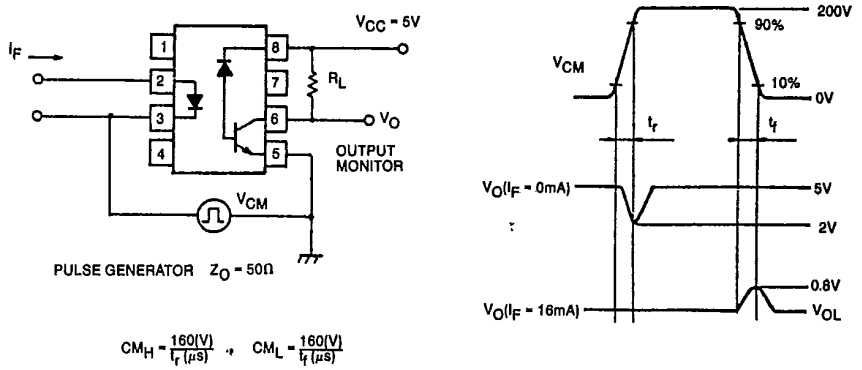
MT6500

Note 8. Common Mode Noise Immunity Test Circuit

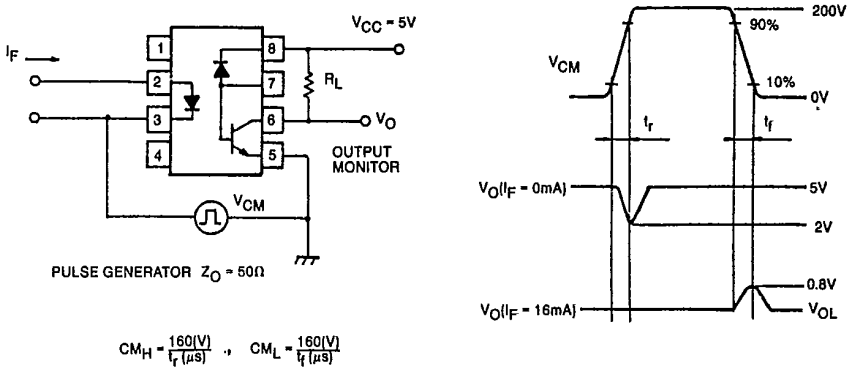


$$CM_H = \frac{160(V)}{t_r(\mu s)} \quad , \quad CM_L = \frac{160(V)}{t_f(\mu s)}$$

Note 9. Device considered a two-terminal device: Pins 1,2,3 and 4 shorted together and Pin 5,6,7 and 8 shorted together.

MT6510

Note 8. Common Mode Noise Immunity Test Circuit



$$CM_H = \frac{160(V)}{t_r(\mu s)} \quad , \quad CM_L = \frac{160(V)}{t_f(\mu s)}$$

Note 9. Device considered a two-terminal device: Pins 1,2,3 and 4 shorted together and Pin 5,6,7 and 8 shorted together.

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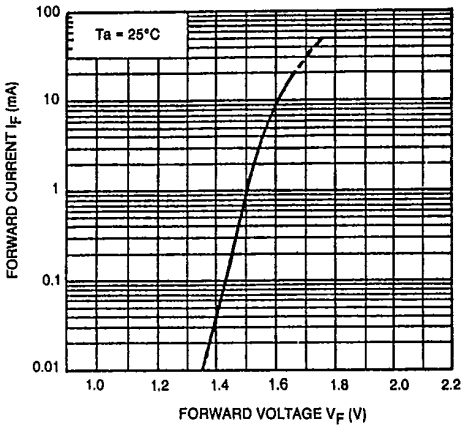
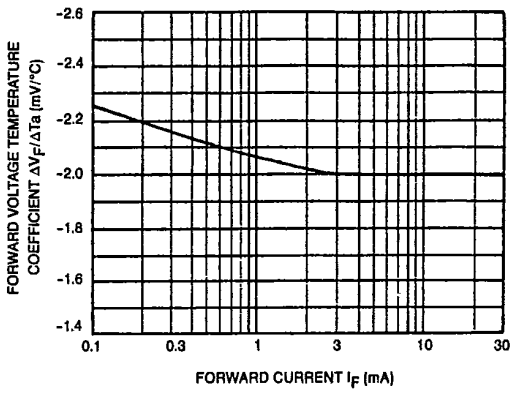
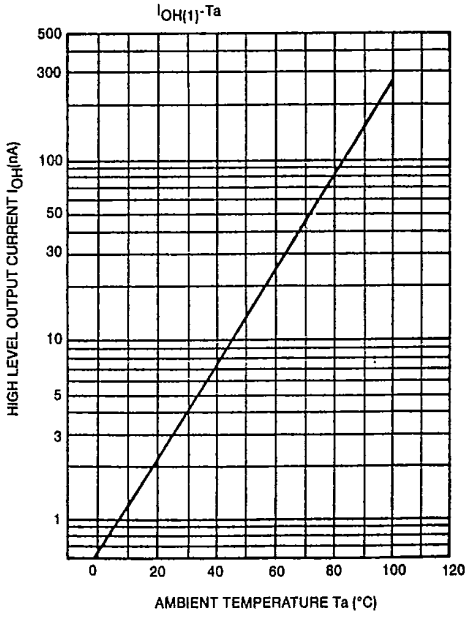
I_F - V_F



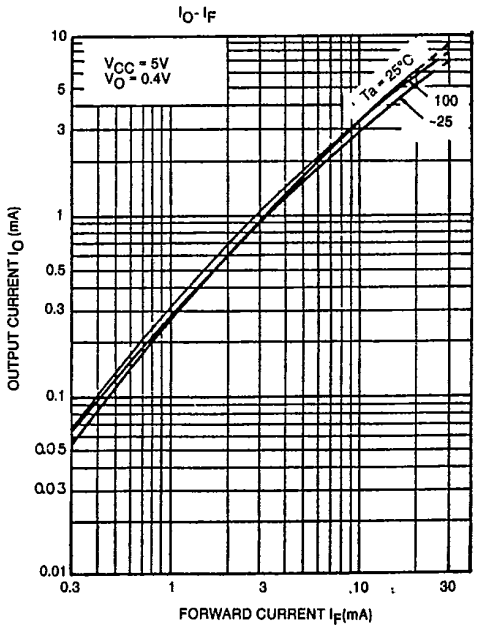
$\Delta V_F / \Delta Ta$ - I_F



$I_{OH(1)}$-Ta



I_O- I_F



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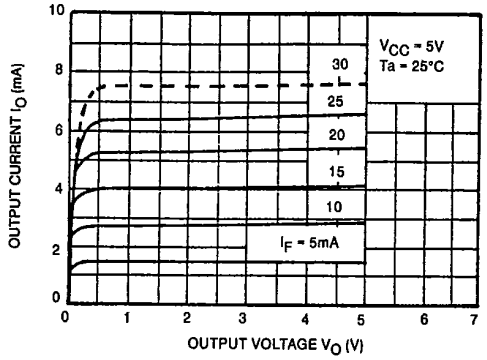
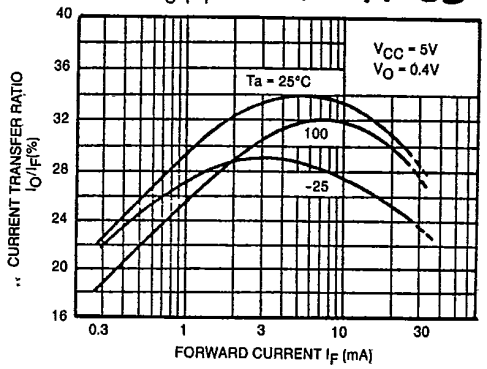
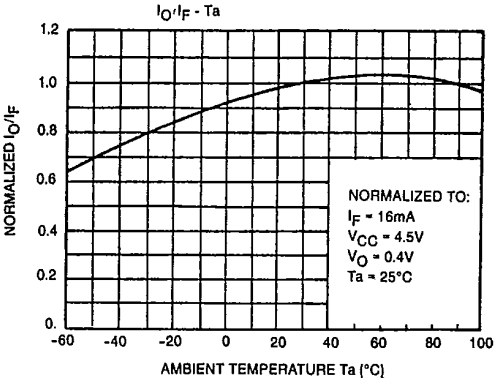
I_O-V_O



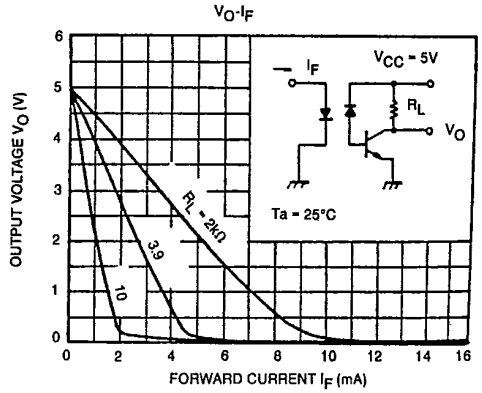
I_O/I_F-I_F



I_O/I_F - Ta



V_O-I_F



t_{pHL},t_{pLH}-R_L