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MT6612 Application Notes

Handset Application

Version 0.5

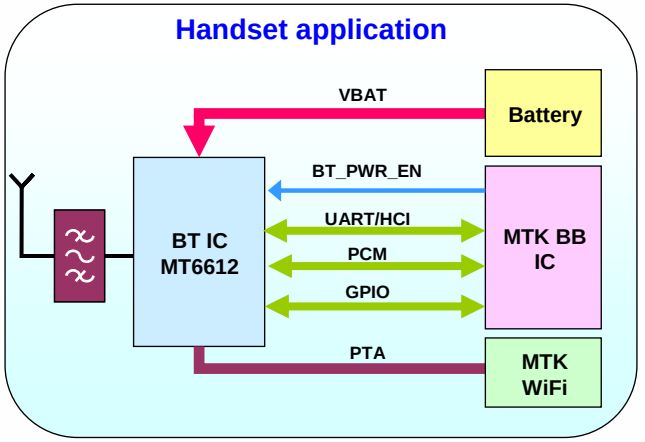
Version

Revision	Date	Comments
V0.5	2009/08/27	Initial release

MT6612 Key Features

- **Package Support**
  - 5mm x 5mm 40-lead (0.5mm pitch) QFN
  - 3.01mm x 3.06mm 45-ball (0.4mm pitch) WLCSP.
- **General**
  - Support BT3.0 and BT 2.1+ EDR spec.
  - Class-1 (9dBm) TX power with integrated PA.
  - Support USB 2.0 full speed interface for laptop and computer peripherals.
- **Platform**
  - Integrated LDO allows directly connect to V_{BAT}.
  - Standard 2-Wire and 1-Wire PTA interface for MTK WiFi chips co-existence.
- **Applications**
  - Mobile Handset and Smartphone
  - Portable Navigation Devices (PND)
  - Laptop and Notebook
  - Computer Peripherals

Application Block Diagram



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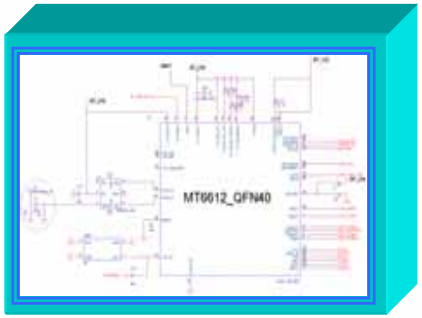
MT6612 Reference Design

MTK Bluetooth Total Solution

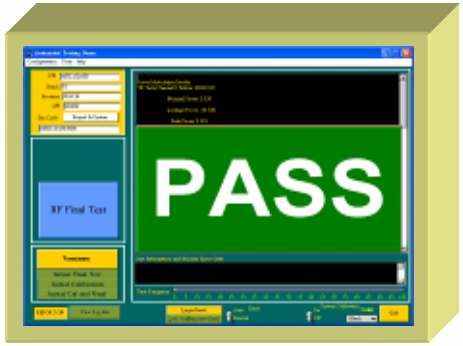
MTK BT Reference Design



Bluetooth MP

Built-in MTK BT SW

Factory Test Tool



Bluetooth BQE

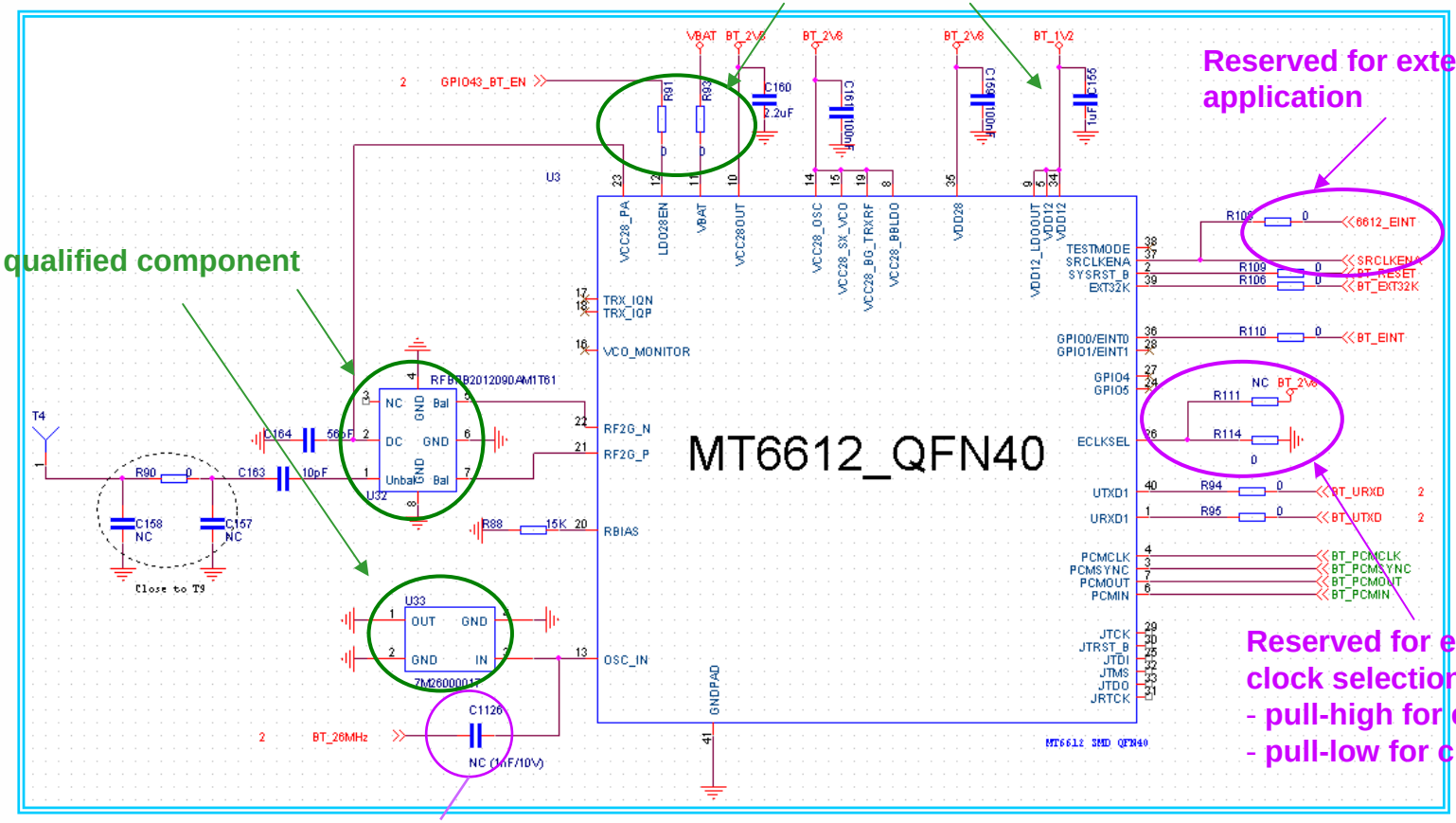
MT6612 Reference Schematic

Compact BOM & Layout Area

- ***Need no external LDO***, **can directly applied from VBAT!**

Integrated Regulator

MTK qualified component

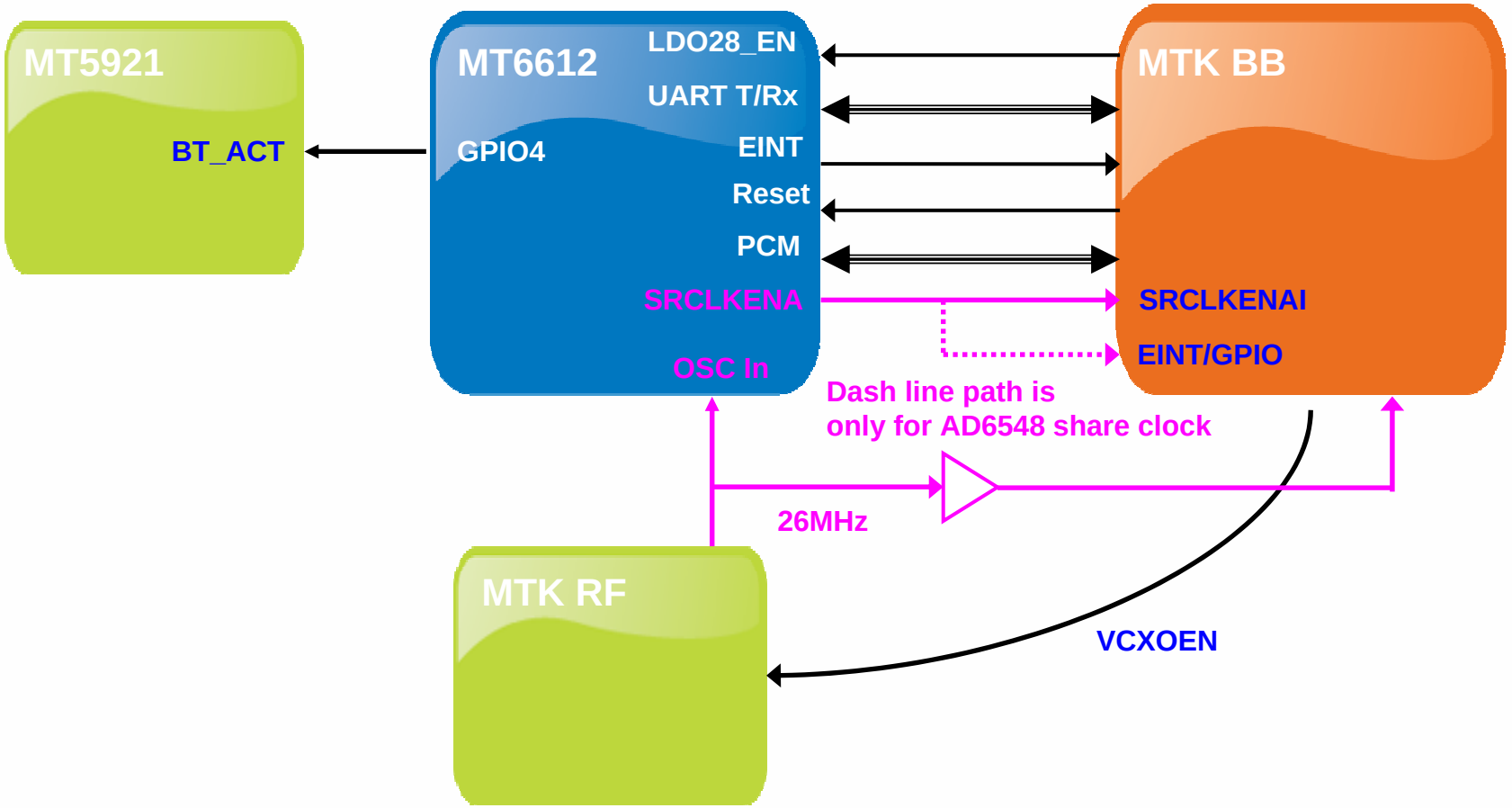


Reserved for external clock application

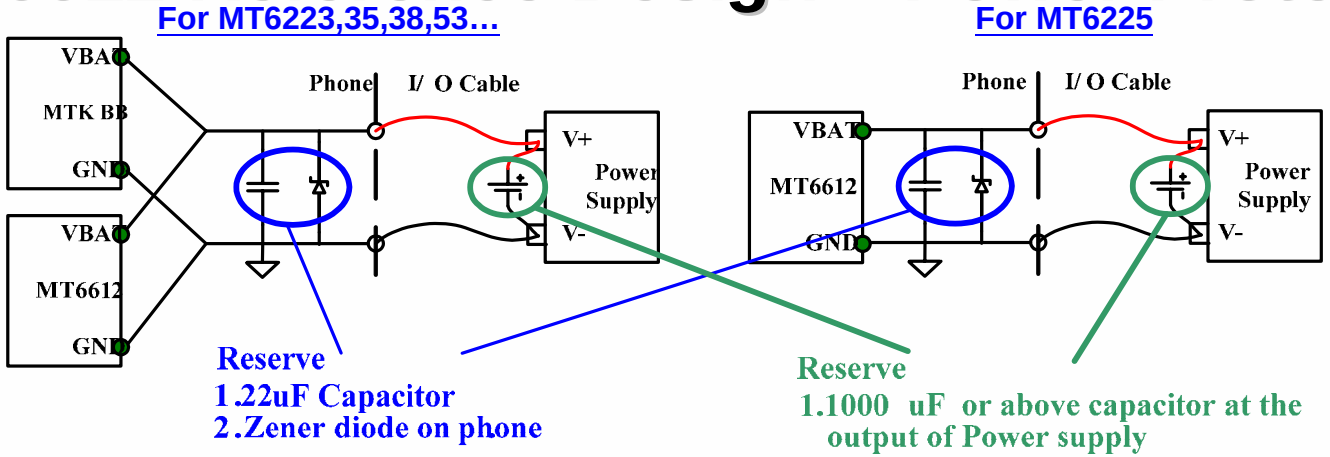
Reserved for external clock selection.
- pull-high for external clock
- pull-low for crystal

Reserved for external clock input

MT6612 Interface



MT6612 Reference Design – Power Protection



Because VBAT is directly applied, battery voltage protection should be applied:

Design notice in Phone side:

1. Add 22uF capacitor.
2. Add Zener diode (5.6V) to protect the IC against low frequency voltage surge. Put it between battery connector and MT6612.

Notice: If using IO connector or test point to supply VBAT for download, manufacture, or repair, should let VBAT trace passing zener diode and 22uF capacitor before entering IC.

Notice: Using 5.6V zener will introduce some leakage when VBAT = 4.2V.
ex. 5.6V zener CZRU52C5V6, will have extra 5uA leakage.

•Design notice in Power Supply side:

Add 1000uF (or above) capacitor at the output of the power supply to reduce the voltage bounce caused by long power cable. And the power cable should be as short as possible. Also add 1000uF (or above) capacitor at the end of power cable (near phone side).

Baseband GPIO Assignment for MT6612 (1/2)

- **BT/Baseband Interface assignment**
  - In the BT/BB interface assign phase, the GPIO should be arranged carefully. Do not use GPIO with conflict power domain (for example, camera power domain).

AD17	URXD2	VDD33_NORM2	VSS33_NORM2	VDDK	VSSK	
U16	SYSRST_B	VDD33_NORM2	VSS33_NORM2	VDDK	VSSK	
AD18	URTS1	VDD33_NORM2	VSS33_NORM2	VDDK	VSSK	
T16	EINT0	VDD33_NORM2	VSS33_NORM2	VDDK	VSSK	
AD19	UCTS1	VDD33_NORM2	VSS33_NORM2	VDDK	VSSK	

Baseband GPIO Assignment for MT6612 (2/2)

– Reserve the default (hardware) pull-down GPIO to LDO28EN pin to avoid

GPIO +0400h	GPIO pull-up/pull-down select register 1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0: Default (after reset state) is pulled-down

GPIO +0440h	GPIO pull-up/pull-down select register 2															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24	GPIO23	GPIO22	GPIO21	PGIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	1

Do not use → 1: Default (after reset state) is pulled-high

Reference assignment

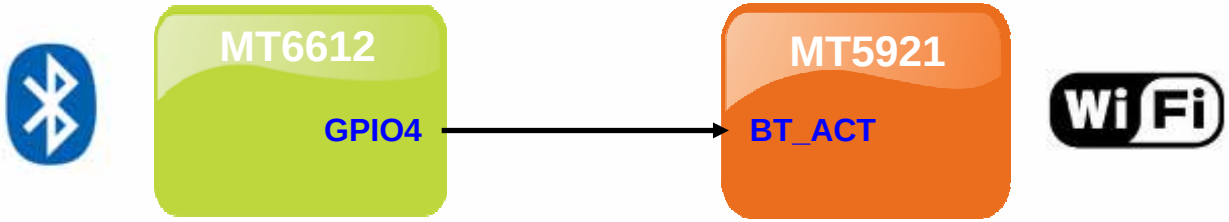
MT6611	MT6238	MT6235	MT6223	MT6229	Notes
LDO28EN	GPIO29	GPIO39	GPIO30	GPIO9	Do not use pulled-up GPIO!
EXT32K	GPIO77	GPIO27	GPIO21	GPIO36	

MT6612 PTA Interface

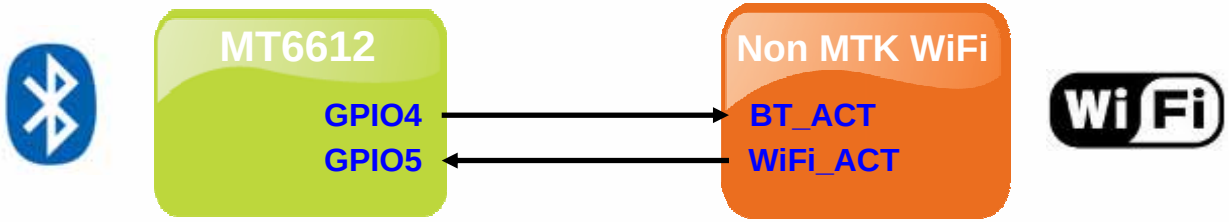
- MT6612 can support 1-wire PTA interconnection for MTK WiFi co-existence.

MT6612's GPIO for PTA	GPIO4	GPIO5
MTK 1-Wire	V	
Standard 2-Wire	V	V

- For MTK WiFi chip:

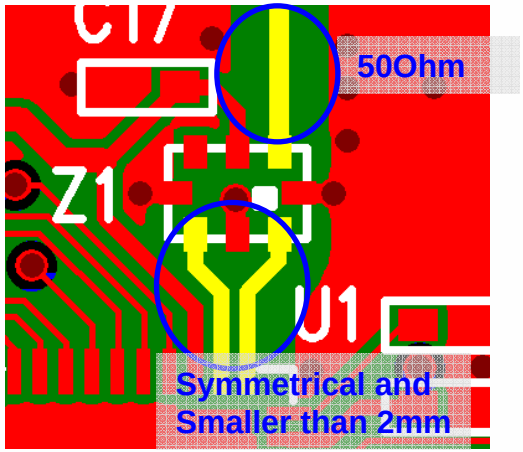


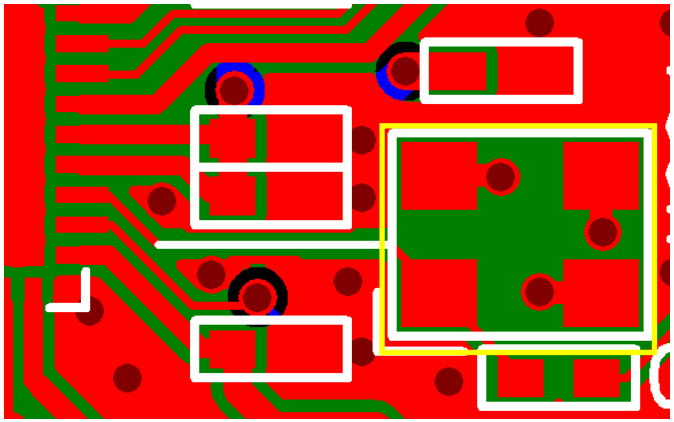
- For non-MTK WiFi:



Reference Layout (1/3)

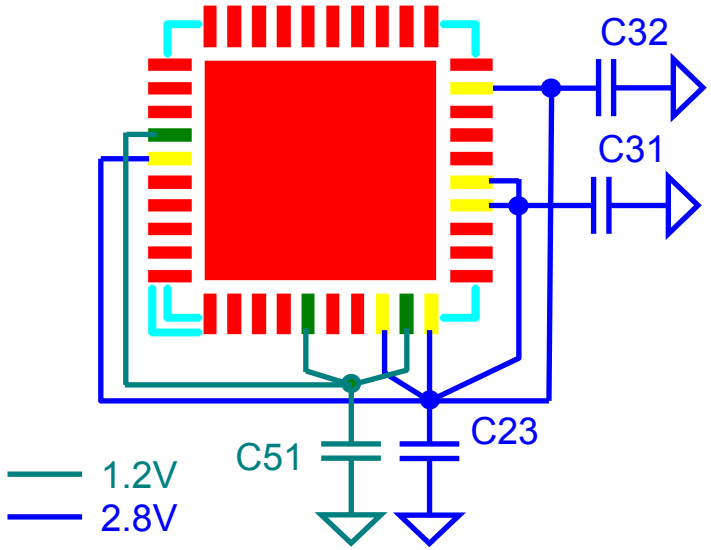
- **RF/Analog part:**
  - Using qualified balance filter, need no external matching network.
  - Balance port routing should be symmetrical and shorter than 2mm, while the single-end trace route should keep 50Ω.
  - Keep out the ground area of crystal.



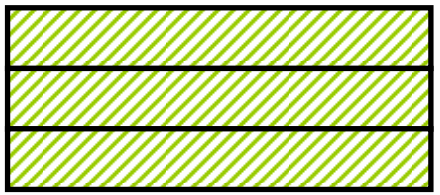


Reference Layout (2/3)

- **Power rail part:**
  - Low cost through-hole process can be adopted.
  - Make star-connection at C23 for 2.8V power trace. Also, star-connected at C51 for 1.2V trace route.
  - Provide complete ground for power traces, do not route power traces in parallel with or crossing to digital or strong disturbance signals.



Component side	Top layer
Signal Layer	2nd layer
Ground plane	3rd layer
Power traces	Bottom layer

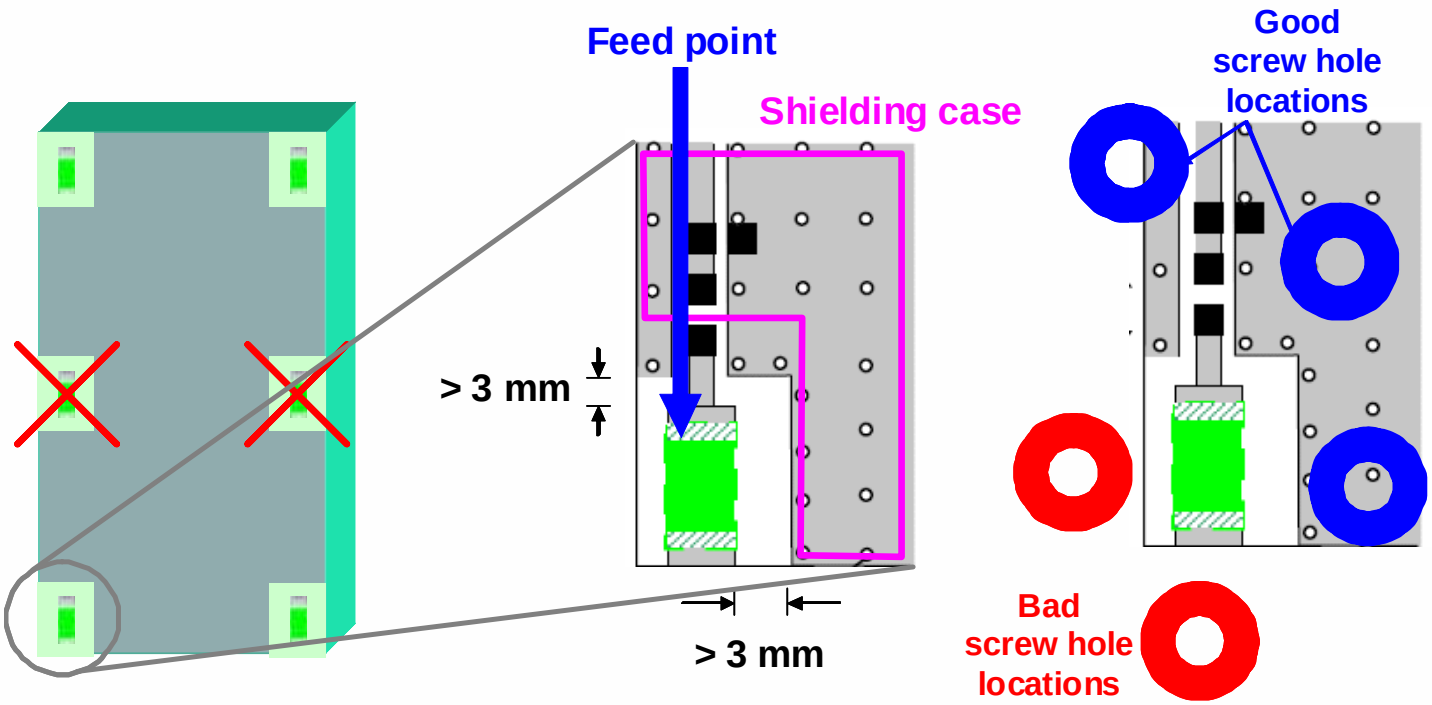


Reference Layout (3/3)

- **Digital part:**
  - The 32k trace **MUST be** shielded by ground along the routing. **DO NOT** place any other trace along with it.
  - 26MHz trace should be shielded by ground from BT to GSM BB and RF when co-clock mechanism is employed. (detailed please refer to MT6612 co-clock application note)
  - **DO NOT** let strong disturbance signal trace across or parallel to BT digital line, especially for **BT_URXD3, BT_UTXD3, PCMCLK, PCMSYNC, PCMIN, PCMOUT.**

BT Antenna Design and Placement

- Place the BT antenna at the corner of the PCB.
- The feed point is directly connected to the antenna.
- Reserve enough distance between the antenna, ground and the shielding case.
- Ground blue screw holes, and don't ground red screw holes.



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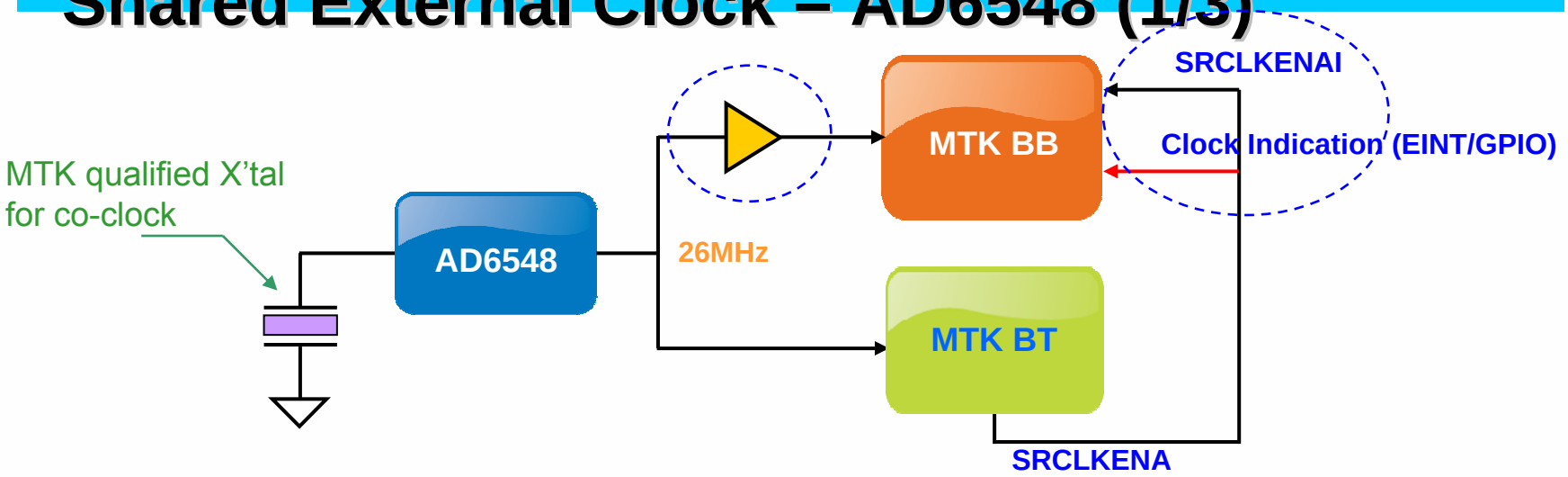
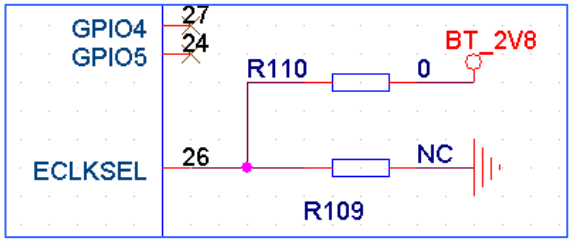
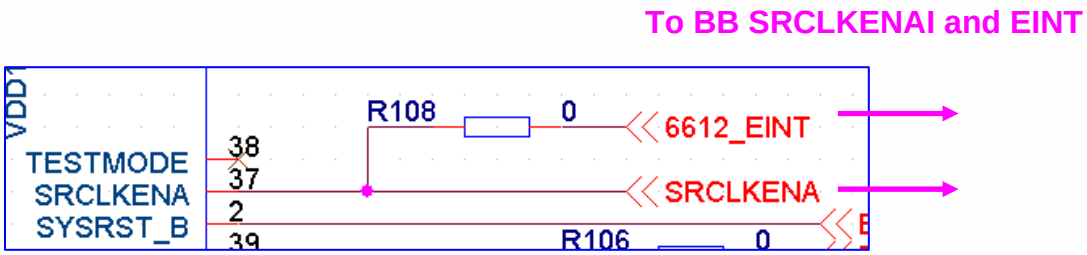
External Clock Sharing

Shared External Clock – AD6548 (1/3)



1. Reserve pull-up and pull-down resistor on ECLKSEL pin to select external or X'tal clock.





2. Connect SRCLKENA to BB's SRCLKENAI and EINT/GPIO (please follow the table for reference assignment)

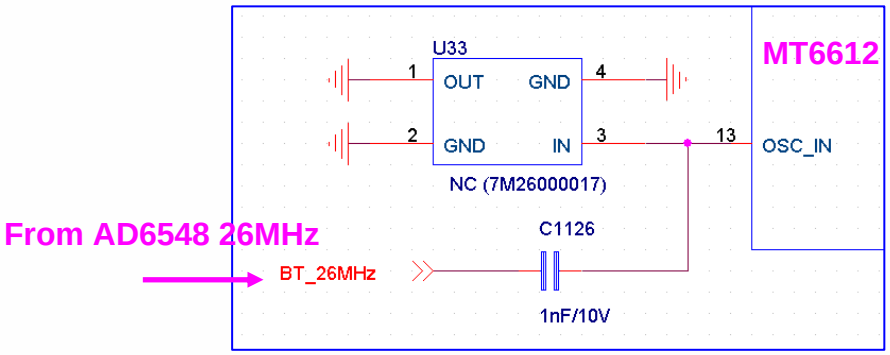
Shared External Clock – AD6548 (2/3)

Assignment for Clock Indication (EINT/GPIO):

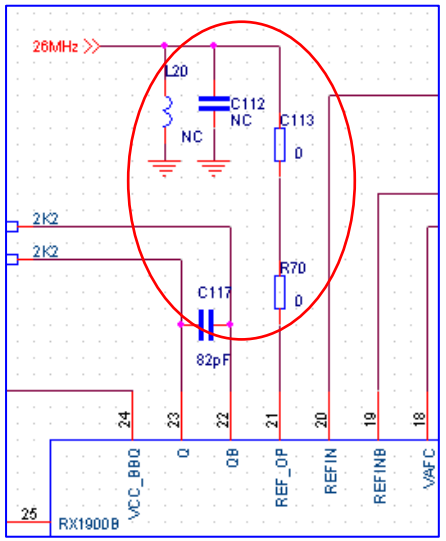
	EINT #	BB Pin	Pin Name	IO Power	GPIO MODE 0	GPIO MODE 1	GPIO MODE 2	GPIO MODE 3	Edge/Level Trigger	HW Debounce
MT6225	EINT4	T3	GPIO0	VDD33	GPIO0	----	----	EINT4	Edge/Level	Yes
	EINT5	U4	GPIO1	VDD33	GPIO1	----	----	EINT5	Edge/Level	Yes
	EINT6	T4	GPIO2	VDD33	GPIO2	----	UCTS1	EINT6	Edge/Level	Yes
	EINT7	U5	GPIO3	VDD33	GPIO3	BSI_RFIN	URTS1	EINT7	Edge/Level	Yes
MT6223	EINT2	C11	EINT2	VDD33	EINT2	GPIO42	----	----	Edge/Level	Yes
	EINT3	D11	EINT3	VDD33	EINT3	GPIO43	MIRQ	----	Edge/Level	Yes
	EINT4	R8	JTRST_B	VDD33	JTRST_B	GPIO26	EINT4	----	Edge/Level	Yes
	EINT5	P8	JTDI	VDD33	JTDI	GPIO27	EINT5	----	Edge/Level	Yes
	EINT6	T9	JTMS	VDD33	JTMS	GPIO28	EINT6	----	Edge/Level	Yes
	EINT7	U14	LCD_CS1_B	VDD33_LCD	LCD_CS1_B	GPIO14	LCD_SCE1_B	EINT7	Edge/Level	Yes
	MIRQ	D11	EINT3	VDD33	EINT3	GPIO43	MIRQ	----		
MT6235	EINT3	E24	EINT3	VDD33	GPIO44	EINT3	DRF_DATA	IRQ2	Edge/Level	Yes
	EINT4	E23	EINT4	VDD33	GPIO45	EINT4	DRF_EN	CLKM3	Edge/Level	Yes
	EINT5	D23	EINT5	VDD33	GPIO46	EINT5	EDICK	----	Edge/Level	Yes
	EINT6	D25	EINT6	VDD33	GPIO47	EINT6	EDIWS	----	Edge/Level	Yes
	EINT7	D24	EINT7	VDD33	GPIO48	EINT7	EDIDAT	----	Edge/Level	Yes
MT6238	EINT0	T16	EINT0	VDD33_NORM2	GPIO77	EINT0	CLKM4	----	Edge/Level	Yes
	EINT1	AB17	EINT1	VDD33_NORM2	GPIO78	EINT1	CLKM5	----	Edge/Level	Yes
	EINT2	AC19	EINT2	VDD33_NORM2	GPIO79	EINT2	DSP_GPO3	TBTXEN	Edge/Level	Yes
	EINT3	AC25	EINT3	VDD33_NORM2	GPIO33	EINT3	DSP_GPO2	TBTXFS	Edge/Level	Yes
	EINT4	AD24	EINT4	VDD33_NORM2	GPIO34	EINT4	DSP_GPO1	TBRXEN	Edge/Level	Yes
	EINT5	T17	EINT5	VDD33_NORM2	GPIO35	EINT5	DSP_GPO0	TBRXFS	Edge/Level	Yes
	EINT6	AE18	EINT6	VDD33_NORM2	GPIO36	EINT6	EDIWS	----	Edge/Level	Yes
	EINT7	AC20	EINT7	VDD33_NORM2	GPIO37	EINT7	EDIDAT	----	Edge/Level	Yes

Shared External Clock – AD6548 (3/3)

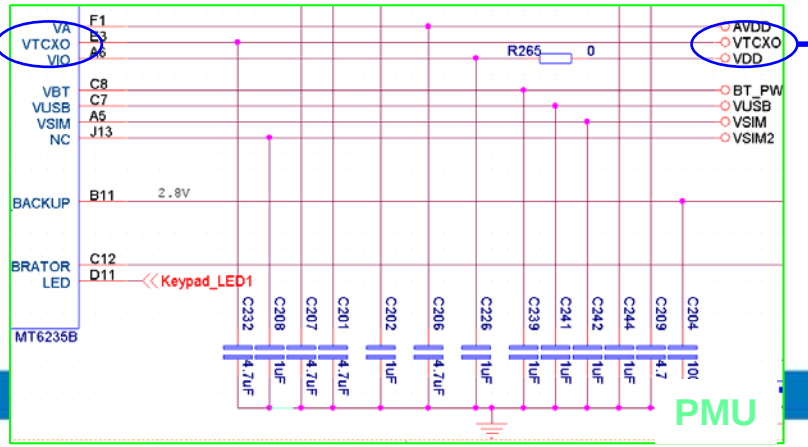
3. Please also reserve X'tal footprint for back-up.

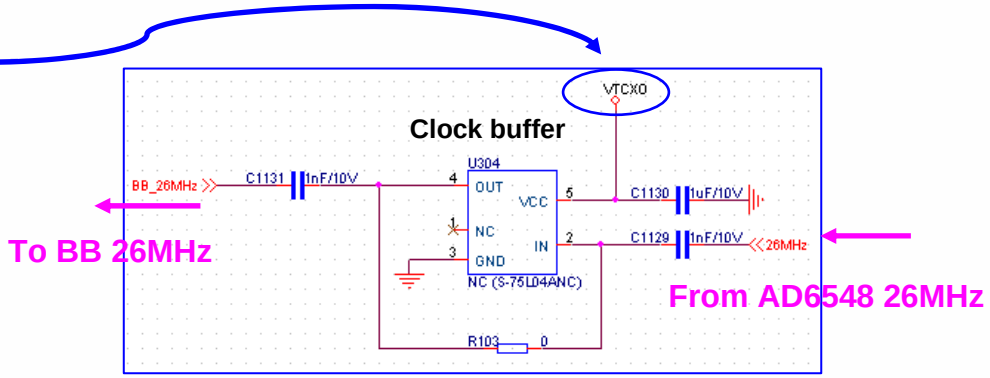


4. In AD6548 26MHz output, reserve LPF footprint and default use 0Ω connection.



5. Please also reserve clock buffer on 26MHz to BB path, connect buffer power to VTCXO.

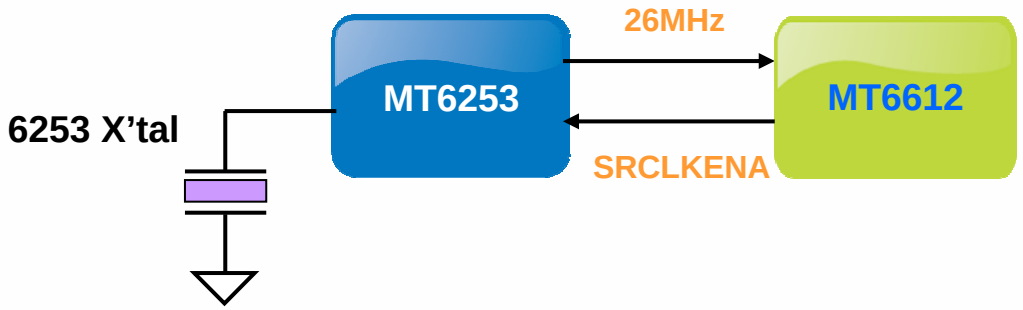




Special Notes for AD6548 Co-clock Layout

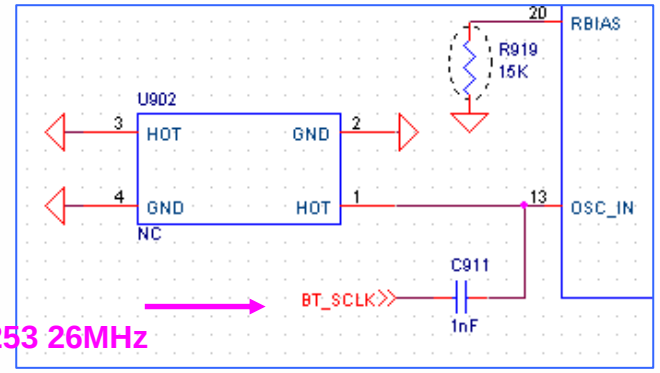
- Follow original design rule for OG and BT if not mentioned.
- **BT close to RF transceiver ! (Highly recommended)**
- 26MHz trace routing rule
  - As short as possible
  - Good shielding with ground to avoid noise & coupling
- Transceiver trace routing rule
  - Have VCXO power good decouple and clean ground.
- Using MTK recommended OG Xtal and clock buffer
- Reserve BT Xtal footprint

Shared External Clock – MT6253 (1/2)



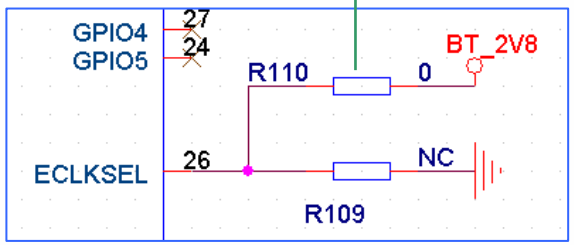
1. Reserve Xtal footprint for backup.
2. Reserve pull-up and pull-down resistor on ECLKSEL pin to select external or X'tal clock.

MT6612



From MT6253 26MHz

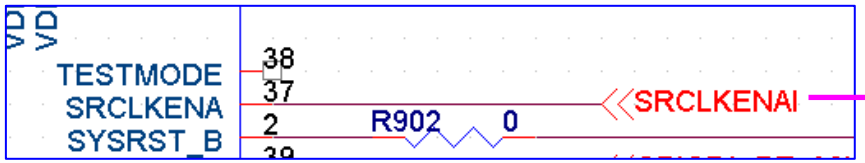
Pull-high for external clock
Pull-low for XTal selection



Shared External Clock – MT6253 (2/2)

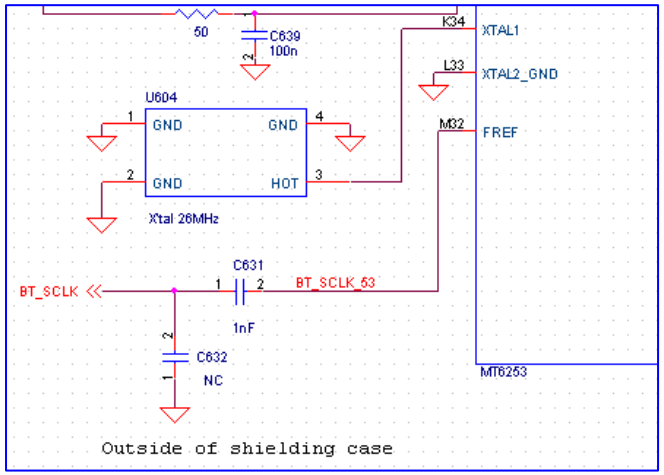
3. Connect SRCLKENA (clock request) to MT6253's SRCLKENAI
4. Connect 26MHz output from MT6253 to 6612 via 1nF AC couple capacitor.

MT6612 SRCLKENA



To MT6253 SRCLKENAI

MT6253



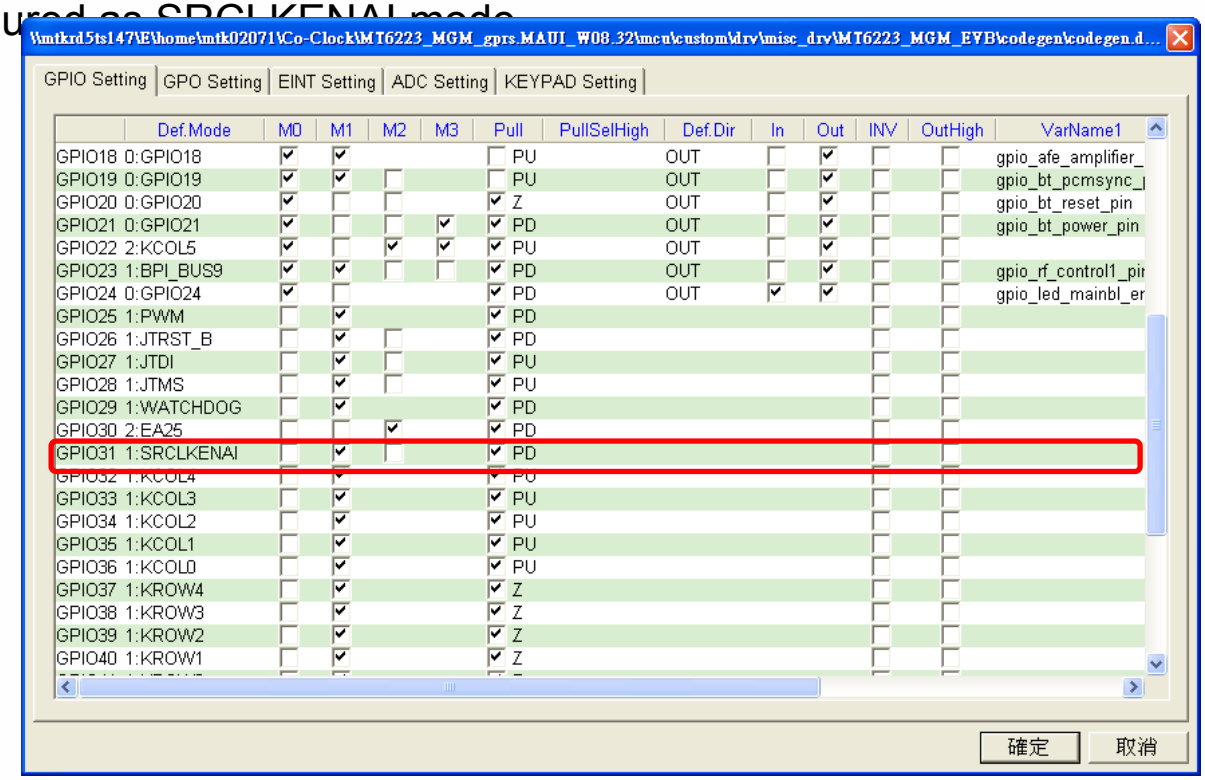
To MT6612 26MHz

Special Notes for MT6253 Co-clock Layout

- Follow original design rule for MT6253 and BT if not mentioned.
- **BT close to RF transceiver ! (Highly recommended)**
- 26MHz trace routing rule
  - As short as possible
  - Good shielding with ground to avoid noise & coupling
- Using MTK recommended MT6253 Xtal.
- Reserve BT Xtal footprint

Shared External Clock – SW Configuration

- Use Drv tool in Custom folder to configure GPIO, the clock request input should be configured as SRCLKENAI mode



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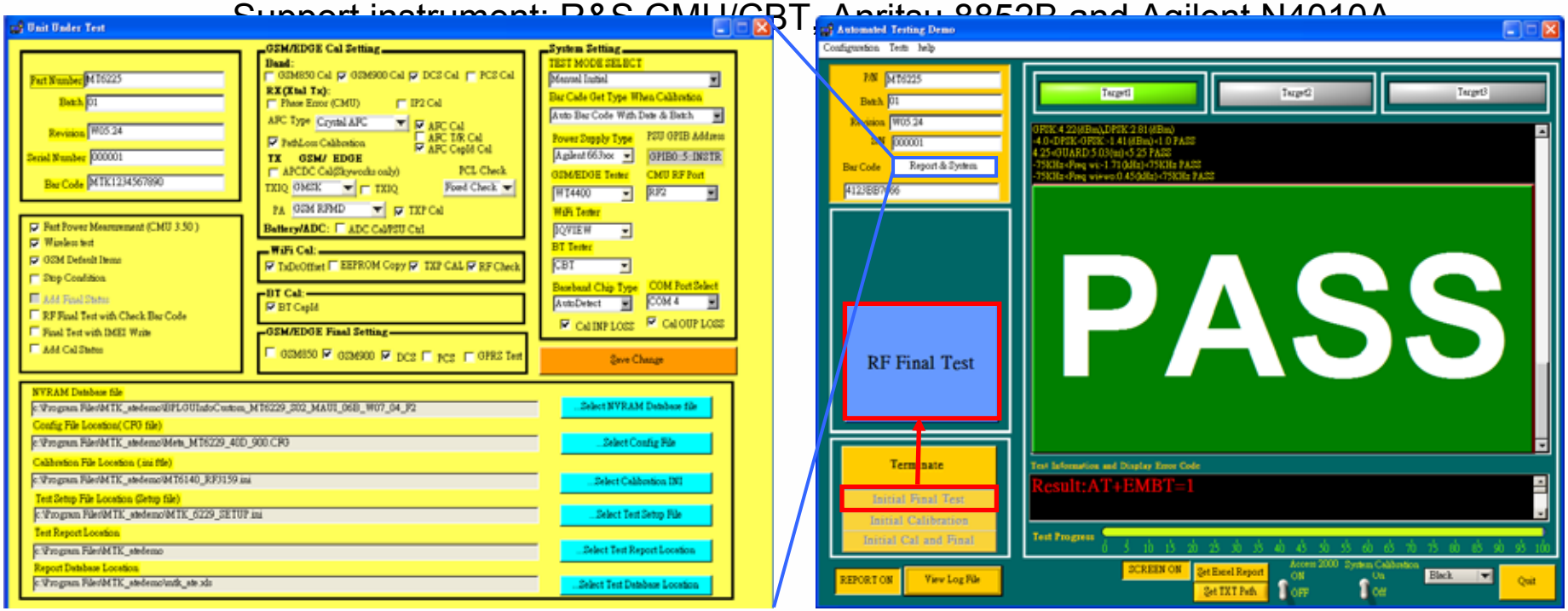
Bluetooth Tool

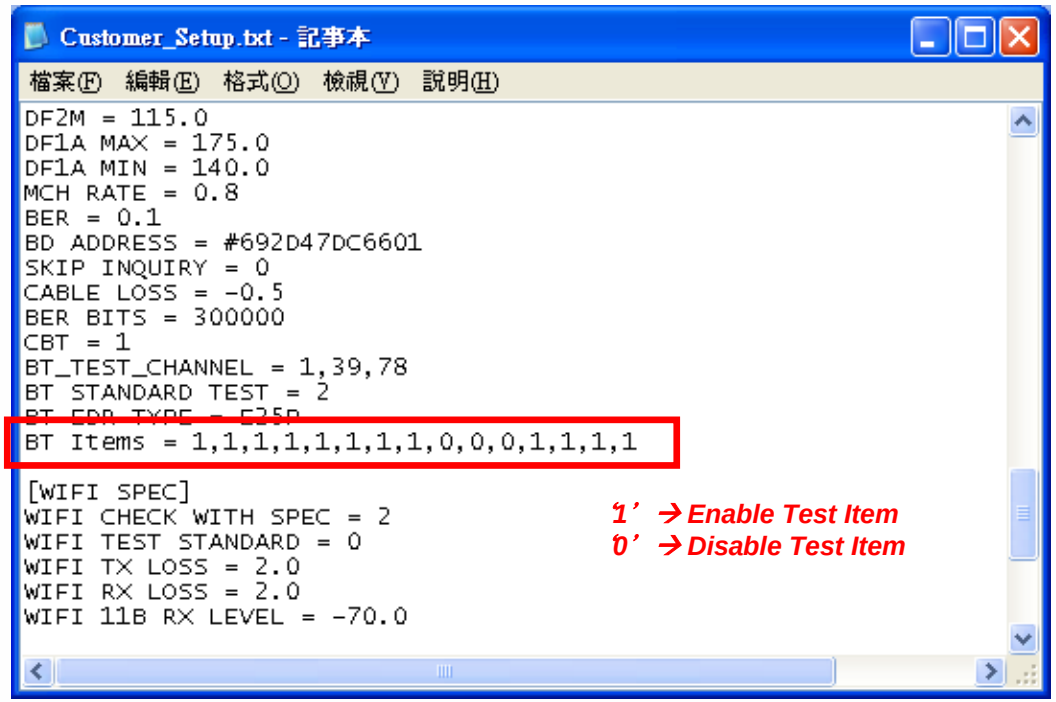
Bluetooth Tool – ATE (1/2)

- ATE tool
  - Used for factory BT RF performance test.
  - Support EDR RF test cases.
  - Support instrument: R&S CMU/CBT, Anritsu 8852B and Agilent N4010A



Bluetooth Tool – ATE (2/2)

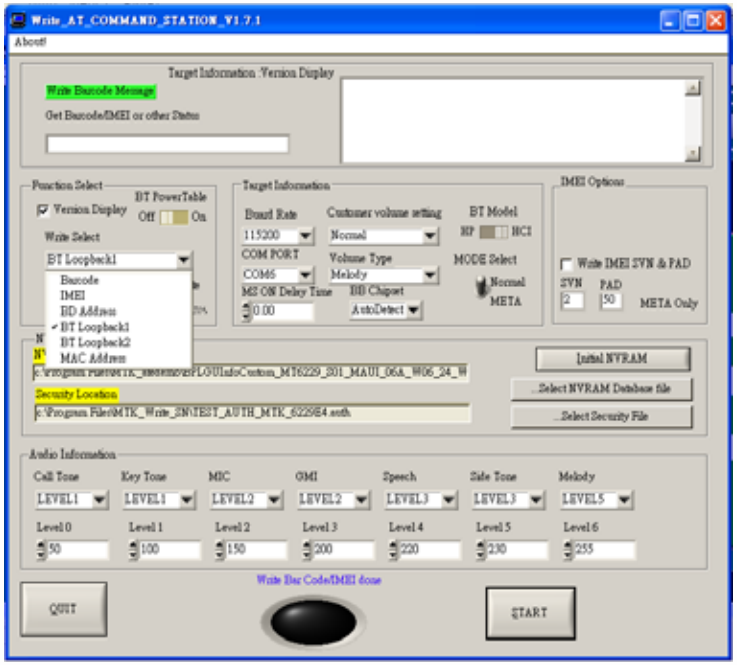
- Configure the test item in Customer_Setup.txt:

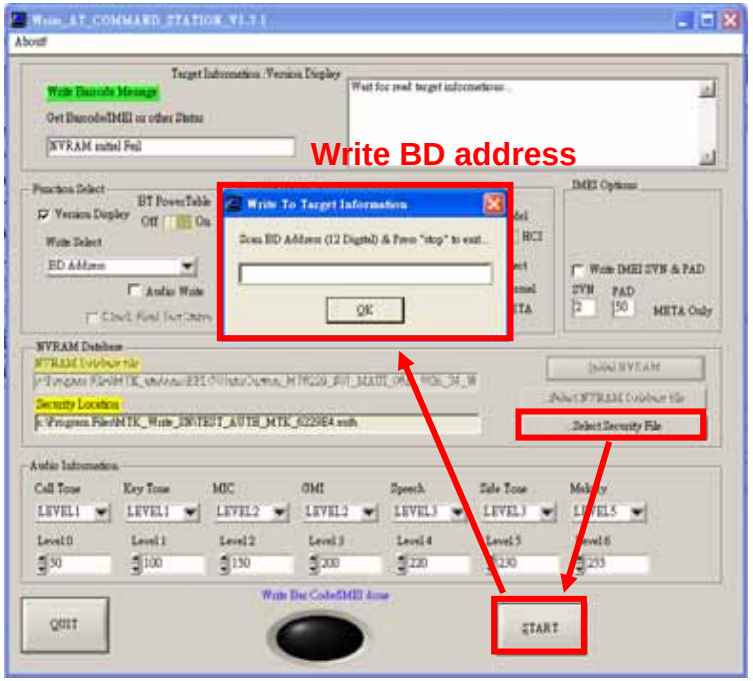


- **BT Items = 1,1,1,1,1,0,0,0,0,0,0,1,1,1,1 →**
  - **BT1.2 power, Initial Carrier Frequency, Carrier Frequency Drift, Modulation Character, Single Slot BER,Multi Slot BER, EDR Relative Power, EDR Modulation Accuracy, EDR Differential Phase Encoding, EDR Sensitivity, EDR BER floor, Reserve , Reserve , Reserve , Reserve**

Bluetooth Tool – SN Writer

- SN Station
  - Can write BD address (Meta mode)
  - PCM Loop back 1 (Normal mode)
  - PCM Loop back 2 (Normal mode)





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2nd Source QVL

MT6612 2nd Source List

- Balance filter

MT6612QFN Qualification List			
Vendor		PN	Dimensions (mm)
ACX	ACX	FB2012-06N2R4M	2.0 x 1.25 x 0.7
WALSIN	WALSIN	RFBPB2012090AM1T61	2.0 x 1.2 x 0.9
Cyntec	Cyntec	TBB-2012-245-C5	2.0 x 1.25 x 0.4
TDK	TDK	DEA202450BT-7190A1	2.0 x 1.25 x 0.6

- Xtal

MT6612QFN X'tal Qualification List					
Vendor		PN	F_0 (MHz)	C_{load} (pF)	Dimensions (mm)
日商電波 NDK	NDK Crystal Bridge to the Future	NX3225SA	26	9.43	3.2 x 2.5 x 0.55

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