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MT6616 Application Note

V0.2

Revise history

Revision	Date	Comments	Pages
V0.1	2010/01/XX	Initial release	
V0.2	2010/3/XX	Modify FM design guide for de-sense	

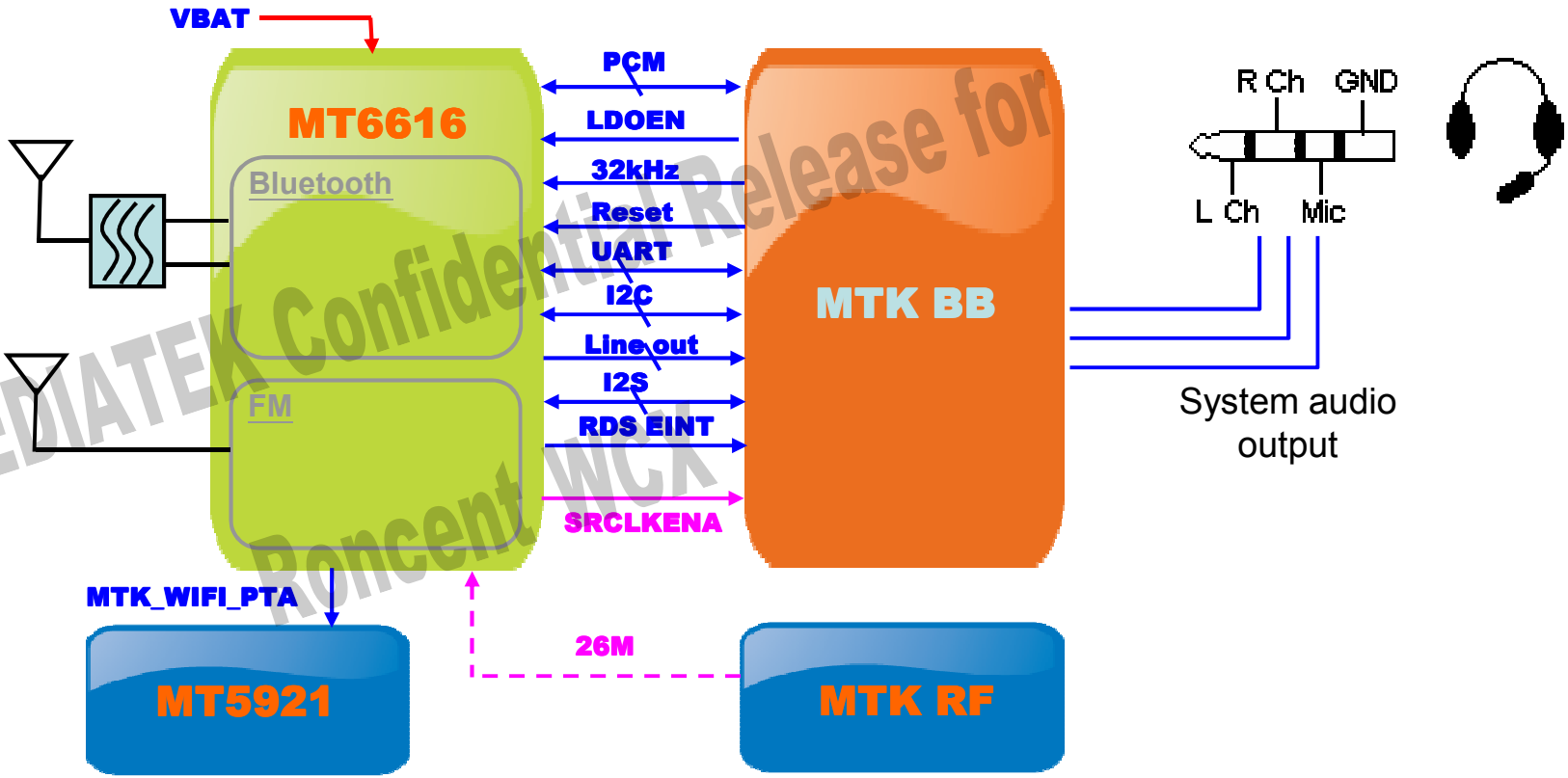
Outline

1. FM receiver
   - ✓ Reference Schematic and Layout
   - ✓ PCB Design Example for MT6616
   - ✓ Audio Interface Design
   - ✓ FM Earphone Antenna Illustrations
2. Bluetooth
   - ✓ Reference Schematic and Layout
   - ✓ MT6616 Power Protection
   - ✓ Interfacing
   - ✓ BT Antenna Placement Guideline
3. External 26MHz Sharing with RF
   - ✓ MT6253
   - ✓ AD6548
   - ✓ MT6160 (3G VCTCXO)

MT6616 System Interface

- Supports QFN & CSP Package
  - ✓ QFN package for low-cost layout design
  - ✓ CSP package for compact layout design (2010 Q1)
- Built-in LDO, LDO cost saved (US$ 0.05)
- Support external 32kHz and 26MHz clock , no Crystal needed.

W1012 MP!



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MT6616 Design Guide – FM Receiver

MT6616 reference circuit

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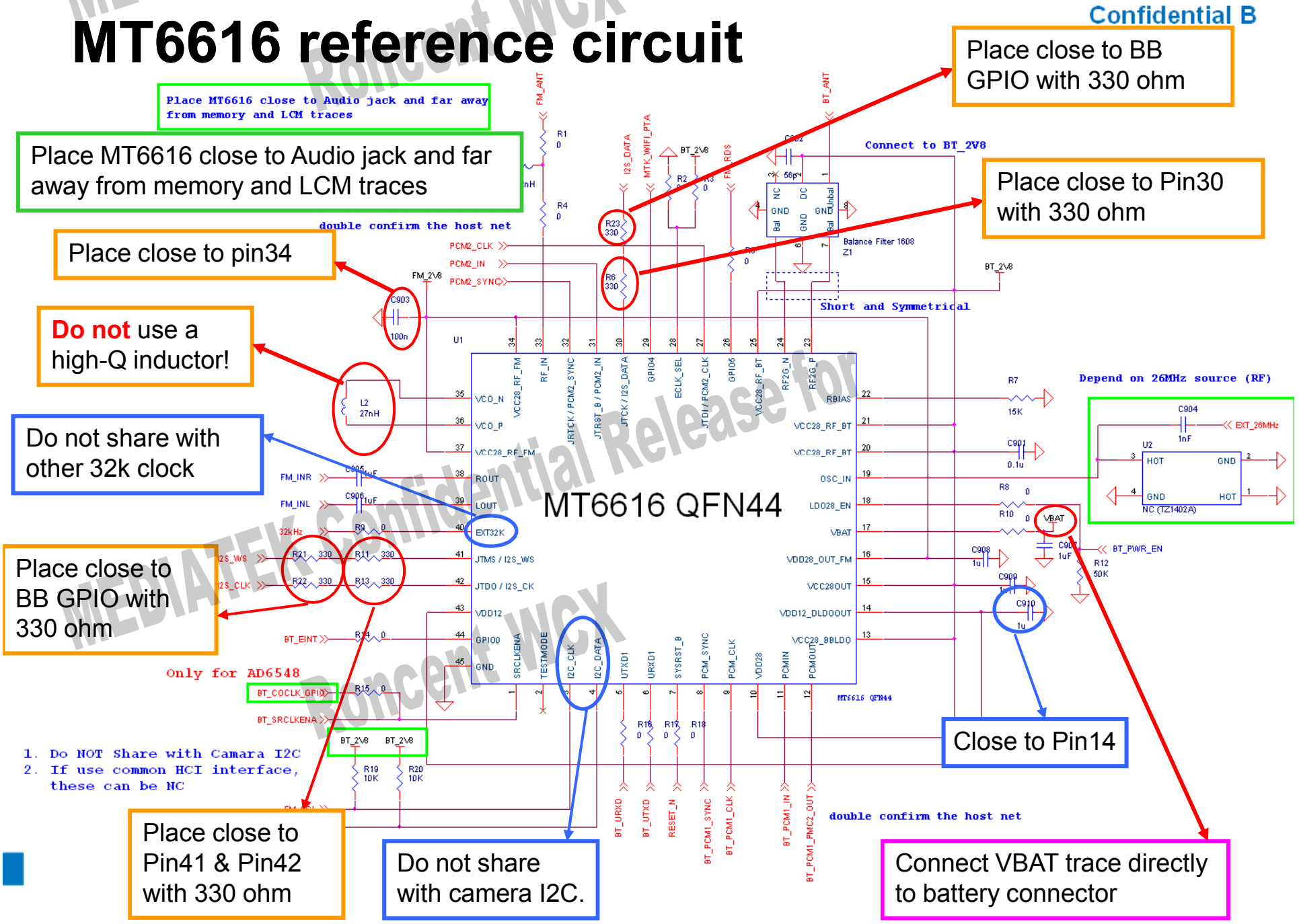

Reference Layout – MT6616 FM

Placement

- Place the FM near the earphone jack. Avoid high-speed digital devices, such as memory and LCM devices, near the RF signal area.
- Bypass cap for power should be placed beside the VCC and VCO pin (MT6616 pin 13,14,15,16,34,35,36,37).
- Place VCO inductor close to pin 35 and 36. Do not let any noisy trace near or cross VCO inductor path

Routing

- FM antenna trace should have a 50Ω impedance.
- Power should be routed to the bypass cap and the VCCVCO pin first, then to all other power pins on the FM chip. See the following pages for example.
- Keep layer2 GND plane under MT6616 chip as complete as possible. See the following pages for example.
- Add series 330 ohm for I2S_data , I2S_WS , I2S_CLK trace to prevent noise coupling
- Use inner layer for I2S_data , I2S_WS , I2S_CLK trace routing.
- Protect the following areas with GND vias and GND planes:
  - **RF signal from the earphone jack all the way to the FM chip;**
  - **32.768 kHz and 26 MHz signal;**
  - **VCO inductor** (MT6616 pins 13,14,15,16,34,35,36,37);

Power Feeding Network Layout Guidelines

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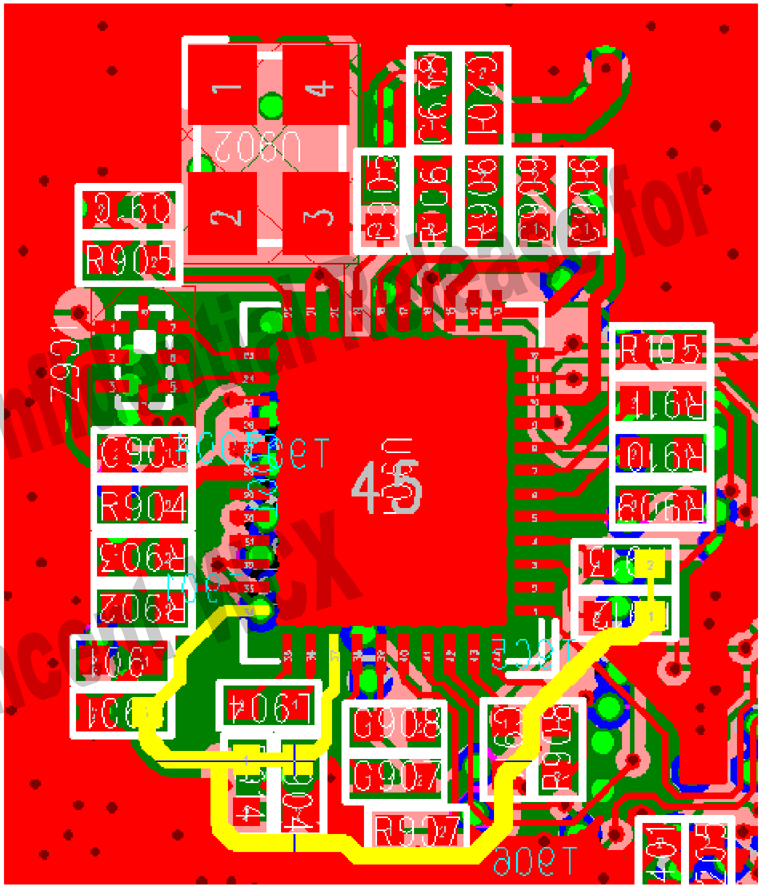
- The FM power should be monopolized: do not connect other blocks to VCC_FM.



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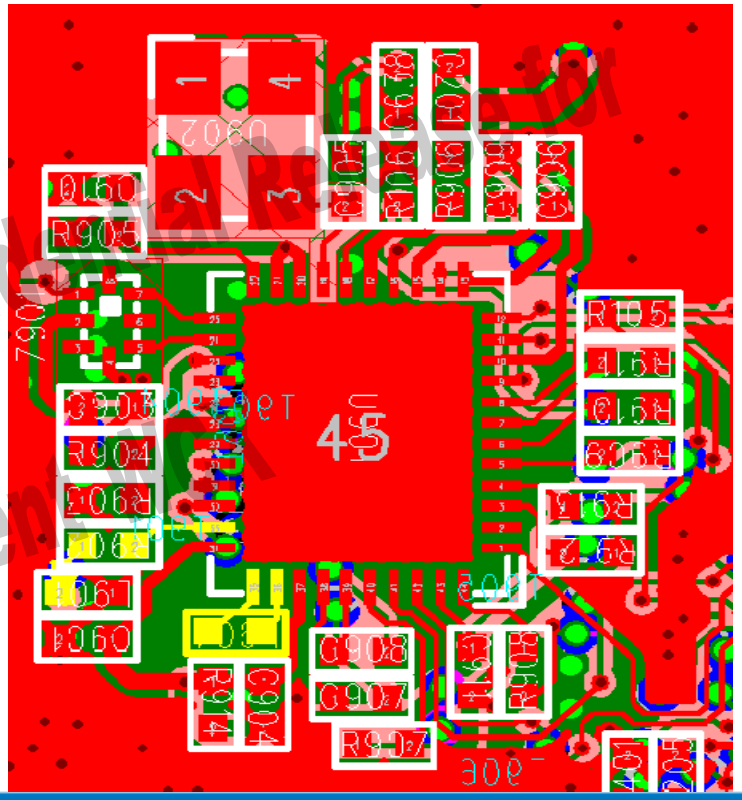
Ground Layout (layer1)

- Assure all bypass caps grounding or front-end matching grounding is solid grounding

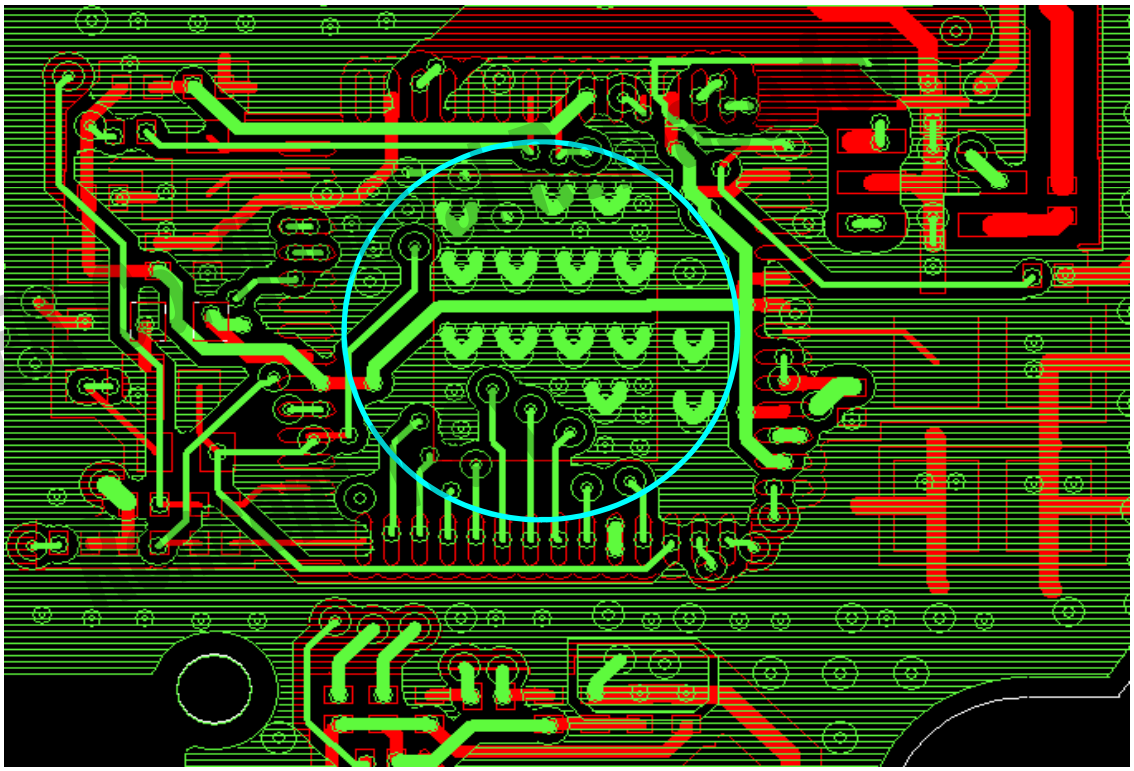
Layer1



Ground Layout (layer2)

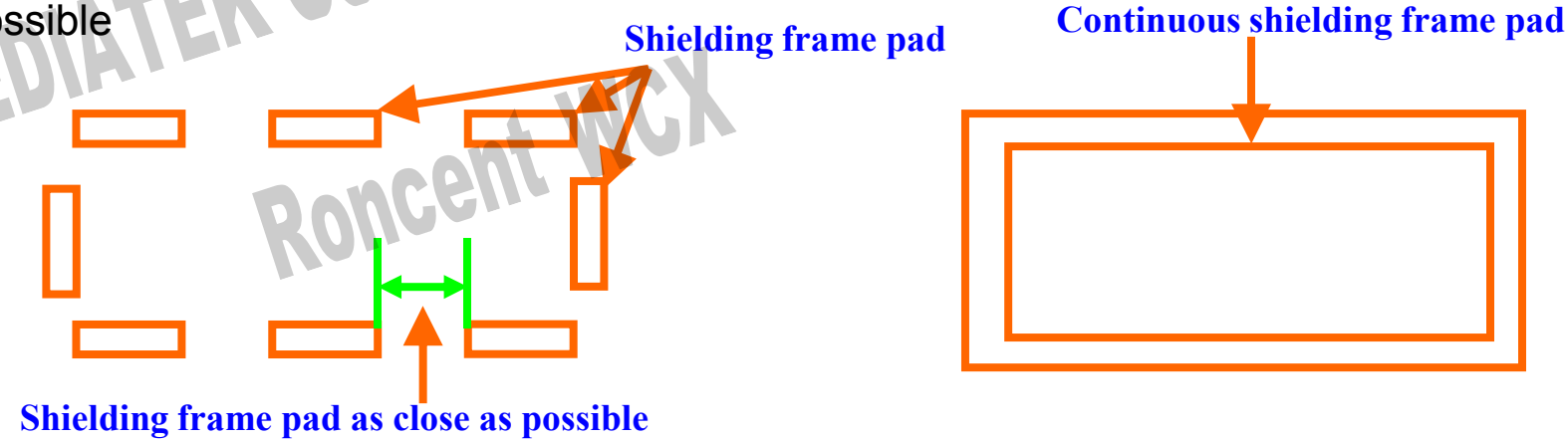
- Keep layer2 GND plane under MT6616 chip as complete as possible to minimize AC return current loop. Broken GND plane will result in large AC return current loop and increase EMI on FM

Layer2



Other System Consideration for FM (1/2)

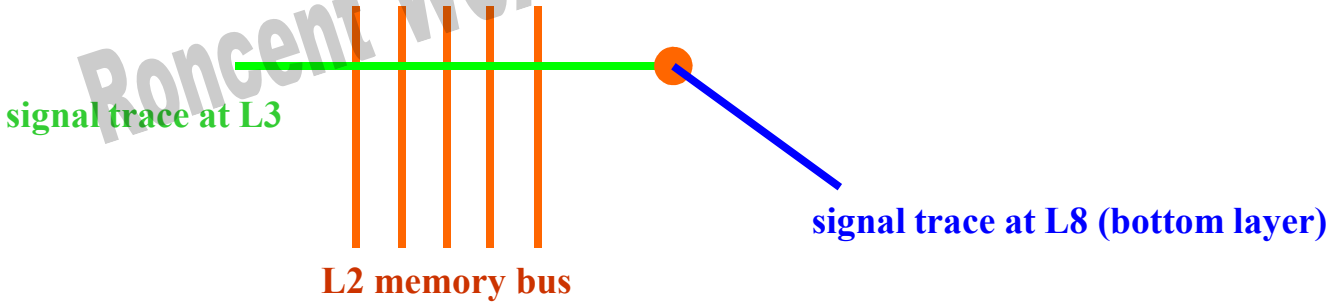
- Rule 1: Protect the BB 32.768kHz crystal layout
  - If the 32.768kHz signal is corrupted by digital signals, FM channel locking may be unstable.
  - BB 32.768kHz crystal layout rules:
  - Place the 32.768kHz crystal unit close to the BB, and L2 beneath crystal needs to be complete ground. The crystal and its traces must be protected by ground vias and ground planes.
  - Do not route power, MCP, FM I2C traces near 32.768kHz crystal circuit.
  - The 32.768kHz traces between crystal unit and BB should be on top layer.
- Rule 2: Backlight driver adoption
  - USE a charge pump backlight driver.
  - Using a DC-DC backlight driver may cause increased noise levels when the backlight is on. Need to take good care of DC-DC traces.
- Don’t dig hole in shielding cover and keep shielding frame pad as close or continuous as possible



Other System Consideration for FM (2/2)

- Since FPC/connectors/LCM screen might result in FM wireless de-sense issue, to keep earphone jack away from the above EMI source is recommended
- USB bus/LCM bus/memory bus traces have to route in inner PCB GND layers with solid GND shielding or route in shielding cover to avoid EMI on FM de-sense
- Since EMI filter is generally applied in LCM traces, to select EMI filter with FM band attenuation is recommended
- Don't let other signal traces crossed or paralleled with memory bus/LCM bus/USB bus, especially the signal traces finally will route in PCB top/bottom layer without shielding

Fail example :



PCB Design example for MT6616

- *MT6253+MT6616*

Outline

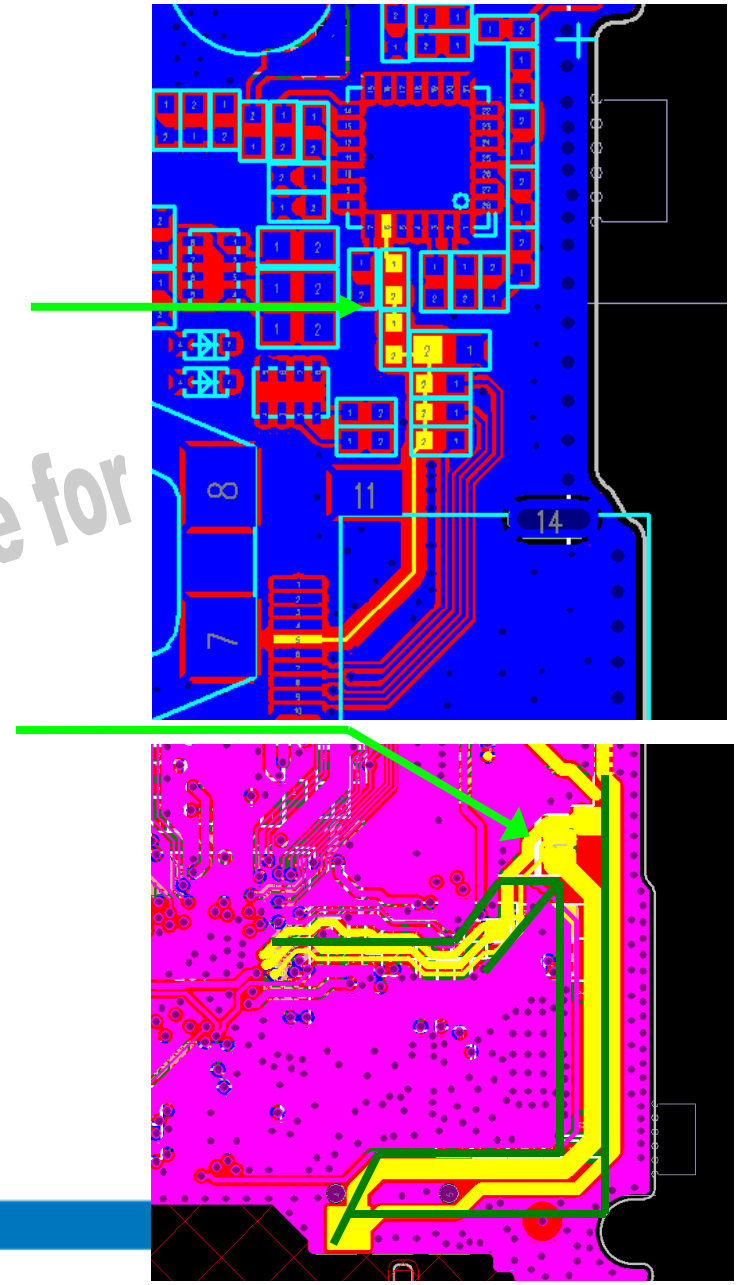
- FM design notes
- Earphone pin definition
- PMU – VBAT , VCORE , Boost1 & Class D
- LCM
- Memory interface
- Debug flow

FM De-sense Design Note

- Noise source
  - Low **chip level EMI**
  - Low slew rate
  - Low switching frequency
  - Low output swing
  - Clock **frequency hopping**
- Path
  - Power trace **star connection**
  - **Inner layer** covered with ground for noise trace routing
  - Adding **bead** for noise suppression
  - **Solid ground** for bypass cap
- FM IC
  - **Place FM chip near earphone jack**
  - Short and **well-shielded** antenna trace
  - Solid ground and bypass cap close to FM chip
  - Protected 32.768KHz clock trace

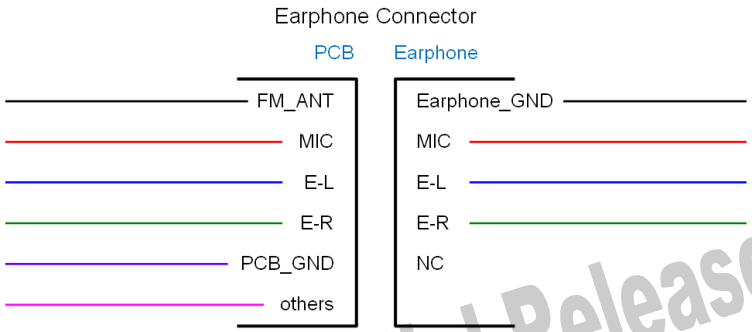
FM Design Note

- FM
  - **Place FM chip near earphone jack**
  - Short and **well-shielded** antenna trace
  - Solid ground and bypass cap close to FM chip
  - Protected 32.768KHz clock trace
- Other noisy trace
  - **VBAT star connection**
  - **Inner layer with ground trace around**
  - Adding series **bead** for noise suppression
  - **Solid ground** for bypass cap

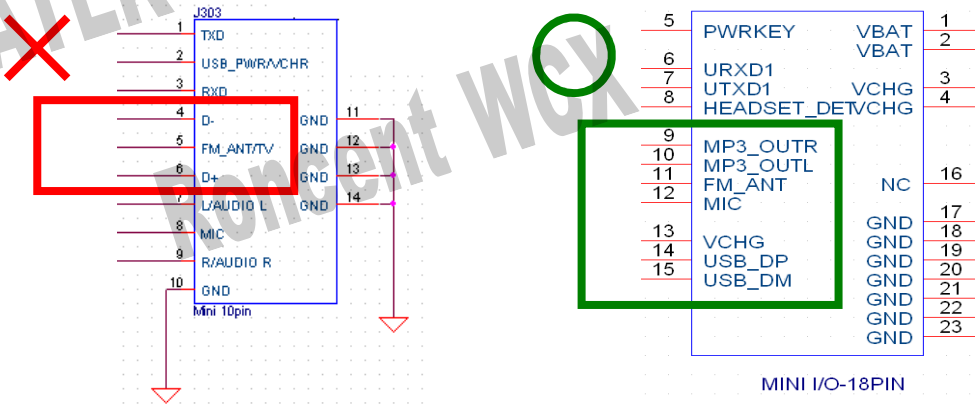


Earphone PIN Definition

- Connect earphone ground to FM_ANT
- Separate FM_ANT pin from USB data pins to avoid noise coupling



- **Not recommend : USB data pins next to FM_ANT pin (x)**

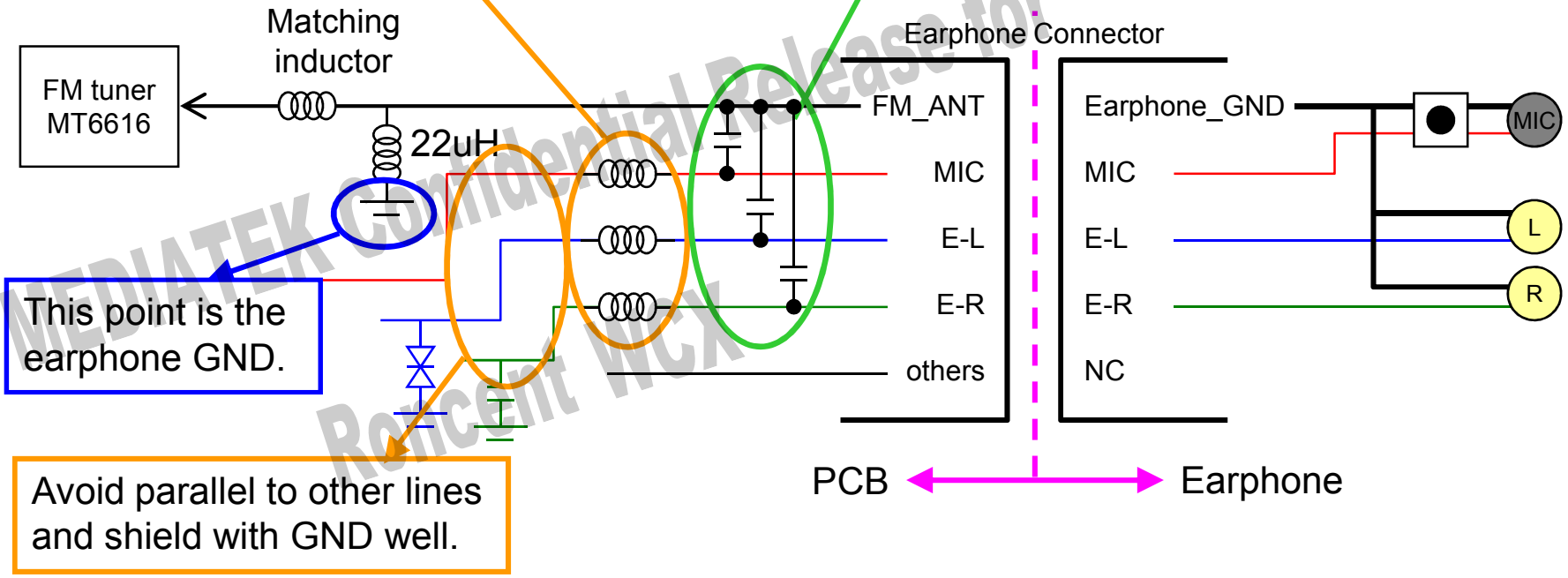


Audio Interface Design Concept

Add beads (BLM18BD252SN1) on headset related pins, to avoid interference (or bypass) path.

These beads should be placed as close to the phone jack as possible.

Add caps (1nF) on L, R paths, to provide extra path for FM.

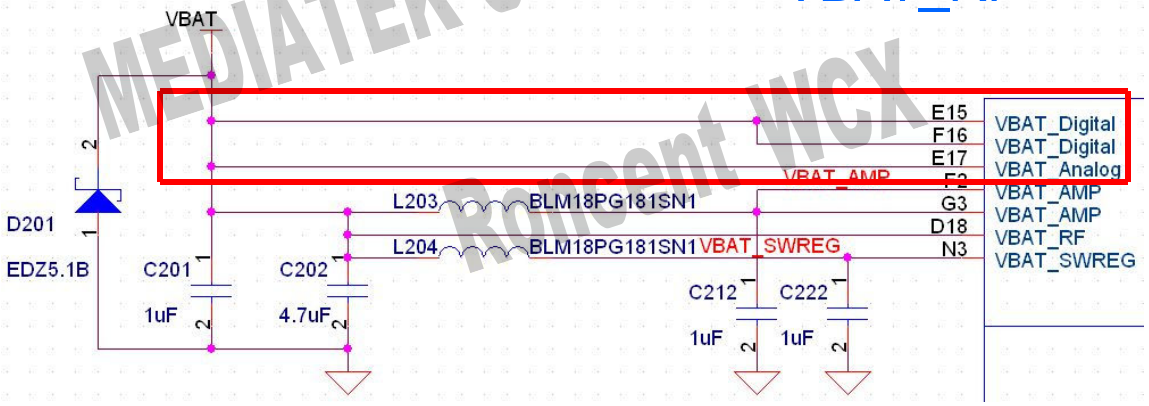


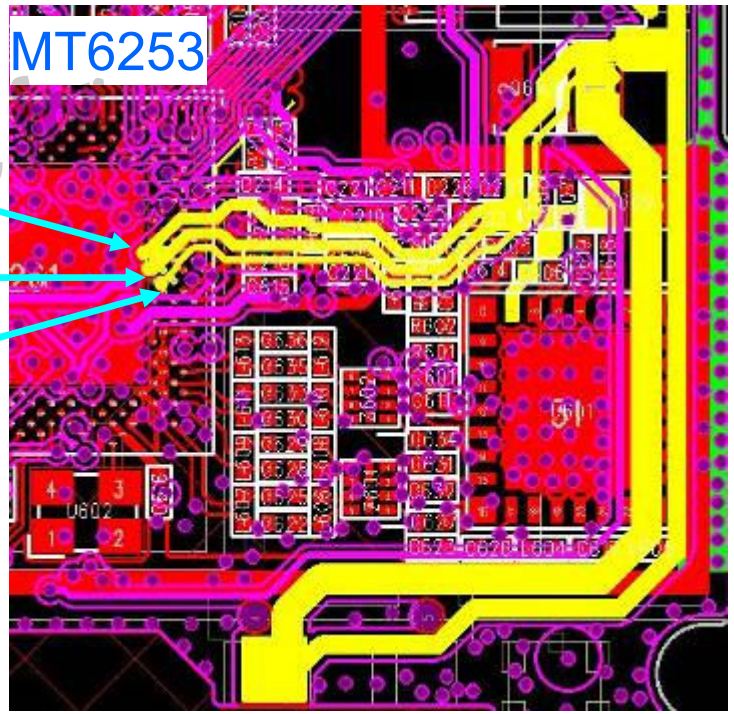
PMU DC/DC switching design notes

- PMU – **VBAT , VCORE , Boost1 and Class D**
- Input power trace **star connection**
- Input & output **bead** close to IC in shielding case
- Input bypass **capacitor** close to IC in shielding case
- Input & output trace **width**
- Input & output solid **ground** and short return ground path

PMU - VBAT Traces (1/2)

- VBAT_Analog and VBAT_RF should separate the VBAT_DIGITAL trace and **star-connect** to the bulk capacitor near battery connector.

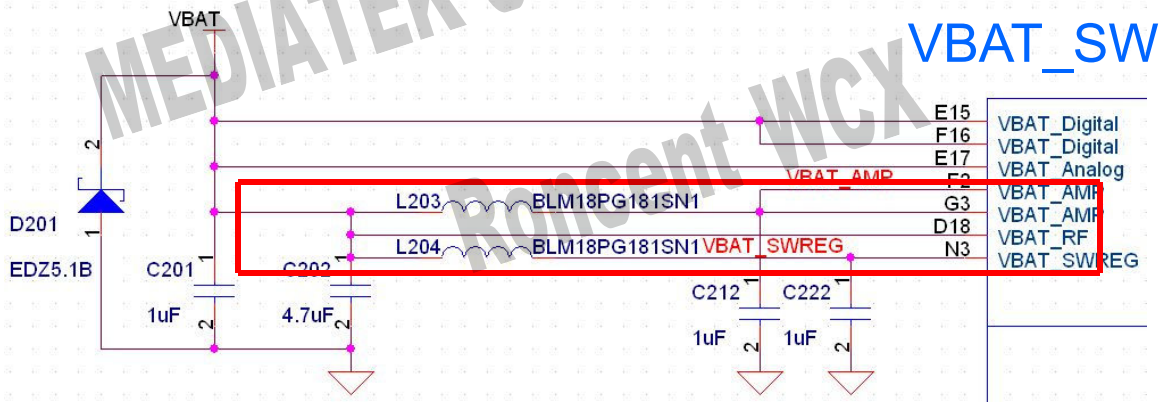


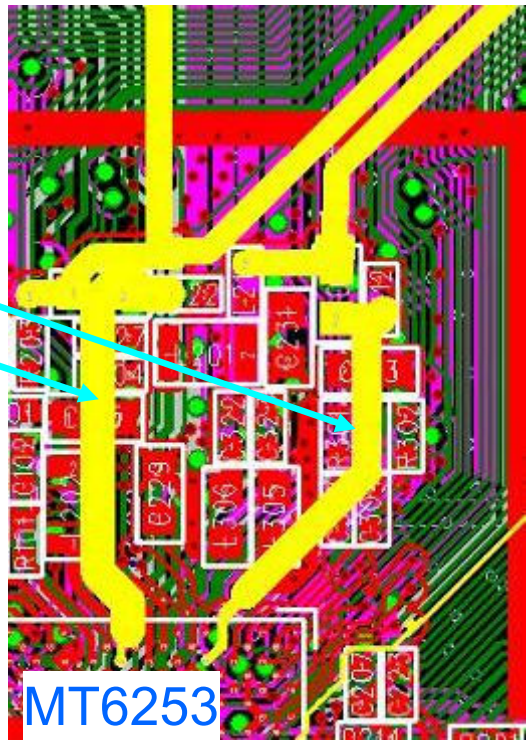


PMU - VBAT Traces (2/2)

- (VBAT_AMP/VBAT_SWREG) should separate the VBAT_DIGITAL trace. **Start connection** from battery connector and **all traces should be in inner layer or under shielding case.**
- **L203/L204/C212/C222 should put close to pin-out and be in shielding case**.
- Enhance the VIA connection (at least >2)
- Solid grounding for C212/C222

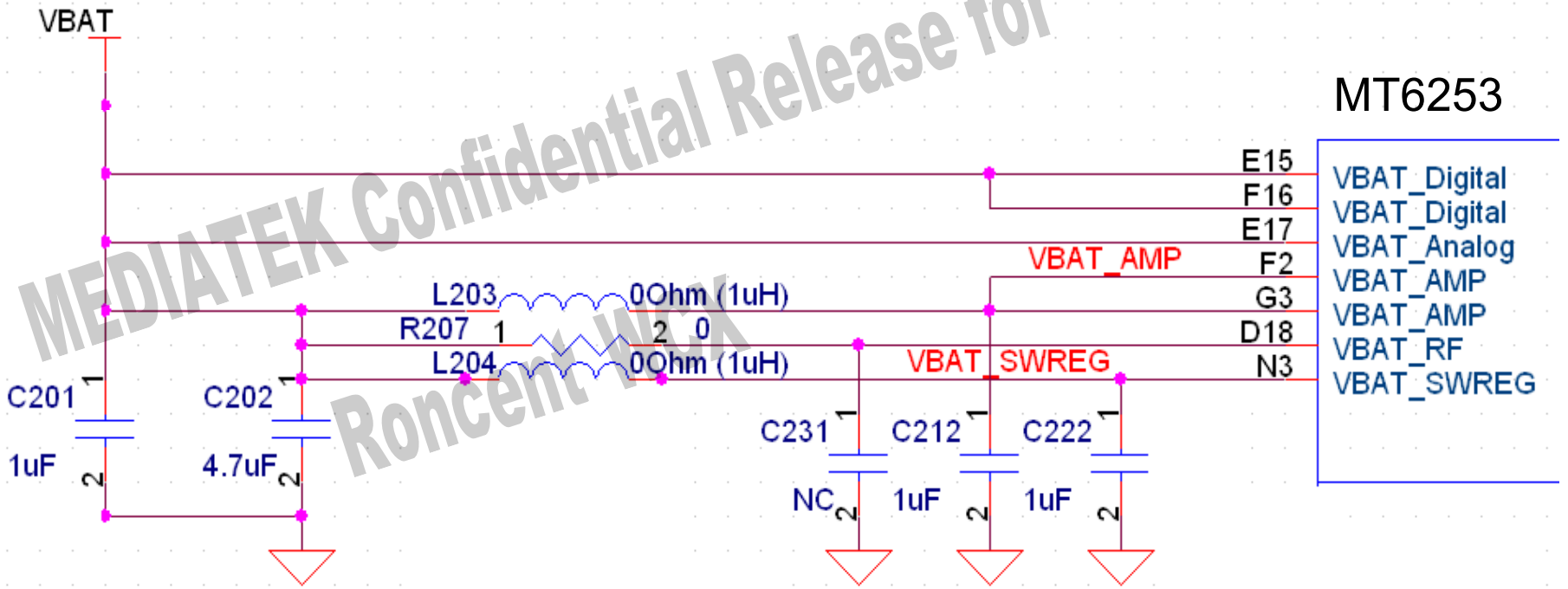
plane via hole directly.





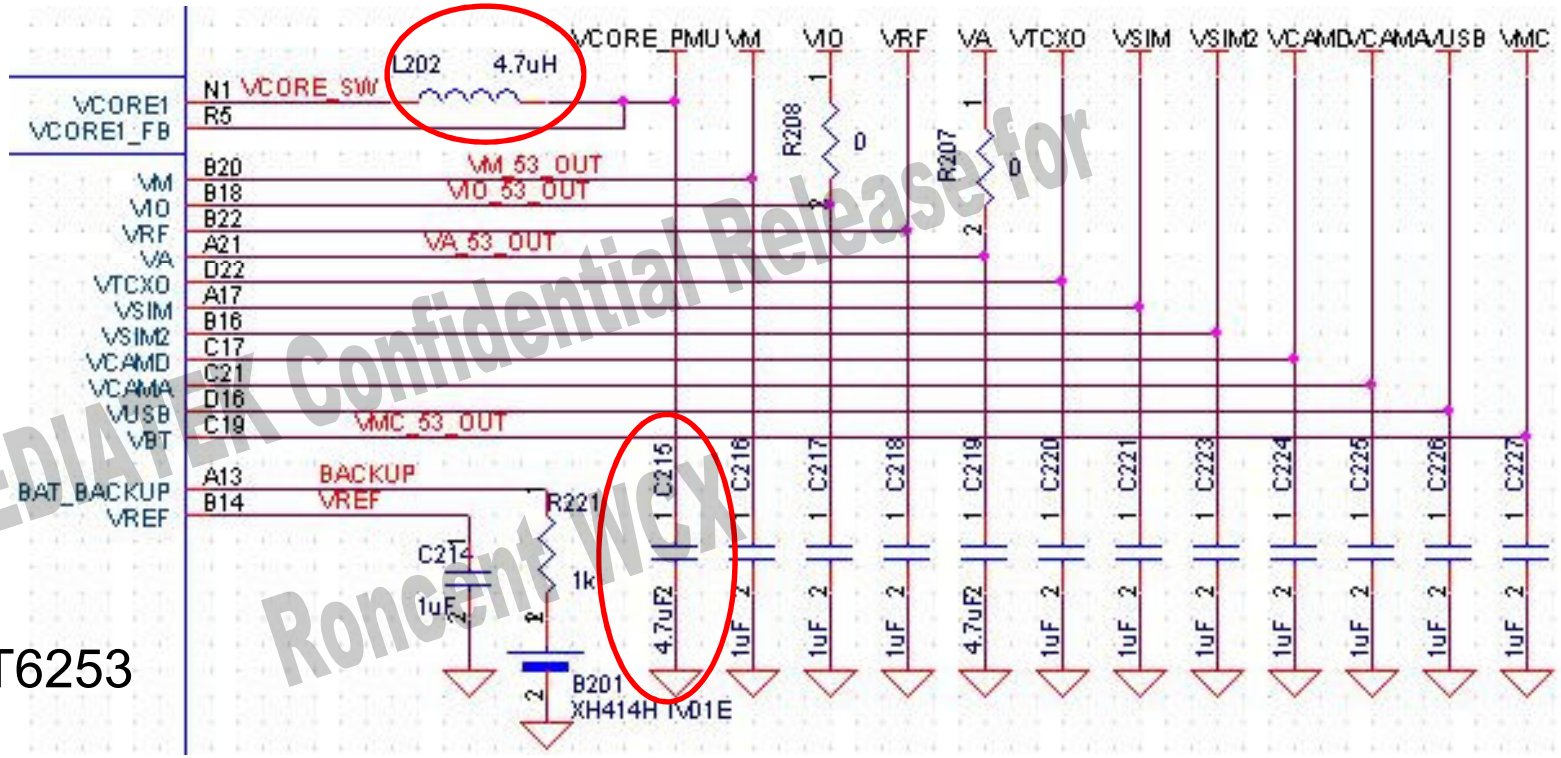
PMU – VCORE (1/2)

- Inner layer routing with GND shielding
- Star connection to CON directly
- VBAT branch line width 28mil at least
- Reserve one bead (BLM15AX102SN1) for L204 and close to IC to avoid switching noise influencing FM de-sense
- Place bypass cap with solid grounding and close to IC



PMU – VCORE (2/2)

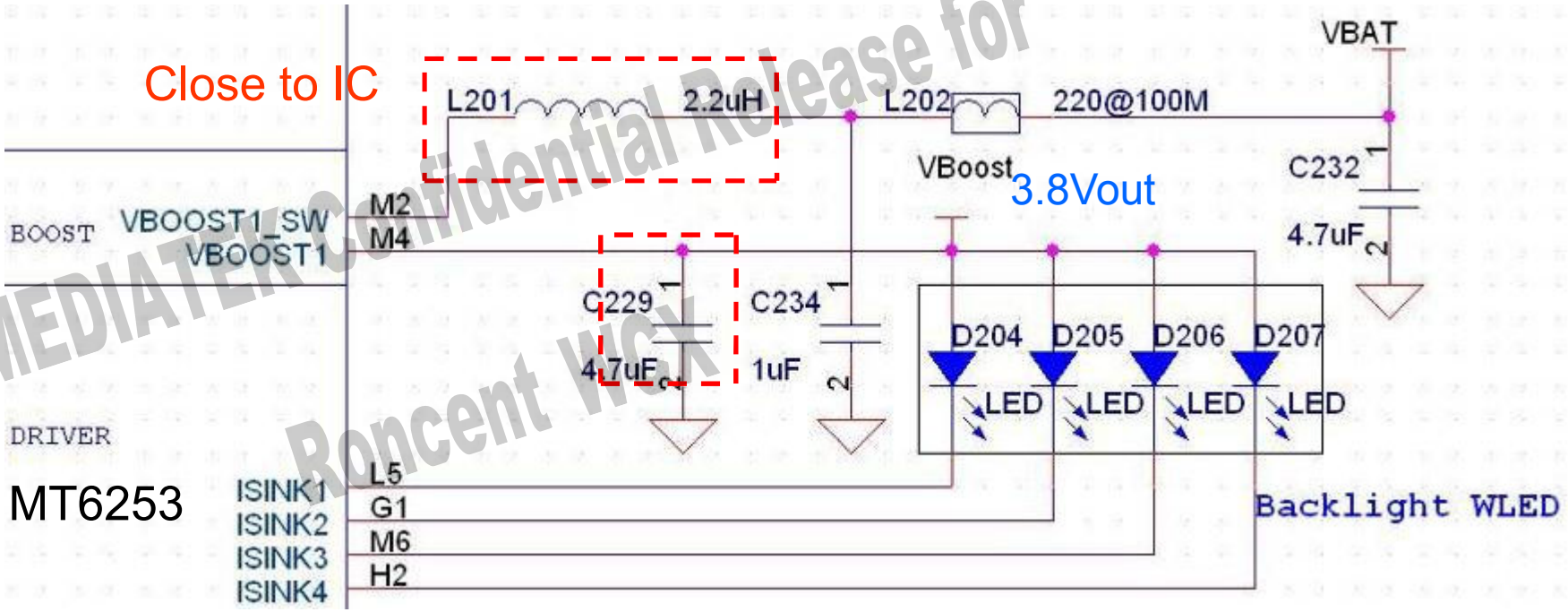
- As for VCORE, please **keep L202 and C215 close to MT6253 and in shielding cover**.



MT6253

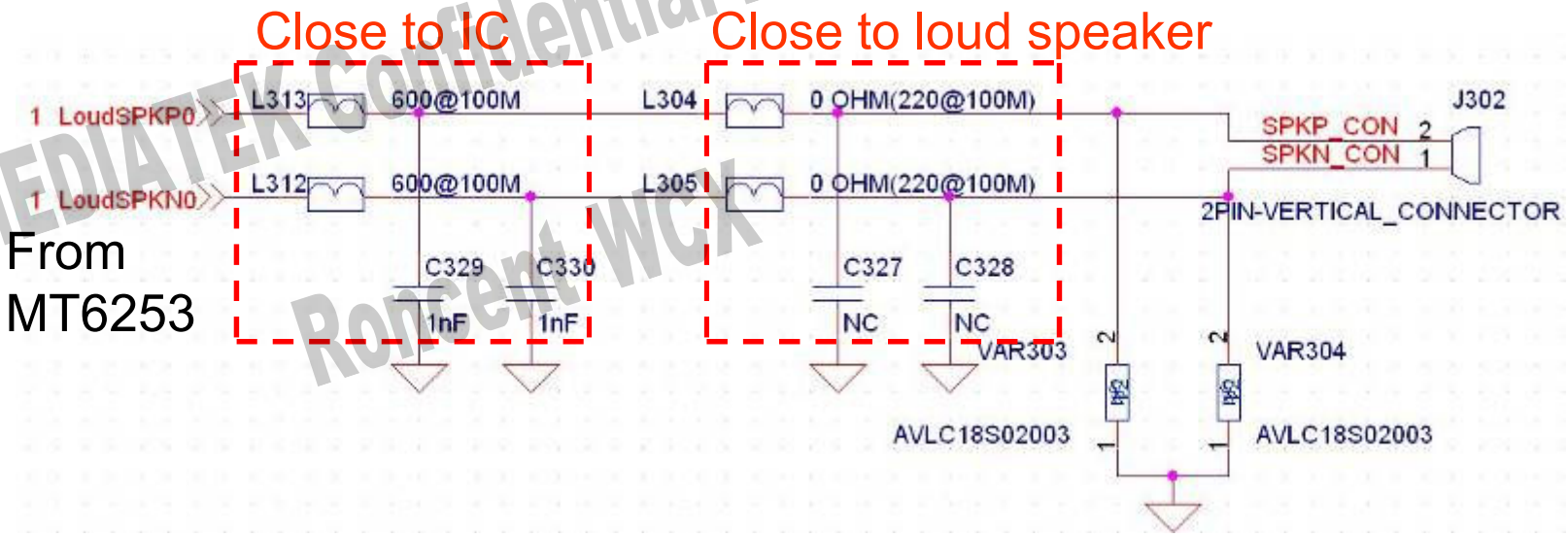
PMU – Boost1 For Parallel LCM

- Set BOOST **Vout=3.8V** and apply ISINK (constant current) for backlight WLED
- Reserve one bead (BLM15AX102SN1) for L202 and close to IC to avoid switching noise influencing FM de-sense
- **Keep L201 and C229 close to MT6253 and put in shield case**.



PMU - Class-D Audio Amplifier Output Filter

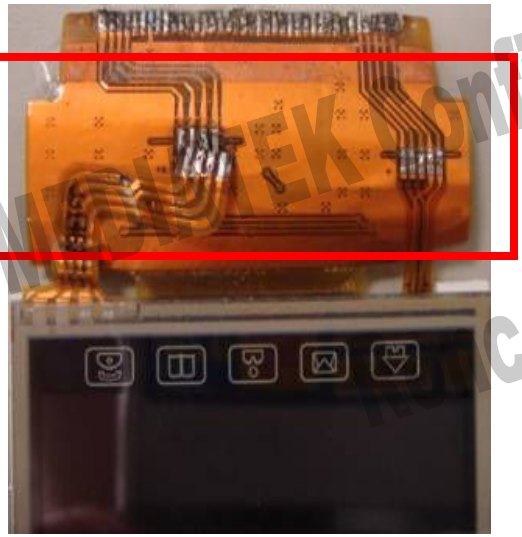
- Use Class AB as back-up
- Reserve 2 stage filter at output stage of Class-D to prevent interference to RF performance.
- 1st stage filter should be close to IC as possible, 2nd stage filter should be close to loud speaker.
- All the traces from IC to 2nd stage filter should not exposed to prevent interference to RF performance



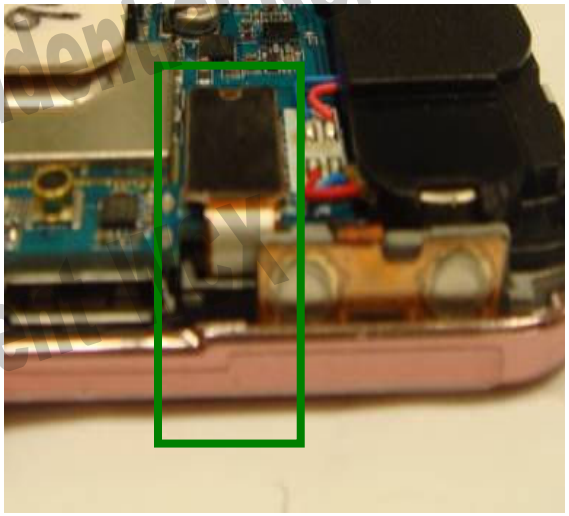
LCM FPC

- Use copper and short FPC to avoid noise radiation
- Shield LCM with ground well
- Reserve EMI filter in LCM data bus and close to LCM FPC connector
  - EMI filter includes FM band attenuation
  - Suppress LCM screen and FPC radiation on FM wireless de-sense

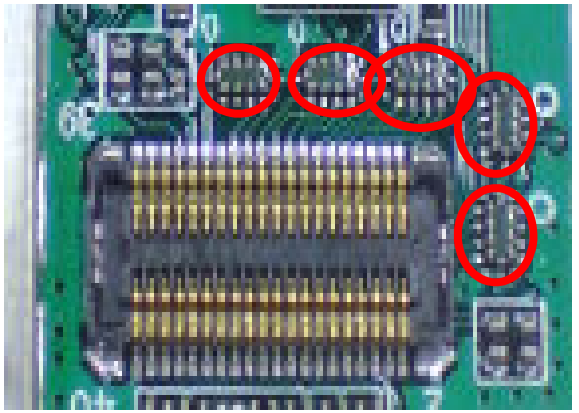
✗ Long and no shielding



○ Short and shielded well

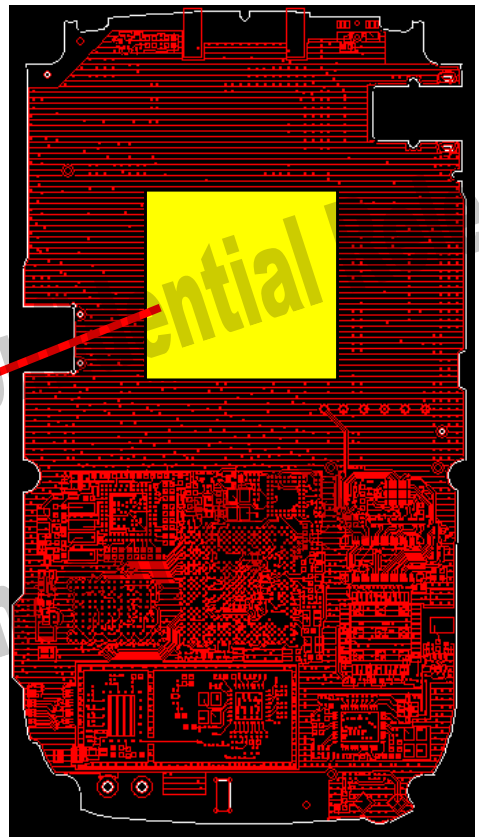


○ EMI filter near FPC connector



LCM Metal

- In order to suppress LCM screen radiation, proper PCB exposed GND area(1/4 LCM metal area at least is recommended) reserving for LCM metal solid grounding is necessary
- if necessary, to insert conductive cloth between LCM metal and PCB exposed GND area can assure solid grounding



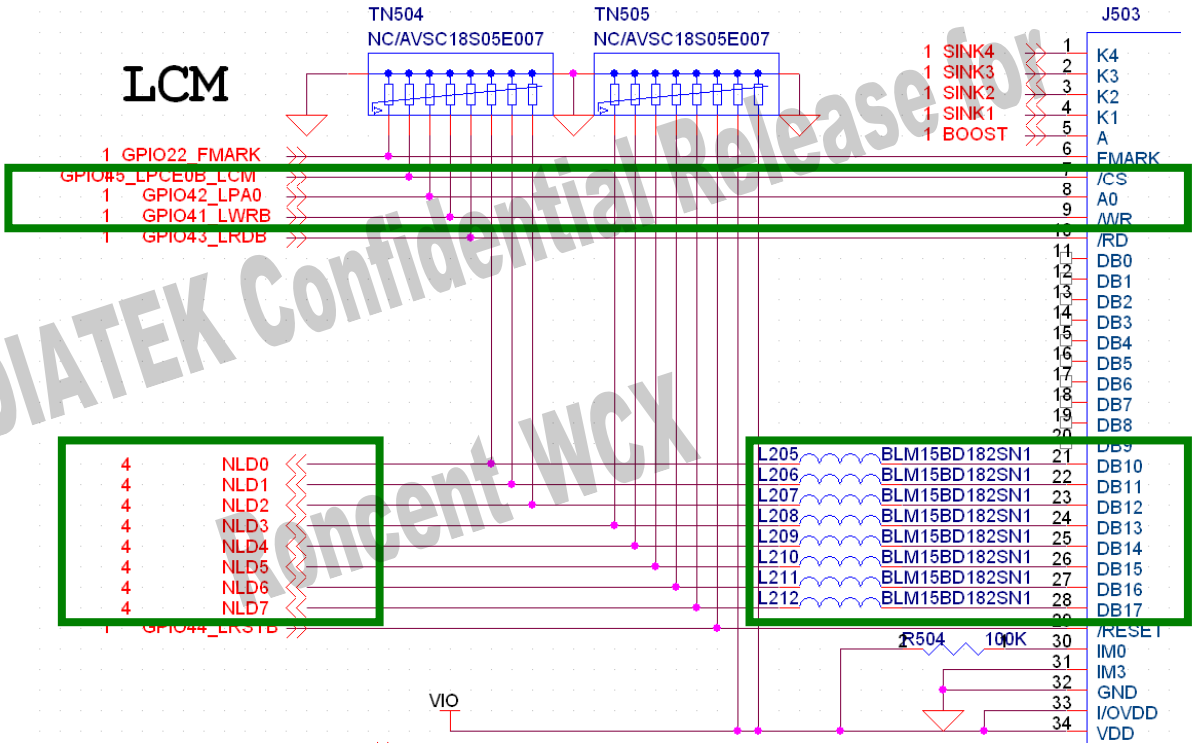
PCB exposed GND area reserving for LCM metal solid grounding

LCM metal

LCM metal overlap PCB exposed GND area

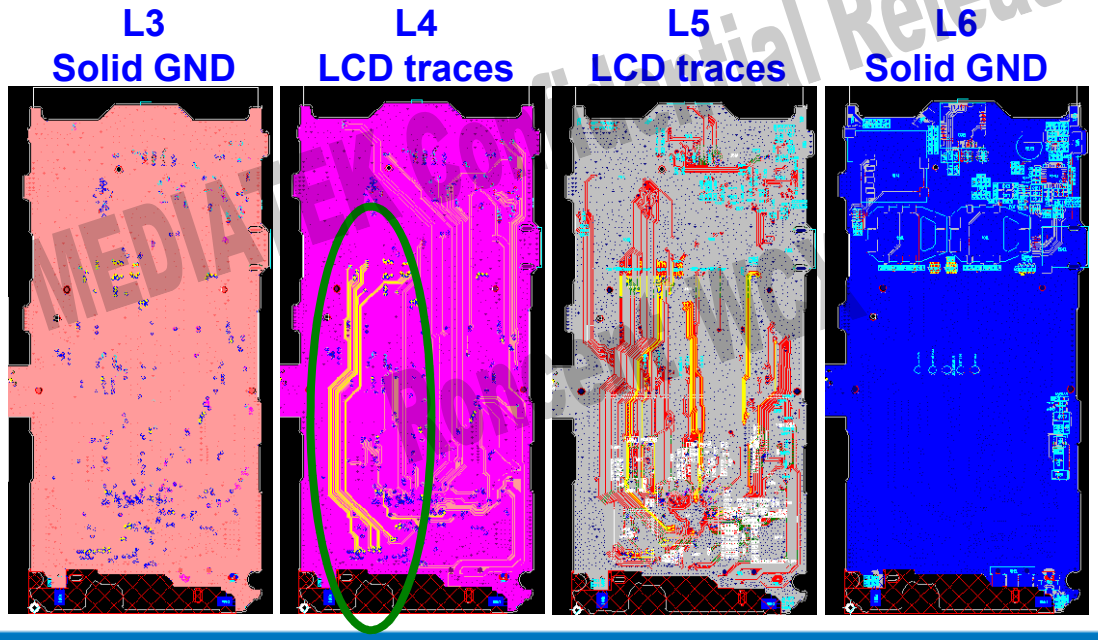
LCM interface (1/2)

- Suggest adding **series beads or EMI filter** on LCD data pins (NLD0-NLD7)
- Use inner layer for LCD trace routing with GND shielding



LCM interface (2/2)

- Short and **inner layer** trace routing
- Solid ground around signal traces
- Avoid parallel with other traces
- Short and copper FPC or add series beads or EMI filter



Tearing-solving & Performance-guaranteed Settings in 6253

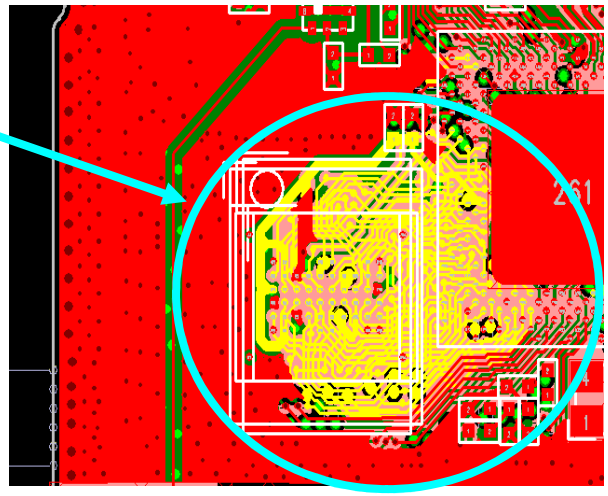
- LCD_write_cycles should be small than or equal to 9/7 when QVGA/WQVGA display under 52MHz LCD clock settings.

LCD resolution								
width	240							
height	320							
pixel per frame	76800							
	tearing-free(75Hz) Safe zone when QVGA in all scenario							
LCD write cycles (cycles	3	4	5	6	7	8	9	10
AHB_freq (MHz)	52	52	52	52	52	52	52	52
LCD write time (ns)	57.69	76.92	96.15	115.38	134.62	153.85	173.08	192.31
frame update time (ms)	8.86	11.82	14.77	17.72	20.68	23.63	26.58	29.54

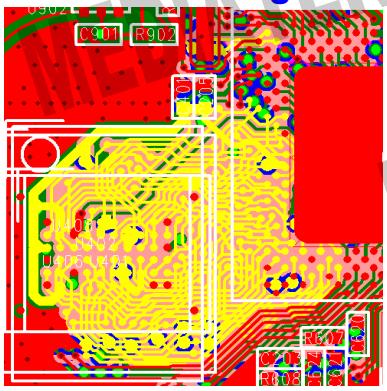
LCD resolution								
width	240							
height	400							
pixel per frame	96000							
	tearing-free(75Hz) Safe zone when WQVGA in all scenario							
LCD write cycles (cycles	3	4	5	6	7	8	9	10
AHB_freq (MHz)	52	52	52	52	52	52	52	52
LCD write time (ns)	57.69	76.92	96.15	115.38	134.62	153.85	173.08	192.31
frame update time (ms)	11.08	14.77	18.46	22.15	25.85	29.54	33.23	36.92

Memory interface (EMI)

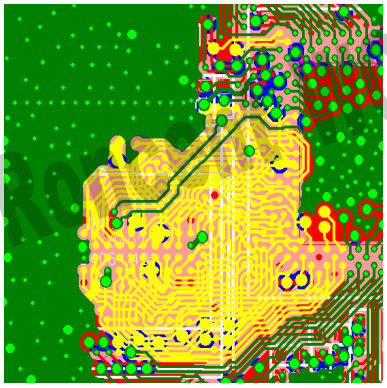
- Place memory close to MT6253 memory pins
- Short ,**inner layer** and shielded trace routing
- Solid ground around signal traces
- Avoid parallel with other traces
- Separated from other signal traces



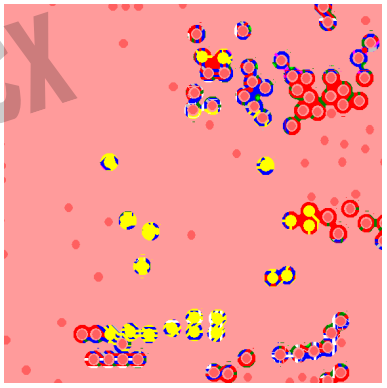
L1
inside shielding case



L2
short EMI traces



L3
Solid GND



FM de-sense debug check list (1/2)

- Check if above rules are followed
- Check original performance
- Check conductive performance
  - Remove FM_ANT series cap and inductor
  - Use external 2.8V supply
  - Use external 32KHz
  - Remove external R/L series cap
  - Use external I2C
- Check earphone jack
  - Modify EINT (earphone detection) to turn on FM w/o earphone
  - Remove series components on FM_ANT neighbor pins
  - Remove FM_ANT neighbor pins

FM de-sense debug check list (2/2)

- Check LCM
  - Shield LCM FPC
  - Shield LCM frame
  - Remove LCM
  - Shield LCM connector pins
  - Add extra series bead on LCM connector pins
- Check memory shielding case
  - Improve grounding
- Check keypad
  - Improve grounding
  - Add extra series bead or bypass cap

FM wireless de-sense debug trick and flow (1/3)

- Traditional method
  - Human ear test to find out FM de-sense channel
  - Use EMI probe to search possible interference source located in de-sense channel
  - Try to deal with possible interference source by shielding, attenuation, bypass, rework, etc. to confirm interference source
- New method
  - Human ear test to find out FM de-sense channel
  - Use a metal stick to touch component and check if any human ear performance degradation in de-sense channel at the same time. If degradation is existent, it is a possible interference source
  - Try to deal with possible interference source by shielding, attenuation, bypass, rework, etc. to confirm interference source

FM wireless de-sense debug trick and flow(2/3)

	Traditional method	New method
Min. detection area	Large	Small
Confirmation way	Indirect	Direct
Rework effort for confirmation (period voice case)	Large	No
Manual scan time	Short	Long
Instrument requirement	Yes	No
EMI source level/signal type indentify	Medium	Low
EMI source location accuracy and speed	Low	High

Win

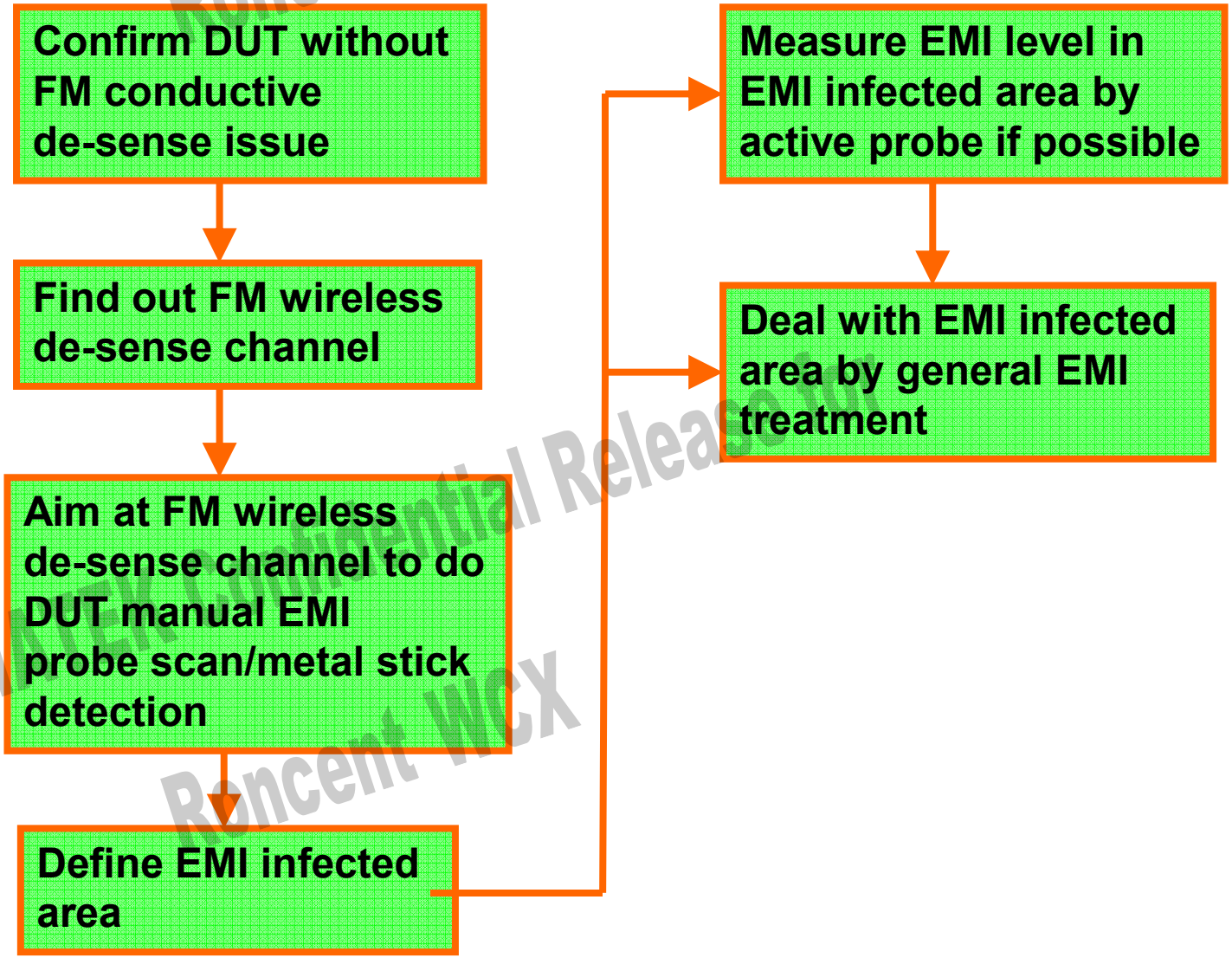
Win

Win

Win

Win

FM wireless de-sense debug trick and flow(3/3)



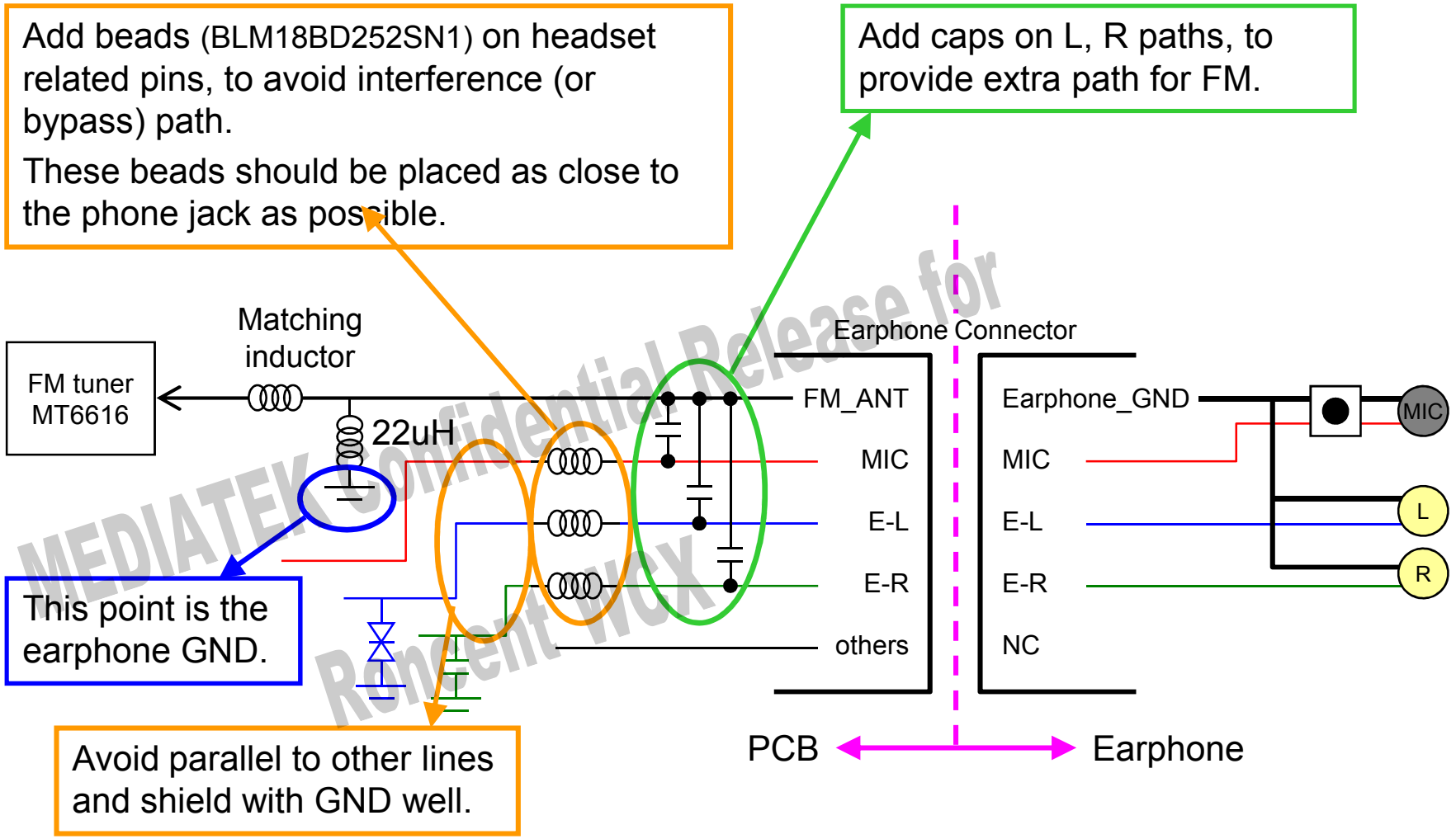
Audio Interface Design

- *2.5mm/3.5mm Earphone*
- *Mini USB Earphone*

Audio Interface Design Guidelines

- On earphone pins AFL, AFR, and MIC:
  - Place **1 nF** shunt capacitors (shunt to earphone GND pin) closest to the earphone jack. To improve earphone echo performance, connect the 3 capacitors from each pin to the earphone GND pin separately. (See next page.)
  - Place the **BLM18BD252SN1** series bead second closest to the earphone jack.
  - No other components can be closer to the earphone jack.
- Earphone GND wire (FM_ANT) should not be connected to the earphone connector shell.
- An earphone **longer than 150 cm** is recommended for better performance.

Audio Interface Design Concept



Wireless Sensitivity Enhancement

- Each earphone suggestions improves wireless sensitivity significantly. The following table shows the improvement amount based on MTK's experiments.

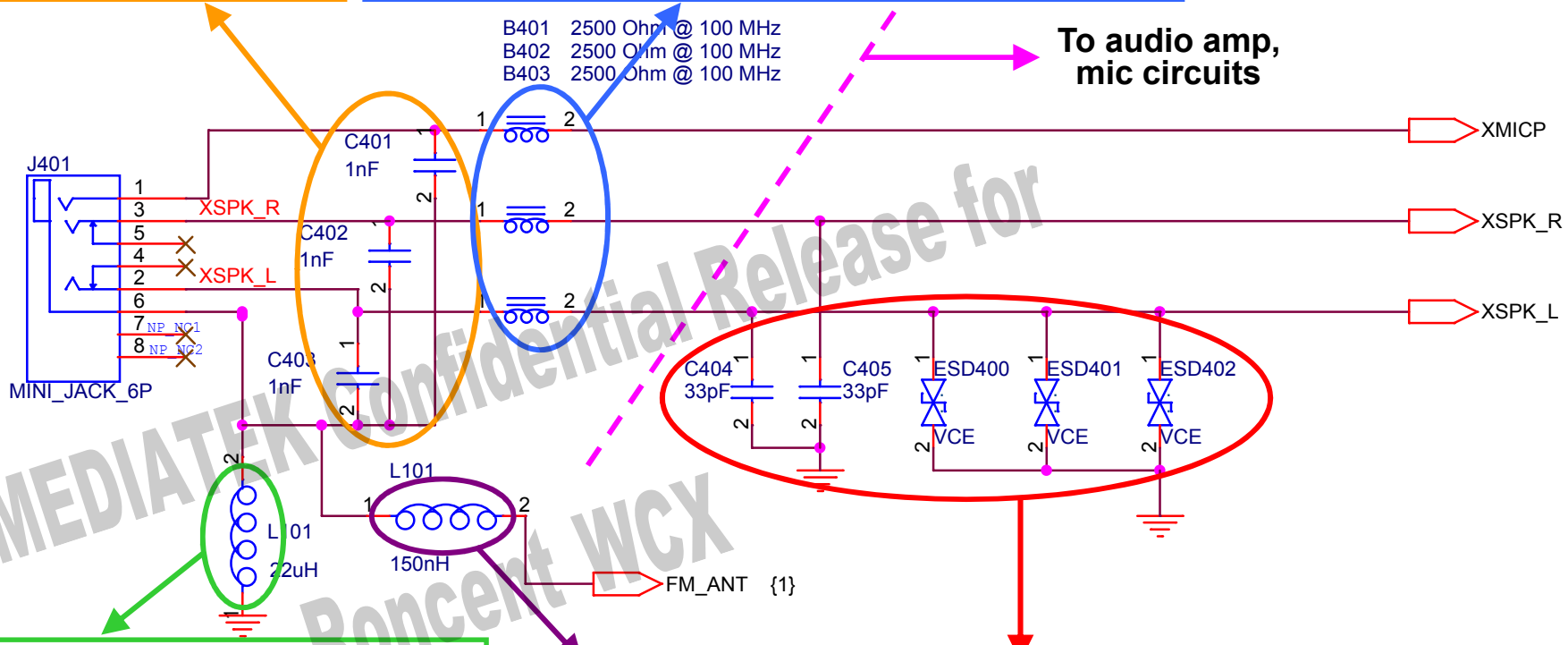
	Improvement amount
Series beads on earphone AFL, AFR, and MIC pins	**14.5 dB**
1 nF shunt cap between earphone AFL, AFR, MIC, and GND pins	**2~3 dB**
Earphone length > 150 cm	**1~2 dB**

2.5mm/3.5mm Earphone Design

Audio Interface Reference Circuit (2.5mm or 3.5mm Earphone Jack)

Shunt these earphone lines with 1nF caps.

Add beads on these lines. **These beads should be placed as close to the earphone jack as possible.**



Connect this 22uH inductor to mobile phone ground. **BLM18BD252SN1** can be used instead of a 22 uH inductor.

Series 150 nH inductor for antenna matching.

These caps cannot be closer to the earphone jack than the beads.

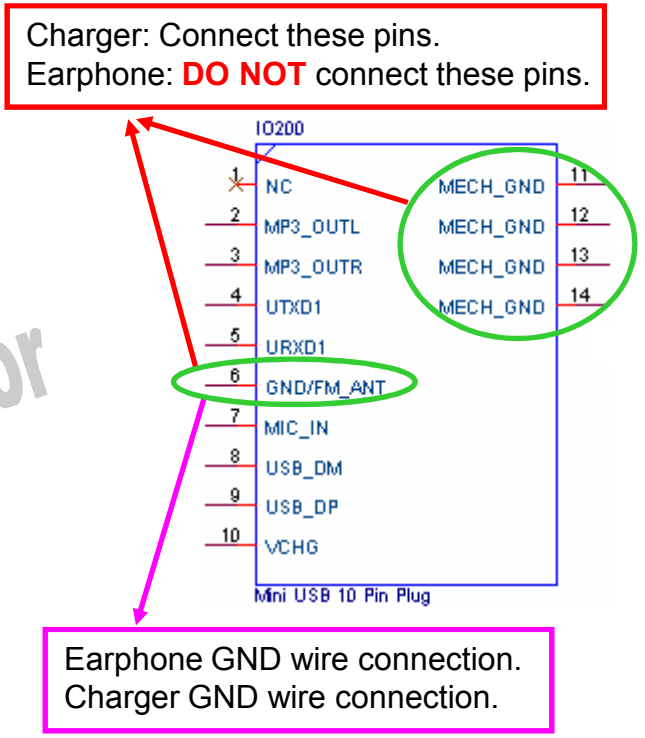
Mini USB Earphone Design

- With only 1 GND pin on IO connector
- With 2 GND pins on IO connector

Mini USB IO Connector Design Recommendation: Only 1 GND Pin on IO Connector

Accessory interior design suggestion

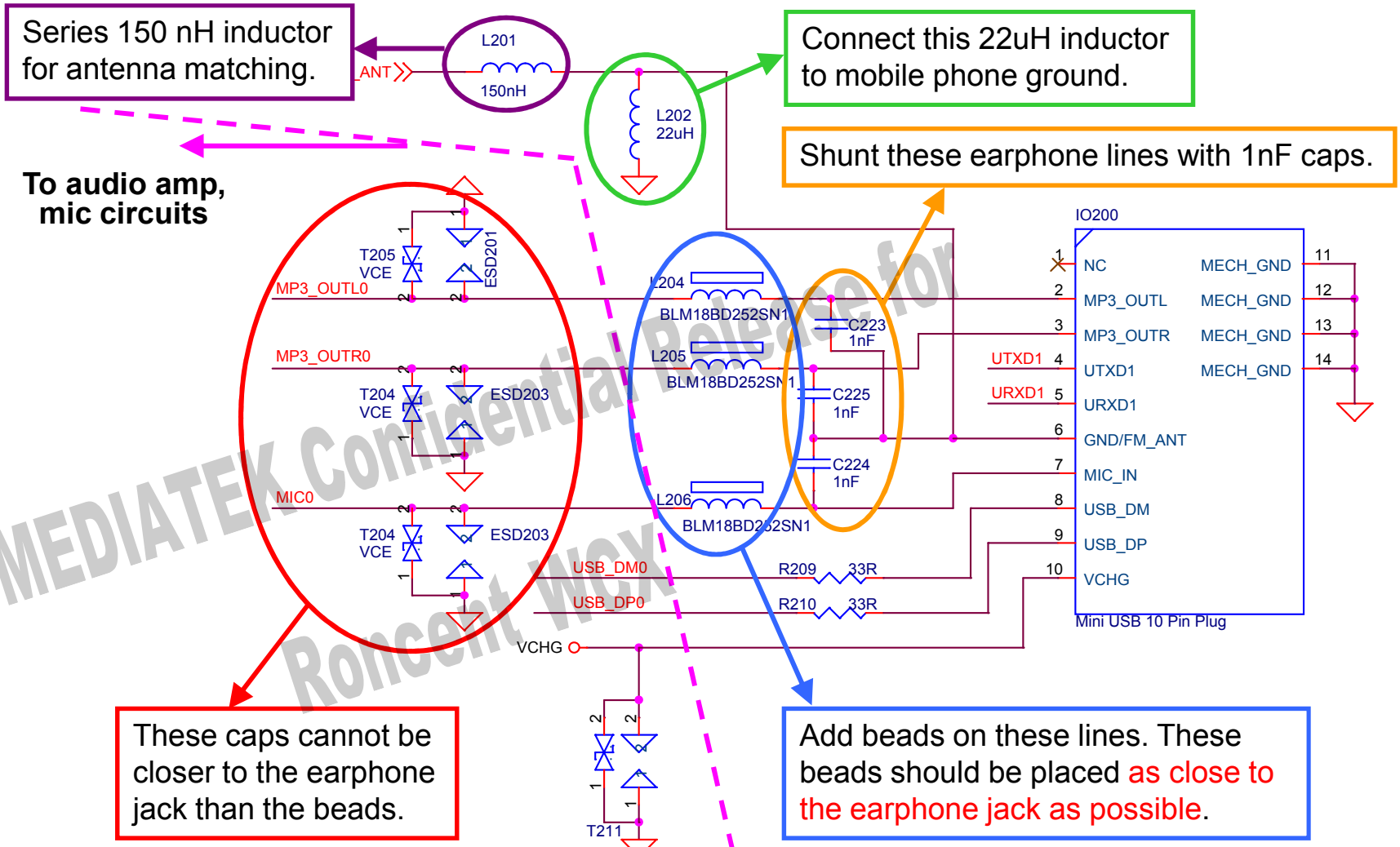
- The earphone GND wire MUST be used for the FM antenna. Inside the earphone, the GND wire CANNOT be connected to any other wire or to the outer shell in any way. Other wires inside the earphone CANNOT be connected to PCB GND.
- The 22uH inductor cannot tolerate high current. For high current application, such as a charger, connect the charger GND wire inside the charger to both the GND/FM_ANT pin and the charger outer shell.
- In this example, the earphone GND wire is connected to IO connector pin6, and the charger GND wire is connected to pin6 and the charger outer shell.



IO connector pin description

IO pin name	Function	Notes for PCB design
GND/FM ANT	GND for all Mini USB accessories and FM antenna.	CANNOT be directly connected to PCB ground. MUST be connected to PCB ground through a 22uH inductor.
MECH_GND	4 outer shell pins of the IO connector. Mainly used for better connector strength. Can also serve as charger GND.	These 4 pins are directly connected to PCB ground. DO NOT connect these pins to the GND/FM_ANT pin.

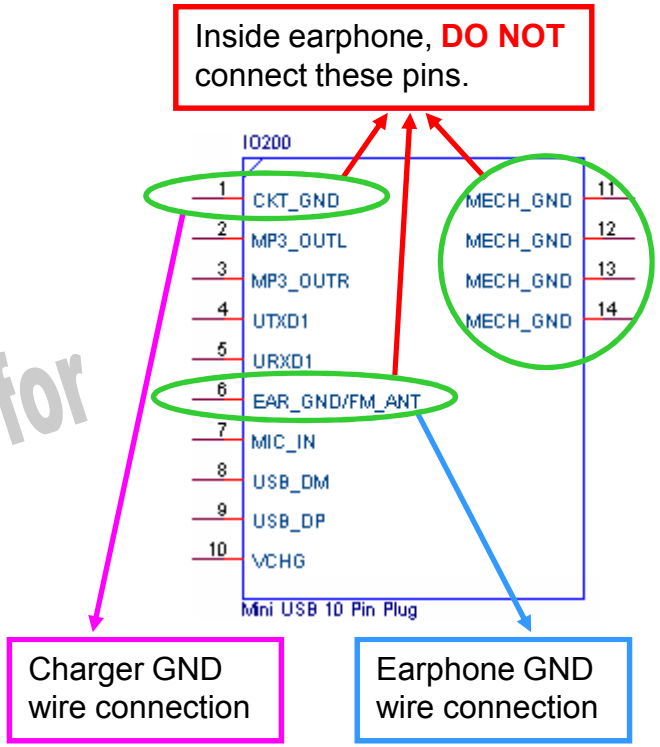
Audio Interface Reference Circuit: Only 1 GND Pin on IO Connector



Mini USB IO Connector Design Recommendation: 2 GND Pins on IO Connector

Accessory interior design suggestion

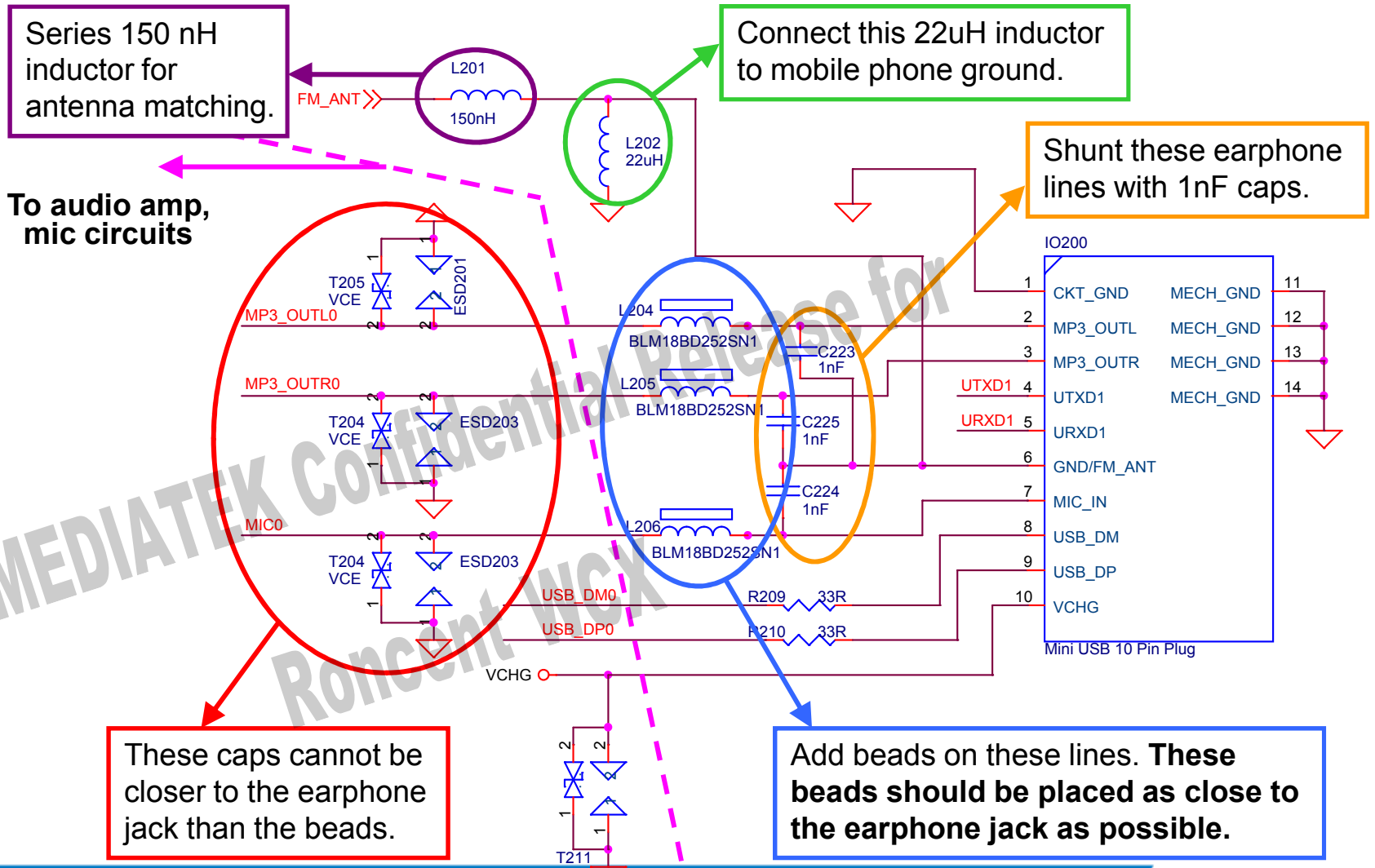
- The earphone GND wire MUST be used for the FM antenna. Inside the earphone, the GND wire CANNOT be connected to any other wire or to the outer shell in any way. Other wires inside the earphone CANNOT be connected to PCB GND.
- The 22uH inductor cannot tolerate high current. For high current applications, such as a charger, use another IO connector pin if available. The charger GND wire inside the charger can also be connected to the charger outer shell.
- In this example, the earphone GND wire is connected to IO connector pin6, and the charger GND wire is connected to pin1 and possibly the charger outer shell as well.



IO connector pin description

IO pin name	Function	Note for PCB design
EAR_GND/FM_ANT	Earphone GND, also FM antenna.	CANNOT be directly connected to PCB ground. MUST be connected to PCB ground through a 22uH inductor.
CKT_GND	GND for Mini USB accessory, with large GND current.	This pin is directly connected to PCB ground. DO NOT connect this pin to the EAR_GND/FM_ANT pin.
MECH_GND	4 outer shell pins of the IO connector. Mainly used for better connector strength. Can also be served as charger GND.	These 4 pins are directly connected to PCB ground. DO NOT connect these pins to EAR_GND/FM_ANT.

Audio Interface Reference Circuit: 2 GND Pins on IO Connector



Component Replacement Suggestions

- Series beads on earphone pins AFL, AFR, and MIC
  - Suggested: 0603-size BLM18BD252SN1 bead
    However, if board space is limited, 0402-size bead BLM15BD182SN1 or BLM15HD182SN1 can be used instead.
- Inductor connecting earphone GND wire to board GND
  - Suggested: 22 uH inductor or BLM18BD252SN1 bead
    However, if the earphone GND pin serves as the only GND path for the charger, then this component must be able to tolerate high current. The components in the table below can be used instead.

Murata part number	Inductor value	Size	Self-resonant frequency	Rated current	Notes
LQH2MCN1R0M02	1.0 uH	0603	100 MHz	485 mA	
LQM21PN1R0MC0D	1.0 uH	0805	90 MHz	800 mA	
LQM21PNR47MC0D	0.47 uH	0805	100 MHz	1100 mA	Usable, but its wireless performance is the worst among the three. Not recommended unless such a high current is required.

FM Design Checklist

Item	Done!	Checkpoint
1	☐	Series beads are placed on the AFL, AFR, and MIC pins of the earphone jack.
2	☐	1 nF shunt caps are placed between the AFL, AFR, MIC, and GND pins of the earphone jack.
3	☐	The earphone is longer than 150 cm.
4	☐	The FM_2V8 bypass cap is placed beside pin34 , and the FM_2V8 feeding network routed is properly.
5	☐	Place 330Ohm close to Pin30,41,42
6	☐	The FM antenna path is routed using a 50Ω RF trace.
7	☐	Follow the FM system layout guide as previous slides . Especially , place MT6616 far away from LCM traces and memory. Connect VBAT trace directly to battery connector.
8	☐	Earphones: Follow MTK's suggestion for GND connection and pin assignment on PCB and inside earphone.

If you require MTK's assistance in FM design, please prepare this checklist and submit it along with schematics, layout files and earphone schematics/data sheet.

More Detailed FM Earphone Antenna Illustrations

- *Illustration of FM earphone antenna*
- *FM earphone antenna pin definition*
- *FM earphone antenna troubleshooting*

Illustration of FM Earphone Antenna (1/2)

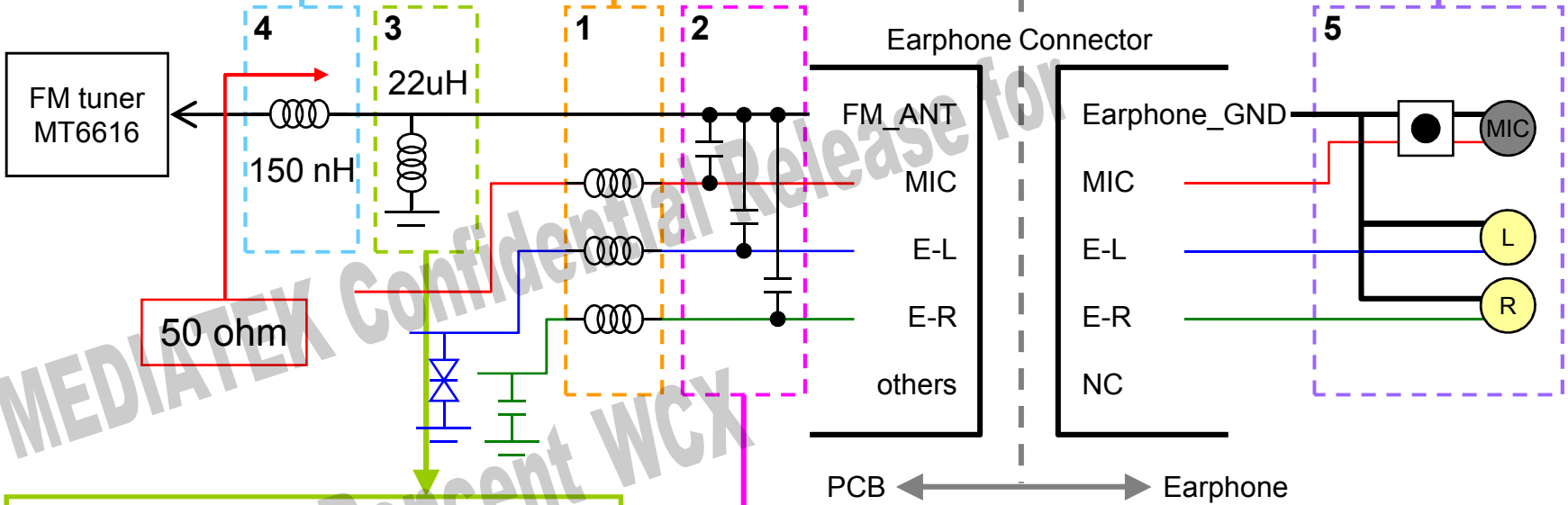
- On next page, there is an illustration to explain the respective purposes of each components. It can help customers to know how to enhance FM wireless performance.
- Besides FM schematics, wrong earphone pin definition also destroys FM wireless performance.
- Notice that the only one path from Earphone_GND to PCB_GND is via FM_ANT Pin and 22uH. If there are another paths existing, FM receiving signal would degrade seriously. **This issues frequently happens on customers' projects.**
- Four pins are enough on earphone including R, L, MIC, and Earphone_GND.
- Only Earphone_GND can be used as FM Antenna.
- Place all FM related components near earphone jack in PCB layout.

Illustration of FM Earphone Antenna (2/2)

4. 150 nH
   Earphone antenna matching

1. Serial Beads 2.5 kOhm @100MHz
   Avoid FM signal loss through R, L, and MIC traces.

5. Earphone length
   165 cm is recommended.

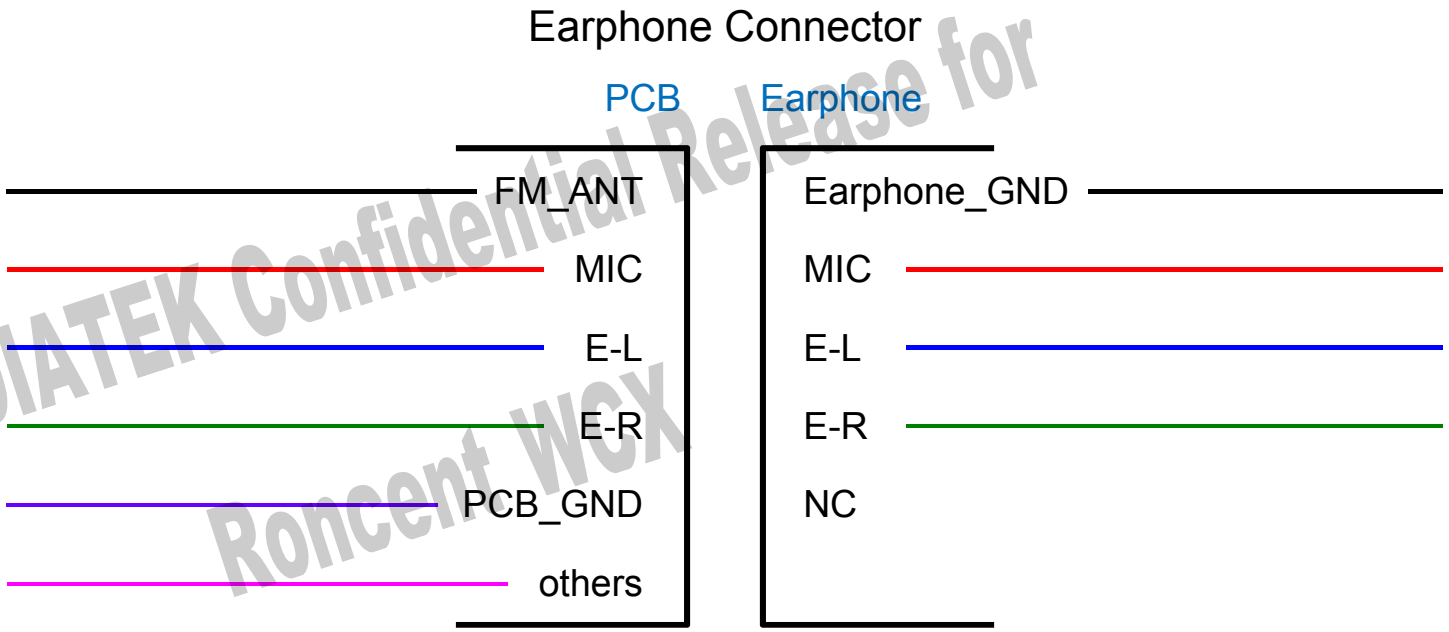


3. 22 uH
   - Earphone GND connects to PCB GND only via this 22 uH.
   - RF choke @100MHz

2. Parallel 1.0 nF CAP_short @100MHz
   Conduct FM signal to FM input from R, L, and MIC traces. FM receiving signal can be enhanced.

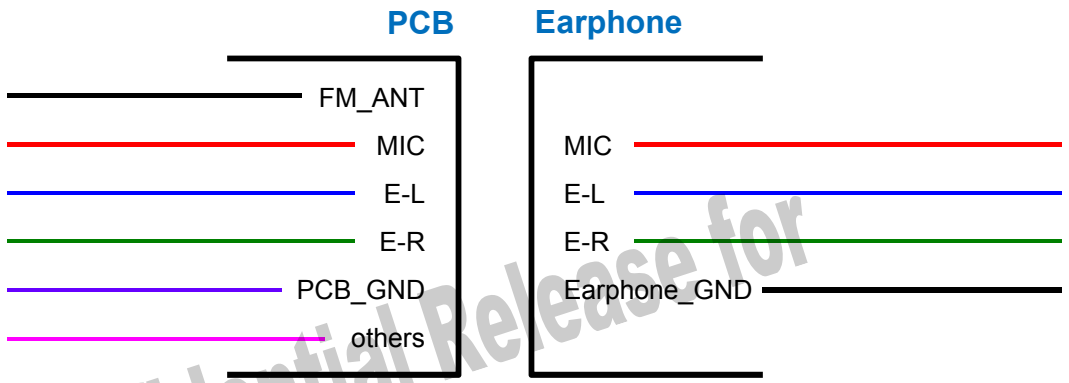
FM Earphone Antenna Pin Definition (1/3)

- The following illustrates the correct pin definition for the FM earphone antenna:

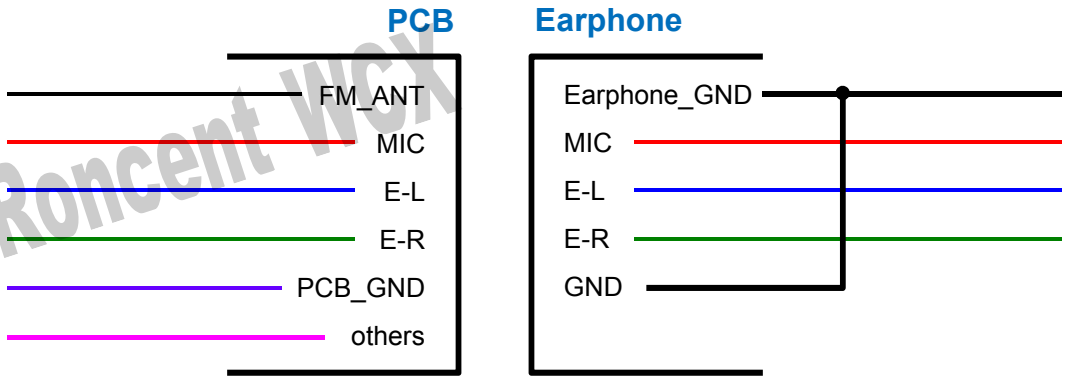


FM Earphone Antenna Pin Definition (2/3)

- Some **incorrect** pin definitions
  - Case 1: Floating FM_ANT pin

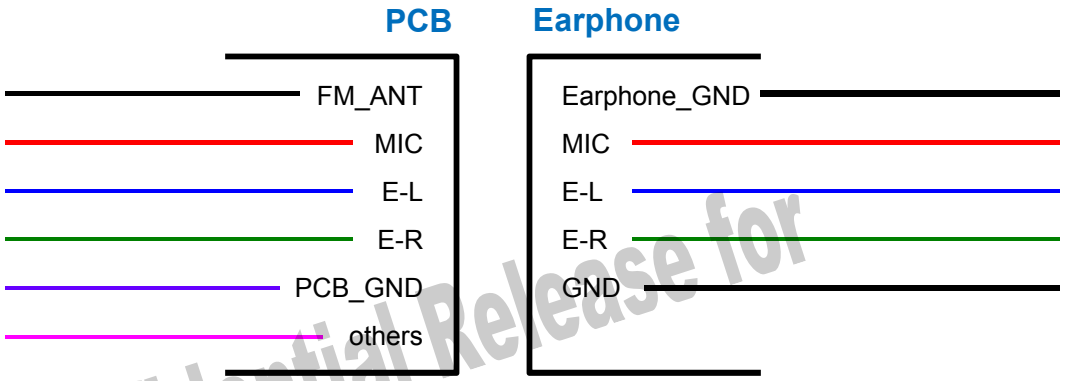


  - Case 2: Earphone_GND connects to both FM_ANT pin and PCB_GND

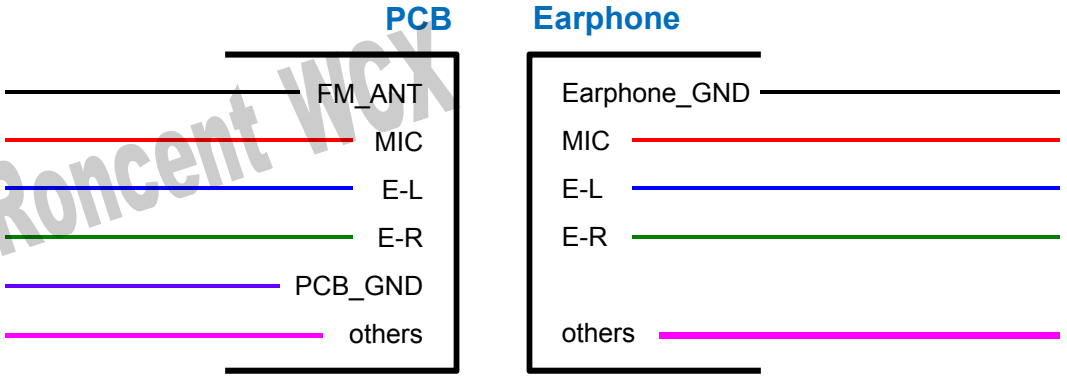


FM Earphone Antenna Pin Definition (3/3)

- Some incorrect pin definitions
  - Case 3: Unnecessary GND pin used on the earphone side



  - Case 4: Unnecessary signal pins used on the earphone side



FM Earphone Antenna Troubleshooting

- Simple troubleshooting techniques:
  a. Check that only four earphone pins are used. (Case 3, Case 4)
  b. Remove the 22 uH inductor.
  c. Plug in the earphone.
  d. Use a digital multimeter to check whether the connections between **PCB_GND**, **FM_ANT** pin, and **Earphone_GND** pin are **OPEN** or **SHORT**.

FM_ANT to Earphone_GND	FM_ANT to PCB_GND	PCB_GND to Earphone_GND	Issue
SHORT	OPEN	OPEN	Correct
OPEN	OPEN	SHORT	Case 1
SHORT	SHORT	SHORT	Case 2

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MEDIATEK

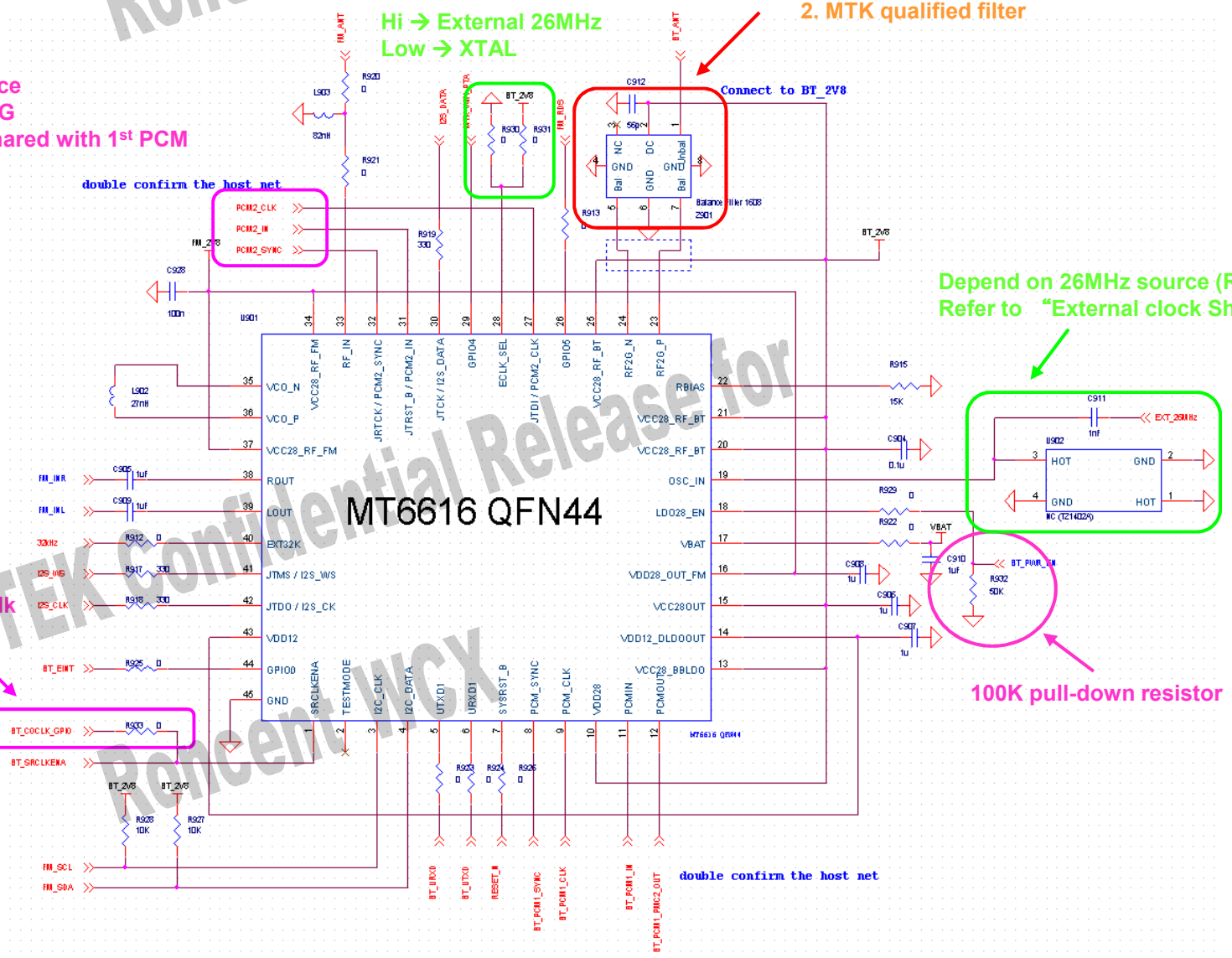
MT6616 Design Guide - Bluetooth

Reference Circuit – MT6616 BT

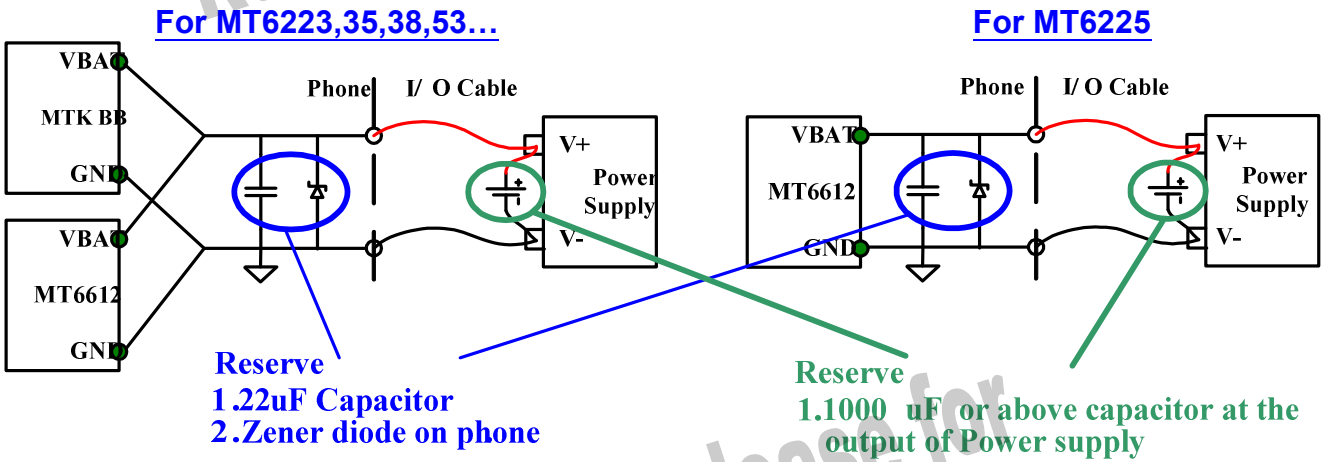
1. [Important!!] Must close to MT6616 IC!!
2. MTK qualified filter

Hi → External 26MHz
Low → XTAL

2nd PCM interface
- MUX with JTAG
- PCMOUT is shared with 1st PCM



MT6616 Reference Design – Power Protection



Because VBAT is directly applied, battery voltage protection should be applied:

Design notice in Phone side:

1. Add 22uF capacitor.
2. Add Zener diode (5.6V) to protect the IC against low frequency voltage surge. Put it between battery connector and MT6612.

Notice: If using IO connector or test point to supply VBAT for download, manufacture, or repair, should let VBAT trace passing zener diode and 22uF capacitor before entering IC.

Notice: Using 5.6V zener will introduce some leakage when VBAT = 4.2V.
ex. 5.6V zener CZRU52C5V6, will have extra 5uA leakage.

•Design notice in Power Supply side:

Add 1000uF (or above) capacitor at the output of the power supply to reduce the voltage bounce caused by long power cable. And the power cable should be as short as possible. Also add 1000uF (or above) capacitor at the end of power cable (near phone side).

Baseband GPIO Assignment for MT6616 (1/2)

- **BT/Baseband Interface assignment**
  - In the BT/BB interface assign phase, the GPIO should be arranged carefully. Do not use GPIO with conflict power domain (for example, camera power domain).
  - Example:

AD17	URXD2	VDD33_NORM2	VSS33_NORM2	VDDK	VSSK	
U16	SYSRST_B	VDD33_NORM2	VSS33_NORM2	VDDK	VSSK	
AD18	URTS1	VDD33_NORM2	VSS33_NORM2	VDDK	VSSK	
T16	EINT0	VDD33_NORM2	VSS33_NORM2	VDDK	VSSK	
AD19	UCTS1	VDD33_NORM2	VSS33_NORM2	VDDK	VSSK	

Baseband GPIO Assignment for MT6616 (2/2)

– Reserve the default (hardware) pull-down GPIO to LDO28EN pin to avoid unwanted leakage.

GPIO +0400h	GPIO pull-up/pull-down select register 1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0: Default (after reset state) is pulled-down

GPIO +0440h	GPIO pull-up/pull-down select register 2															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24	GPIO23	GPIO22	GPIO21	PGIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	1

Do not use → 1: Default (after reset state) is pulled-high

Reference assignment

MT6616	MT6238	MT6235	MT6223	MT6229	Notes
LDO28EN	GPIO29	GPIO39	GPIO30	GPIO9	Do not use pulled-up GPIO!
EXT32K	GPIO77	GPIO27	GPIO21	GPIO36	

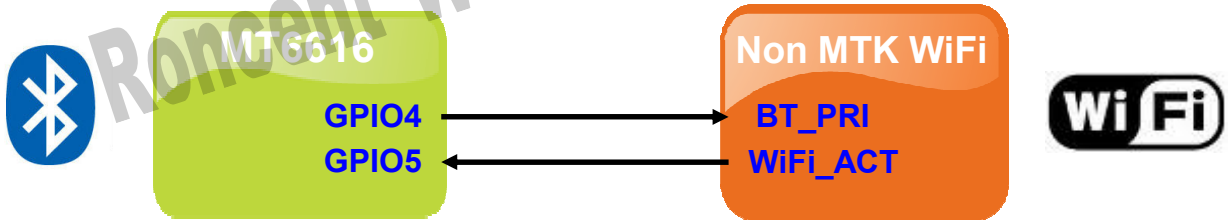
MT6616 PTA Interface

- MT6616 can support 1-wire PTA interconnection for MTK WiFi co-existence.

MT6616's GPIO for PTA	GPIO4	GPIO5 (FM_RDS)
MTK 1-Wire	V	
Standard 2-Wire	V	V

- For MTK WiFi chip:

- For non-MTK WiFi:



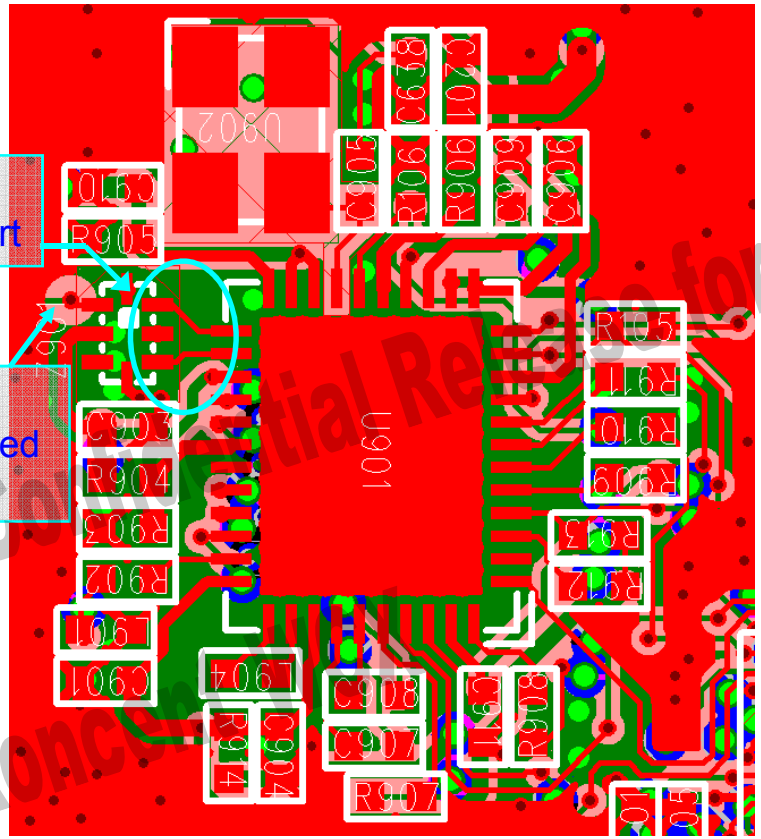
Dual-PCM for G+C Application

	MT6616 Pin number (QFN-44)	
	1st PCM	2nd PCM
CLK	9	27
SYNC	8	32
IN	11	31
OUT	12	12

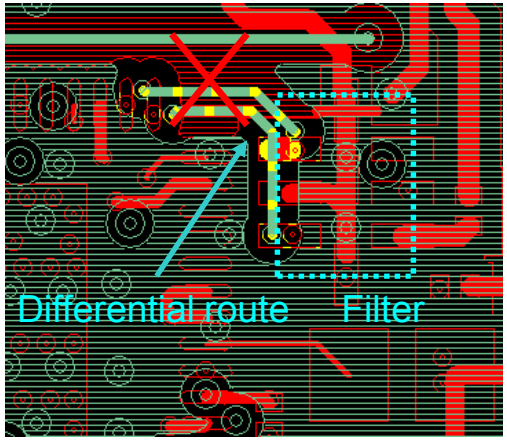
- PCMOUT is shared for 1st and 2nd PCM interface.
  - To prevent from leakage, VIO of PCM for G- and C- modem should be the same.
  - Reserve series-0Ω resistor on PCMOUT to C-network path.
- PCM format (CLK=128K, Short/Long sync, MSB/LSB, etc) setting should be same for G and C modem.
- GPIO configure should also be careful to prevent unwanted leakage.

BT Part Layout Guideline (1/2)

- **Layout criterion:**



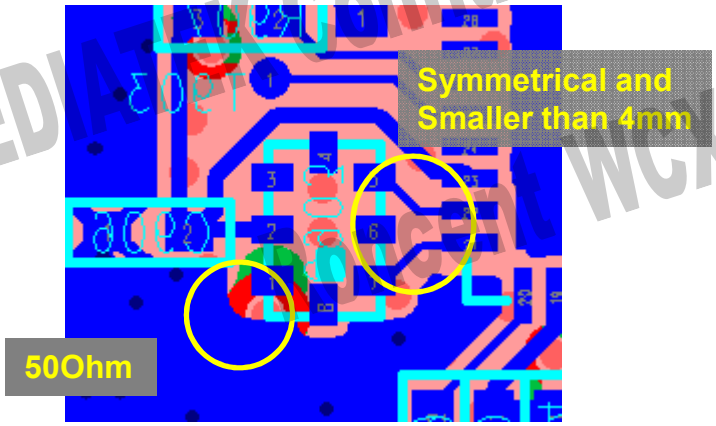
BAD design example:
→Differential trace not symmetrical and long.

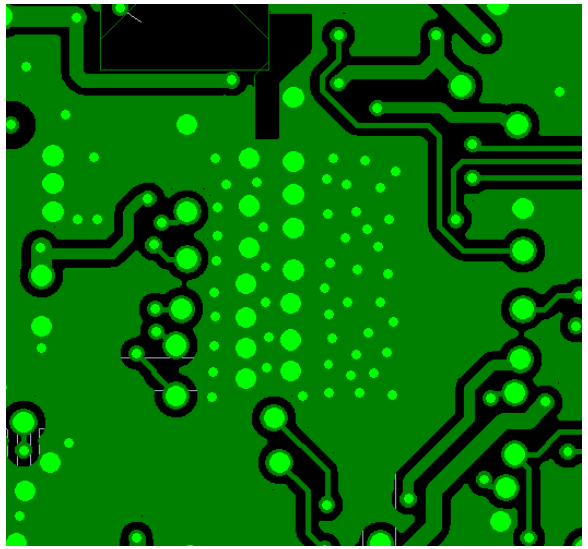


BT Part Layout Guideline (2/2)

- **RF/Analog part:**
  - Using qualified balance filter, need no external matching network.
  - Balance port routing should be symmetrical and shorter than 4mm, while the single-end trace route should keep 50Ω.
- **Power rail part:**
  - Make star-connection at C905 (pin-15) for 2.8V power trace.
  - Provide complete ground for power traces, do not route power traces in parallel with or crossing to digital or strong disturbance signals.
- **26MHz from RF:**
  - MUST be well shielded by ground.

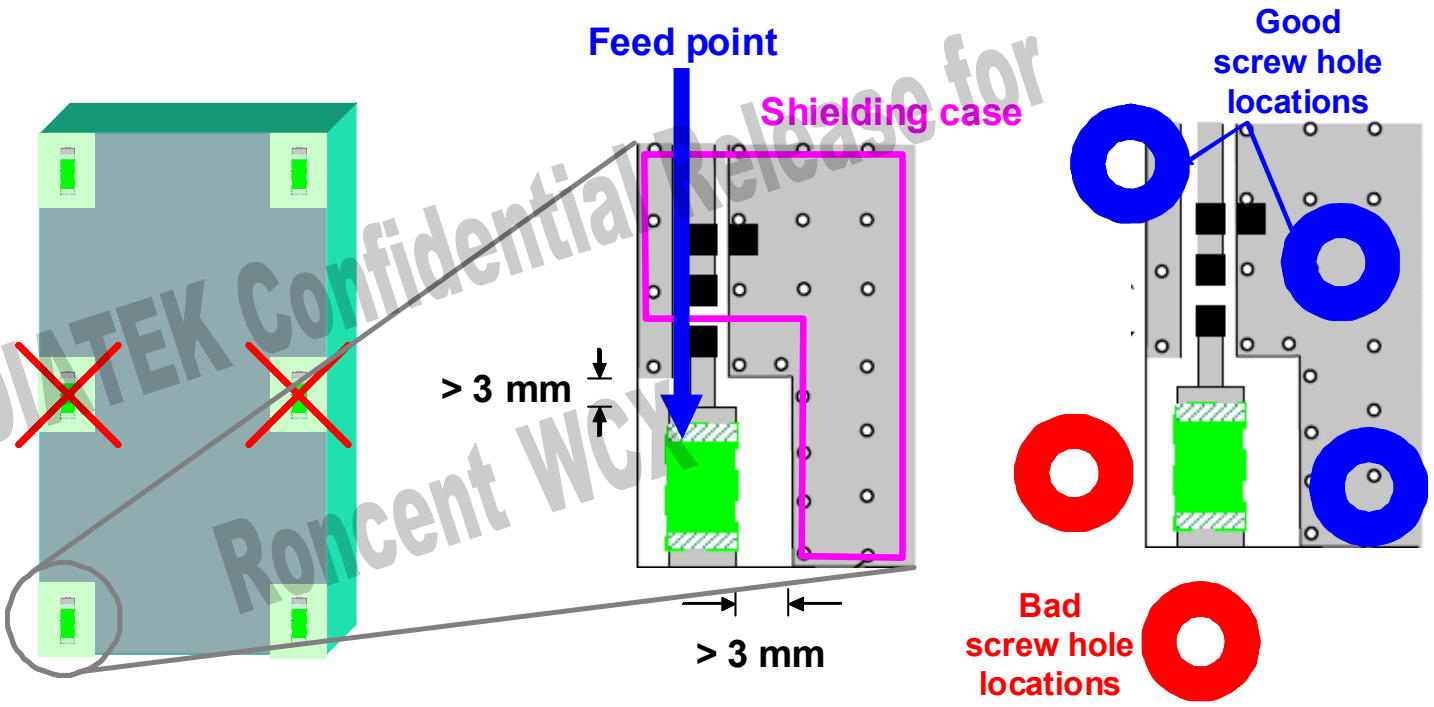
No separate ground plane but add more ground via.





BT Antenna Placement Guideline

- Place the BT antenna at the corner of the PCB.
- The feed point is directly connected to the antenna.
- Reserve enough distance between the antenna, ground and the shielding case.
- Ground blue screw holes, and don't ground red screw holes.



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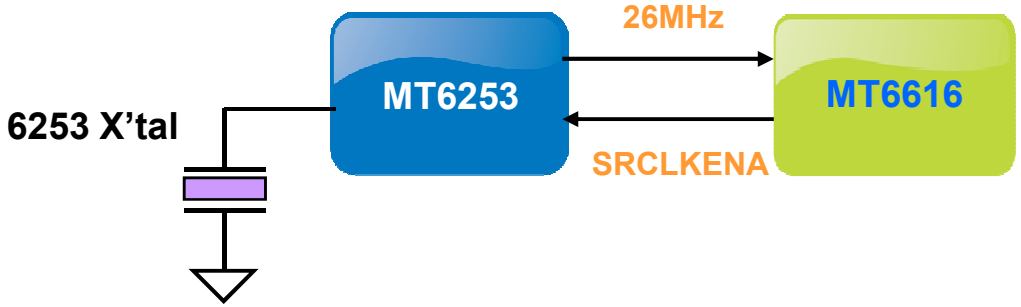
MEDIATEK

External Clock Sharing

External Clock Sharing

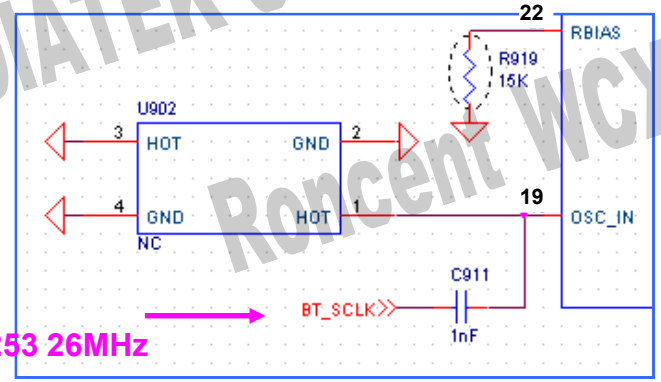
- MT6253
- AD6548
- MT6268+MT6160 (Othello-3)

Shared External Clock – MT6253 (1/2)



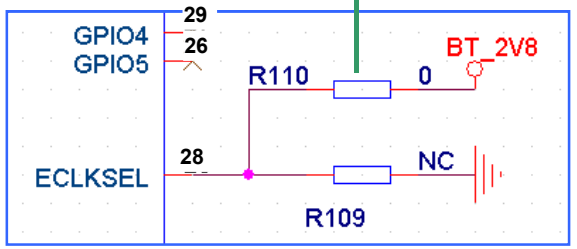
1. Reserve Xtal footprint for backup.
2. Reserve pull-up and pull-down resistor on ECLKSEL pin to select external or X'tal clock.

MT6616



Hi for external clock
Low for XTAL selection

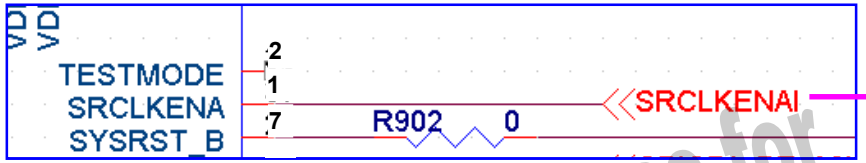
MT6616



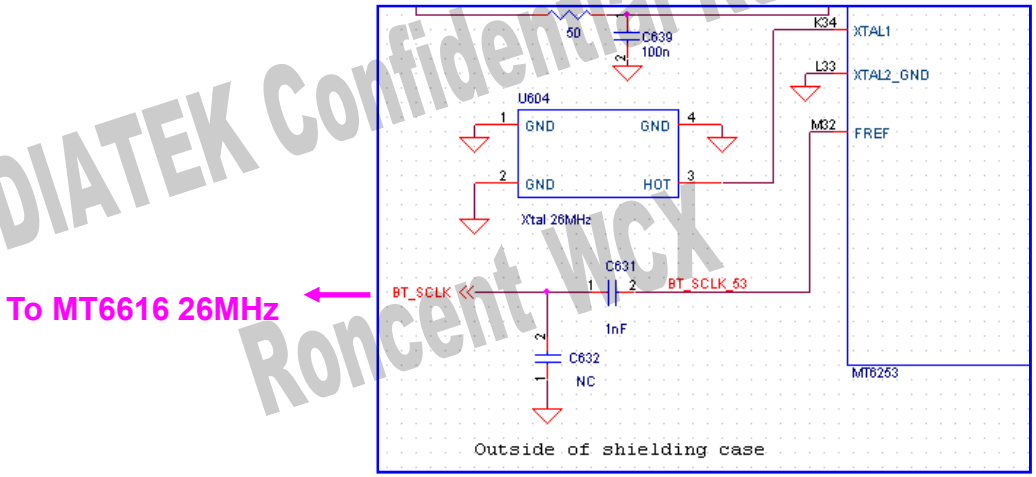
Shared External Clock – MT6253 (2/2)

3. Connect SRCLKENA (clock request) to MT6253's SRCLKENAI
4. Connect 26MHz output from MT6253 to 6616 via 1nF AC couple capacitor.

MT6616

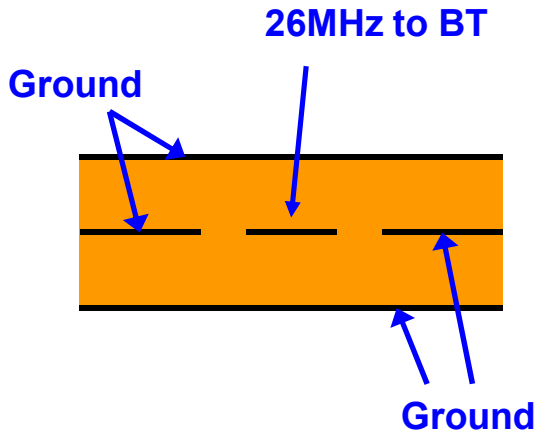


MT6253



Special Notes for MT6253 Co-clock Layout

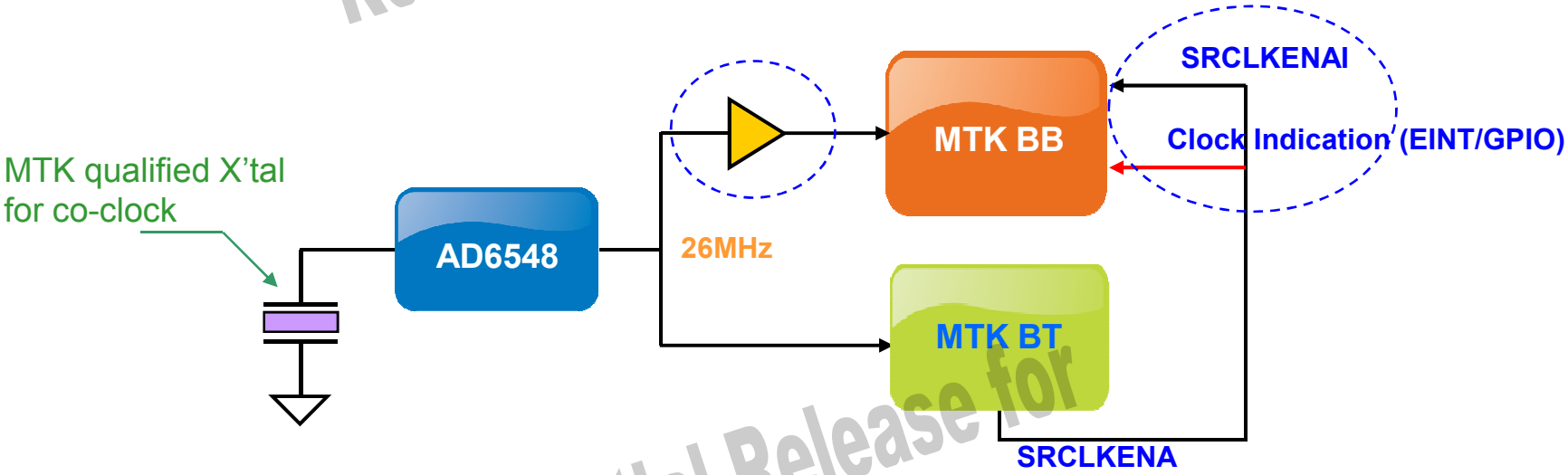
- Follow original design rule for MT6253 and BT if not mentioned.
- **BT close to RF transceiver ! (Highly recommended)**
- 26MHz trace routing rule
  - As short as possible
  - Good shielding with ground to avoid noise & coupling
- Using MTK recommended MT6253 Xtal.
- Reserve BT Xtal footprint



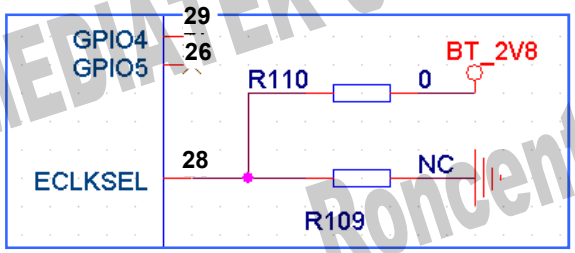
for MT6253+6616 co-clock

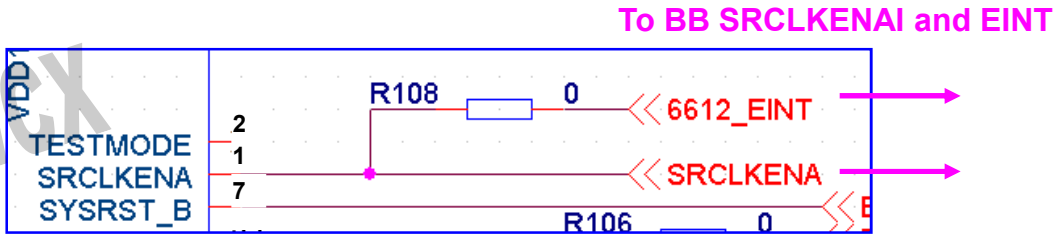
Reduce BT Xtal cost (0.13USD) without any effort!

Shared External Clock – AD6548 (1/3)



1. Reserve pull-up and pull-down resistor on ECLKSEL pin to select external or X'tal clock.





2. Connect SRCLKENA to BB's SRCLKENAI and EINT/GPIO (please follow the table for reference assignment)

Shared External Clock – AD6548 (2/3)

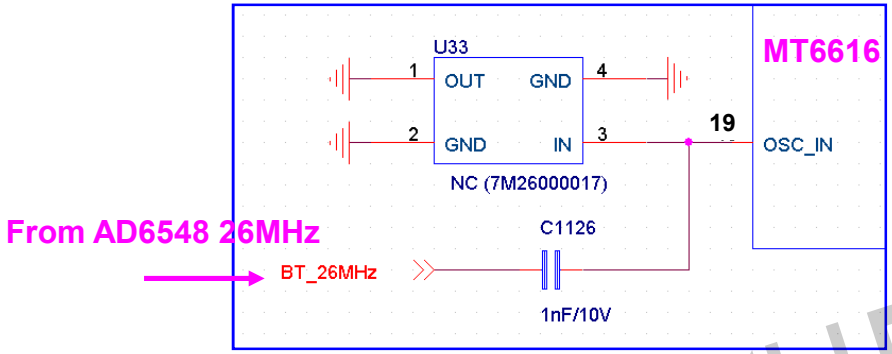
Assignment for Clock Indication (EINT/GPIO):

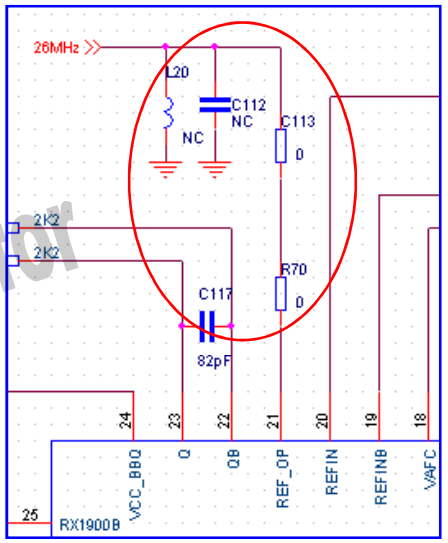
	EINT #	BB Pin	Pin Name	IO Power	GPIO MODE 0	GPIO MODE 1	GPIO MODE 2	GPIO MODE 3	Edge/Level Trigger	HW Debounce
MT6225	EINT4	T3	GPIO0	VDD33	GPIO0	----	----	EINT4	Edge/Level	Yes
	EINT5	U4	GPIO1	VDD33	GPIO1	----	----	EINT5	Edge/Level	Yes
	EINT6	T4	GPIO2	VDD33	GPIO2	----	UCTS1	EINT6	Edge/Level	Yes
	EINT7	U5	GPIO3	VDD33	GPIO3	BSI_RFIN	URTS1	EINT7	Edge/Level	Yes
MT6223	EINT2	C11	EINT2	VDD33	GPIO42	EINT2	MIRQ	----	Edge/Level	Yes
	EINT3	D11	EINT3	VDD33	GPIO43	EINT3	----	----	Edge/Level	Yes
	EINT4	R8	JTRST_B	VDD33	GPIO26	JTRST_B	EINT4	----	Edge/Level	Yes
	EINT5	P8	JTDI	VDD33	GPIO27	JTDI	EINT5	----	Edge/Level	Yes
	EINT6	T9	JTMS	VDD33	GPIO28	JTMS	EINT6	----	Edge/Level	Yes
MT6235	EINT3	E24	EINT3	VDD33	GPIO44	EINT3	DRF_DATA	IRQ2	Edge/Level	Yes
	EINT4	E23	EINT4	VDD33	GPIO45	EINT4	DRF_EN	CLKM3	Edge/Level	Yes
	EINT5	D23	EINT5	VDD33	GPIO46	EINT5	EDICK	----	Edge/Level	Yes
	EINT6	D25	EINT6	VDD33	GPIO47	EINT6	EDIWS	----	Edge/Level	Yes
	EINT7	D24	EINT7	VDD33	GPIO48	EINT7	EDIDAT	----	Edge/Level	Yes
MT6238	EINT0	T16	EINT0	VDD33_NORM2	GPIO77	EINT0	CLKM4	----	Edge/Level	Yes
	EINT1	AB17	EINT1	VDD33_NORM2	GPIO78	EINT1	CLKM5	----	Edge/Level	Yes
	EINT2	AC19	EINT2	VDD33_NORM2	GPIO79	EINT2	DSP_GPO3	TBTXEN	Edge/Level	Yes
	EINT3	AC25	EINT3	VDD33_NORM2	GPIO33	EINT3	DSP_GPO2	TBTXFS	Edge/Level	Yes
	EINT4	AD24	EINT4	VDD33_NORM2	GPIO34	EINT4	DSP_GPO1	TBRXEN	Edge/Level	Yes
	EINT5	T17	EINT5	VDD33_NORM2	GPIO35	EINT5	DSP_GPO0	TBRXFS	Edge/Level	Yes
	EINT6	AE18	EINT6	VDD33_NORM2	GPIO36	EINT6	EDIWS	----	Edge/Level	Yes
	EINT7	AC20	EINT7	VDD33_NORM2	GPIO37	EINT7	EDIDAT	----	Edge/Level	Yes

Shared External Clock – AD6548 (3/3)

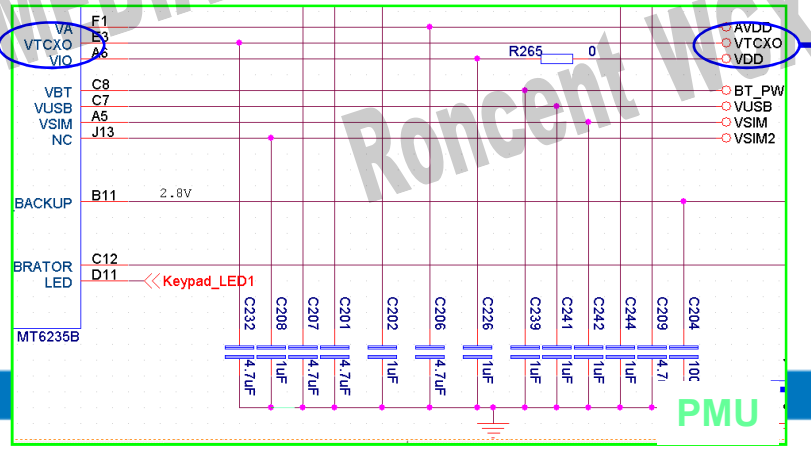
3. Please also reserve X'tal footprint for back-up.

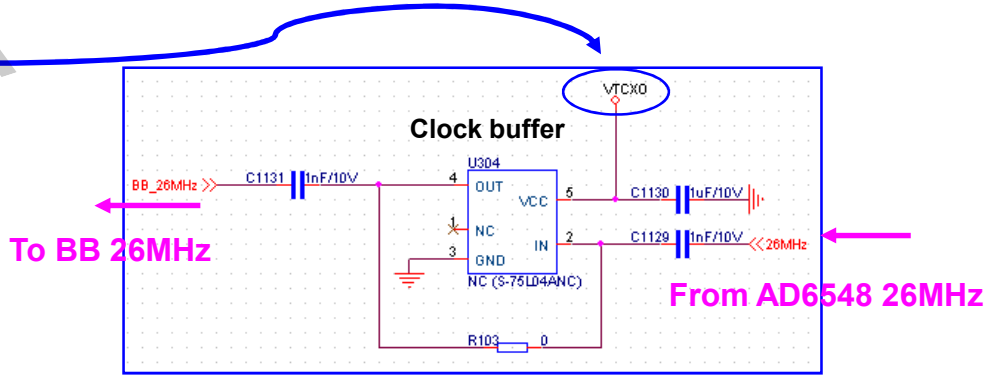
4. In AD6548 26MHz output, reserve LPF footprint and default use 0Ω connection.





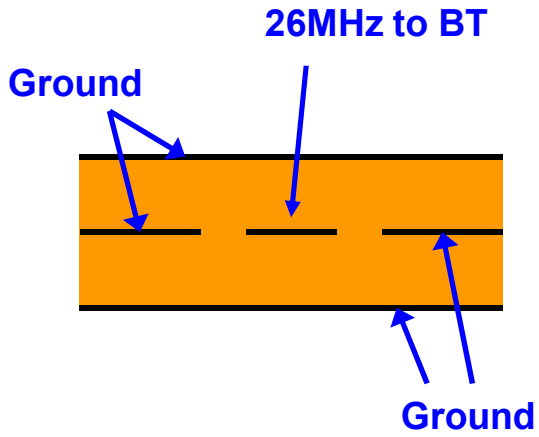
5. Place clock buffer on 26MHz to BB path and connect buffer power to VTCXO.





Special Notes for AD6548 Co-clock Layout

- Follow original design rule for OG and BT if not mentioned.
- **BT close to RF transceiver ! (Highly recommended)**
- 26MHz trace routing rule
  - As short as possible
  - Good shielding with ground to avoid noise & coupling
- Transceiver trace routing rule
  - Have VCXO power good decouple and clean ground.
- Using MTK recommended OG Xtal and clock buffer
- Reserve BT Xtal footprint

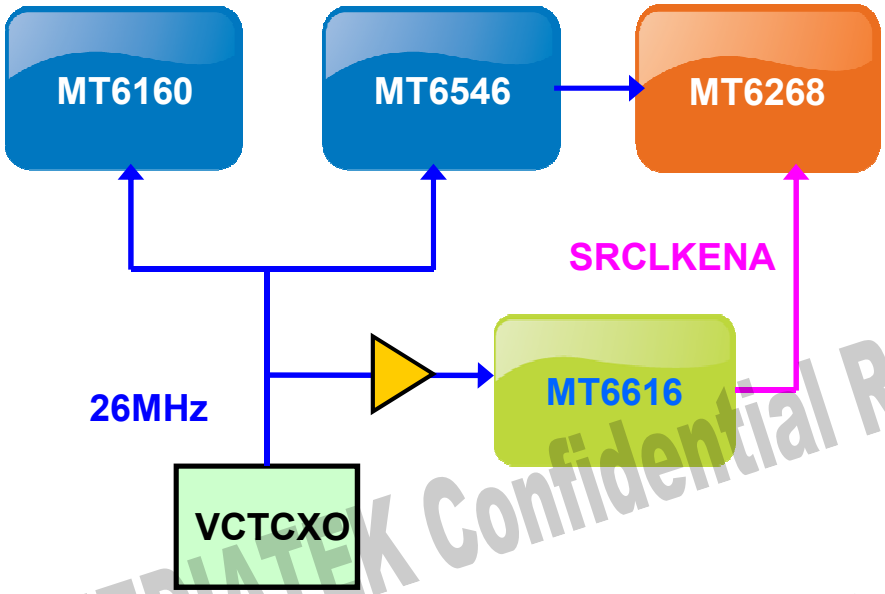


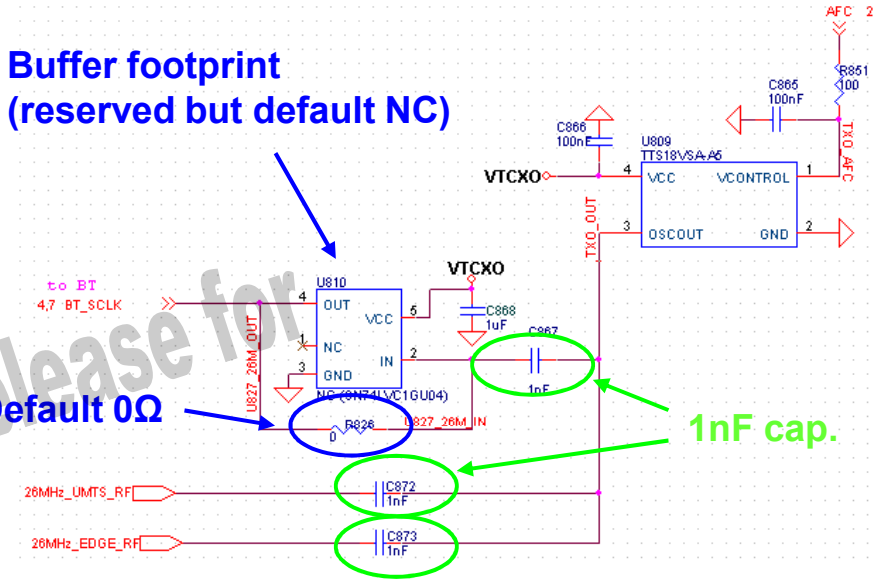
for AD6548+MT6612 co-clock only

Note that wake up BB cause additional 1mA idle current

Cost down 0.13USD

Shared External Clock – MT6268 (1/2)



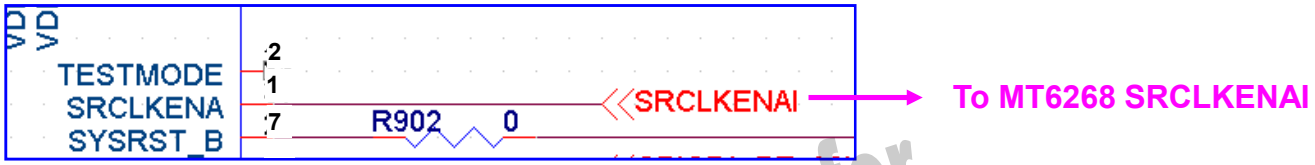


- Direct share VTCXO 26MHz output through 1nF AC couple cap.
- Reserve clock buffer footprint on BT path and default is 0Ω-through.

Shared External Clock – MT6268 (2/2)

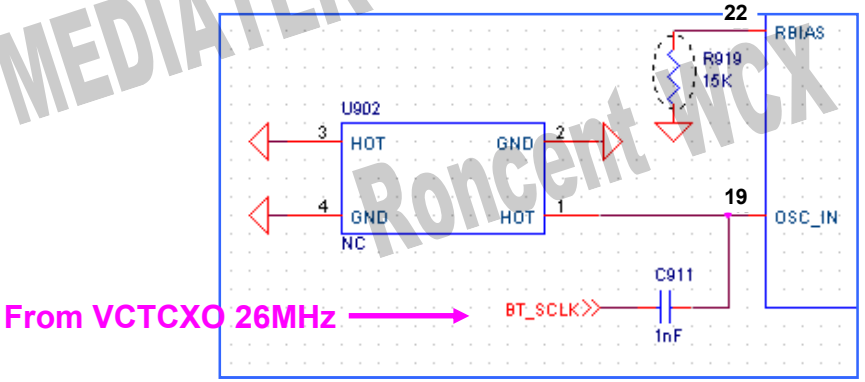
1. Connect SRCLKENA (clock request) to MT6268's SRCLKENAI
2. Connect 26MHz output from VCTCXO to 6612 via 1nF AC couple capacitor.

MT6616



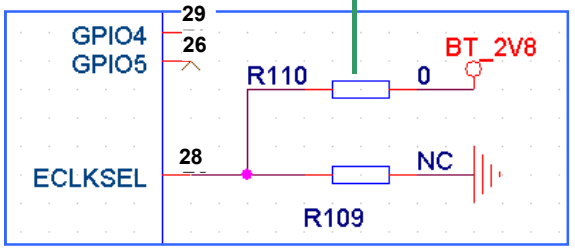
3. Reserve Xtal footprint for backup.
4. Reserve pull-up and pull-down resistor on ECLKSEL pin to select external or X'tal clock.

MT6616



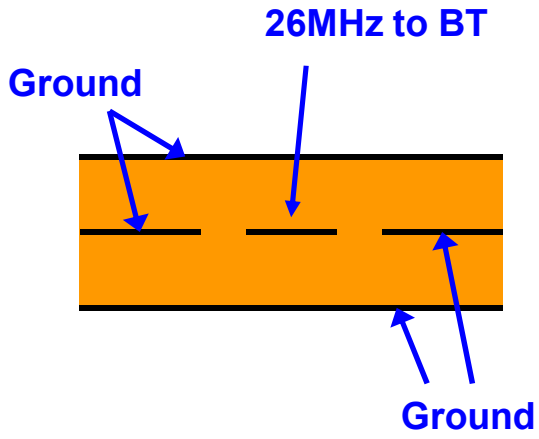
Hi for external clock
Low for XTAL selection

MT6616



Special Notes for MT6268 Co-clock Layout

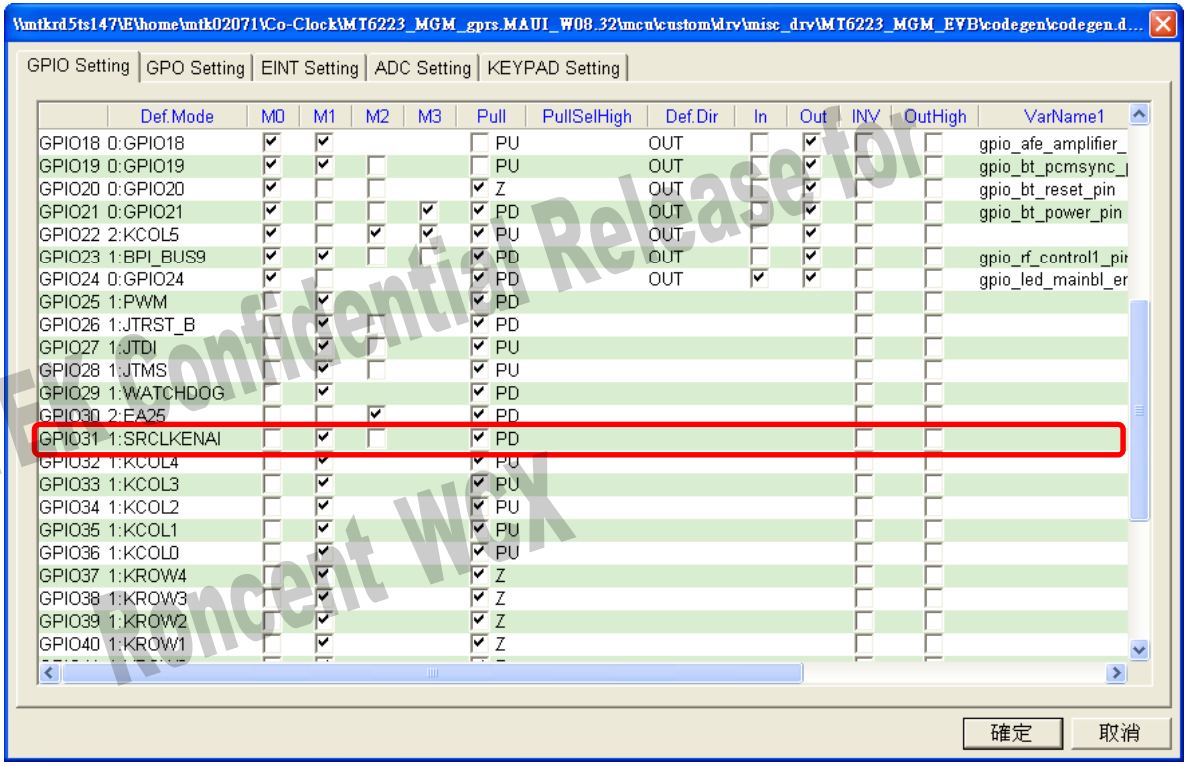
- Follow original design rule for MT6268 and BT if not mentioned.
- 26MHz trace routing to BT must **be surrounded by ground to have good shielding.**
- Reserve BT Xtal footprint.



Shared External Clock – SW Configuration (1/4)

Step 1 (for MT6253 AND AD6548). Use Drv tool in Custom folder to configure clock request input should be configured as SRCLKENAI mode.

MT6253 AND AD6548 AND MT6160



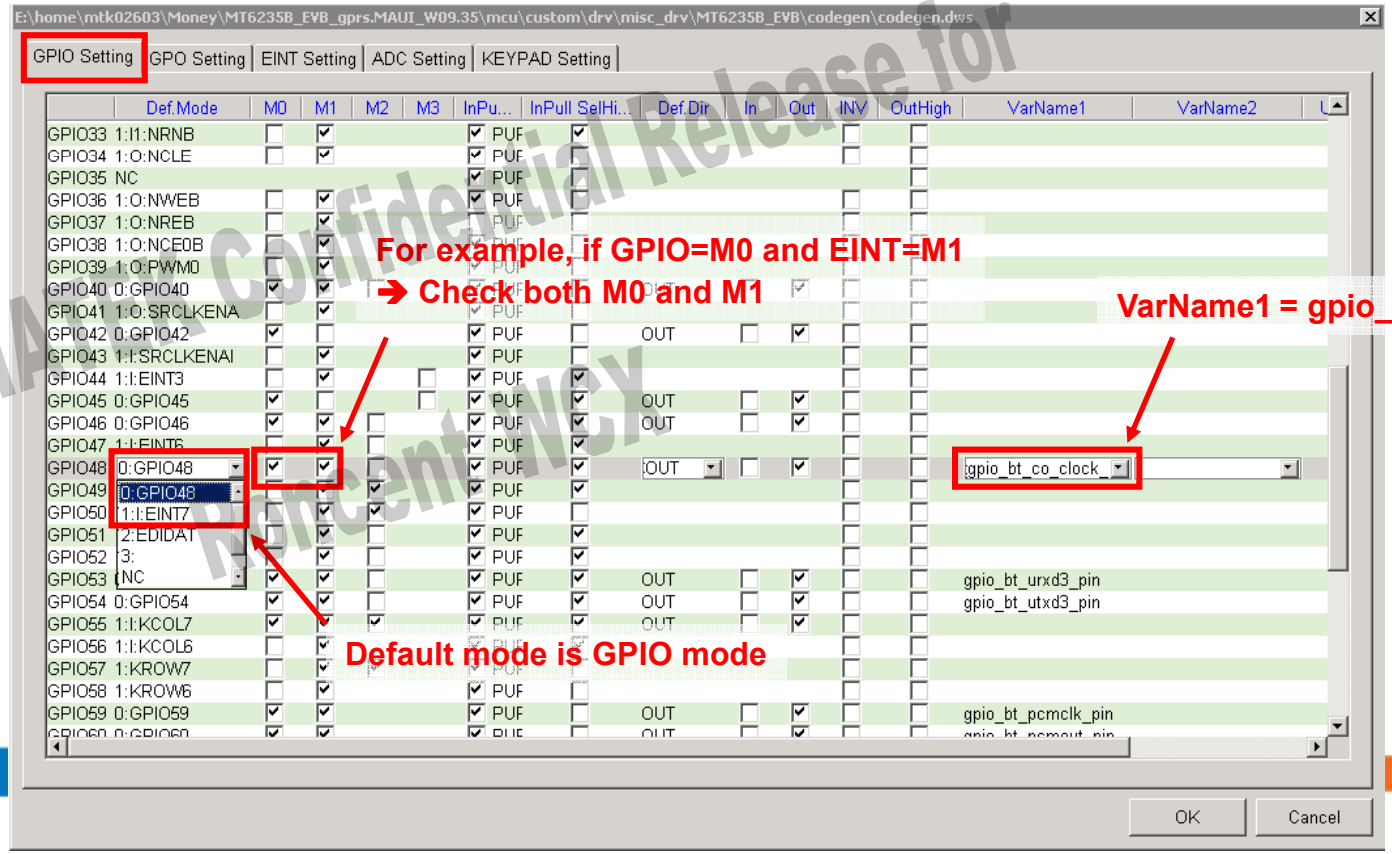
Shared External Clock – SW Configuration (2/4)

For AD6548 clock sharing, need more steps to configure:

AD6548 only

Step 2 (for AD6548). In GPIO setting page, set clock indication signal

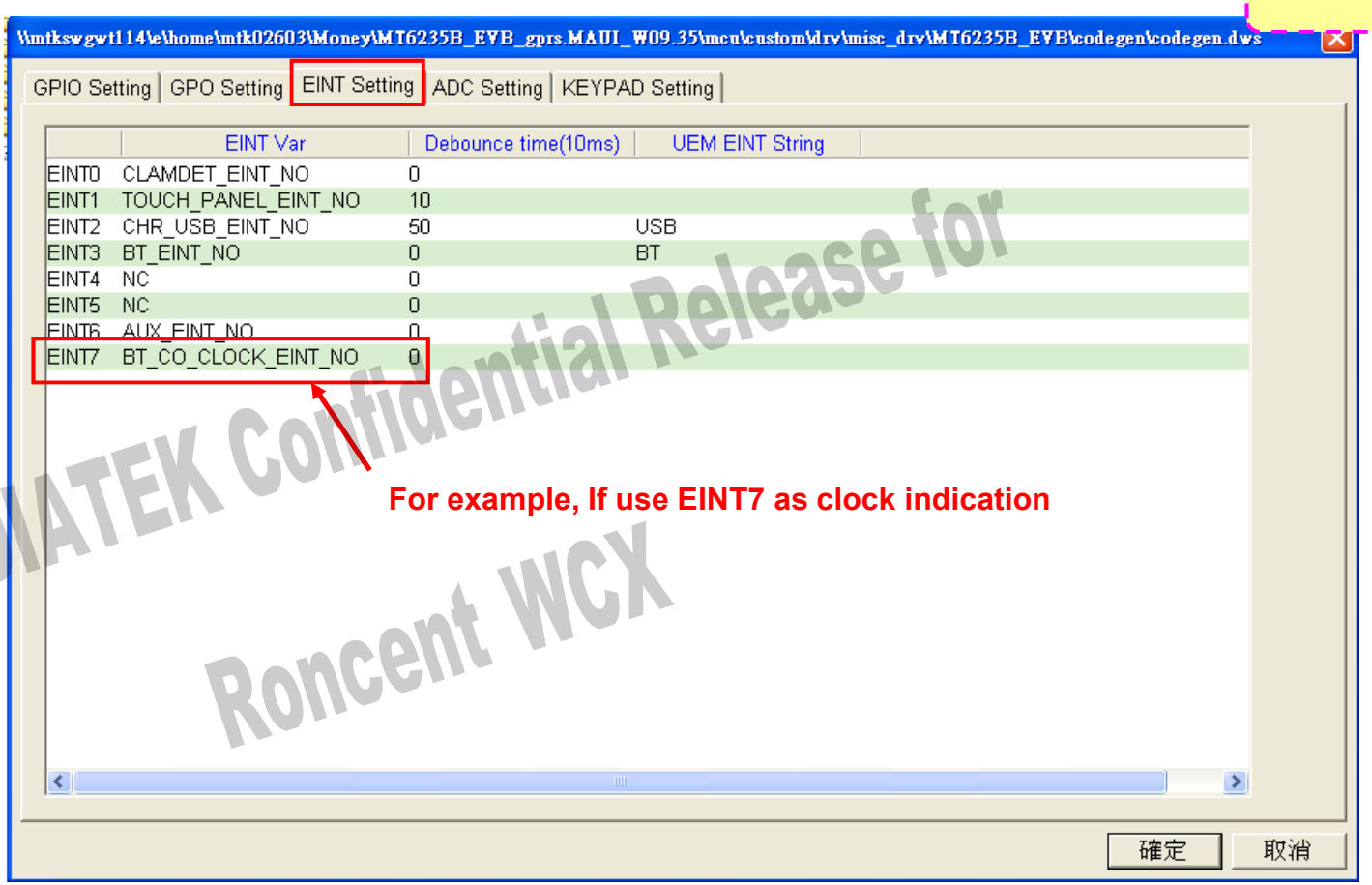
- → Def mode = GPIO
- → Check both GPIO and EINT mode (for example, if GPIO=M0 and EINT=M1 ➔ then check M0 and M1)
- → VarName1 = gpio_bt_co_clock



Shared External Clock – SW Configuration (3/4)

Step 3 (for AD6548). In EINT setting page, set the corresponding EINT Var as BT_CO_CLOCK_EINT_NO.

AD6548 only



Shared External Clock – SW Configuration (4/4)

Step 4 (for AD6548).

Modified IS_BT_COCLOCK_SUPPORT in the following .h file:

\mcu\custom\l1_rf\AD6548_CUSTOM\ l1d_custom_rf.h

as:

AD6548 only

```
/*AD6548*/ #define IS_BT_COCLOCK_SUPPORT 1
```

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