MT6750 LTE-A Smartphone Application Processor Functional Specification

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Document Revision History

Revision	Date	Author	Description
1.0	2015-11-17	Gene Yeh	First release
1.1	2015-12-09	WX Lin, CJ Jan	1. Updated ISP specification. 2. Updated pin description. 3. Updated EINT table.
1.2	2015-12-30	CJ Jan	1. Updated system configuration. 2. Updated POD logo. 3. Updated top marking. 4. Updated PDN table. 5. Updated power-on sequence. 6. Removed USB3.0 feature. 7. Updated image size of video snapshot. 8. Updated EMI bus clock frequency. 9. Updated GPU triangle rate and shader rate. 10. Updated MCU system bus frequency.
1.3	2016-02-15	CJ Jan	1. Modified pin description in Table 2-1, Table 2-3. 2. Modified Table 2-37 PDN specifications. 3. Added chapter 5.5 USB.

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Preface

Acronyms for register types

R/W	For both read and write access
RO	Read only
RC	Read only. After the register bank is read, every bit that is HIGH(1) will be cleared to LOW(0) automatically.
WO	Write only
W1S	Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be set to 1. Data bits that are LOW(0) have no effects on the corresponding bit.
W1C	Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be cleared to 0. Data bits that are LOW(0) have no effects on the corresponding bit.

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1 System Overview

The MT6750 device (see Figure 1-1), with integrated Bluetooth, FM, WLAN and GPS modules, is a highly integrated baseband platform incorporating both modem and application processing subsystems to enable LTE/LTE-A and C2K smart phone applications. The chip integrates ARM® Cortex-A53 operating up to 1.5GHz, an ARM® Cortex-R4 MCU and powerful multi-standard video codec. In addition, an extensive set of interfaces and connectivity peripherals are included to interface to cameras, touch-screen displays and MMC/SD cards.

The application processor, an Octa-core ARM® Cortex-A53 MPCore™ equipped with NEON engine offers processing power necessary to support the latest OpenOS along with its demanding applications such as web browsing, email, GPS navigation and games. All are viewed on a high resolution touch screen display with graphics enhanced by the 2D and 3D graphics acceleration.

The multi-standard video accelerator and an advanced audio subsystem are also integrated to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders.

ARM® Cortex-R4, DSP, and 2G and 3G coprocessors combined provide a powerful modem subsystem capable of supporting LTE Cat 6, Category 29 HSDPA downlink and Category 8 HSUPA uplink data rates, Category 14 TD-HSDPA downlink and Category 6 TD-HSUPA uplink, as well as Class 12 GPRS, EDGE.

MT6750 also embodies wireless communication device, including WLAN, Bluetooth and GPS. With four advanced radio technologies integrated into one single chip, MT6750 provides the best and most convenient connectivity solution in the industry.

The enhanced overall quality is achieved for simultaneous voice, data and audio/video transmission on mobile phones and Media Tablets. The small footprint with low-power consumption greatly reduces the PCB layout resource.

1.1 Highlighted Features Integrated in MT6750

- Quad-core ARM® Cortex-A53 MPCore™ operating at 1.5GHz and the other quad-core ARM® Cortex-A53 MPCore™ operating at 1.0GHz
- LPDDR3 up to 4GB, clock 650MHz (LPDDR3-1300)
- LTE Cat 6 (300Mps)
- Embedded connectivity system including WLAN/BT/FM/GPS
- Resolution up to HD (1,280*720)
- OpenGL ES 3.0 3D graphic accelerator
- ISP supports 16MP@30fps.
- HEVC 1080p @ 30fps decoder
- H.264 1080p @ 30fps encoder
- Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)

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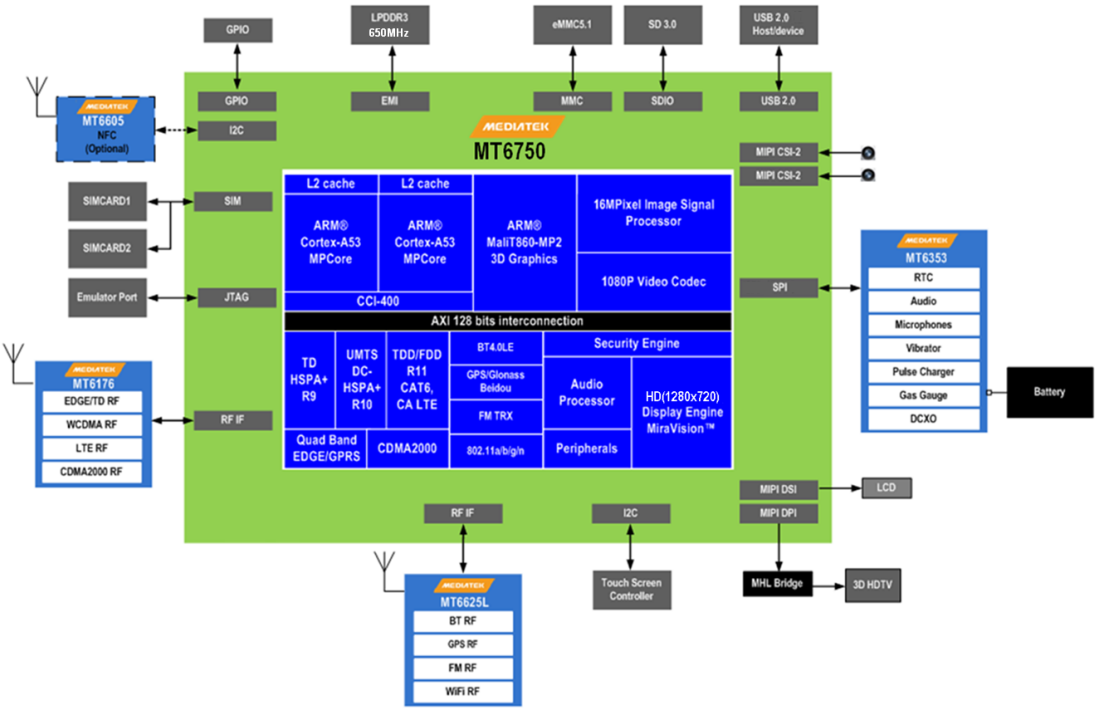

Figure 1-1. High-level MT6750 functional block diagram

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1.2 Platform Features

- **General**
  - Smartphone, two MCU subsystems architecture
  - eMMC boot support
  - Supports LPDDR-3

- **AP MCU subsystem**
  - Quad-core ARM® 1.5GHz Cortex-A53 MPCoreTM and another quad-core ARM® 1.0Ghz Cortex-A53 MPCoreTM
  - NEON multimedia processing engine with SIMDv2/VFPv4 ISA support
  - 32KB L1 I-cache and 32KB L1 D-cache for each cluster
  - 512KB L2 cache for each cluster
  - DVFS technology with adaptive operating voltage from 0.8V to 1.125V

- **MD MCU subsystem**
  - Two ARM® Cortex-R4 processors with max. 800MHz operation frequency
  - 64KB I-cache, 64KB D-cache
  - 512KB TCM (tightly-coupled memory)
  - Coresonic DSP for running LTE modem tasks
  - FD216 DSP for running modem/voice tasks, with max. 312MHz operation frequency
  - High-performance AXI and AHB bus
  - General DMA engine and dedicated DMA channels for peripheral data transfer
  - Watchdog timer for system error recovery
  - Power management for clock gating control

- **MD external interfaces**
  - Dual SIM/USIM interface
  - Interface pins with RF and radio-related peripherals (antenna tuner, PA, etc.)

- **Security**
  - ARM® TrustZone® Security

- **External memory interface**
  - LPDDR3 up to 4GB
  - Single channel with 32-bit data bus width
  - Memory clock up to 650MHz (LPDDR3-1300)
  - Self-refresh/partial self-refresh mode
  - Low-power operation
  - Programmable slew rate for memory controller's IO pads
  - Dual rank memory device
  - Advanced bandwidth arbitration control

- **Peripherals**
  - USB2.0 host mode
  - eMMC5.1
  - 2 UART for debugging and applications
  - 2 SPI masters for external devices
  - 5 I2C to control peripheral devices, e.g. CMOS image sensor, LCM or FM receiver module
  - Max. 3 PWM channels (depending on system configuration/IO usage)
  - I2S for connection with optional external hi-end audio codec
  - GPIOs
  - 3 sets of memory card controllers supporting SD/SDHC/MS/MSPRO/MMC and SDIO2.0/3.0 protocols

- **Operating conditions**
  - Core voltage: 0.9V/1.0V
  - I/O voltage: 1.8V/2.8V/3.3V
  - Memory: 1.2V
  - LCM interface: 1.8V
  - Clock source: 26MHz, 32.768kHz

- **Package**
  - Type: VFBGA
  - 13.0mm*13.4mm
  - Height: Max. 0.9mm

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- Ball count: 873 balls (not finalized)
- Ball pitch: 0.4mm

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1.3 Modem Features

- **LTE**
  - FDD/TDD Up to 300Mbps downlink, 50Mbps uplink
  - Downlink carrier aggregation (CA) ability; 1.4 to 20MHz RF bandwidth per component carrier (CC) and up to 2 CCs
  - 8*2 downlink SU-MIMO per component carrier
  - Downlink MU-MIMO per component carrier
  - Supports feICIC
  - Supports MBMS
  - Uplink CoMP ability

- **3G UMTS FDD supported features**
  - 3G modem supports most main features in 3GPP Release 7 and Release 8
  - CPC (DTX in CELL_DCH, UL DRX DL DRX), HS-SCCH-less, HS-DSCH
  - Dual cell operation
  - MAC-ehs
  - 2 DRX (receiver diversity) schemes in URA_PCH and CELL_PCH
  - Uplink Cat. 7 (16QAM), throughput up to 11.5Mbps
  - Downlink Cat. 24 (64QAM, dual-cell HSDPA), throughput up to 42.2Mbps
  - Fast dormancy
  - ETWS
  - Network selection enhancements

- **TD-SCDMA**
  - CDMA/HSDPA/HSUPA baseband
  - TD-SCDMA Bands 34, 39 & 40 and Quad band GSM/EDGE
  - Circuit-switched voice and data; packet-switched data
  - 384/384Kbps class in UL/DL for TD-SCDMA
  - TD-HSDPA: 2.8Mbps DL (Cat.14)
  - TD-HSUPA: 2.2Mbps UL (Cat.6)
  - F8/F9 ciphering/integrity protection

- **Radio interface and baseband front-end**
  - High dynamic range delta-sigma ADC converts the downlink analog I and Q signals to digital baseband.
  - 10-bit D/A converter for Automatic Power Control (APC)
  - Programmable radio Rx filter with adaptive gain control
  - Dedicated Rx filter for FB acquisition
  - Baseband Parallel Interface (BPI) with programmable driving strength
  - Supports multi-band

- **GSM modem and voice CODEC**
  - Dial tone generation
  - Noise reduction
  - Echo suppression
  - Advanced side-tone oscillation reduction
  - Digital side-tone generator with programmable gain
  - 2 programmable acoustic compensation filters
  - GSM quad vocoders for adaptive multi-rate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
  - GSM channel coding, equalization and A5/1, A5/2 and A5/3 ciphering
  - GPRS GEA1, GEA2 and GEA3 ciphering
  - Programmable GSM/GPRS/EDGE modem
  - Packet switched data with CS1/CS2/CS3/CS4 coding schemes
  - GSM circuit switch data
  - GPRS/EDGE Class 12
  - Supports SAIC (Single Antenna Interference Cancellation) technology
  - VAMOS (Voice services over Adaptive Multi-user channels on One Slot) technology in R9 spec

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- **CDMA2000 modem interfaces**
  - Supports CDMA2000 1xRTT (releases 0) and CDMA2000 HRPD/1xEV-DO Revision 0 and A
  - Supports maximum 1x data rates of 153.6kbps for forward and reverse links and DO data rates of 3.1Mbps for forward link and 1.8Mbps for reverse link
  - Hybrid operation between 1x and HRPD
  - Simultaneous Hybrid Dual Receiver (SHDR) support
  - Supports 1x Diversity
  - Supports SRLTE

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1.4 Connectivity Features

MT6750 includes four wireless connectivity functions:

- WLAN
- Bluetooth
- GPS
- FM Receiver

The RF parts of those four blocks are placed on chip MT6625. With four advanced radio technologies integrated on one chip, MT6750/MT6625 is the best and most convenient connectivity solution in the industry, implementing advanced and sophisticated Radio Coexistence algorithms and hardware mechanisms. It supports single antenna sharing among 2.4GHz Bluetooth, 2.4GHz/5GHz WLAN and 1.575GHz for GPS. The enhanced overall quality is achieved for simultaneous voice, data and audio/video transmission on mobile phones and Media Tablets. The small footprint with low-power consumption greatly reduces PCB layout resource. MT6750 also supports 802.11ac WLAN in advanced assorted with MT6630.

- **Supports integrated Wi-Fi/Bluetooth/GPS**
  - Single antenna for Bluetooth and WLAN/GPS/Bluetooth
  - Self calibration
  - Single TCXO and TMS for GPS, BT and WLAN
  - Best-in-class current consumption performance
  - Intelligent BT/WLAN coexistence scheme that goes beyond PTA signaling (e.g. transmit window and duration that take into account protocol exchange sequence, frequency, etc.)

- **Wi-Fi**
  - Dual-band (2.4GHz/5GHz) single stream 802.11 a/b/g/n MAC/BB/RF
  - 802.11 d/h/k compliant
  - Security: WFA WPA/WPA2 personal, WPS2.0, WAPI (hardware)
  - QoS: WFA WMM, WMM PS
  - 802.11n optional features: STBC, A-MPDU, Blk-Ack, RIFS, MCS Feedback, 20/40MHz coexistence (PCO), unscheduled PSMP
  - Supports 802.11w protected managed frames
  - Supports Wi-Fi Direct (WFA P-2-P standard) and Wi-Fi Miracast (Wi-Fi Display)
  - Supports Wi-Fi HotSpot 2.0
  - Integrated 2.4GHz PA with max. 19dBm CCK output power and 5GHz PA with max. 17dBm OFDM 54Mbps output power
  - Typical Rx sensitivity with companion chip modem: -75dBm at 11g 54Mbps mode and -75.5dBm at 11a 54Mbps mode
  - Per packet TX power control

- **Bluetooth**
  - Bluetooth specification v2.1+EDR
  - Bluetooth specification 3.0+HS compliance
  - Bluetooth v4.0 Low Energy (LE)
  - Integrated PA with 6dBm (class 1) transmit power
  - Typical Rx sensitivity with companion chip modem: GFSK -92.5dBm, DQPSK -91.5dBm, 8-DPSK -86dBm
  - Best-in-class BT/Wi-Fi coexistence performance
  - Up to 4 piconets simultaneously with background inquiry/page scan
  - Supports Scatternet
  - Packet Loss Concealment (PLC) function for better voice quality

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  - Low-power scan function to reduce power consumption in scan modes

- **GPS**
  - Supports dual-band reception concurrently
    - GPS/Galileo only (GPS only)
    - GPS/Galileo - GLONASS (G+G)
    - GPS/Beidou (G+B)
  - Supports SBAS (Satellite-Based Augmentation Systems): WAAS/MSAS/EGNOS/GAGAN
  - Best-in-class sensitivity performance
    - -165 dBm tracking sensitivity
    - -163 dBm hot start sensitivity
    - -148 dBm cold start sensitivity
    - -151 dBm warm start sensitivity
  - AGPS sensitivity is 6dB design margin over 3GPP
  - Full A-GPS capability (E911/SUPL/EPO/HotStill)
  - Active interference cancellation for up to 12 in-band tones
  - Supports both TCXO and TMS (Thermister Crystal) clock source
  - 5Hz update rate

- **FM**
  - 65-108MHz with 50kHz step
  - RDS/RBDS
  - Digital stereo demodulator
  - Simplified digital audio interface (I2S)
  - Stereo noise reduction
  - Audio sensitivity 2dBμVemf (SINAD=26dB)
  - Audio SINAD 60dB
  - Anti-jamming
  - Integrated short antenna

- **WBT IPD**
  - Integrated matching network, balance band-pass filter, GPS-WBT diplexer
  - Fully integrated in one IPD die
  - Single and dual antenna operation

- **GPS IPD**
  - Integrated high-pass type matching network and 5th-order ellipse low-pass filter
  - Fully integrated in one IPD die
  - Single and dual antenna operation

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1.5 Multimedia Features

- **Display**
  - Portrait panel resolution up to HD (1,280*720)
  - MIPI DSI interface (4 data lanes)
  - MiraVisionTM for picture quality enhancement
  - Embedded LCD gamma correction
  - True colors
  - 12 overlay layers with per-pixel alpha channel and gamma table
  - Spatial and temporal dithering
  - Side-by-side format output to stereo 3D panel in both portrait and landscape modes
  - Color enhancement
  - Adaptive contrast enhancement
  - Image/video/graphic sharpness enhancement
  - Dynamic backlight scaling
  - Wide gamut

- **Graphics**
  - OpenGL ES 3.1/3.0/2.0/1.1 3D graphic accelerator capable of processing 130M tri/sec and 1,040M pixel/sec @ 520MHz
  - OpenCL ES 1.1 full profile

- **Image**
  - Integrated image signal processor supports 16MP@30fps.
  - Electronic image stabilization
  - Video stabilization
  - Preference color adjustment
  - Noise reduction
  - Multiple frame noise reduction for image capture
  - Temporal noise reduction for video recording
  - Lens shading correction
  - Auto sensor defect pixel correction
  - Supports AE/AWB/AF
  - Edge enhancement (sharpness)
  - Face detection and visual tracking
  - Video face beautification
  - Zero shutter delay image capture
  - Captures video size image when recording video
  - 2 MIPI CSI-2 high-speed camera serial interfaces; both are 4 data lane
  - PIP (picture in picture)
  - Hardware JPEG encoder: Baseline encoding with 130M pixel/sec Continuous shot with 100M pixel/sec
  - Supports YUV422/YUV420 color format and EXIF/JFIF format

- **Video**
  - HEVC decoder 1080p @ 30fps/40Mbps
  - VP9 decoder 1080p @ 30fps/40Mbps
  - H.264 decoder: Baseline 1080p @ 30fps/40Mbps
  - H.264 decoder: Main/high profile 1080p @30fps/40Mbps
  - Sorenson H.263/H.263 decoder: 1080p @ 30fps/40Mbps
  - MPEG-4 SP/ASP decoder: 1080p @ 30fps/40Mbps
  - DIVX4/DIVX5/DIVX6/DIVX HD/XVID decoder: 1080p @ 30fps/40Mbps
  - MPEG2 decoder 1080p @ 30fps/40Mbps
  - MPEG-4 encoder: Simple profile D1 @ 30fps
  - H.263 encoder: Simple profile D1 @ 30fps
  - H.264 encoder: High profile 1080p @ 30fps
  - HEVC encoder: Main profile 720p @ 30fps

- **Audio**
  - Audio content sampling rates supported: 8kHz to 192kHz
  - Audio content sample formats supported: 8-bit/16-bit/24-bit, Mono/Stereo
  - Interfaces supported: I2S, PCM

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  - External CODEC I2S interface supports 16-bit/24-bit, Mono/Stereo, 8kHz to 192kHz.
  - 4-band IIR compensation filter to enhance loudspeaker responses
  - Proprietary audio post-processing technologies: BesLoudness(MB-DRC), BesSurround, Android built-in post processing
  - Audio encoding: AMR-NB, AMR-WB, AAC, OGG, ADPCM
  - Audio decoding: WAV, MP3, MP2, AAC, AMR-NB, AMR-WB, MIDI, Vorbis, APE, AAC-plus v1, AAC-plus v2, FLAC, WMA, ADPCM

- **Speech**
  - Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)
  - CTM
  - Noise reduction
  - Noise suppression
  - Noise cancellation
  - Dual-MIC noise cancellation
  - Echo cancellation
  - Echo suppression
  - Dual-MIC voice tracking
  - Dual-MIC sound recording w/o Wind Noise Rejection
  - MagiLoudness (enhances the voice clarity based on near end environment noise)
  - MagiClarity (maximizes loudness while controlling the maximum receiver output power; feed-forward receiver protection)
  - Compensation filter and digital gain for both uplink and downlink paths

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1.6 General Description

MediaTek's MT6750 is a highly integrated LTE/LTE-A System-on-Chip (SoC) which incorporates advanced features, e.g. LTE cat.6, Octa HMP cores, 3D graphics (OpenGL|ES 3.1), 16M camera ISP, LPDDR3-1300, HD display and 1080p video codec. MT6750 helps phone manufacturers build high-performance LTE/LTE-A smart phones with PC-like browser, 3D gaming and cinema class home entertainment experiences.

The World-leading Technology!
Based on MediaTek's world-leading mobile chip SoC architecture with advanced 28nm process, MT6750 is the brand-new generation smart phone SoC integrating MediaTek LTE-A modem, Octa-core ARM® Cortex-A53 MPCore™, 3D graphics and high-definition 1080p video decoder.

Rich in Features, High-Value Product!
To enrich the camera features, MT6750 equips a 16M camera ISP with advanced features, e.g. auto focus, electrical stabilization, auto sensor defect pixel correction, continuous video AF, face detection, face beautify, burst shot, optical zoom, panorama view, picture in picture, video in video and video face beautification.

Incredible Browser Experience!
The powerful CPU architecture with NEON multimedia processing engine brings PC-like browser experiences while keeping low standby power. GPU supporting OpenGL|ES 3.1 also provides you with excellent multimedia experiences.

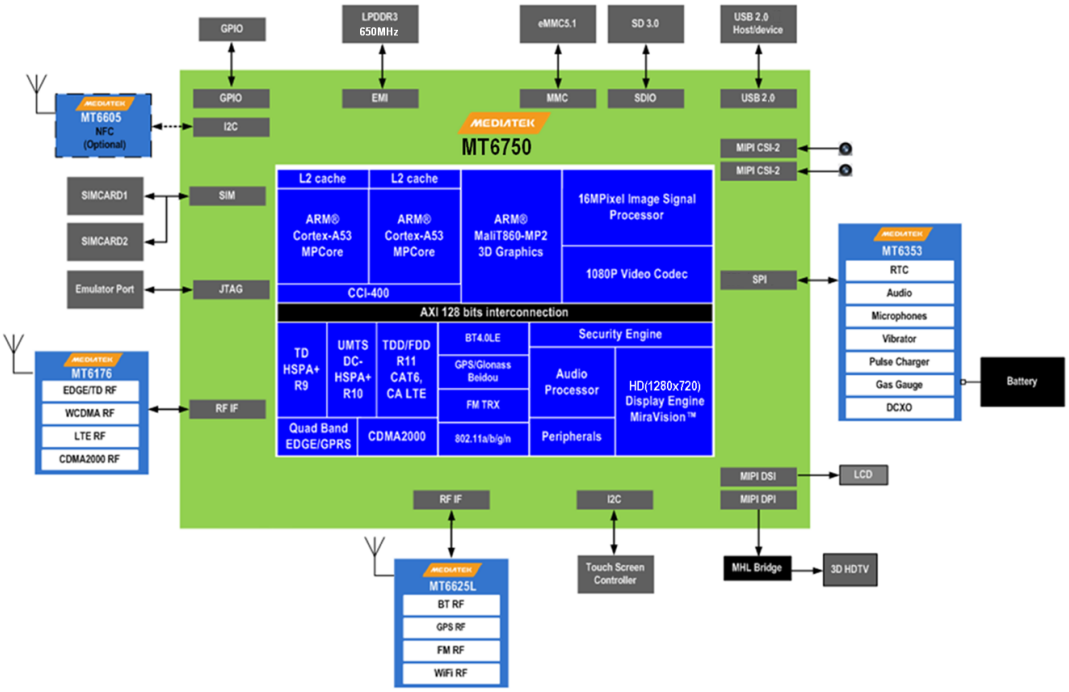

Figure 1-2. Block diagram of MT6750

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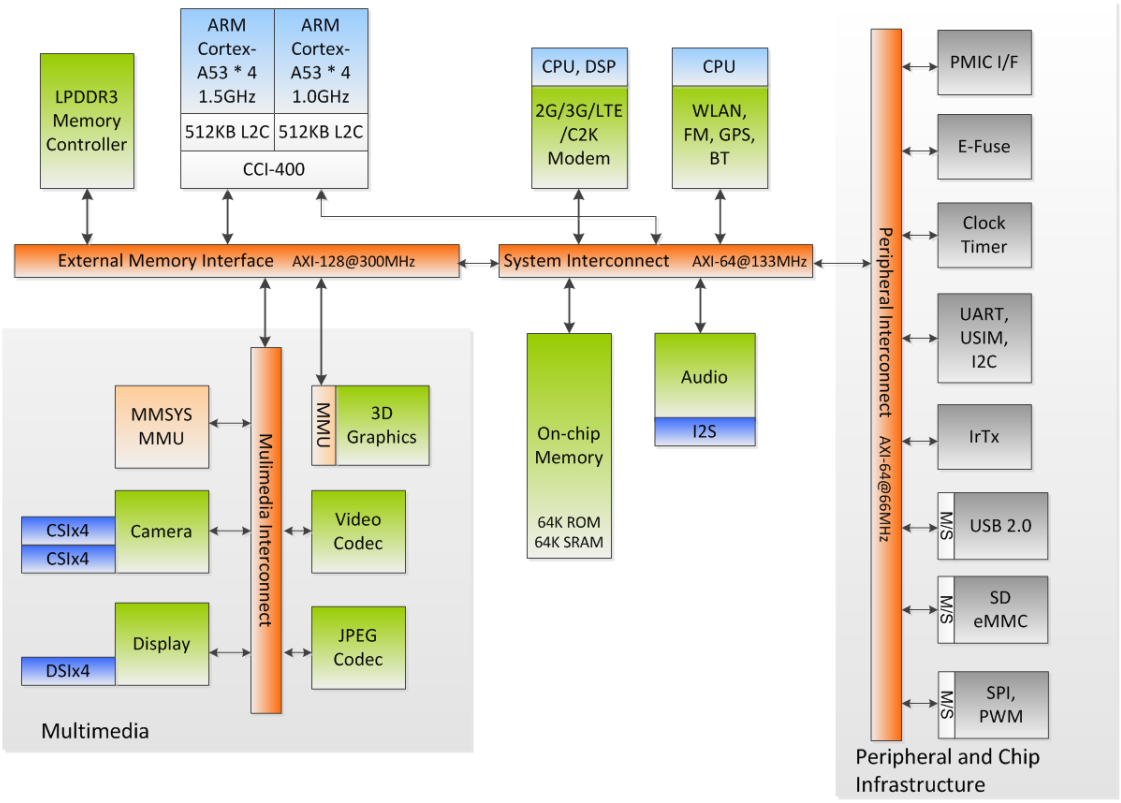

Figure 1-3. Bus structure of MT6750

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2 Product Description

2.1 Pin Description

2.1.1 Ball Map View

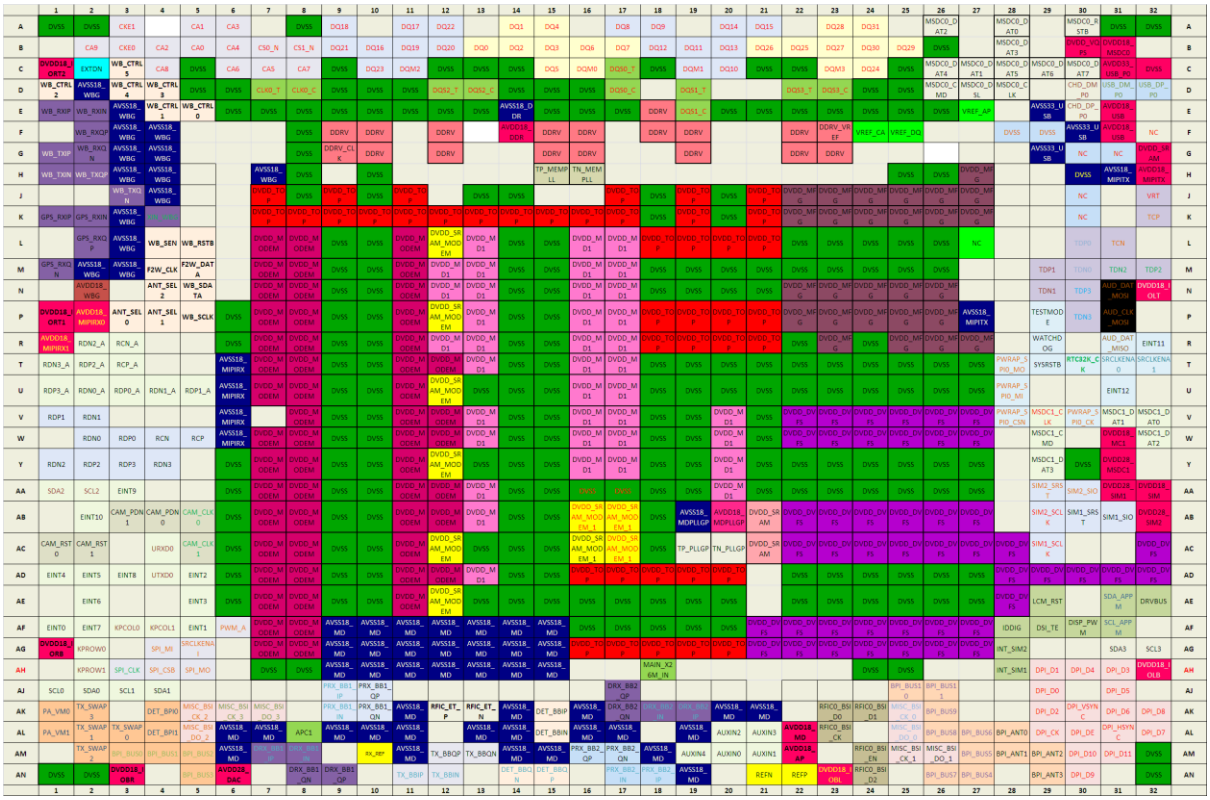

Figure 2-1. Ball map view

2.1.2 Pin Coordinate

Table 2-1. Pin coordinate

Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A1	DVSS	AL15	DET_BBIN	K32	TCP
A11	DQ17	AL16	AVSS18_MD	K4	XIN_WBG
A12	DQ22	AL17	AVSS18_MD	K7	DVDD_TOP
A14	DQ1	AL19	AVSS18_MD	K8	DVDD_TOP
A15	DQ4	AL2	TX_SWAP1	K9	DVDD_TOP
A17	DQ8	AL20	AUXIN2	L10	DVSS
A18	DQ9	AL21	AUXIN3	L11	DVDD_MODEM
A2	DVSS	AL22	AVDD18_MD	L12	DVDD_SRAM_MODEM
A20	DQ14	AL23	RFIC0_BSI_CK	L13	DVDD_MD1

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A21	DQ15	AL25	MISC_BSI_DO_0	L14	DVSS
A23	DQ28	AL26	BPI_BUS8	L15	DVSS
A24	DQ31	AL27	BPI_BUS6	L16	DVDD_MD1
A26	MSDC0_DAT2	AL28	BPI_ANT0	L17	DVDD_MD1
A28	MSDC0_DAT0	AL29	DPI_CK	L18	DVDD_TOP
A3	CKE1	AL3	TX_SWAP0	L19	DVDD_TOP
A30	MSDC0_RSTB	AL30	DPI_DE	L2	GPS_RXQP
A31	DVSS	AL31	DPI_HSYNC	L20	DVDD_TOP
A32	DVSS	AL32	DPI_D7	L21	DVDD_TOP
A5	CA1	AL4	DET_BPI1	L22	DVSS
A6	CA3	AL5	MISC_BSI_DO_2	L23	DVSS
A8	DVSS	AL6	AVSS18_MD	L24	DVSS
A9	DQ18	AL7	AVSS18_MD	L25	DVSS
AA1	SDA2	AL8	APC1	L26	DVSS
AA10	DVSS	AL9	AVSS18_MD	L27	NC
AA11	DVDD_MODEM	AM10	RX_REF	L3	AVSS18_WBG
AA12	DVDD_MODEM	AM11	AVSS18_MD	L30	TDP0
AA13	DVDD_MD1	AM12	TX_BBQP	L31	TCN
AA14	DVSS	AM13	TX_BBQN	L4	WB_SEN
AA15	DVSS	AM14	AVSS18_MD	L5	WB_RSTB
AA16	DVSS	AM15	AVSS18_MD	L7	DVDD_MODEM
AA17	DVSS	AM16	PRX_BB2_QP	L8	DVDD_MODEM
AA18	DVSS	AM17	PRX_BB2_QN	L9	DVSS
AA19	DVSS	AM18	AVSS18_MD	M1	GPS_RXQN
AA2	SCL2	AM19	AUXIN4	M10	DVSS
AA20	DVDD_MD1	AM2	TX_SWAP2	M11	DVDD_MODEM
AA21	DVSS	AM20	AUXIN0	M12	DVDD_MD1
AA22	DVSS	AM21	AUXIN1	M13	DVDD_MD1
AA23	DVSS	AM22	AVDD18_AP	M14	DVSS
AA24	DVSS	AM24	RFIC0_BSI_EN	M15	DVSS
AA25	DVSS	AM25	MISC_BSI_CK_1	M16	DVDD_MD1
AA26	DVSS	AM26	MISC_BSI_DO_1	M17	DVDD_MD1
AA27	DVSS	AM27	BPI_BUS5	M18	DVSS
AA29	SIM2_SRST	AM28	BPI_ANT1	M19	DVSS
AA3	EINT9	AM29	BPI_ANT2	M2	AVSS18_WBG
AA30	SIM2_SIO	AM3	BPI_BUS0	M20	DVSS
AA31	DVDD28_SIM1	AM30	DPI_D10	M21	DVSS
AA32	DVDD18_SIM	AM31	DPI_D11	M22	DVSS
AA6	DVSS	AM32	DVSS	M23	DVSS
AA7	DVDD_MODEM	AM4	BPI_BUS1	M24	DVSS
AA8	DVDD_MODEM	AM5	BPI_BUS2	M25	DVSS
AA9	DVSS	AM6	AVSS18_MD	M26	DVSS
AB10	DVSS	AM7	DRX_BB1_IP	M29	TDP1
AB11	DVDD_MODEM	AM8	DRX_BB1_IN	M3	AVSS18_WBG
AB12	DVDD_MODEM	AN1	DVSS	M30	TDN0
AB13	DVDD_MD1	AN11	TX_BBIP	M31	TDN2
AB14	DVSS	AN12	TX_BBIN	M32	TDP2
AB15	DVSS	AN14	DET_BBQN	M4	F2W_CLK
AB16	DVDD_SRAM_MODEM_1	AN15	DET_BBQP	M5	F2W_DATA
AB17	DVDD_SRAM_MODEM_1	AN17	PRX_BB2_IN	M7	DVDD_MODEM

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
AB18	DVSS	AN18	PRX_BB2_IP	M8	DVDD_MODEM
AB19	AVSS18_MDPLLGP	AN19	AVSS18_MD	M9	DVSS
AB2	EINT10	AN2	DVSS	N10	DVSS
AB20	AVDD18_MDPLLGP	AN21	REFN	N11	DVDD_MODEM
AB21	DVDD_SRAM	AN22	REFP	N12	DVDD_MD1
AB22	DVDD_DVFS	AN23	DVDD18_IOBL	N13	DVDD_MD1
AB23	DVDD_DVFS	AN24	RFIC0_BSI_D2	N14	DVSS
AB24	DVDD_DVFS	AN26	BPI_BUS7	N15	DVSS
AB25	DVDD_DVFS	AN27	BPI_BUS4	N16	DVDD_MD1
AB26	DVDD_DVFS	AN29	BPI_ANT3	N17	DVDD_MD1
AB27	DVDD_DVFS	AN3	DVDD18_IOBR	N18	DVSS
AB29	SIM2_SCLK	AN30	DPI_D9	N19	DVSS
AB3	CAM_PDN1	AN32	DVSS	N2	AVDD18_WBG
AB30	SIM1_SRST	AN5	BPI_BUS3	N20	DVSS
AB31	SIM1_SIO	AN6	AVDD28_DAC	N21	DVSS
AB32	DVDD28_SIM2	AN8	DRX_BB1_QN	N22	DVDD_MFG
AB4	CAM_PDN0	AN9	DRX_BB1_QP	N23	DVDD_MFG
AB5	CAM_CLK0	B10	DQ16	N24	DVDD_MFG
AB6	DVSS	B11	DQ19	N25	DVDD_MFG
AB7	DVDD_MODEM	B12	DQ20	N26	DVDD_MFG
AB8	DVDD_MODEM	B13	DQ0	N29	TDN1
AB9	DVSS	B14	DQ2	N30	TDP3
AC1	CAM_RST0	B15	DQ3	N31	AUD_DAT_MOSI
AC10	DVSS	B16	DQ6	N32	DVDD18_IOLT
AC11	DVDD_MODEM	B17	DQ7	N4	ANT_SEL2
AC12	DVDD_SRAM_MODEM	B18	DQ12	N5	WB_SDATA
AC13	DVSS	B19	DQ11	N7	DVDD_MODEM
AC14	DVSS	B2	CA9	N8	DVDD_MODEM
AC15	DVSS	B20	DQ13	N9	DVSS
AC16	DVDD_SRAM_MODEM_1	B21	DQ26	P1	DVDD18_IORT1
AC17	DVDD_SRAM_MODEM_1	B22	DQ25	P10	DVSS
AC18	DVSS	B23	DQ27	P11	DVDD_MODEM
AC19	TP_PLLGP	B24	DQ30	P12	DVDD_SRAM_MODEM
AC2	CAM_RST1	B25	DQ29	P13	DVDD_MD1
AC20	TN_PLLGP	B26	DVSS	P14	DVSS
AC21	DVDD_SRAM	B28	MSDC0_DAT3	P15	DVSS
AC22	DVDD_DVFS	B3	CKE0	P16	DVDD_MD1
AC23	DVDD_DVFS	B30	DVDD_VQPS	P17	DVDD_MD1
AC24	DVDD_DVFS	B31	DVDD18_MSDC0	P18	DVDD_TOP
AC25	DVDD_DVFS	B4	CA2	P19	DVDD_TOP
AC26	DVDD_DVFS	B5	CA0	P2	AVDD18_MIPIRX0
AC27	DVDD_DVFS	B6	CA4	P20	DVDD_TOP
AC28	DVDD_DVFS	B7	CS0_N	P21	DVDD_TOP
AC29	SIM1_SCLK	B8	CS1_N	P22	DVDD_MFG
AC32	DVDD_DVFS	B9	DQ21	P23	DVDD_MFG
AC4	URXD0	C1	DVDD18_IORT2	P24	DVDD_MFG
AC5	CAM_CLK1	C10	DQ23	P25	DVDD_MFG
AC6	DVSS	C11	DQM2	P26	DVDD_MFG
AC7	DVDD_MODEM	C12	DVSS	P27	AVSS18_MIPITX

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
AC8	DVDD_MODEM	C13	DVSS	P29	TESTMODE
AC9	DVSS	C14	DVSS	P3	ANT_SEL0
AD1	EINT4	C15	DQ5	P30	TDN3
AD10	DVSS	C16	DQM0	P31	AUD_CLK_MOSI
AD11	DVDD_MODEM	C17	DQS0_T	P4	ANT_SEL1
AD12	DVDD_MODEM	C18	DVSS	P5	WB_SCLK
AD13	DVDD_MD1	C19	DQM1	P6	DVSS
AD14	DVSS	C2	EXTDN	P7	DVDD_MODEM
AD15	DVSS	C20	DQ10	P8	DVDD_MODEM
AD16	DVDD_TOP	C21	DVSS	P9	DVSS
AD17	DVDD_TOP	C22	DVSS	R1	AVDD18_MIPIRX1
AD18	DVDD_TOP	C23	DQM3	R10	DVSS
AD19	DVDD_TOP	C24	DQ24	R11	DVDD_MODEM
AD2	EINT5	C25	DVSS	R12	DVDD_MD1
AD20	DVDD_TOP	C26	MSDC0_DAT4	R13	DVDD_MD1
AD22	DVSS	C27	MSDC0_DAT1	R14	DVSS
AD23	DVSS	C28	MSDC0_DAT5	R15	DVSS
AD24	DVSS	C29	MSDC0_DAT6	R16	DVDD_MD1
AD25	DVSS	C3	WB_CTRL5	R17	DVDD_MD1
AD26	DVSS	C30	MSDC0_DAT7	R18	DVDD_TOP
AD27	DVSS	C31	AVDD33_USB_P0	R19	DVDD_TOP
AD28	DVDD_DVFS	C32	DVSS	R2	RDN2_A
AD29	DVDD_DVFS	C4	CA8	R20	DVDD_TOP
AD3	EINT8	C5	DVSS	R21	DVDD_TOP
AD30	DVDD_DVFS	C6	CA6	R22	DVSS
AD31	DVDD_DVFS	C7	CA5	R23	DVDD_MFG
AD32	DVDD_DVFS	C8	CA7	R24	DVSS
AD4	UTXD0	C9	DVSS	R25	DVDD_MFG
AD5	EINT2	D1	WB_CTRL2	R26	DVDD_MFG
AD6	DVSS	D10	DVSS	R27	DVDD_MFG
AD7	DVDD_MODEM	D11	DVSS	R29	WATCHDOG
AD8	DVDD_MODEM	D12	DQS2_T	R3	RCN_A
AD9	DVSS	D13	DQS2_C	R31	AUD_DAT_MISO
AE10	DVSS	D14	DVSS	R32	EINT11
AE11	DVDD_MODEM	D15	DVSS	R6	DVSS
AE12	DVDD_SRAM_MODEM	D16	DVSS	R7	DVDD_MODEM
AE13	DVSS	D17	DQS0_C	R8	DVDD_MODEM
AE14	DVSS	D19	DQS1_T	R9	DVSS
AE15	DVSS	D2	AVSS18_WBG	T1	RDN3_A
AE16	DVSS	D22	DQS3_T	T10	DVSS
AE17	DVSS	D23	DQS3_C	T11	DVDD_MODEM
AE18	DVSS	D24	DVSS	T12	DVDD_MODEM
AE19	DVSS	D25	DVSS	T13	DVDD_MD1
AE2	EINT6	D26	MSDC0_CMD	T14	DVSS
AE20	DVSS	D27	MSDC0_DSL	T15	DVSS
AE22	DVSS	D28	MSDC0_CLK	T16	DVDD_MD1
AE23	DVSS	D3	WB_CTRL4	T17	DVDD_MD1
AE24	DVSS	D30	CHD_DM_P0	T18	DVSS
AE25	DVSS	D31	USB_DM_P0	T19	DVSS
AE26	DVSS	D32	USB_DP_P0	T2	RDP2_A
AE27	DVSS	D4	WB_CTRL3	T20	DVSS

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AE28	DVDD_DVFS	D5	DVSS	T21	DVSS
AE29	LCM_RST	D6	DVSS	T22	DVSS
AE31	SDA_APPM	D7	CLKO_T	T23	DVSS
AE32	DRVBUS	D8	CLKO_C	T24	DVSS
AE5	EINT3	D9	DVSS	T25	DVSS
AE6	DVSS	E1	WB_RXIP	T26	DVSS
AE7	DVDD_MODEM	E10	DVSS	T27	DVSS
AE8	DVDD_MODEM	E11	DVSS	T28	PWRAP_SPIO_MO
AE9	DVSS	E12	DVSS	T29	SYSRSTB
AF1	EINT0	E13	DVSS	T3	RCP_A
AF10	AVSS18_MD	E14	AVSS18_DDR	T30	RTC32K_CK
AF11	AVSS18_MD	E15	DVSS	T31	SRCLKENA0
AF12	AVSS18_MD	E16	DVSS	T32	SRCLKENA1
AF13	AVSS18_MD	E17	DVSS	T6	AVSS18_MIPIRX
AF14	AVSS18_MD	E18	DDRV	T7	DVDD_MODEM
AF15	AVSS18_MD	E19	DQS1_C	T8	DVDD_MODEM
AF16	DVSS	E2	WB_RXIN	T9	DVSS
AF17	DVSS	E20	DVSS	U1	RDP3_A
AF18	DVSS	E21	DVSS	U10	DVSS
AF19	DVSS	E22	DVSS	U11	DVDD_MODEM
AF2	EINT7	E23	DVSS	U12	DVDD_SRAM_MODEM
AF20	DVSS	E24	DVSS	U13	DVSS
AF21	DVDD_DVFS	E25	DVSS	U14	DVSS
AF22	DVDD_DVFS	E26	DVSS	U15	DVSS
AF23	DVDD_DVFS	E27	VREF_AP	U16	DVDD_MD1
AF24	DVDD_DVFS	E29	AVSS33_USB	U17	DVDD_MD1
AF25	DVDD_DVFS	E3	AVSS18_WBG	U18	DVSS
AF26	DVDD_DVFS	E30	CHD_DP_P0	U19	DVSS
AF27	DVDD_DVFS	E31	AVDD18_USB	U2	RDN0_A
AF28	IDDIG	E4	WB_CTRL1	U20	DVSS
AF29	DSI_TE	E5	WB_CTRL0	U21	DVSS
AF3	KPCOL0	E6	DVSS	U22	DVSS
AF30	DISP_PWM	E7	DVSS	U23	DVSS
AF31	SCL_APPM	E8	DVSS	U24	DVSS
AF4	KPCOL1	E9	DVSS	U25	DVSS
AF5	EINT1	F10	DDRV	U26	DVSS
AF6	PWM_A	F12	DDRV	U27	DVSS
AF7	DVDD_MODEM	F14	AVDD18_DDR	U28	PWRAP_SPIO_MI
AF8	DVDD_MODEM	F15	DDRV	U3	RDP0_A
AF9	AVSS18_MD	F16	DDRV	U31	EINT12
AG1	DVDD18_IORB	F18	DDRV	U4	RDN1_A
AG10	AVSS18_MD	F19	DDRV	U5	RDP1_A
AG11	AVSS18_MD	F2	WB_RXQP	U6	AVSS18_MIPIRX
AG12	AVSS18_MD	F22	DDRV	U7	DVDD_MODEM
AG13	AVSS18_MD	F23	DDRV_VREF	U8	DVDD_MODEM
AG14	AVSS18_MD	F24	VREF_CA	U9	DVSS
AG15	AVSS18_MD	F25	VREF_DQ	V1	RDP1
AG16	DVDD_TOP	F28	DVSS	V10	DVSS
AG17	DVDD_TOP	F29	DVSS	V11	DVDD_MODEM
AG18	DVDD_TOP	F3	AVSS18_WBG	V12	DVDD_MODEM
AG19	DVDD_TOP	F30	AVSS33_USB	V13	DVDD_MD1
AG2	KPROW0	F31	AVDD18_USB	V14	DVSS

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
AG20	DVDD_TOP	F32	NC	V15	DVSS
AG21	DVDD_DVFS	F4	AVSS18_WBG	V16	DVDD_MD1
AG22	DVDD_DVFS	F8	DVSS	V17	DVDD_MD1
AG23	DVDD_DVFS	F9	DDRV	V18	DVSS
AG24	DVDD_DVFS	G1	WB_TXIP	V19	DVSS
AG25	DVDD_DVFS	G10	DDRV	V2	RDN1
AG26	DVDD_DVFS	G12	DDRV	V20	DVDD_MD1
AG27	DVDD_DVFS	G15	DDRV	V21	DVSS
AG28	INT_SIM2	G16	DDRV	V22	DVDD_DVFS
AG31	SDA3	G19	DDRV	V23	DVDD_DVFS
AG32	SCL3	G2	WB_RXQN	V24	DVDD_DVFS
AG4	SPI_MI	G22	DDRV	V25	DVDD_DVFS
AG5	SRCLKENAI	G23	DDRV	V26	DVDD_DVFS
AG7	DVDD_MODEM	G29	AVSS33_USB	V27	DVDD_DVFS
AG8	DVDD_MODEM	G3	AVSS18_WBG	V28	PWRAP_SPI0_CSN
AG9	AVSS18_MD	G30	NC	V29	MSDC1_CLK
AH10	AVSS18_MD	G31	NC	V30	PWRAP_SPI0_CK
AH11	AVSS18_MD	G32	VDD_SRAM	V31	MSDC1_DAT1
AH12	AVSS18_MD	G4	AVSS18_WBG	V32	MSDC1_DAT0
AH13	AVSS18_MD	G8	DVSS	V6	AVSS18_MIPIRX
AH14	AVSS18_MD	G9	DDRV_CLK	V8	DVDD_MODEM
AH15	AVSS18_MD	H1	WB_TXIN	V9	DVSS
AH18	MAIN_X26M_IN	H10	DVSS	W10	DVSS
AH2	KPROW1	H15	TP_MEMPLL	W11	DVDD_MODEM
AH24	DVSS	H16	TN_MEMPLL	W12	DVDD_MODEM
AH25	DVSS	H2	WB_TXQP	W13	DVDD_MD1
AH28	INT_SIM1	H25	DVSS	W14	DVSS
AH29	DPI_D1	H26	DVSS	W15	DVSS
AH3	SPI_CLK	H27	DVDD_MFG	W16	DVDD_MD1
AH30	DPI_D4	H3	AVSS18_WBG	W17	DVDD_MD1
AH31	DPI_D3	H30	DVSS	W18	DVSS
AH32	DVDD18_IOLB	H31	AVSS18_MIPITX	W19	DVSS
AH4	SPI_CSB	H32	AVDD18_MIPITX	W2	RDN0
AH5	SPI_MO	H4	AVSS18_WBG	W20	DVDD_MD1
AH7	DVSS	H7	AVSS18_WBG	W21	DVSS
AH8	DVSS	H8	DVSS	W22	DVDD_DVFS
AH9	AVSS18_MD	J10	DVSS	W23	DVDD_DVFS
AJ1	SCL0	J11	DVDD_TOP	W24	DVDD_DVFS
AJ10	PRX_BB1_QP	J13	DVSS	W25	DVDD_DVFS
AJ17	DRX_BB2_QP	J14	DVSS	W26	DVDD_DVFS
AJ2	SDA0	J17	DVDD_TOP	W27	DVDD_DVFS
AJ25	BPI_BUS10	J18	DVSS	W29	MSDC1_CMD
AJ26	BPI_BUS11	J19	DVDD_TOP	W3	RDP0
AJ29	DPI_D0	J20	DVSS	W31	DVDD18_MC1
AJ3	SCL1	J21	DVDD_TOP	W32	MSDC1_DAT2
AJ31	DPI_D5	J22	DVDD_MFG	W4	RCN
AJ4	SDA1	J23	DVDD_MFG	W5	RCP
AJ9	PRX_BB1_IP	J24	DVDD_MFG	W6	AVSS18_MIPIRX
AK1	PA_VM0	J25	DVDD_MFG	W7	DVDD_MODEM
AK10	PRX_BB1_QN	J26	DVDD_MFG	W8	DVDD_MODEM
AK11	AVSS18_MD	J27	DVDD_MFG	W9	DVSS
AK12	RFIC_ET_P	J3	WB_TXQN	Y1	RDN2

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
AK13	RFIC_ET_N	J30	NC	Y10	DVSS
AK14	AVSS18_MD	J32	VRT	Y11	DVDD_MODEM
AK15	DET_BBIP	J4	AVSS18_WBG	Y12	DVDD_SRAM_MODEM
AK16	AVSS18_MD	J7	DVDD_TOP	Y13	DVSS
AK17	DRX_BB2_QN	J8	DVSS	Y14	DVSS
AK18	DRX_BB2_IN	J9	DVDD_TOP	Y15	DVSS
AK19	DRX_BB2_IP	K1	GPS_RXIP	Y16	DVDD_MD1
AK2	TX_SWAP3	K10	DVDD_TOP	Y17	DVDD_MD1
AK20	AVSS18_MD	K11	DVDD_TOP	Y18	DVSS
AK21	AVSS18_MD	K12	DVDD_TOP	Y19	DVSS
AK23	RFIC0_BSI_D0	K13	DVDD_TOP	Y2	RDP2
AK24	RFIC0_BSI_D1	K14	DVDD_TOP	Y20	DVDD_MD1
AK25	MISC_BSI_CK_0	K15	DVDD_TOP	Y21	DVSS
AK26	BPI_BUS9	K16	DVDD_TOP	Y22	DVSS
AK29	DPI_D2	K17	DVDD_TOP	Y23	DVSS
AK30	DPI_VSYNC	K18	DVSS	Y24	DVSS
AK31	DPI_D6	K19	DVDD_TOP	Y25	DVSS
AK32	DPI_D8	K2	GPS_RXIN	Y26	DVSS
AK4	DET_BPI0	K20	DVSS	Y27	DVSS
AK5	MISC_BSI_CK_2	K21	DVDD_TOP	Y29	MSDC1_DAT3
AK6	MISC_BSI_CK_3	K22	DVDD_MFG	Y3	RDP3
AK7	MISC_BSI_DO_3	K23	DVDD_MFG	Y30	DVSS
AK9	PRX_BB1_IN	K24	DVDD_MFG	Y31	DVDD28_MSDC1
AL1	PA_VM1	K25	DVDD_MFG	Y4	RDN3
AL10	AVSS18_MD	K26	DVDD_MFG	Y6	DVSS
AL11	AVSS18_MD	K27	DVDD_MFG	Y7	DVDD_MODEM
AL13	AVSS18_MD	K3	AVSS18_WBG	Y8	DVDD_MODEM
AL14	AVSS18_MD	K30	NC	Y9	DVSS

2.1.3 Detailed Pin Description

Table 2-2. Acronym for pin type

Abbreviation	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-direction
DI	Digital input
DO	Digital output
DIO	Digital bi-direction
P	Power
G	Ground

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Table 2-3. Detailed pin description (using LPDDR3)

Pin name	Pin no.	Type	Description	Power domain
SYSTEM				
SYSRSTB	T29	DIO	System reset input	DVDD18_IOLT
WATCHDOG	R29	DO	Watchdog reset output	DVDD18_IOLT
TESTMODE	P29	DIO	Test mode	DVDD18_IOLT
RTC32K_CK	T30	DIO	RTC 32K input	DVDD18_IOLT
SRCLKENA0	T31	DIO	Output signal; control 26Hz/Buck/LDO normal mode or sleep mode. (High: normal mode; low : sleep mode or low power mode)	DVDD18_IOLT
SRCLKENA1	T32	DIO	Output signal; control VRF18. (High: VRF18 on; low: VRF18 off)	DVDD18_IOLT
SRCLKENAI	AG5	DIO	Input signal; NFC 26MHz request signal. (High means NFC chip requests system to provide 26MHz to NFC chip.)	DVDD18_IORB
PMIC				
PWRAP_SPI0_MO	T28	DIO	PMIC SPI control interface	DVDD18_IOLT
PWRAP_SPI0_MI	U28	DIO	PMIC SPI control interface	DVDD18_IOLT
PWRAP_SPI0_CSN	V28	DIO	PMIC SPI control interface	DVDD18_IOLT
PWRAP_SPI0_CK	V30	DIO	PMIC SPI control interface	DVDD18_IOLT
AUD_CLK_MOSI	P31	DIO	PMIC audio input interface	DVDD18_IOLT
AUD_DAT_MISO	R31	DIO	PMIC audio input interface	DVDD18_IOLT
AUD_DAT_MOSI	N31	DIO	PMIC audio input interface	DVDD18_IOLT
SIM				
SIM1_SCLK	AC29	DIO	SIM1 clock, PMIC interface	DVDD28_SIM1
SIM1_SIO	AB31	DIO	SIM1 data, PMIC interface	DVDD28_SIM1
SIM1_SRST	AB30	DIO	SIM1 data, PMIC interface	DVDD28_SIM1
SIM2_SCLK	AB29	DIO	SIM2 clock, PMIC interface	DVDD28_SIM2
SIM2_SIO	AA30	DIO	SIM2 data, PMIC interface	DVDD28_SIM2
SIM2_SRST	AA29	DIO	SIM2 data, PMIC interface	DVDD28_SIM2
INT_SIM1	AH28	DIO	SIM1 interrupt	DVDD18_IOLB
INT_SIM2	AG28	DIO	SIM2 interrupt	DVDD18_IOLB
LCD				
DSI_TE	AF29	DIO	Parallel display interface tearing effect	DVDD18_IOLB
LCM_RST	AE29	DIO	Parallel display interface reset signal	DVDD18_IOLB
DPI_HSYNC	AL31	DIO	Parallel display interface HSYNC	DVDD18_IOLB
DPI_VSYNC	AK30	DIO	Parallel display interface VSYNC	DVDD18_IOLB
DPI_CK	AL29	DIO	Parallel display interface CLK	DVDD18_IOLB
DPI_DE	AL30	DIO	Parallel display interface DE	DVDD18_IOLB
DPI_D11	AM31	DIO	Data pin 11 for DPI parallel LCD interface	DVDD18_IOLB

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Pin name	Pin no.	Type	Description	Power domain
DPI_D10	AM30	DIO	Data pin 10 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D9	AN30	DIO	Data pin 9 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D8	AK32	DIO	Data pin 8 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D7	AL32	DIO	Data pin 7 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D6	AK31	DIO	Data pin 6 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D5	AJ31	DIO	Data pin 5 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D4	AH30	DIO	Data pin 4 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D3	AH31	DIO	Data pin 3 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D2	AK29	DIO	Data pin 2 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D1	AH29	DIO	Data pin 1 for DPI parallel LCD interface	DVDD18_IOLB
DPI_D0	AJ29	DIO	Data pin 0 for DPI parallel LCD interface	DVDD18_IOLB
PWM				
PWM_A	AF6	DIO	PWM_A	DVDD18_IORB
DISP_PWM	AF30	DIO	Display PWM	DVDD18_IOLB
Keypad Interface				
KPCOL0	AF3	DIO	Keypad column 0	DVDD18_IORB
KPCOL1	AF4	DIO	Keypad column 1	DVDD18_IORB
KPROW0	AG2	DIO	Keypad row 0	DVDD18_IORB
KPROW1	AH2	DIO	Keypad row 1	DVDD18_IORB
SPI				
SPI_CSB	AH4	DIO	SPI chip select	DVDD18_IORB
SPI_MI	AG4	DIO	SPI data in	DVDD18_IORB
SPI_MO	AH5	DIO	SPI data out	DVDD18_IORB
SPI_CLK	AH3	DIO	SPI clock	DVDD18_IORB
BPI				
BPI_BUS0	AM3	DIO	BPI_BUS0	DVDD18_IOBR
BPI_BUS1	AM4	DIO	BPI_BUS1	DVDD18_IOBR
BPI_BUS2	AM5	DIO	BPI_BUS2	DVDD18_IOBR
BPI_BUS3	AN5	DIO	BPI_BUS3	DVDD18_IOBR
BPI_BUS4	AN27	DIO	BPI_BUS4	DVDD18_IOBL
BPI_BUS5	AM27	DIO	BPI_BUS5	DVDD18_IOBL
BPI_BUS6	AL27	DIO	BPI_BUS6	DVDD18_IOBL
BPI_BUS7	AN26	DIO	BPI_BUS7	DVDD18_IOBL
BPI_BUS8	AL26	DIO	BPI_BUS8	DVDD18_IOBL
BPI_BUS9	AK26	DIO	BPI_BUS9	DVDD18_IOBL

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Pin name	Pin no.	Type	Description	Power domain
BPI_BUS10	AJ25	DIO	BPI_BUS10	DVDD18_IOBL
BPI_BUS11	AJ26	DIO	BPI_BUS11	DVDD18_IOBL
BPI_ANT0	AL28	DIO	BPI_ANT0	DVDD18_IOBL
BPI_ANT1	AM28	DIO	BPI_ANT1	DVDD18_IOBL
BPI_ANT2	AM29	DIO	BPI_ANT2	DVDD18_IOBL
DET_BPI0	AK4	DIO	DET_BPI0	DVDD18_IOBL
DET_BPI1	AL4	DIO	DET_BPI1	DVDD18_IOBL
TX_SWAP0	AL3	DIO	TX_SWAP0	DVDD18_IOBR
TX_SWAP1	AL2	DIO	TX_SWAP1	DVDD18_IOBR
TX_SWAP2	AM2	DIO	TX_SWAP2	DVDD18_IOBR
TX_SWAP3	AK2	DIO	TX_SWAP3	DVDD18_IOBR
PA_VM0	AK1	DIO	PA_VM0	DVDD18_IOBR
PA_VM1	AL1	DIO	PA_VM1	DVDD18_IOBR
BSI				
RFIC0_BSI_CK	AL23	DIO	RFIC0 BSI CLK	DVDD18_IOBL
RFIC0_BSI_D0	AK23	DIO	RFIC0 BSI DATA0	DVDD18_IOBL
RFIC0_BSI_D1	AK24	DIO	RFIC0 BSI DATA1	DVDD18_IOBL
RFIC0_BSI_D2	AN24	DIO	RFIC0 BSI DATA2	DVDD18_IOBL
RFIC0_BSI_EN	AM24	DIO	RFIC0 BSI CS	DVDD18_IOBL
MISC_BSI_DO_0	AL25	DIO	MISC_BSI_DO_0	DVDD18_IOBL
MISC_BSI_CK_0	AK25	DIO	MISC_BSI_CK_0	DVDD18_IOBL
MISC_BSI_DO_1	AM26	DIO	MISC_BSI_DO_1	DVDD18_IOBL
MISC_BSI_CK_1	AM25	DIO	MISC_BSI_CK_1	DVDD18_IOBL
MISC_BSI_DO_2	AL5	DIO	MISC_BSI_DO_2	DVDD18_IOBR
MISC_BSI_CK_2	AK5	DIO	MISC_BSI_CK_2	DVDD18_IOBR
MISC_BSI_DO_3	AK7	DIO	MISC_BSI_DO_3	DVDD18_IOBR
MISC_BSI_CK_3	AK6	DIO	MISC_BSI_CK_3	DVDD18_IOBR
MSDC1				
MSDC1_CLK	V29	DIO	MSDC1 clock output	DVDD28_MSDC1
MSDC1_CMD	W29	DIO	MSDC1 command pin	DVDD28_MSDC1
MSDC1_DAT0	V32	DIO	MSDC1 data0 pin	DVDD28_MSDC1
MSDC1_DAT1	V31	DIO	MSDC1 data1 pin	DVDD28_MSDC1
MSDC1_DAT2	W32	DIO	MSDC1 data2 pin	DVDD28_MSDC1
MSDC1_DAT3	Y29	DIO	MSDC1 data3 pin	DVDD28_MSDC1
MSDC0				
MSDC0_CLK	D28	DIO	MSDC0 clock output	DVDD18_MSDC0
MSDC0_CMD	D26	DIO	MSDC0 command pin	DVDD18_MSDC0
MSDC0_DAT0	A28	DIO	MSDC0 data0 pin	DVDD18_MSDC0
MSDC0_DAT1	C27	DIO	MSDC0 data1 pin	DVDD18_MSDC0
MSDC0_DAT2	A26	DIO	MSDC0 data2 pin	DVDD18_MSDC0
MSDC0_DAT3	B28	DIO	MSDC0 data3 pin	DVDD18_MSDC0
MSDC0_DAT4	C26	DIO	MSDC0 data4 pin	DVDD18_MSDC0
MSDC0_DAT5	C28	DIO	MSDC0 data5 pin	DVDD18_MSDC0

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Pin name	Pin no.	Type	Description	Power domain
MSDC0_DAT6	C29	DIO	MSDC0 data6 pin	DVDD18_MSDC0
MSDC0_DAT7	C30	DIO	MSDC0 data7 pin	DVDD18_MSDC0
MSDC0_DSL	D27	DIO	MSDC0 DSL pin	DVDD18_MSDC0
MSDC0_RSTB	A30	DIO	MSDC0 Reset pin	DVDD18_MSDC0
EFUSE				
DVDD_VQPS	B30	DIO	E-FUSE blowing power control	DVDD_VQPS
EMI				
DQ0	B13	DIO	DRAM interface	DDRV
DQ1	A14	DIO	DRAM interface	DDRV
DQ2	B14	DIO	DRAM interface	DDRV
DQ3	B15	DIO	DRAM interface	DDRV
DQ4	A15	DIO	DRAM interface	DDRV
DQ5	C15	DIO	DRAM interface	DDRV
DQ6	B16	DIO	DRAM interface	DDRV
DQ7	B17	DIO	DRAM interface	DDRV
DQ8	A17	DIO	DRAM interface	DDRV
DQ9	A18	DIO	DRAM interface	DDRV
DQ10	C20	DIO	DRAM interface	DDRV
DQ11	B19	DIO	DRAM interface	DDRV
DQ12	B18	DIO	DRAM interface	DDRV
DQ13	B20	DIO	DRAM interface	DDRV
DQ14	A20	DIO	DRAM interface	DDRV
DQ15	A21	DIO	DRAM interface	DDRV
DQ16	B10	DIO	DRAM interface	DDRV
DQ17	A11	DIO	DRAM interface	DDRV
DQ18	A9	DIO	DRAM interface	DDRV
DQ19	B11	DIO	DRAM interface	DDRV
DQ20	B12	DIO	DRAM interface	DDRV
DQ21	B9	DIO	DRAM interface	DDRV
DQ22	A12	DIO	DRAM interface	DDRV
DQ23	C10	DIO	DRAM interface	DDRV
DQ24	C24	DIO	DRAM interface	DDRV
DQ25	B22	DIO	DRAM interface	DDRV
DQ26	B21	DIO	DRAM interface	DDRV
DQ27	B23	DIO	DRAM interface	DDRV
DQ28	A23	DIO	DRAM interface	DDRV
DQ29	B25	DIO	DRAM interface	DDRV
DQ30	B24	DIO	DRAM interface	DDRV
DQ31	A24	DIO	DRAM interface	DDRV
DQM0	C16	DIO	DRAM interface	DDRV
DQM1	C19	DIO	DRAM interface	DDRV
DQM2	C11	DIO	DRAM interface	DDRV
DQM3	C23	DIO	DRAM interface	DDRV

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Pin name	Pin no.	Type	Description	Power domain
DQS0_C	D17	DIO	DRAM interface	DDRV
DQS0_T	C17	DIO	DRAM interface	DDRV
DQS1_C	E19	DIO	DRAM interface	DDRV
DQS1_T	D19	DIO	DRAM interface	DDRV
DQS2_C	D13	DIO	DRAM interface	DDRV
DQS2_T	D12	DIO	DRAM interface	DDRV
DQS3_C	D23	DIO	DRAM interface	DDRV
DQS3_T	D22	DIO	DRAM interface	DDRV
CA0	B5	DIO	DRAM interface	DDRV
CA1	A5	DIO	DRAM interface	DDRV
CA2	B4	DIO	DRAM interface	DDRV
CA3	A6	DIO	DRAM interface	DDRV
CA4	B6	DIO	DRAM interface	DDRV
CA5	C7	DIO	DRAM interface	DDRV
CA6	C6	DIO	DRAM interface	DDRV
CA7	C8	DIO	DRAM interface	DDRV
CA8	C4	DIO	DRAM interface	DDRV
CA9	B2	DIO	DRAM interface	DDRV
CKE0	B3	DIO	DRAM interface	DDRV
CLK0_C	D8	DIO	DRAM interface	DDRV_CLK
CLK0_T	D7	DIO	DRAM interface	DDRV_CLK
CS0_N	B7	DIO	DRAM interface	DDRV
CS1_N	B8	DIO	DRAM interface	DDRV
VREF_AP	E27	DIO	DRAM interface	DDRV_VREF
VREF_CA	F24	DIO	DRAM interface	DDRV_VREF
VREF_DQ	F25	DIO	DRAM interface	DDRV_VREF
EXTDN	C2	DIO	DRAM interface	DDRV
CAM				
CAM_CLK0	AB5	DIO	Master clock to 1st sensor	DVDD18_IORB
CAM_CLK1	AC5	DIO	Master clock to 2nd sensor	DVDD18_IORB
CAM_RST0	AC1	DIO	Reset control to 1st sensor	DVDD18_IORB
CAM_PDN0	AB4	DIO	Power down to 1st sensor	DVDD18_IORB
CAM_RST1	AC2	DIO	Reset control to 2nd sensor	DVDD18_IORB
CAM_PDN1	AB3	DIO	Power down to 2nd sensor	DVDD18_IORB
I2C				
SCL0	AJ1	DIO	I2C0 clock	DVDD18_IORB
SCL1	AJ3	DIO	I2C1 clock	DVDD18_IORB
SCL2	AA2	DIO	I2C2 clock	DVDD18_IORB
SCL3	AG32	DIO	I2C3 clock	DVDD18_IOLB
SDA0	AJ2	DIO	I2C0 data	DVDD18_IORB
SDA1	AJ4	DIO	I2C1 data	DVDD18_IORB
SDA2	AA1	DIO	I2C2 data	DVDD18_IORB
SDA3	AG31	DIO	I2C3 data	DVDD18_IOLB

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Pin name	Pin no.	Type	Description	Power domain
CONN				
WB_CTRL0	E5	DIO	WB control for CONN_RF	DVDD18_IORT2
WB_CTRL1	E4	DIO	WB control for CONN_RF	DVDD18_IORT2
WB_CTRL2	D1	DIO	WB control for CONN_RF	DVDD18_IORT2
WB_CTRL3	D4	DIO	WB control for CONN_RF	DVDD18_IORT2
WB_CTRL4	D3	DIO	WB control for CONN_RF	DVDD18_IORT2
WB_CTRL5	C3	DIO	WB control for CONN_RF	DVDD18_IORT2
WB_RSTB	L5	DIO	Reset for CONN_RF	DVDD18_IORT
WB_SEN	L4	DIO	SPI for CONN_RF	DVDD18_IORT
WB_SCLK	P5	DIO	SPI for CONN_RF	DVDD18_IORT
WB_SDATA	N5	DIO	SPI for CONN_RF	DVDD18_IORT
F2W_CLK	M4	DIO	AUD_IN from CONN_RF	DVDD18_IORT
F2W_DATA	M5	DIO	AUD_IN from CONN_RF	DVDD18_IORT
ABB				
DRX_BB2_QP	AJ17	AIO	DRX_BB2_QP	AVDD18_MD
DRX_BB2_QN	AK17	AIO	DRX_BB2_QN	AVDD18_MD
DRX_BB2_IN	AK18	AIO	DRX_BB2_IN	AVDD18_MD
DRX_BB2_IP	AK19	AIO	DRX_BB2_IP	AVDD18_MD
PRX_BB2_QP	AM16	AIO	PRX_BB2_QP	AVDD18_MD
PRX_BB2_QN	AM17	AIO	PRX_BB2_QN	AVDD18_MD
PRX_BB2_IN	AN17	AIO	PRX_BB2_IN	AVDD18_MD
PRX_BB2_IP	AN18	AIO	PRX_BB2_IP	AVDD18_MD
TX_BBQP	AM12	AIO	TX_BBQP	AVDD18_MD
TX_BBQN	AM13	AIO	TX_BBQN	AVDD18_MD
TX_BBIN	AN12	AIO	TX_BBIN	AVDD18_MD
TX_BBIP	AN11	AIO	TX_BBIP	AVDD18_MD
PRX_BB1_QP	AJ10	AIO	PRX_BB1_QP	AVDD18_MD
PRX_BB1_QN	AK10	AIO	PRX_BB1_QN	AVDD18_MD
PRX_BB1_IN	AK9	AIO	PRX_BB1_IN	AVDD18_MD
PRX_BB1_IP	AJ9	AIO	PRX_BB1_IP	AVDD18_MD
DRX_BB1_QP	AN9	AIO	DRX_BB1_QP	AVDD18_MD
DRX_BB1_QN	AN8	AIO	DRX_BB1_QN	AVDD18_MD
DRX_BB1_IN	AM8	AIO	DRX_BB1_IN	AVDD18_MD
DRX_BB1_IP	AM7	AIO	DRX_BB1_IP	AVDD18_MD
APC1	AL8	AIO	Automatic power control for modem	AVDD18_MD
MAIN_X26M_IN	AH18	AIO	26MHz clock input for AP and modem	AVDD18_MD
DET_BBIN	AL15	AIO	DET_BBIN	AVDD18_MD
DET_BBIP	AK15	AIO	DET_BBIP	AVDD18_MD
DET_BBQP	AN15	AIO	DET_BBQP	AVDD18_MD
DET_BBQN	AN14	AIO	DET_BBQN	AVDD18_MD
AUXIN0	AM20	AIO	AuxADC external input channel 0	AVDD18_MD
AUXIN1	AM21	AIO	AuxADC external input channel 1	AVDD18_MD

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Pin name	Pin no.	Type	Description	Power domain
AUXIN2	AL20	AIO	AuxADC external input channel 2	AVDD18_MD
AUXIN3	AL21	AIO	AuxADC external input channel 3	AVDD18_MD
AUXIN4	AM19	AIO	AuxADC external input channel 4	AVDD18_MD
REFP	AN22	AIO	Reference bandgap voltage	AVDD18_MD
REFN	AN21	AIO	Reference ground of bandgap	AVDD18_MD
RFIC_ET_N	AK13	AIO	Envelope tracking	AVDD18_MD
RFIC_ET_P	AK12	AIO	Envelope tracking	AVDD18_MD
MIPI				
TDN0	M30	AIO	DSI0 lane 0 N	AVDD18_MIPITX
TDP0	L30	AIO	DSI lane 0 P	AVDD18_MIPITX
TDN1	N29	AIO	DSI lane 1 N	AVDD18_MIPITX
TDP1	M29	AIO	DSI0 lane 1 P	AVDD18_MIPITX
TDN2	M31	AIO	DSI0 lane 2 N	AVDD18_MIPITX
TDP2	M32	AIO	DSI0 lane 2 P	AVDD18_MIPITX
TDN3	P30	AIO	DSI0 lane 3 N	AVDD18_MIPITX
TDP3	N30	AIO	DSI0 lane 3 P	AVDD18_MIPITX
TCN	L31	AIO	DSI0 CK lane N	AVDD18_MIPITX
TCP	K32	AIO	DSI0 CK lane P	AVDD18_MIPITX
VRT	J32	AO	External resistor for DSI bias Connect 1.5K ohm 1% resistor to ground.	AVDD18_MIPITX
RDN0	W2	AIO	CSI0 lane0 N	AVDD18_MIPIRX0
RDP0	W3	AIO	CSI0 lane0 P	AVDD18_MIPIRX0
RDN1	V2	AIO	CSI0 lane1 N	AVDD18_MIPIRX0
RDP1	V1	AIO	CSI0 lane 1 P	AVDD18_MIPIRX0
RDN2	Y1	AIO	CSI0 lane2 N	AVDD18_MIPIRX0
RDP2	Y2	AIO	CSI0 lane2 P	AVDD18_MIPIRX0
RDN3	Y4	AIO	CSI0 lane3 N	AVDD18_MIPIRX0
RDP3	Y3	AIO	CSI0 lane3 P	AVDD18_MIPIRX0
RCN	W4	AIO	CSI0 CK lane N	AVDD18_MIPIRX0
RCP	W5	AIO	CSI0 CK lane P	AVDD18_MIPIRX0
RDN0_A	U2	AIO	CSI1 lane 0 N	AVDD18_MIPIRX1
RDP0_A	U3	AIO	CSI1 lane 0 P	AVDD18_MIPIRX1
RDN1_A	U4	AIO	CSI1 lane 1 N	AVDD18_MIPIRX1
RDP1_A	U5	AIO	CSI1 lane 1 P	AVDD18_MIPIRX1
RDN2_A	R2	AIO	CSI1 lane 2 N	AVDD18_MIPIRX1
RDP2_A	T2	AIO	CSI1 lane 2 P	AVDD18_MIPIRX1
RDN3_A	T1	AIO	CSI1 lane 3 N	AVDD18_MIPIRX1
RDP3_A	U1	AIO	CSI1 lane 3 P	AVDD18_MIPIRX1
RCN_A	R3	AIO	CSI1 CK lane N	AVDD18_MIPIRX1
RCP_A	T3	AIO	CSI1 CK lane P	AVDD18_MIPIRX1
USB				
USB_DM_P0	D31	AIO	USB D+ differential data line	AVDD33_USB_P0

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Pin name	Pin no.	Type	Description	Power domain
USB_DP_P0	D32	AIO	USB D- differential data line	AVDD33_USB_P0
CHD_DM_P0	D30	AIO	BC1.1 charger DP	AVDD33_USB_P0
CHD_DP_P0	E30	AIO	BC1.1 charger DM	AVDD33_USB_P0
WBG				
WB_RXQN	G2	AIO	RX_QN for WIFI/BT Rx	AVDD18_WBG
WB_RXQP	F2	AIO	RX_QP for WIFI/BT Rx	AVDD18_WBG
WB_RXIP	E1	AIO	RX_IN for WIFI/BT Rx	AVDD18_WBG
WB_RXIN	E2	AIO	RX_IP for WIFI/BT Rx	AVDD18_WBG
WB_TXQP	H2	AIO	TX_QP for WIFI/BT Tx	AVDD18_WBG
WB_TXQN	J3	AIO	TX_QN for WIFI/BT Tx	AVDD18_WBG
WB_TXIN	H1	AIO	TX_IN for WIFI/BT Tx	AVDD18_WBG
WB_TXIP	G1	AIO	TX_IP for WIFI/BT Tx	AVDD18_WBG
GPS_RXQN	M1	AIO	RX_QN for GPS Rx	AVDD18_WBG
GPS_RXQP	L2	AIO	RX_QP for GPS Rx	AVDD18_WBG
GPS_RXIP	K1	AIO	RX_IN for GPS Rx	AVDD18_WBG
GPS_RXIN	K2	AIO	RX_IP for GPS Rx	AVDD18_WBG
XIN_WBG	K4	AIO	26MHz clock input for WBG	AVDD18_WBG
MISC				
DRVBUS	AE32	DIO	This signal enables to drive 5V on Vbus. 0: Not drive Vbus 1: Drive 5V on Vbus	
IDDIG	AF28	DIO	Indicates whether the connected plug is a mini-A or mini-B 0: Connected plug is a mini-A (ID is connected to GND). 1: Connected plug is a mini-B (ID is floating).	
TN_PLLGP	AC20	AIO	Reserved	
TP_PLLGP	AC19	AIO	Reserved	
TN_MEMPLL	H16	AIO	Reserved	
TP_MEMPLL	H15	AIO	Reserved	
Analog Power				
AVDD18_AP	AM22	P	Analog power input 1.8V	
AVDD18_MD	AL22	P	Analog power input 1.8V for modem	
AVDD18_MDPLLGP	AB20	P	Analog power input 1.8V for PLL	
AVDD18_MIPIRX0	P2	P	Analog power for MIPI CSI	
AVDD18_MIPIRX1	R1	P	Analog power for MIPI CSI	
AVDD18_MIPITX	H32	P	Analog power for MIPI	
AVDD18_USB	E31	P	Analog power 1.8V for USB	
AVDD18_WBG	N2	P	Analog power 1.8V for WBG (Wi-Fi, BT, GPS)	
AVDD28_DAC	AN6	P	Analog power 1.8V for DAC	
AVDD18_USB	E31	P	Analog power 1.8V for USB	
AVDD33_USB_P0	C31	P	Analog power 3.3V for USB	

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Pin name	Pin no.	Type	Description	Power domain
AVDD33_USB_P1	C32	P	Analog power 3.3V for USB	
Digital Power				
DDRV	E18	P	Digital power input for DDR	-
DDRV_CLK	G9	P	Digital power input for DDR	-
DDRV_VREF	F23	P	Digital power input for DDR	-
DVDD_DVFS	AB22	P	Digital power input for DVFS	-
DVDD_MFG	H27	P	Digital power input for GPU	-
DVDD_MODEM	AA11	P	Digital power input for LTE	-
DVDD_SRAM_MODEM	AC12	P	Digital power input for LTE	-
DVDD_MD1	AA13	P	Digital power input for LTE	-
DVDD_SRAM	AB21	P	Digital power input for SRAM	-
DVDD_TOP	AD16	P	Digital power input for Vcore	-
DVDD18_IOLT	N32	P	Digital power input for IO (region 1)	-
DVDD18_IOLB	AH32	P	Digital power input for IO (region 2)	
DVDD18_IOBL	AN23	P	Digital power input for IO (region 3)	
DVDD18_IOBR	AN3	P	Digital power input for IO (region 4)	-
DVDD18_IORB	AG1	P	Digital power input for IO (region 5)	
DVDD18_IORT1	P1	P	Digital power input for IO (region 6)	
DVDD18_IORT2	C1	P	Digital power input for IO (region 7)	
DVDD18_MSDC0	B31	P	Digital power input for MSDC0	
DVDD18_MC1	W31	P	Digital power input for MSDC1	
DVDD28_MSDC1	Y31	P	Digital power input for MSDC1	
DVDD18_SIM	AA32	P	Digital power input for SIM1/2	
DVDD28_SIM1	AA31	P	Digital power input for SIM1	
DVDD28_SIM2	AB32	P	Digital power input for SIM2	
Analog Ground				
AVSS18_MD	AF10	G	Analog ground input for modem	
AVSS18_MDPLLGP	AB19	G	Analog ground input for PLL	
AVSS18_MIPIRX	T6	G	Analog ground input for MIPI RX	
AVSS18_MIPITX	H31	G	Analog ground input for MIPI TX	
AVSS18_WBG	D2	G	Analog ground input for WBG	
AVSS33_USB	E29	G	Analog ground input for USB	
Digital Ground				
GND		G		-

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Table 2-4. Acronym for table of state of pins

Abbreviation	Description
I	Input
LO	Low output
HO	High output
XO	Low or high output
PU	Pull-up
PD	Pull-dowm
-	No PU/PD
0~N	Aux. function number
X	Delicate function pin

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2.2 Electrical Characteristic

2.2.1 Absolute Maximum Ratings

Table 2-5. Absolute maximum ratings for power supply

Symbol or pin name	Description	Min.	Max.	Unit
AVDD18_DDR AVDD18_MDPLLGP	Analog power input 1.8V for PLL & DDR	1.7	1.9	V
AVDD18_AP	Analog power input 1.8V for AuxADC, TSENSE	1.7	1.9	V
AVDD18_MD	Analog power input 1.8V for BBTX, BBRX	1.7	1.9	V
AVDD28_DAC	Analog power input 2.8V for APC	2.66	2.94	V
AVDD18_MIPITX	Analog power for MIPI DSI	1.7	1.9	V
AVDD18_MIPIRX0 AVDD18_MIPIRX1	Analog power for MIPI CSI0 & CSI1	1.7	1.9	V
AVDD33_USB_P0 AVDD33_USB_P1	Analog power 3.3V for USB	3.135	3.465	V
AVDD18_USB	Analog power 1.8V for USB	1.7	1.9	V
AVDD18_WBG	Analog power 1.8V for connectivity ABB	1.7	1.9	V
DVDD18_IOLT DVDD18_SIM DVDD18_IOLB DVDD18_IOBL DVDD18_IOBR DVDD18_IORB DVDD18_IORT1 DVDD18_IORT2 DVDD18_BIAS1 DVDD18_BIAS2 DVDD18_BIAS3 DVDD18_MC1	Digital power input for 1.8V IO	1.62	1.98	V
DVDD18_MSDC0	Digital power input for MSDC0	1.62	1.98	V
DVDD28_MSDC1	Digital power input for MSDC1	1.7	3.6	V
DVDD28_SIM1	Digital power input for SIM1	1.7	3.6	V
DVDD28_SIM2	Digital power input for SIM2	1.7	3.6	V
DDRV DDRV_CLK DDRV_VREF	Digital power input for DRAM	1.14	1.3	V
DVDD_DVFS	Digital power input for DVFS	0.7	1.125	V
DVDD_GPU	Digital power input for GPU	0.93	1.125	V
DVDD_MD1	Digital power input for MD1	0.9	0.9	V
DVDD_SRAM_MODEM	Digital power input for MD SRAM	1.0	1.1	V
DVDD_MODEM	Digital power input for MODEM	0.85	1.0	V
DVDD_SRAM	Digital power input for SRAM	0.7	1.125	V
DVDD_TOP	Digital power input for TOP	0.7	1.0	V

Warning: *Stressing the device beyond the absolute maximum ratings may cause permanent damage. These are stress ratings only.*

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2.2.2 Recommended Operating Conditions

Table 2-6. Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
AVDD18_DDR AVDD18_MDPLLGP	Analog power input 1.8V for PLL & DDR	1.7	1.8	1.89	V
AVDD18_AP	Analog power input 1.8V for AuxADC, TSENSE	1.71	1.8	1.89	V
AVDD18_MD	Analog power input 1.8V for BBTX, BBRX	1.71	1.8	1.89	V
AVDD28_DAC	Analog power input 2.8V for APC	2.66	2.8	2.94	V
AVDD18_MIPITX	Analog power for MIPI DSI	1.71	1.8	1.89	V
AVDD18_MIPIRX0 AVDD18_MIPIRX1	Analog power for MIPI CSI0 & CSI1	1.71	1.8	1.89	V
AVDD33_USB_P0 AVDD33_USB_P1	Analog power 3.3V for USB	3.135	3.3	3.465	V
AVDD18_USB	Analog power 1.8V for USB	1.71	1.8	1.89	V
AVDD18_WBG	Analog power 1.8V for connectivity ABB	1.71	1.8	1.89	V
DVDD18_IOLT DVDD18_SIM DVDD18_IOLB DVDD18_IOBL DVDD18_IOBR DVDD18_IORB DVDD18_IORT1 DVDD18_IORT2 DVDD18_BIAS1 DVDD18_BIAS2 DVDD18_BIAS3 DVDD18_MC1	Digital power input for 1.8V IO	1.62	1.8	1.98	V
DVDD18_MSDC0	Digital power input for MSDC0	1.62	1.8	1.98	V
DVDD28_MSDC1	Digital power input for MSDC1	1.7	1.8	1.95	V
		2.7	3.3	3.6	
		2.66	2.8	2.94	
DVDD28_SIM1 DVDD28_SIM2	Digital power input for SIM1/SIM2	2.7	3.3	3.6	V
		1.7	1.8	1.9	
DDRV DDRV_CLK DDRV_VREF	Digital power input for EMI (LPDDR2/3)	1.14	1.2	1.3	V
DVDD_DVFS	Digital power input for DVFS	0.7	1.0	1.125	V
DVDD_GPU	Digital power input for GPU	0.93	1.0	1.125	V
DVDD_MD1	Digital power input for MD1	0.9	0.9	0.9	V
DVDD_SRAM_MODEM	Digital power input for MD SRAM	1.0	1.0	1.1	V
DVDD_MODEM	Digital power input for MODEM	0.85	0.9	1.0	V
DVDD_SRAM	Digital power input for SRAM	0.7	0.9	1.125	V
DVDD_TOP	Digital power input for TOP	0.7	0.9	1.0	V

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2.2.3 Storage Condition

1. Shelf life in sealed bag: 12 months at < 40°C and < 90% relative humidity (RH).
2. After the bag is opened, devices subjected to infrared reflow, vapor-phase reflow or equivalent processing must be:
   - Mounted within 168 hours in factory condition of 30°C/60% RH, or
   - Stored at 20% RH
3. Devices require baking before being mounted, if they are placed
   - For 192 hours at 40°C +5°C/-0°C and < 5% RH in low temperature device containers, or
   - For 24 hours at 125°C +5°C/-0°C in high temperature device containers.

2.2.4 DC Electrical Characteristics

2.2.4.1 RTC DC Electrical Characteristics

Table 2-7. RTC DC electrical characteristics (DVDD18_IOLT =1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IOLT		DVDD18_IOLT + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IOLT	V
VOH	DC output logic low voltage	0.75*DVDD18_IOLT			V
VOL	DC output logic high voltage			0.25*DVDD18_IOLT	V
F_{RTC}	Input clock frequency		32		KHz
DC_{RTC}	Input signal duty cycle	45	50	55	%

2.2.4.2 SPI, I2S DC Electrical Characteristics

Table 2-8. SPI, I2S DC electrical characteristics (DVDD18_IORB =1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IORB		DVDD18_IORB + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IORB	V
VOH	DC output logic low voltage	0.75*DVDD18_IORB			V
VOL	DC Output logic high voltage			0.25*DVDD18_IORB	V

2.2.4.3 I2C0, I2C1, I2C2 DC Electrical Characteristics

Table 2-9. I2C0, I2C1, I2C2 DC electrical characteristics (DVDD18_IORB =1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IORB		DVDD18_IORB + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IORB	V
VOL	DC output logic high voltage			0.2*DVDD18_IORB	V

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2.2.4.4 I2C3 DC Electrical Characteristics

Table 2-10. I2C3 DC electrical characteristics (DVDD18_IOLB =1.8V)

Parameters	Descriptions	Min.	Typ	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IOLB		DVDD18_IOLB + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IOLB	V
VOL	DC output logic high voltage			0.2*DVDD18_IOLB	V

2.2.4.5 MSDC0 DC Electrical Characteristics

Table 2-11. MSDC0 DC electrical characteristics (DVDD28_MSDC0=1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	1.3		2.0	V
VIL	Input logic high voltage	-0.3		0.58	V
VOH	DC output logic low voltage	1.4			V
VOL	DC output logic high voltage			0.45	V

2.2.4.6 MSDC1 DC Electrical Characteristics

Table 2-12. MSDC1 DC electrical characteristics (DVDD28_MSDC1=2.8V/3.3V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.625* DVDD28_MSDC1		DVDD28_MSDC1 + 0.3	V
VIL	Input logic high voltage	-0.3		0.25* DVDD28_MSDC1	V
VOH	DC output logic low voltage	0.75* DVDD28_MSDC1		DVDD28_MSDC1 + 0.3	V
VOL	DC output logic high voltage	-0.3		0.125* DVDD28_MSDC1	V

Table 2-13. MSDC1 DC electrical characteristics (DVDD28_MSDC1=1.8V)

Parameters	Descriptions	Min	Typ	Max	Unit
VIH	Input logic low voltage	1.27		DVDD28_MSDC1 + 0.3	V
VIL	Input logic high voltage	-0.3		0.58	V
VOH	DC output logic low voltage	1.4		DVDD28_MSDC1 + 0.3	V
VOL	DC output logic high voltage	-0.3		0.45	V

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2.2.4.7 SIM DC Electrical Characteristics

Table 2-14. SIM DC electrical characteristics

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
SIM1_SIO						
Input high voltage	DVDD28_SIM1 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.4	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.27	V
Input high voltage	DVDD28_SIM1 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.6	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM1_SCLK						
Input high voltage	DVDD28_SIM1 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.22	V
Input high voltage	DVDD28_SIM1 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM1_SRST						
Input high voltage	DVDD28_SIM1 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V
Input high voltage	DVDD28_SIM1 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V
SIM2_SIO						
Input high voltage	DVDD28_SIM2 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.4	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.27	V
Input high voltage	DVDD28_SIM2= 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.6	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM2_SCLK						
Input high voltage	DVDD28_SIM2 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V

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Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.22	V
Input high voltage	DVDD28_SIM2 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM2_SRST						
Input high voltage	DVDD28_SIM2 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V
Input high voltage	DVDD28_SIM2 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V

2.2.5 AC Electrical Characteristics and Timing Diagram

2.2.5.1 External Memory Interface for LPDDR3

The external memory interface, shown in Figure 2-2, Figure 2-3 and Figure 2-4, is used to connect LPDDR3 device for MT6750. It includes pins CLK_T, CLK_C, CKE[1:0], CS[1:0], DQS[3:0], DQS#[3:0], CA[9:0] and DQ[31:0]. Table 2-15 summarizes the symbol definition and the related timing specifications.

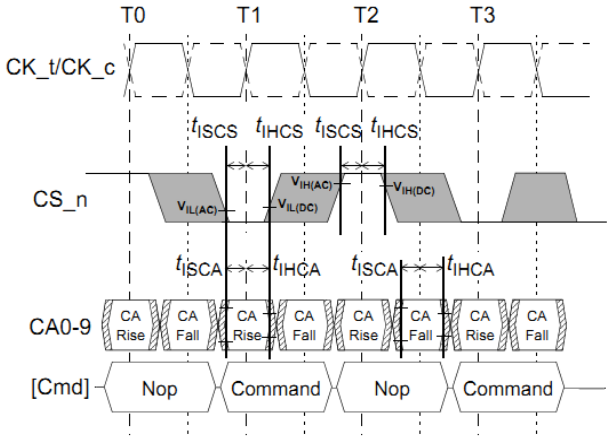

Figure 2-2. Basic timing parameter for LPDDR3 commands

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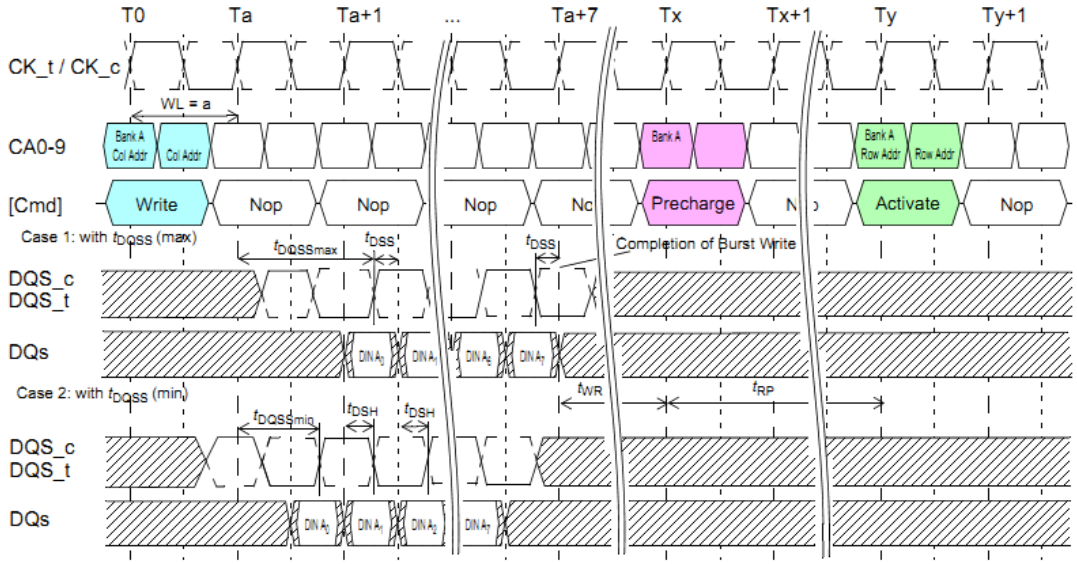

Figure 2-3. Basic timing parameter for LPDDR3 write

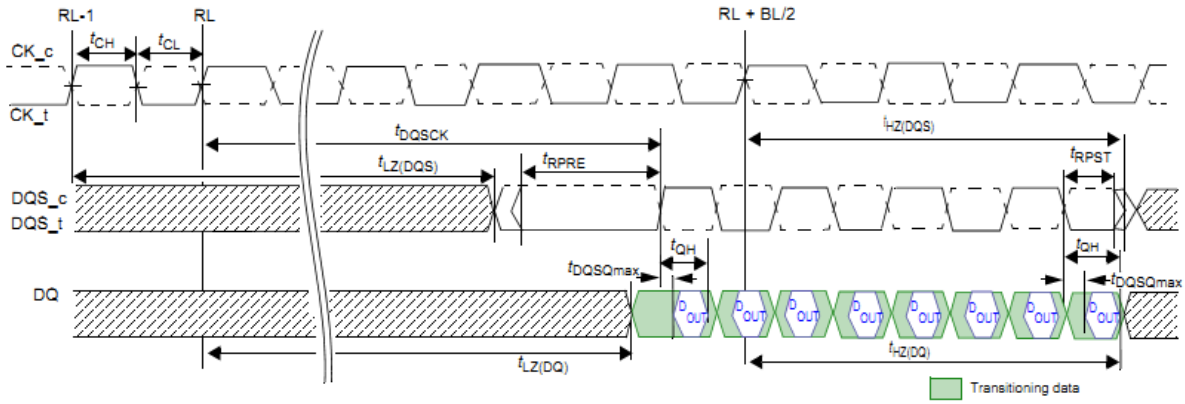

Figure 2-4. Basic LPDDR3 read timing parameter

Table 2-15. LPDDR3 AC timing parameter table of external memory interface

Symbol	Description	Min.	Typ.	Max.	Unit
tCK	Clock cycle time	1.071		100	ns
tDQSCK	DQS output access time from CK/CK'	2.5		5.5	ns
tCH	Clock high level width	0.45		0.55	tCK
tCL	Clock low level width	0.45		0.55	tCK
tDS	DQ & DM input setup time	0.13			ns
tDH	DQ & DM input hold time	0.13			ns
tDIPW	DQ and DM input pulse width	0.35			tCK
tDQSS	Write command to 1st DQS latching transition	0.75		1.25	tCK
tDSS	DQS falling edge to CK setup time	0.2			tCK
tDSH	DQS falling edge hold time from CK	0.2			tCK

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Symbol	Description	Min.	Typ.	Max.	Unit
tWPST	Write postamble	0.4			tCK
tWPRE	Write preamble	0.8			tCK
tISCA	Address & control input setup time	0.13			ns
tIHCA	Address & control input hold time	0.13			ns
tISCS	CS_ input setup time	0.23			ns
tIHCS	CS_ input hold time	0.23			ns
tIPWCA	Address and control input pulse width	0.35			tCK
tIPWCS	CS_ input pulse width	0.7			tCK
tCKE	CKE minimum pulse width (HIGH and LOW pulse width)	Max. (7.5ns, 3tCK)			ns
tISCKE	CKE input setup time	0.25			tCK
tIHCKE	CKE input hold time	0.25			tCK
tCPDED	Command path disable delay	2			tCK
tLZ(DQS)	DQS low-impedance time from CK/CK’	tDQSCK (MIN) - 0.3			ns
tHZ(DQS)	DQS high-impedance time from CK/CK’			tDQSCK (MAX) – 0.1	ns
tLZ(DQ)	DQ low-impedance time from CK/CK’	tDQSCK (MIN) - 0.3			ns
tHZ(DQ)	DQ high-impedance time from CK/CK’			tDQSCK (MAX) + [1.4*tDQSQ (MAX)]	ns
tDQSQ	DQS-DQ skew			0.115	ns
tDQSH	DQS input high-level width	0.4			tCK
tDQSL	DQS input low-level width	0.4			tCK
tQSH	DQS output high pulse width	tCH - 0.05			tCK
tQSL	DQS output low pulse width	tCL - 0.05			tCK
tQH	DQ/DQS output hold time from DQS	Min. (tQSH, tQSL)			ns
tMRW	MODE register Write command period	Max. (10tCK, 15)			ns
tMRR	MODE register Read command period	4			tCK
tMRD	Mode register set command delay	Max. (10tCK, 14)			ns
tRPRE	Read preamble	0.9			tCK
tRPST	Read postamble	0.3			tCK
tRAS	ACTIVE to PRECHARGE command period	Max. (42ns, 3tCK)		70000	ns
tRC	ACTIVE to ACTIVE command period	tRAS + tRPab (with all-bank pre-charge) tRAS + tRPpb (with per-bank pre-charge)			ns

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Symbol	Description	Min.	Typ.	Max.	Unit
tRFC	AUTO REFRESH to ACTIVE/AUTO REFRESH command period	56			ns
tRCD	ACTIVE to READ or WRITE delay	Max. (18ns, 3tCK)			ns
tRPpb	Row PRECHARGE Time (single bank)	Max. (18ns, 3tCK)			ns
tRPab	Row PRECHARGE Time (all banks)	Max. (21ns, 3tCK)			ns
tRRD	ACTIVE bank A to ACTIVE bank B delay	Max. (10ns, 2tCK)			ns
tWR	WRITE recovery time	Max. (15ns, 4tCK)			ns
tWTR	Internal write to READ command time	Max. (7.5ns, 4tCK)			ns
tXSR	SELF REFRESH exit to next valid command	Max. (tRFCab + 10ns, 2tCK)			ns
tXP	EXIT power down to next valid command delay	Max. (7.5ns, 3tCK)			ns
tREFW	Refresh period			32	ms
tRFCab	Refresh cycle time	130			ns
tRFCpb	Per bank refresh cycle time	60			ns
tRTP	Internal READ to PRECHARGE command delay	Max. (7.5ns, 4tCK)			ns
tCCD	CAS-to-CAS delay	4			tCK

2.2.5.2 SPI AC Timing Characteristics

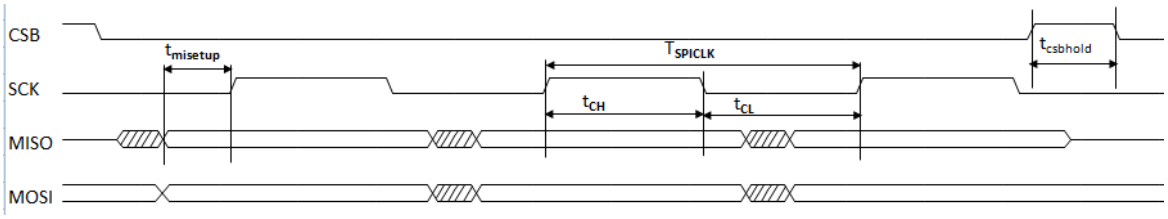

Figure 2-5. SPI timing diagram

Table 2-16. SPI AC timing parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
SPI clock period	T_{SPICLK}	18.2	-	-	ns
SPI clock low time	t_{CL}	9.1	-	-	ns
SPI clock high time	t_{CH}	9.1	-	-	ns
SPI CSB hold time	$t_{csbhold}$	9.1	-	-	ns
SPI MISO setup time (MISO 80%, SCK 20%)	$t_{misetup}$	28.5	-	-	ns

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2.2.5.3 I2S AC Timing Characteristics

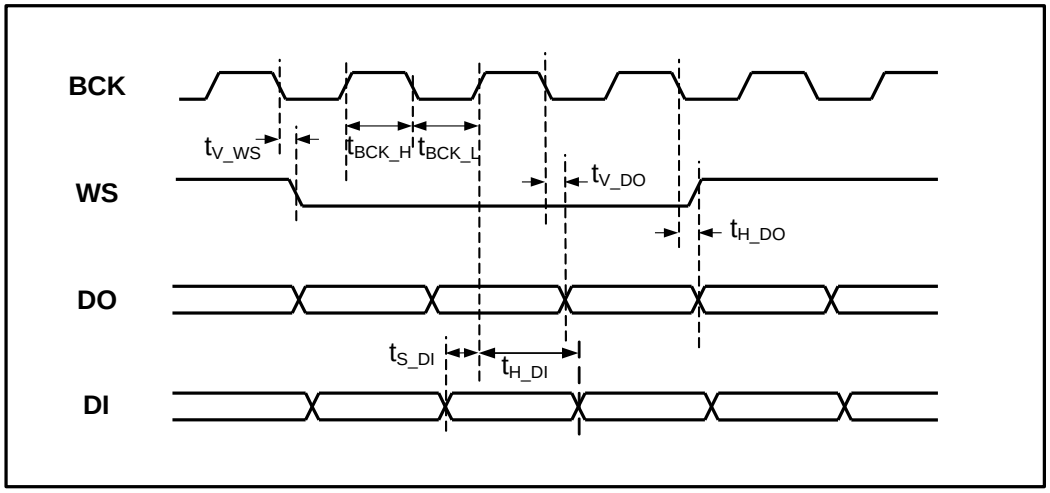

Figure 2-6. I2S master mode timing diagram

Table 2-17. I2S AC timing parameters

Parameter	Description	Min.	Typ.	Max.	Unit
f_S	Sampling frequency	8	-	192	kHz
t_{WS}	Word select period	32	-	64	$1/f_{BCK}$
f_{MCK}	Master clock frequency	-	-	24.576	MHz
f_{BCK}	Serial clock frequency	32 * f_S	-	64 * f_S	MHz
t_{BCK_H}	BCK high-level time	-	0.5	-	$1/f_{BCK}$
t_{BCK_L}	BCK low-level time	-	0.5	-	$1/f_{BCK}$
t_{V_WS}	WS valid time	-	-	0.2	$1/f_{BCK}$
t_{H_WS}	WS hold time	0	-	-	$1/f_{BCK}$
t_{V_DO}	DO valid time	-	-	0.2	$1/f_{BCK}$
t_{H_DO}	DO hold time	0	-	-	$1/f_{BCK}$
t_{S_DI}	DI setup time	0.2	-	-	$1/f_{BCK}$
t_{H_DI}	DI hold time	0.2	-	-	$1/f_{BCK}$

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2.2.5.4 I2C AC Timing Characteristics

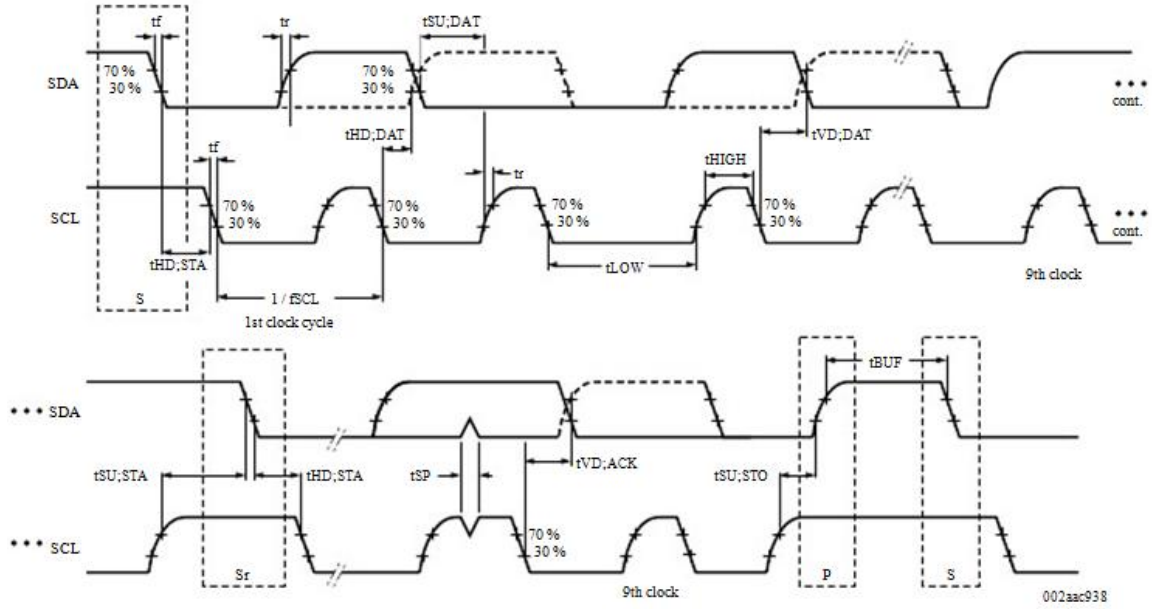

Figure 2-7. I2C timing diagram of standard mode (100kHz) and fast mode (400kHz)

Table 2-18. I2C AC timing parameters

Symbol	Standard mode	Fast mode	Unit	Note
$t_{HD;STA}$	2.5	0.625	µs	Can be extended by 0x28, extension configuration register.
t_{LOW}	5	1.25	µs	
t_{HIGH}	5	1.25	µs	
$t_{SU;STA}$	2.5	0.625	µs	
$t_{HD;DAT}$	2.5	0.625	µs	
$t_{SU;DAT}$	2.5	0.625	µs	
$t_{SU;STO}$	2.5	0.625	µs	Can be extended by 0x28, extension configuration register.

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2.2.5.5 MSDC AC Timing Characteristics

2.2.5.5.1 Default Speed Timing

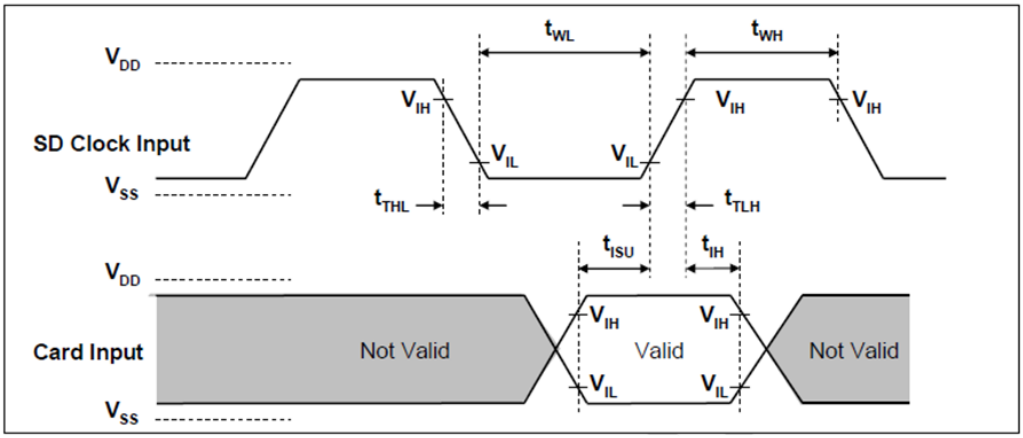

Figure 2-8. MSDC input timing diagram of default speed

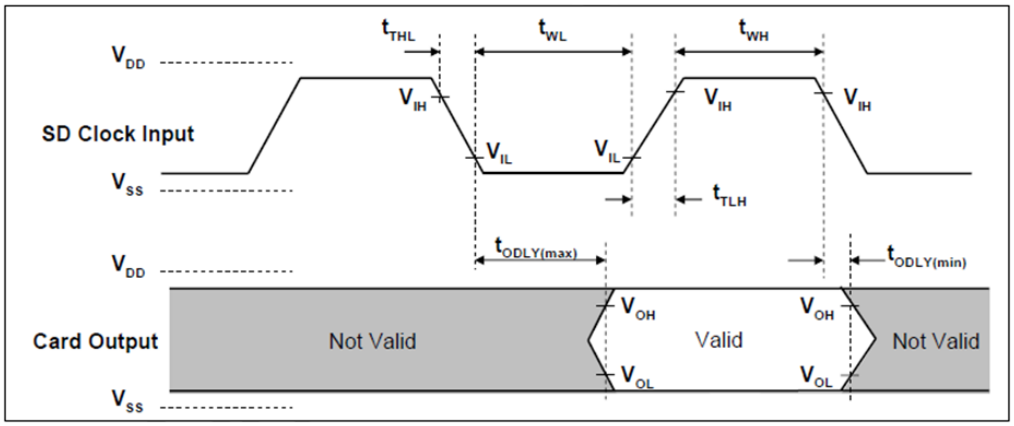

Figure 2-9. MSDC output timing diagram of default speed

Table 2-19. MSDC AC timing parameters of default speed

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL}))					
Clock frequency data transfer mode	f_{PP}	0	25	MHz	$C_{CARD} \leqq 10pF$ (1 card)
Clock frequency identification mode	f_{OD}	0[1] / 100	400	kHz	$C_{CARD} \leqq 10pF$ (1 card)
Clock low time	t_{WL}	10		ns	$C_{CARD} \leqq 10pF$ (1 card)
Clock high time	t_{WH}	10		ns	$C_{CARD} \leqq 10pF$ (1 card)
Clock rise time	t_{TLH}		10	ns	$C_{CARD} \leqq 10pF$ (1 card)
Clock fall time	t_{THL}		10	ns	$C_{CARD} \leqq 10pF$ (1 card)
Input CMD, DAT (referenced to CLK)					

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Parameter	Symbol	Min.	Max.	Unit	Remark
Input setup time	T_{ISU}	5		ns	$C_{CARD} \leqq 10pF$ (1 card)
Input hold time	T_{IH}	5		ns	$C_{CARD} \leqq 10pF$ (1 card)
Output CMD, DAT (referenced to CLK)					
Output delay time during data transfer mode	T_{ODLY}	0	14	ns	$C_L \leqq 40pF$ (1 card)
Output delay time during identification mode	T_{ODLY}	0	50	ns	$C_L \leqq 40pF$ (1 card)

2.2.5.5.2 High Speed Timing

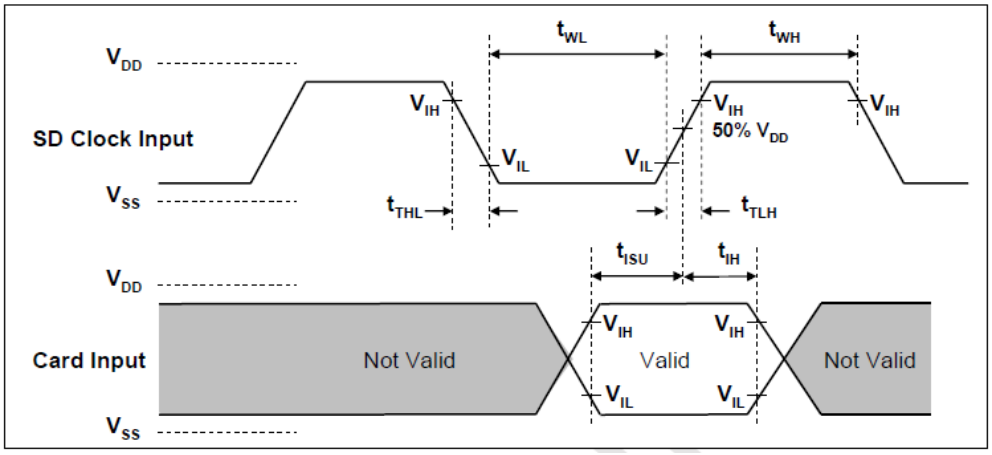

Figure 2-10. MSDC input timing diagram of high speed

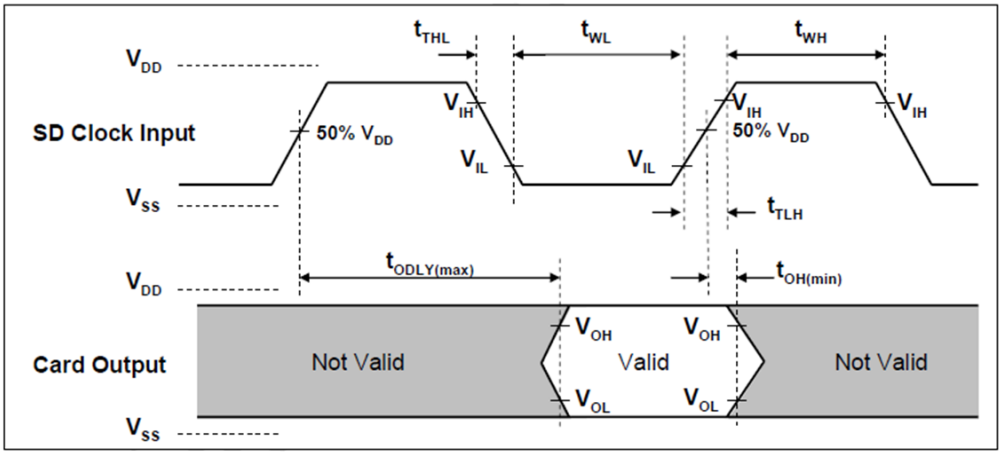

Figure 2-11. MSDC output timing diagram of high speed

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Table 2-20. MSDC AC timing parameters of high speed

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL}))					
Clock frequency data transfer mode	f_{PP}	0	50	MHz	$C_{CARD} \leqq 10pF$ (1 card)
Clock low time	t_{WL}	7		ns	$C_{CARD} \leqq 10pF$ (1 card)
Clock high time	t_{WH}	7		ns	$C_{CARD} \leqq 10pF$ (1 card)
Clock rise time	t_{TLH}		3	ns	$C_{CARD} \leqq 10pF$ (1 card)
Clock fall time	t_{THL}		3	ns	$C_{CARD} \leqq 10pF$ (1 card)
Input CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	6		ns	$C_{CARD} \leqq 10pF$ (1 card)
Input hold time	t_{IH}	2		ns	$C_{CARD} \leqq 10pF$ (1 card)
Output CMD, DAT (referenced to CLK)					
Output delay time during data transfer mode	t_{ODLY}		14	ns	$C_L \leqq 40pF$ (1 card)
Output hold time	t_{OH}	2.5		ns	$C_L \geqq 15pF$ (1 card)
Total system capacitance for each line	C_L		40	pF	1 card

2.2.5.5.3 SDR12/SDR25/SDR50/SDR104 Mode Timing

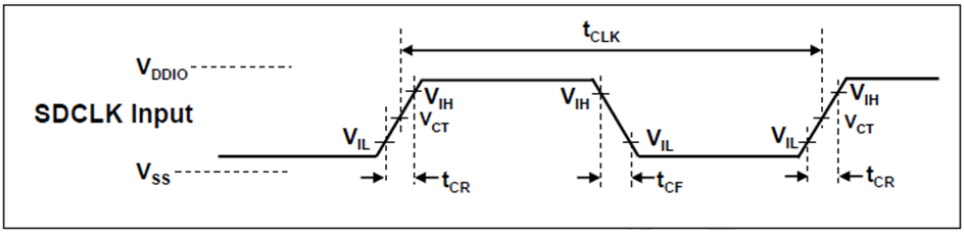

Figure 2-12. MSDC clock timing diagram of SDR12/SDR25/SDR50/SDR104 mode

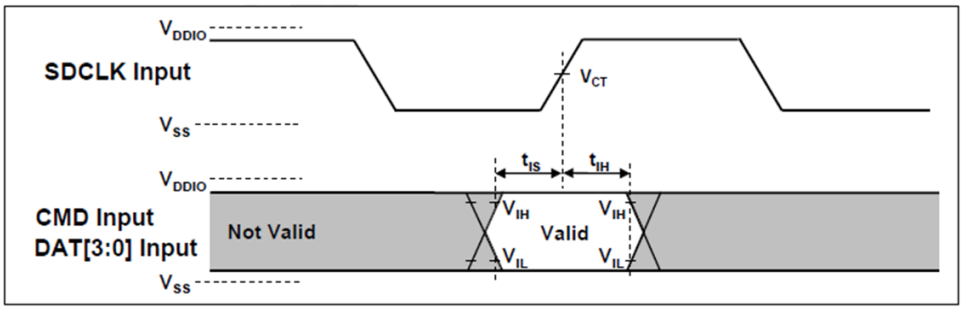

Figure 2-13. MSDC input timing diagram of SDR50/SDR104 mode

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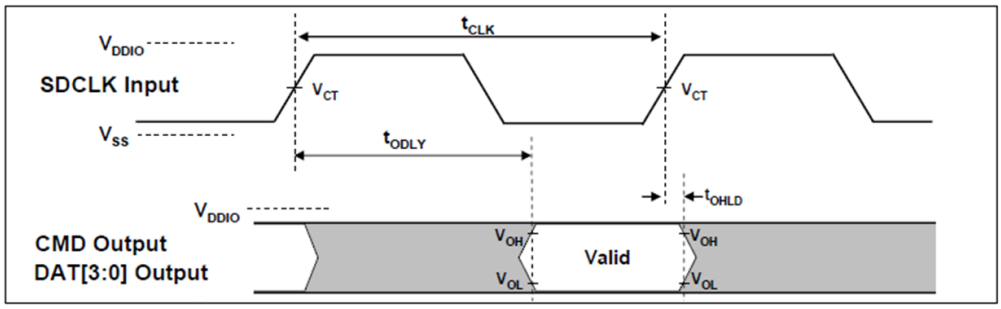

Figure 2-14. MSDC output timing diagram of fixed data window (SDR12/SDR25/SDR50)

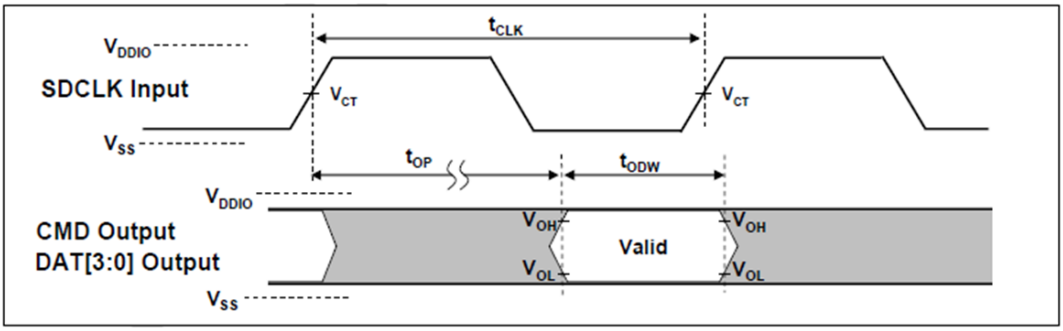

Figure 2-15. MSDC output timing diagram of variable window (SDR104)

Table 2-21. MSDC AC timing parameters of SDR12/SDR25/SDR50/SDR104 mode

Symbol	Min.	Max.	Unit	Remark
Clock CLK				
t_{CLK}	4.8	-	ns	208MHz (Max), Between rising edge, V_{CT}=0.975V
t_{CR}, t_{CF}	-	0.2*t_{CLK}	ns	t_{CR}, t_{CF} < 0.96ns (max) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF} < 2.00ns (max) at 100MHz, C_{CARD}=10pF The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	
Input CMD, DAT (SDR104)				
t_{IS}	1.40	-	ns	C_{CARD}=10pF, V_{CT}=0.975V
t_{IH}	0.80		ns	C_{CARD}=5pF, V_{CT}=0.975V
Input CMD, DAT (SDR50)				
t_{IS}	3.00	-	ns	C_{CARD}=10pF, V_{CT}=0.975V
t_{IH}	0.80	-	ns	C_{CARD}=5pF, V_{CT}=0.975V
Output CMD, DAT (SDR12/SDR25/SDR50)				
t_{ODLY}	-	7.5	ns	t_{CLK}≧10.0ns, C_L=30pF, using driver type B, for SDR50
t_{ODLY}		14	Ns	t_{CLK}≧20.0ns, C_L=40pF, using driver type B, for SDR25 and SDR12

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Symbol	Min.	Max.	Unit	Remark
T_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min), C_L=15pF
Output CMD, DAT (SDR104)				
t_{OP}	0	2	UI	Card output phase
Δ t_{OP}	-350	+1550	ps	Delay varioation due to temperature change after tunung.
t_{ODW}	0.6	-	UI	t_{ODW}=2.88ns at 208MHz

2.2.5.5.4 DDR50 Speed Mode Timing

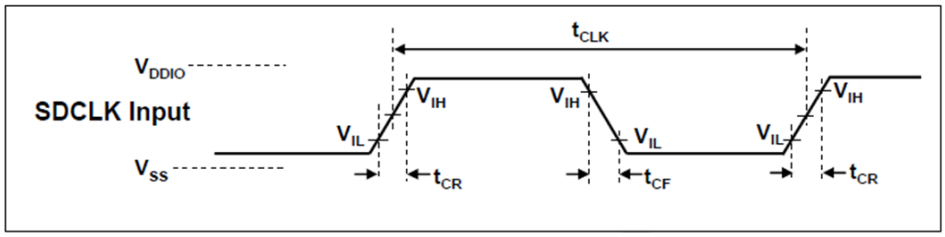

Figure 2-16. MSDC clock timing diagram of DDR50 speed mode.

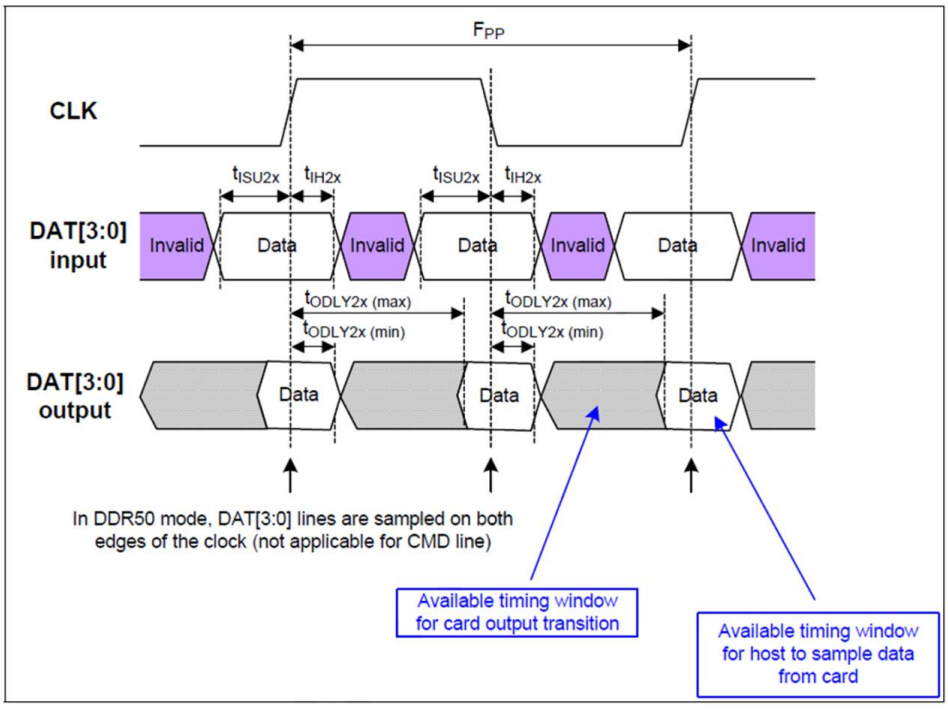

Figure 2-17. MSDC input/output timing diagram of DDR50 speed mode

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Table 2-22. MSDC AC timing parameters of DDR50 speed mode

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input setup time	t_{ISU}	6	-	ns	$C_{CARD} \leqq 10pF$ (1 card)
Input hold time	t_{IH}	0.8	-	ns	$C_{CARD} \leqq 10pF$ (1 card)
Output CMD (referenced to CLK rising edge)					
Output delay time during data transfer mode	t_{ODLY}	-	13.7	ns	$C_L \leqq 30pF$ (1 card)
Output hold time	t_{OH}	1.5	-	ns	$C_L \geqq 15pF$ (1 card)
Input DAT (referenced to CLK rising and falling edge)					
Input setup time	t_{ISU}	3	-	ns	$C_{CARD} \leqq 10pF$ (1 card)
Input hold time	t_{IH}	0.8	-	ns	$C_{CARD} \leqq 10pF$ (1 card)
Output DAT (referenced to CLK rising and falling edge)					
Output delay time during data transfer mode	t_{ODLY}	-	7.0	ns	$C_L \leqq 25pF$ (1 card)
Output hold time	t_{OH}	1.5	-	Ns	$C_L \geqq 15pF$ (1 card)

2.2.5.5.5 HS200 Speed Timing

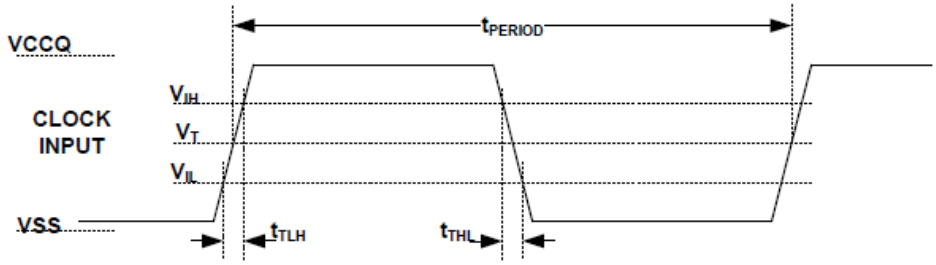
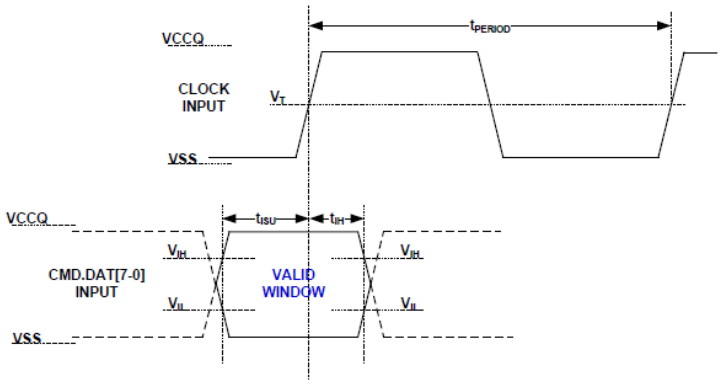


Figure 2-18. MSDC clock timing diagram of HS200



NOTE 1 t_{ISU} and t_{IH} are measured at V_{IL}(max.) and V_{IH}(min.).
NOTE 2 V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).

Figure 2-19. MSDC input timing diagram of HS200

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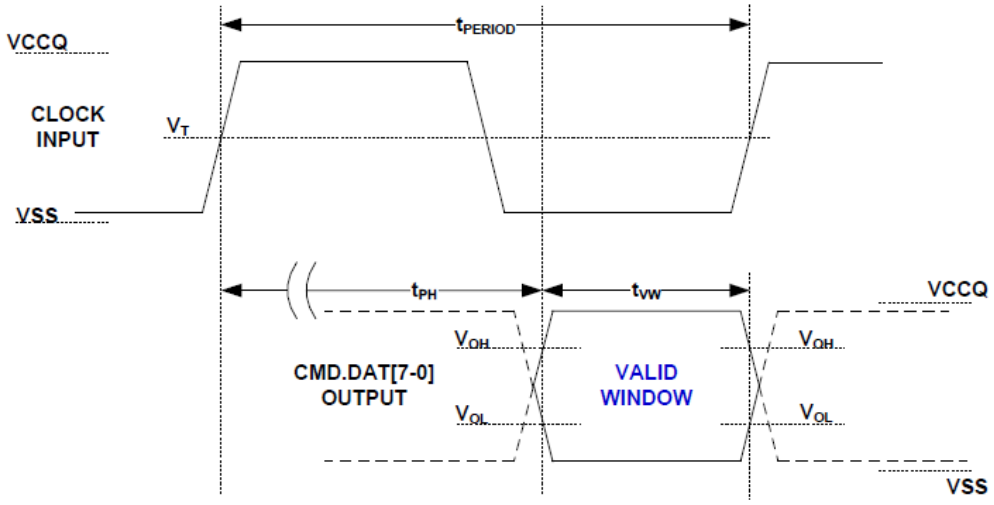

Figure 2-20. MSDC output timing diagram of HS200

Table 2-23. MSDC AC timing parameters of HS200

Symbol	Min.	Max.	Unit	Remark
Clock CLK				
t_{PERIOD}	5	-	ns	200MHz (Max), between rising edge
t_{TLH}, t_{THL}	-	0.2 * t_{PERIOD}	ns	t_{TLH}, t_{THL} < 1ns (max) at 200MHz, C_{DEVICE}=6pF The absolute maximum value of t_{TLH}, t_{THL} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	
Input CMD, DAT				
t_{ISU}	1.40	-	ns	C_{DEVICE}≦6pF
t_{IH}	0.80		ns	C_{DEVICE}≦6pF
Output CMD, DAT				
t_{PH}	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift.
Δ T_{PH}	-350 (Δ T=-20℃)	+1550 (Δ T=90℃)	ps	Delay varioation due to temperature change after tunung. Total allowable shift of output valid window (T_{VW}) from last system Tuning procedure Δ T_{PH} is 2600ps forΔ T from -25°C to 125°C during operation.
t_{VW}	0.575	-	UI	t_{VW}=2.88ns at 208MHz
Note: Unit Interval (UI) is one bit nominal time. For example, UI=5ns at 200MHz.				

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2.2.5.5.6 HS400 Speed Timing

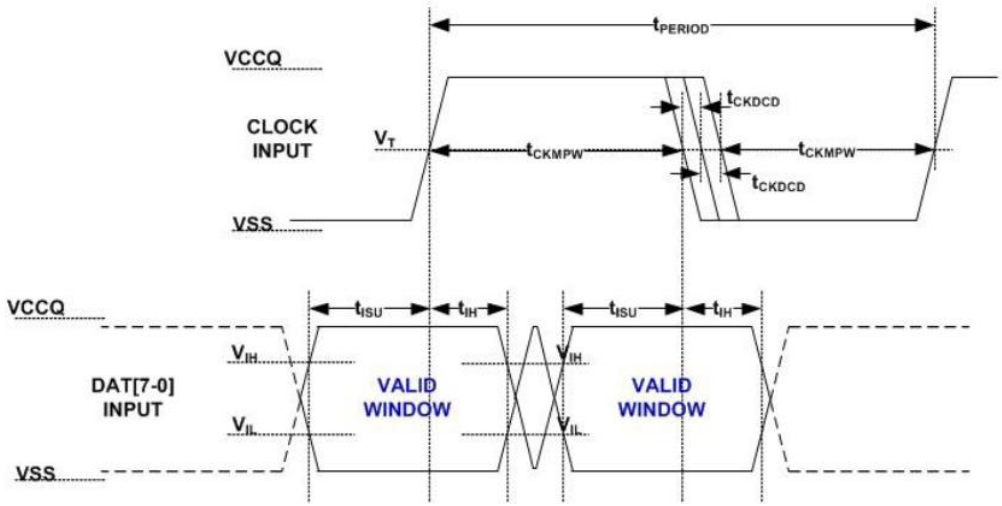

Figure 2-21. MSDC input timing diagram of HS400

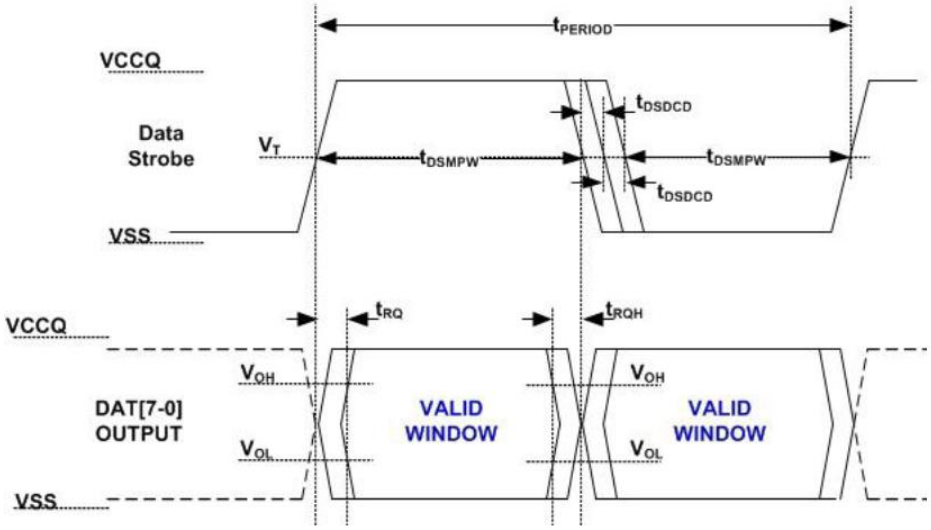

Figure 2-22. MSDC output timing diagram of HS400

Table 2-24. MSDC AC timing parameters of HS400

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CLK					
Cycle time data transfer mode	t_{PERIOD}	5		ns	200MHz (max), between rising edges. With respect to V_T
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL}
Duty cycle distortion	t_{CKDCD}	0.0	0.3	ns	Allowable deviation from an ideal 50% duty cycle. With respect to V_T. Includes

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Parameter	Symbol	Min.	Max.	Unit	Remark
					jitter, phase noise
Minimum pulse width	t_{CKMPW}	2.2		ns	With respect to V_T.
Input DAT (referenced to CLK)					
Input setup time	t_{ISUddr}	0.4		ns	$C_{Device} \leqq 6pF$. With respect to V_{IH}/V_{IL}
Input hold time	t_{IHddr}	0.4		ns	$C_{Device} \leqq 6pF$. With respect to V_{IH}/V_{IL}
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL}
Data Strobe					
Cycle time data transfer mode	t_{PERIOD}	5		ns	200MHz (max), between rising edges. With respect to V_T
Slew rate	SR	1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Duty cycle distortion	t_{DSDCD}	0.0	0.2	ns	Allowable deviation from the input CLK duty cycle distortion (t_{CKDCD}). With respect to V_T. Includes jitter, phase noise
Minimum pulse width	t_{DSMPW}	2.0		ns	With respect to V_T.
Read pre-amble	t_{RPRE}	0.4		t_{PERIOD}	Max value is specified by manufacturer. Value up to infinite is valid.
Read post-amble	t_{RPST}	0.4		t_{PERIOD}	Max value is specified by manufacturer. Value up to infinite is valid.
Input DAT (referenced to Data Strobe)					
Output skew	t_{RQ}		0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Output hold skew	t_{RQH}		0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Slew rate	SR	1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load

2.2.5.6 SIM AC Timing Characteristics

Table 2-25. SIM AC timing parameters

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
SIM1_SCLK						
Rise and fall time	DVDD28_SIM1 = 1.8V	T_{rise_fall}	N/A	50	50	Ns
Clock duty		Duty	47	50	53	%
Rise and fall time	DVDD28_SIM1 = 3.0V	T_{rise_fall}	N/A	18	18	ns
Clock duty		Duty	47	50	53	%
SIM1_SIO						
Rise and fall time	DVDD28_SIM1 = 1.8V	T_{rise_fall}	N/A	50	1000	ns
Rise and fall time	DVDD28_SIM1 = 3.0V	T_{rise_fall}	N/A	50	1000	ns

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Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
SIM1_SRST						
Rise and fall time	DVDD28_SIM1 = 1.8V	T_{rise_fall}	N/A	18	1000	ns
Rise and fall time	DVDD28_SIM1 = 3.0V	T_{rise_fall}	N/A	18	1000	ns
SIM2_SCLK						
Rise and fall time	DVDD28_SIM2 = 1.8V	T_{rise_fall}	N/A	50	50	ns
Clock duty		Duty	47	50	53	%
Rise and fall time	DVDD28_SIM2 = 3.0V	T_{rise_fall}	N/A	18	18	ns
Clock duty		Duty	47	50	53	%
SIM2_SIO						
Rise and fall time	DVDD28_SIM2 = 1.8V	T_{rise_fall}	N/A	50	1000	ns
Rise and fall time	DVDD28_SIM2 = 3.0V	T_{rise_fall}	N/A	50	1000	ns
SIM2_SRST						
Rise and fall time	DVDD28_SIM2 = 1.8V	T_{rise_fall}	N/A	18	1000	ns
Rise and fall time	DVDD28_SIM2 = 3.0V	T_{rise_fall}	N/A	18	1000	ns

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2.3 System Configuration

2.3.1 Mode Selection

Table 2-26. Mode selection

Pin name	Description
[0] AUD_DAT_MOSI [1] PWRAP_SPI0_CSN	00: Use CAM pins for legacy JTAG 01: Use MSDC1 pins for legacy JTAG 10: No dedicate JTAG 11: Use SPI pin for legacy JTAG

2.3.2 Constant Tie Pins

Table 2-27. Constant tied pins

Pin name	Description
TESTMODE	Test mode (tied to GND)

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2.4 Power-on Sequence

The power-on/off sequence is shown in the following figure:

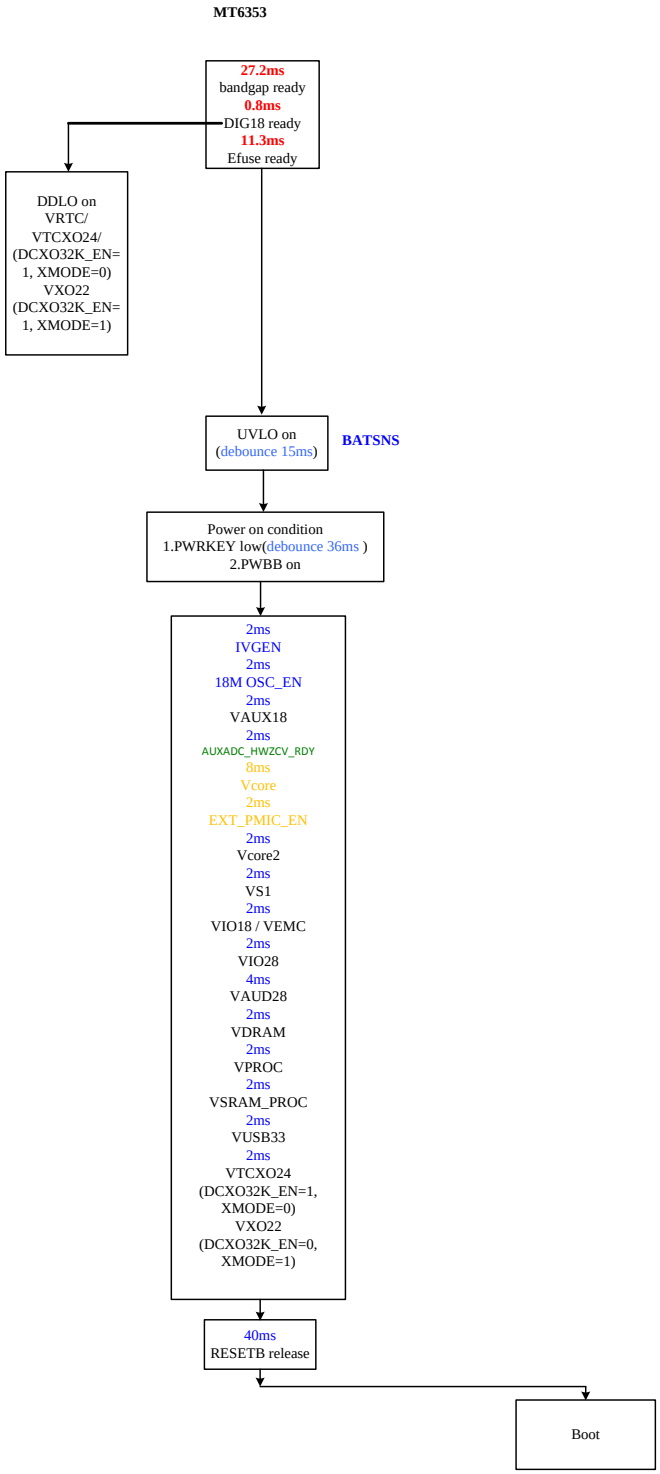

Figure 2-23. Power on sequence

Refer to PMIC datasheet for detailed timing sequence.

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2.5 Analog Baseband

2.5.1 Introduction

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are some dedicated interfaces for data transfer. The common control interface translates the APB bus write and read cycle for specific addresses related to analog front-end control. In the write or read of any of these control registers, there is a latency associated with the transfer of data to or from the analog front-end. Dedicated data interface of each analog block is implemented in the corresponding digital block. An analog block includes the following analog functions for the complete GSM/GPRS/WCDMA/LTE base-band signal processing:

- Base-band Rx: For I/Q channels base-band A/D conversion
- Base-band Tx: For I/Q channels base-band D/A conversion and smoothing filtering
- ETDAC: A DAC output to control buck-converter for envelop tracking technique.
- DETADC: A ADC that detects calibration, thermal data from RF chip.
- RF control: A DAC for automatic power control (APC) is included.The outputs are provided to external RF power amplifiers.
- Auxiliary ADC: Provides an ADC for auxiliary analog functions monitoring.
- Clock generation: One clock-squarer for shaping the input sinwave clock and 20 PLLs providing clock signals to base-band TRx, DSP, MCU, USB, MSDC units.

2.5.2 Features

The analog blocks include the following analog functions for complete GSM/GPRS/WCDMA base-band signal processing:

- BBRX
- BBTX
- ETDAC
- DETADC
- APC-DAC
- AUXADC
- Phase locked loop
- Temperature sensor

2.5.3 Block Diagram

2.5.3.1 BBRX

2.5.3.1.1 Block Descriptions

The receiver (Rx) performs baseband I/Q channels downlink analog-to-digital conversion:

1. Analog input multiplexer: For each channel, a 2-input multiplexer is included.

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2. A/D converter: 8 high performance sigma-delta ADCs perform I/Q digitization for further digital signal processing.

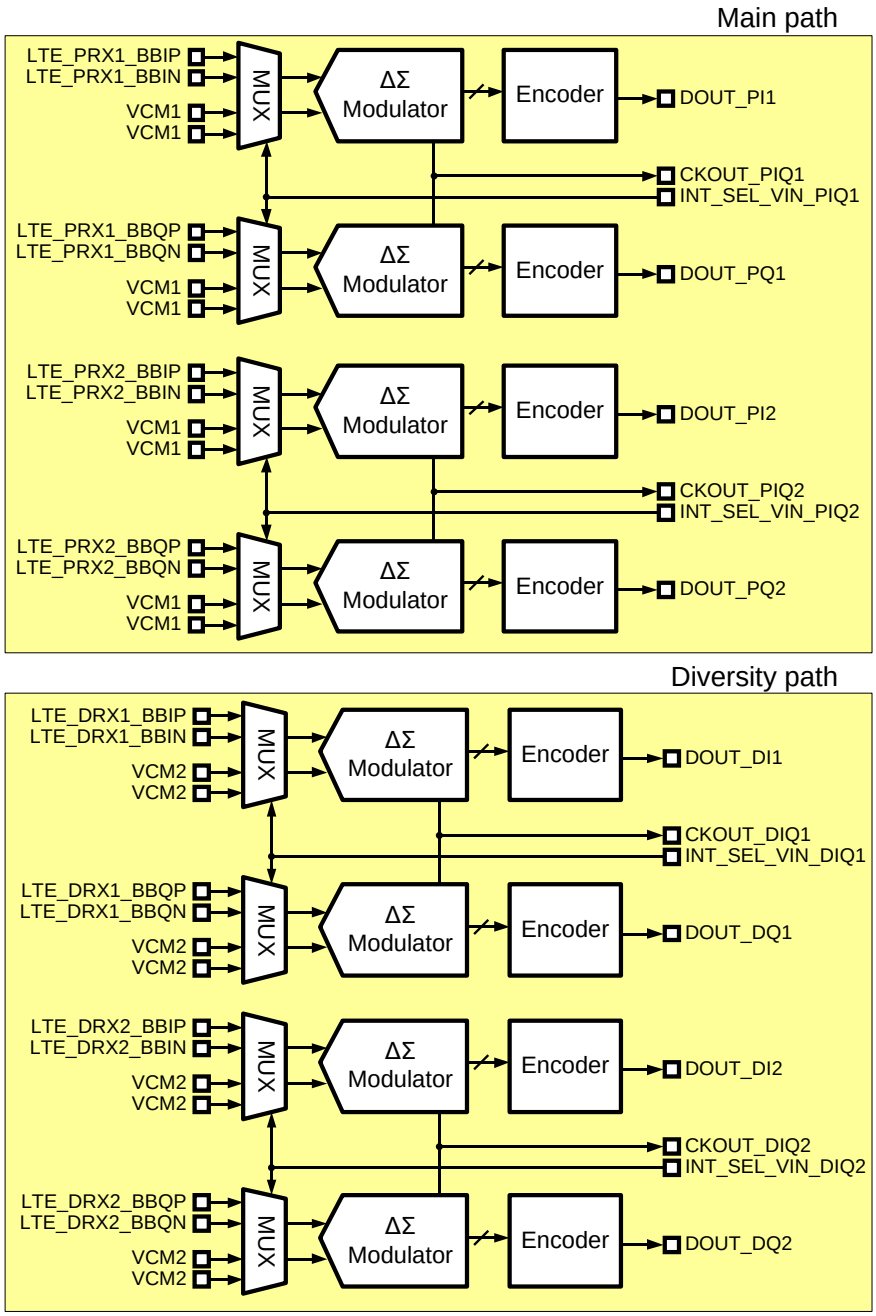

Figure 2-24. Block diagram of BBRX-ADC

2.5.3.1.2 Functional Specifications

See the table below for the functional specifications of the base-band downlink receiver.

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Table 2-28. Baseband downlink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Differential analog input voltage (peak-to-peak)			2.4	V
VCM	Common mode input voltage	0.65	0.7	0.75	V
FC	Input clock frequency	208		832	MHz
	Input clock duty cycle	49.5	50	50.5	%
RIN	Differential input resistance	2.8		20.8	kΩ
FS	Output sampling rate	208		832	MSPS
VOS	Differential input referred offset			10	mV
SIN	Signal to in-band noise	70		89	dB
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	–20		80	°C
	Current consumption (per channel) – Power-up – Power-down		 12.3 10		 mA uA

2.5.3.2 BBTX

2.5.3.2.1 Block Descriptions

BBTX includes two channel DACs with the 1st order low pass filter. The DACs are PMOS current-steering topology with NMOS constant sinking current and the active RC filter performs current to voltage buffer.

The bitwidth of DACs is 11-bit which is encoded into 7 bits of thermometer code and 8 binary code by digital hard macro inside BBTX layout. The encoded bits are timing synchronized by D-type flip-flop which is toggled by the analog local clock. The MD-PLL delivers 832MHz differential clock to BBTX. A clock divider translates the 832MHz to 416MHz for DACs and AFIFO inside mixedsys.

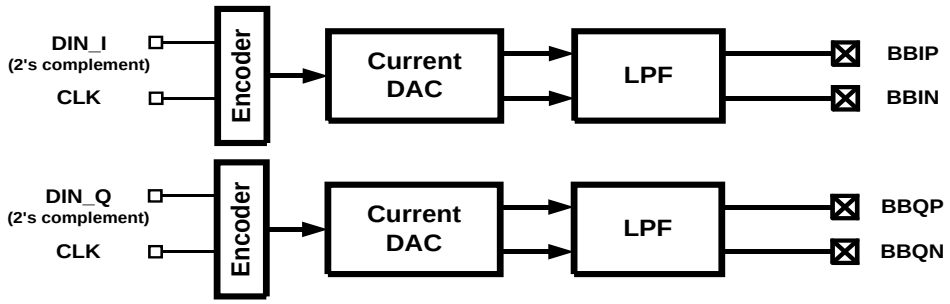

Figure 2-25. Block diagram of BBTX

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2.5.3.2.2 Functional Specifications

Table 2-29. BBTX specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{ocm}	DC output common mode voltage	0.615	0.65	0.685	V
V_{fs}	DAC output swing		2100		mV
N	DAC resolution		11.0		bit
F_s	Sampling clock		416		MHz
G_{mis}	3-sigma I/Q gain mismatch	-0.2		0.2	dB
V_{os}	3-sigma output differential DC offset			20	mV
F_{3dB}	3dB corner freq.		20/40		MHz
Dinb	Inband Droop		0.1		dB
DNL			1		LSB
INL			2		LSB
IM3	In-band two-tone test swing V1=V2=290/sqrt(2) mV		-58	-55	dBc
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption (per channel) – Power-up – Power-down		 8 10		 mA uA

2.5.3.3 ETDAC

2.5.3.3.1 Block Descriptions

The ETDAC (Envelope Tracking DAC) provides analog envelope signal to external ET modulator. It includes:

1. 11-bit D/A converter: Converts digital modulated signals to analog domain. The input to the DAC is sampled at 416MHz rate with the 11-bit resolution.
2. Smoothing filter: The low-pass filter performs smoothing function for DAC output signals with a 20/40MHz 1st-order Butterworth frequency response.

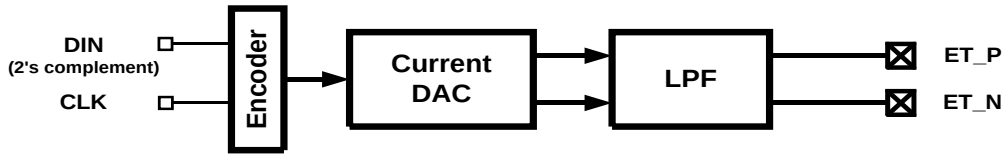

Figure 2-26. Block diagram of ETDAC

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2.5.3.3.2 Functional Specfications

Table 2-30. ETDAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		11		Bit
FS	Sampling rate		416		MSPS
IM3	3rd order Intermodulation distortion		-60	-50	dB
	Output swing (full swing)		2		Vppd
VOCM	Output CM voltage	0.6		0.85	V
	Output capacitance (single-ended)			10	PF
	Output resistance (differential)		100		KΩ
DNL	Differential nonlinearity	-1		+1	LSB
INL	Integral nonlinearity	-2		+2	LSB
FCUT	Filter -3dB cutoff frequency (calibrated)		20/40		MHz
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption – Power-up – Power-down		 4.5 10		 mA uA

2.5.3.4 DETADC

2.5.3.4.1 Block Descriptions

The DETADC (DETection ADC) performs I/Q-channel path detections from RF chip:

1. Input buffer: For each channel, isolates RF signals from high-speed ADCs.
2. 12-bit A/D converters: Convert the detected signals to 12-bit digital data sampled at 104MHz.

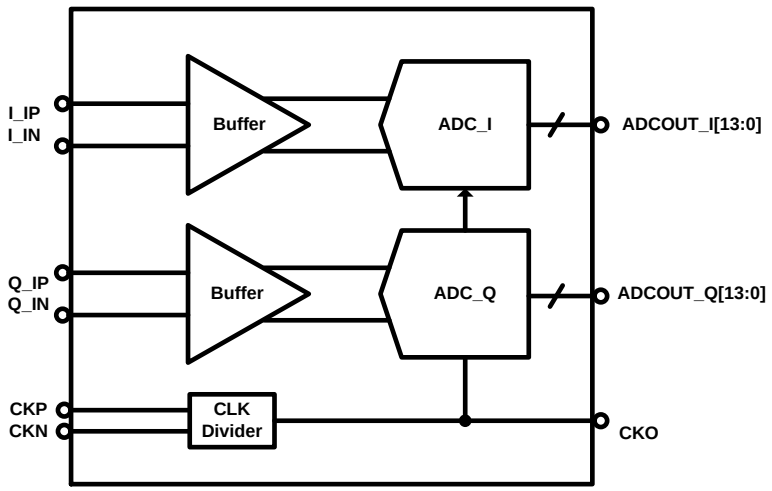

Figure 2-27. Block diagram of DETADC

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2.5.3.4.2 Functional Specifications

See the table below for the functional specifications of DETADC

Table 2-31. DETADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Analog input voltage (differential peak-to-peak)		1.2		V
VCM	Common mode input voltage		0.55		V
RIN	Input resistance	1.6	2	2.4	kΩ
CIN	Input capacitance		2	3	pF
FS	Sampling rate		104		MSPS
VOS	Differential input referred offset		30		mV
SNDR	Signal-to-noise-and-distortion ratio		60		dB
DR	Dynamic range		63		dB
THD	Total harmonic distortion		-66		dBc
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	–20		80	°C
	Current consumption (per channel) – Power-up – Power-down		 6 1		 mA uA

2.5.3.5 APC-DAC

2.5.3.5.1 Block Descriptions

See the figure below. APC-DAC is designed to produce a single-ended output signal at APC pin.

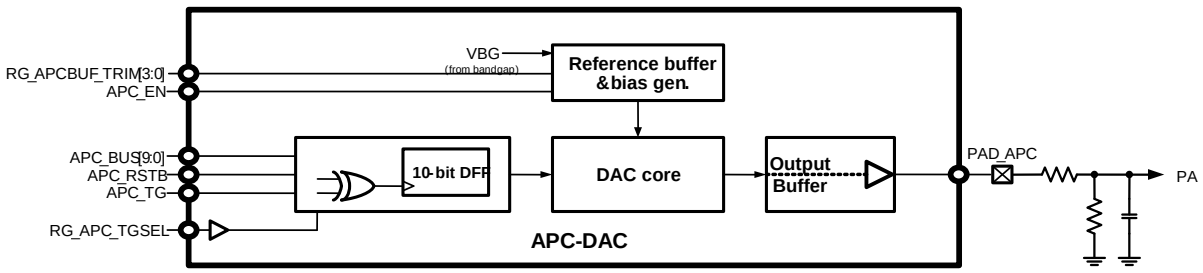

Figure 2-28. Block diagram of APC-DAC

2.5.3.5.2 Functional Specifications

See the table below for the functional specifications of the APC-DAC.

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Table 2-32. APC-DAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
F_S	Clock rate	1.0833		2.1666	MS/s
T_S	Settling time (99% full-swing settling)			5	us
$V_{O,max}$	Maximum output			AVDD – 0.2	V
C_L	Output loading capacitance		220	2200	pF
DNL	Differential nonlinearity (code 30 ~ 970)		±1.0		LSB
INL	Integral nonlinearity (code 30 ~ 970)		±2.0		LSB
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	–20		85	°C
	Current consumption – Power-up – Power-down		 450 20		 uA uA

2.5.3.6 AUXADC

2.5.3.6.1 Block Descriptions

The auxiliary ADC includes the following functional blocks:

1. Analog multiplexer: Selects signal from one of the auxiliary input channels. There are 16 input channels of AUXADC. Some are for internal voltage measurement and some for external voltage measurement. Environmental messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
2. 12-bit A/D converter: Converts the multiplexed input signal to 12-bit digital data.

2.5.3.6.2 Functional Specifications

See the table below for the functional specifications of auxiliary ADC.

Table 2-33. AUXADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		12		Bit
FC	Clock rate		3.25		MHz
FS	Sampling rate @ N-Bit		4/(N+8)		MSPS
	Input swing	0.05		1.45	V
CIN	Input capacitance Unselected channel Selected channel (PAD loading excluded)		 50 4		 fF pF
	Clock latency		N+8		1/FC

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Symbol	Parameter	Min.	Typ.	Max.	Unit
DNL	Differential nonlinearity		+1.0/-1.0		LSB
INL	Integral nonlinearity		+2.0/-2.0		LSB
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Accuracy			+-10	mV

2.5.3.7 Clock Squarer

2.5.3.7.1 Block Descriptions

For most VCXO, the output clock waveform is sinusoidal with too small amplitude (about several hundred mV) to make digital circuits function well. The clock squarer is designed to convert such a small signal to a rail-to-rail clock signal with excellent duty-cycle.

2.5.3.7.2 Functional Specifications

See the table below for the functional specifications of clock squarer.

Table 2-34. Clock squarer specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency	13	26		MHz
Fout	Output clock frequency	13	26		MHz
Vin	Input signal amplitude	350	500	1,000	mVpp
DcycIN	Input signal duty cycle		50		%
DcycOUT	Output signal duty cycle	DcycIN-5		DcycIN+5	%
TR	Rise time on pin CLKSQOUT			5	ns/pF
TF	Fall time on pin CLKSQOUT			5	ns/pF
	Maximum Positive Overshoot			1.98	V
	Minimum Negative Overshoot	-0.1			V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		650		uA

2.5.3.8 Temperature Sensor

2.5.3.8.1 Block Descriptions

In order to monitor the temperature of CPUs, several temperature sensors are provided. The temperature sensor is made of substrate BJT in the CMOS process. The voltage output of temperature sensor is measured by AUXADC.

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2.5.3.8.2 Functional Specifications

See the table below for the functional specifications of temperature sensor.

Table 2-35. Temperature sensor specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Resolution		0.15		°C
	Temperature range	0		85	°C
	Accuracy	-5		5	°C
	Active current		60		uA
	Quiescent current		10		uA

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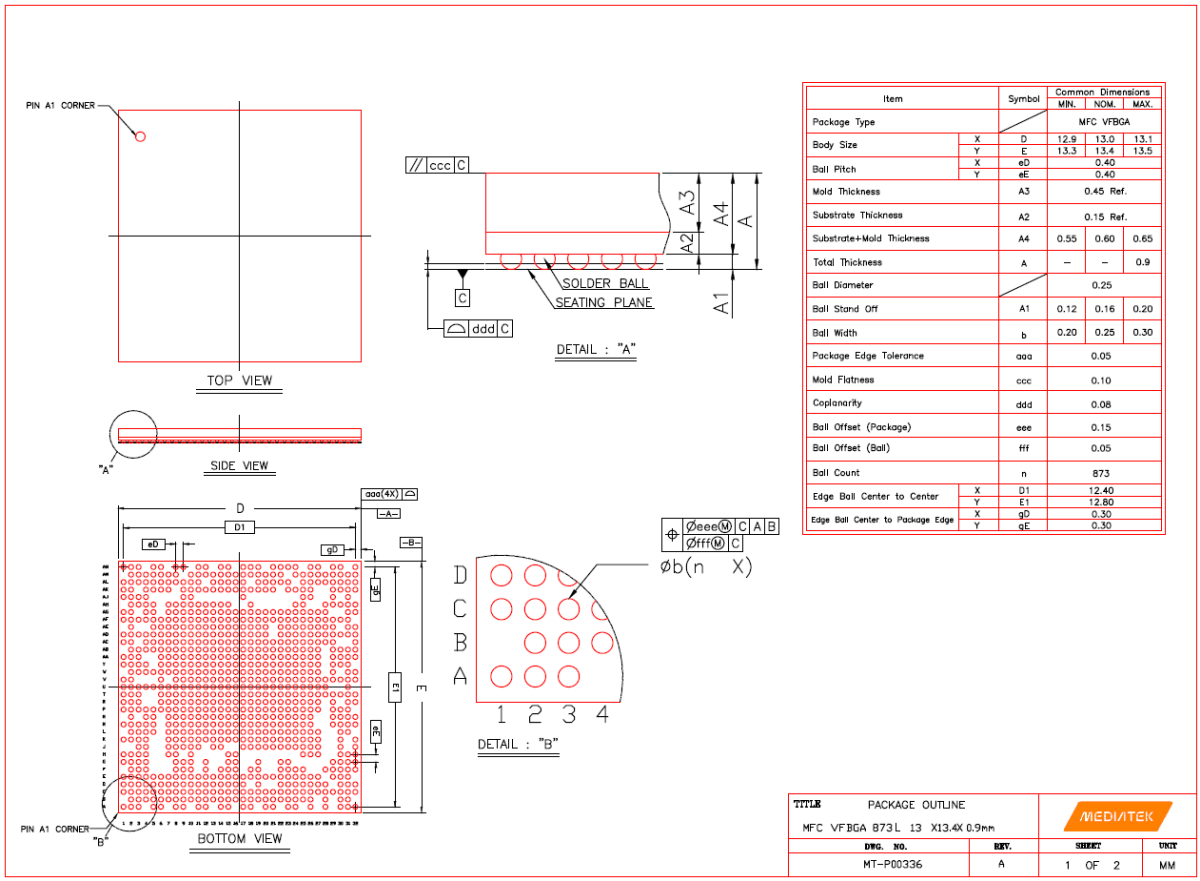
2.6 Package Information

2.6.1 Package Outlines



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type			MFC VFBGA		
Body Size	X	D	12.9	13.0	13.1
	Y	E	13.3	13.4	13.5
Ball Pitch	X	eD		0.40	
	Y	eE		0.40	
Mold Thickness		A3		0.45 Ref.	
Substrate Thickness		A2		0.15 Ref.	
Substrate+Mold Thickness		A4	0.55	0.60	0.65
Total Thickness		A	–	–	0.9
Ball Diameter				0.25	
Ball Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa		0.05	
Mold Flatness		ccc		0.10	
Coplanarity		ddd		0.08	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		873	
Edge Ball Center to Center	X	D1		12.40	
	Y	E1		12.80	
Edge Ball Center to Package Edge	X	gD		0.30	
	Y	gE		0.30	

TITLE	PACKAGE OUTLINE		
MFC VFBGA 873L 13 X13.4X 0.9mm			
DWG. NO.	REV.	SHEET	UNIT
MT-P00336	A	1 OF 2	MM

Figure 2-29. Outlines and dimensions of TFBGA 13mm*13.4mm, 873-ball, 0.4mm pitch package

2.6.2 Thermal Operating Specifications

Table 2-36. Thermal operating specifications

Symbol	Description	Value	Unit	Note
	Max. operating junction temperature	125	°C	
	Package thermal resistances in nature convection	37.65	°C/Watt	

2.6.3 Lead-free Packaging

The chip is provided in a lead-free package and meets RoHS requirements.

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2.6.4 MSL

MSL of this chip is 3.

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2.7 Power Delivery Network

Table 2-37. PDN specifications

Power rail	R_{DC} (mohm)	Remote_R_{DC} (mohm)	Low frequency band ZAC (mΩ)	High frequency band ZAC (mΩ)
			@low frequency band	@high frequency band
DVFS1	14	0.8	11@0.2MHz -> 11@10MHz	11@10MHz -> 94@120MHz
VSRAM	130	x	130@0Hz -> 130@5MHz	130@5MHz -> 4700@50MHz
VEMI (DDR)	40	x	40@0Hz -> 40@45MHz	40@45MHz -> 210@250MHz
VEMI (DDR)@DRAM	28	x	28@0Hz -> 28@35MHz	28@35MHz -> 71@100MHz
VCORE	17	5.0	20@0.2MHz -> 20@9MHz	20@9MHz -> 110@55MHz
VGPU	16	3.5	16@0.2MHz -> 16@6MHz	16@6MHz -> 230@90MHz
VMODEM+VMDSRAM	17	6.0	21@0.2MHz -> 21@9MHz	21@9MHz -> 155@80MHz
VMD1	34	14.0	39@0.2MHz -> 39@11MHz	39@11MHz -> 250@85MHz

Note: Refer to document "MT6750_PDN_Checking_Notice.pdf" on DCC for more design concepts.

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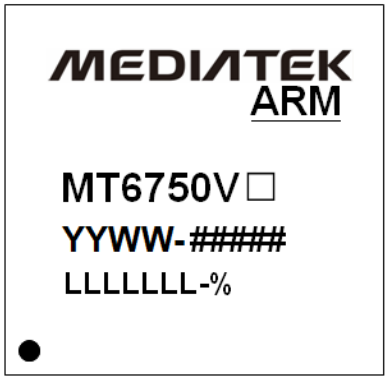
2.8 Ordering Information

2.8.1 Top Marking Definition



- □: "-E" Engineering sample
- YYWW: Date code
- #####: Subcontractor code
- LLLLLLL: Die lot No.

Figure 2-30. Top marking of MT6750

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3 MCU and Bus Fabric

3.1 MCU System

3.1.1 Introduction

MCUSYS is a subsystem responsible for running operating system and application programs in MT6750. It comprises with four Cortex-A53 cores into 1 cluster, and Generic Interrupt Controller (GIC). A 325MHz 128-bit AXI bus is directly connected to External Memory Interface (EMI) to minimize the access latency to DRAM and provide sufficient memory bandwidth. The peripheral system and on-chip storage are bridged through a 182MHz/64-bit AXI bus, and the outstanding capability of AXI protocol allows the system to exploit its maximum throughput from eight CPU cores.

MCUSYS supports DVFS technology which allows CPU to run at different frequency/voltage configurations for different application requirements. When in standby mode, MCUSYS can be completely shut down to further save power consumption and optimize the battery usage on mobile devices.

3.1.2 Features

3.1.2.1 Cluster 0, Cortex-A53 Specifications

- Four-core ARM® Cortex-A53 MPCore™ operating at 1GHz
- Supports ARMv8-A architecture for both 32 and 64-bit execution state
- Supports NEON multimedia processing engine with SIMDv2/VFPv4 ISA
- Optionally supports ARMv8 Cryptographic extension
- 32KB L1 I-cache and 32KB L1 D-cache
- 512KB unified L2 cache for CPU cluster
- DVFS technology with adaptive operating voltage from 0.95V to 1.25V
- Supports ARM Jazelle technology

3.1.2.2 Cluster 1, Cortex-A53 Specifications

- Four-core ARM® Cortex-A53 MPCore™ operating at 1.5GHz
- Supports ARMv8-A architecture for both 32 and 64-bit execution state
- Supports NEON multimedia processing engine with SIMDv2/VFPv4 ISA
- Optionally supports ARMv8 Cryptographic extension
- 32KB L1 I-cache and 32KB L1 D-cache
- 512KB unified L2 cache for CPU cluster
- DVFS technology with adaptive operating voltage from 0.95V to 1.25V
- Supports ARM Jazelle technology

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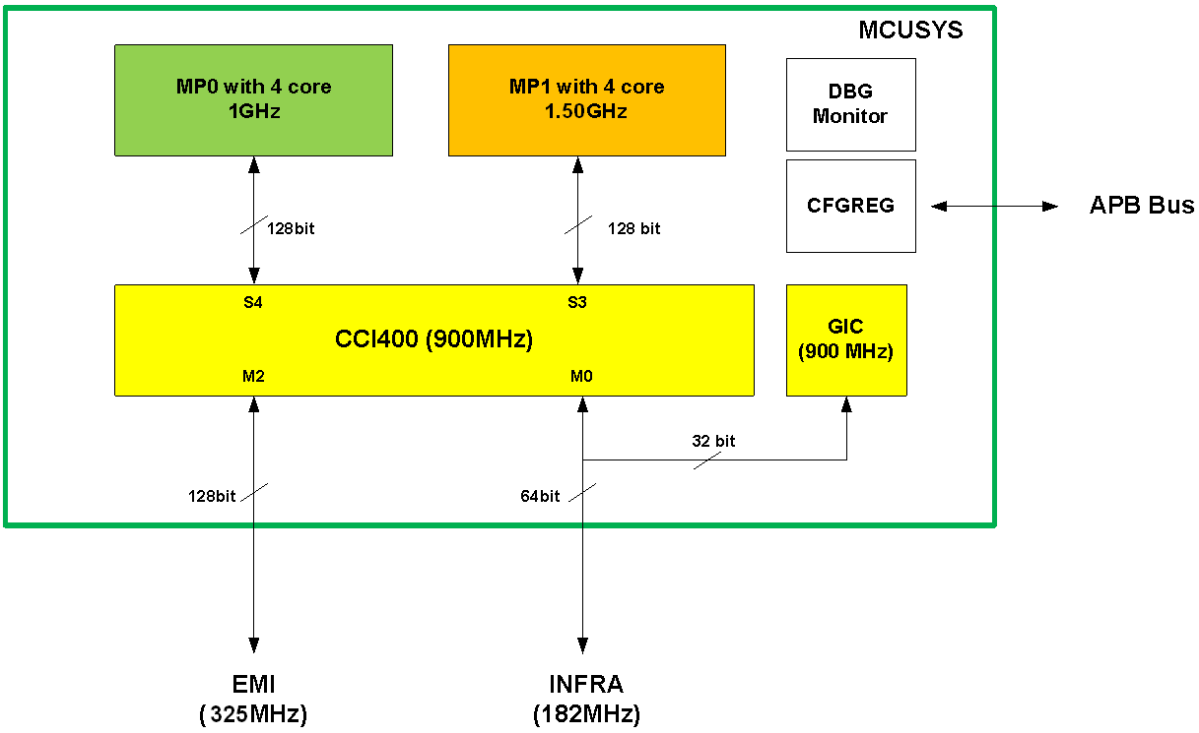
3.1.2.3 Clock Modes between Clusters and AXI Bus Fabric

The CPU and AXI bus fabric are asynchronous. CPU and AXI bus fabric also support Dynamic Clock Management (DCM) mechanism to dynamically turn off the clock when no transactions are on the bus interface. CPU, cluster and AXI bus fabric can also support DVFS technology to lower power consumption.

3.1.3 Block Diagram



3.1.4 Interrupt Controller

MT6750 uses ARM GIC400 interrupt controller for interrupt management. GIC400 is embedded inside MCUSYS alongside CCI to minimize the interrupt handling latency. For the interrupt connected to GIC400, see the table below for details. The GIC interrupts are separated into 2 categories, the Private Peripheral Interrupts (PPI) and Shared Peripheral Interrupts (SPI). PPI occupies the first 32 interrupt slots in GIC and are banked for each CPU core. SPI begins from the 33rd interrupt and is shared by all CPU cores.

Table 3-1. Interrupt request list for Cortex-A53

GIC ID	Interrupt source/name	Polarity	Trigger type
0	Software generated interrupt 0	H	Edge
1	Software generated interrupt 1	H	Edge
2	Software generated interrupt 2	H	Edge

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GIC ID	Interrupt source/name	Polarity	Trigger type
3	Software generated interrupt 3	H	Edge
4	Software generated interrupt 4	H	Edge
5	Software generated interrupt 5	H	Edge
6	Software generated interrupt 6	H	Edge
7	Software generated interrupt 7	H	Edge
8	Software generated interrupt 8	H	Edge
9	Software generated interrupt 9	H	Edge
10	Software generated interrupt 10	H	Edge
11	Software generated interrupt 11	H	Edge
12	Software generated interrupt 12	H	Edge
13	Software generated interrupt 13	H	Edge
14	Software generated interrupt 14	H	Edge
15	Software generated interrupt 15	H	Edge
16	(Reserved)	-	-
17	(Reserved)	-	-
18	(Reserved)	-	-
19	(Reserved)	-	-
20	(Reserved)	-	-
21	(Reserved)	-	-
22	(Reserved)	-	-
23	(Reserved)	-	-
24	(Reserved)	-	-
25	Virtual maintenance interrupt	L	Level
26	Hypervisor timer event	L	Level
27	Virtual timer event	L	Level
28	Legacy nFIQ	L	Level
29	Secure physical timer event	L	Level
30	Non-secure physical timer event	L	Level
31	Legacy nIRQ	L	Level
32	mp0_NIRQOUT[0]	L	Level
33	mp0_NIRQOUT[1]	L	Level
34	mp0_NIRQOUT[2]	L	Level
35	mp0_NIRQOUT[3]	L	Level
36	mp1_NIRQOUT[0]	L	Level
37	mp1_NIRQOUT[1]	L	Level
38	mp1_NIRQOUT[2]	L	Level
39	mp1_NIRQOUT[3]	L	Level
40	mp0_NPMUIRQ[0]	L	Level
41	mp0_NPMUIRQ[1]	L	Level
42	mp0_NPMUIRQ[2]	L	Level
43	mp0_NPMUIRQ[3]	L	Level

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GIC ID	Interrupt source/name	Polarity	Trigger type
44	mp1_NPMUIRQ[0]	L	Level
45	mp1_NPMUIRQ[1]	L	Level
46	mp1_NPMUIRQ[2]	L	Level
47	mp1_NPMUIRQ[3]	L	Level
48	mp0_NCNTHPIRQ[0]	L	Level
49	mp0_NCNTHPIRQ[1]	L	Level
50	mp0_NCNTHPIRQ[2]	L	Level
51	mp0_NCNTHPIRQ[3]	L	Level
52	mp1_NCNTHPIRQ[0]	L	Level
53	mp1_NCNTHPIRQ[1]	L	Level
54	mp1_NCNTHPIRQ[2]	L	Level
55	mp1_NCNTHPIRQ[3]	L	Level
56	mp0_NCNTVIRQ[0]	L	Level
57	mp0_NCNTVIRQ[1]	L	Level
58	mp0_NCNTVIRQ[2]	L	Level
59	mp0_NCNTVIRQ[3]	L	Level
60	mp1_NCNTVIRQ[0]	L	Level
61	mp1_NCNTVIRQ[1]	L	Level
62	mp1_NCNTVIRQ[2]	L	Level
63	mp1_NCNTVIRQ[3]	L	Level
64	mp0_NCNTPSIRQ[0]	L	Level
65	mp0_NCNTPSIRQ[1]	L	Level
66	mp0_NCNTPSIRQ[2]	L	Level
67	mp0_NCNTPSIRQ[3]	L	Level
68	mp1_NCNTPSIRQ[0]	L	Level
69	mp1_NCNTPSIRQ[1]	L	Level
70	mp1_NCNTPSIRQ[2]	L	Level
71	mp1_NCNTPSIRQ[3]	L	Level
72	mp0_NCNTPNSIRQ[0]	L	Level
73	mp0_NCNTPNSIRQ[1]	L	Level
74	mp0_NCNTPNSIRQ[2]	L	Level
75	mp0_NCNTPNSIRQ[3]	L	Level
76	mp1_NCNTPNSIRQ[0]	L	Level
77	mp1_NCNTPNSIRQ[1]	L	Level
78	mp1_NCNTPNSIRQ[2]	L	Level
79	mp1_NCNTPNSIRQ[3]	L	Level
80	mp0_NEXTERRIRQ	L	Level
81	mp1_NEXTERRIRQ	L	Level
82	mp0_CTIIRQ_SYNC[0]	L	Level
83	mp0_CTIIRQ_SYNC[1]	L	Level

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GIC ID	Interrupt source/name	Polarity	Trigger type
84	mp0_CTIIRQ_SYNC[2]	L	Level
85	mp0_CTIIRQ_SYNC[3]	L	Level
86	mp1_CTIIRQ_SYNC[0]	L	Level
87	mp1_CTIIRQ_SYNC[1]	L	Level
88	mp1_CTIIRQ_SYNC[2]	L	Level
89	mp1_CTIIRQ_SYNC[3]	L	Level
90	CCI_NEVNTCNTOVERFLOW[0]	L	Level
91	CCI_NEVNTCNTOVERFLOW[1]	L	Level
92	CCI_NEVNTCNTOVERFLOW[2]	L	Level
93	CCI_NEVNTCNTOVERFLOW[3]	L	Level
94	CCI_NEVNTCNTOVERFLOW[4]	L	Level
95	CCI_NERRORIRQ	L	Level
96	xgpt_irq[0]	H	Level
97	xgpt_irq[1]	H	Level
98	xgpt_irq[2]	H	Level
99	xgpt_irq[3]	H	Level
100	xgpt_irq[4]	H	Level
101	xgpt_irq[5]	H	Level
102	xgpt_irq[6]	H	Level
103	xgpt_irq[7]	H	Level
104	(Reserved)	-	-
105	usb_mcu_int_b_1p	L	Level
106	ts_irq_b	L	Edge
107	ts_batch_irq_b	L	Edge
108	lowbattery_irq_b	L	Edge
109	pwm_irq_b	L	Level
110	ptp_therm_irq_b	L	Level
111	msdc0_irq_b	L	Level
112	msdc1_irq_b	L	Level
113	msdc2_irq_b	L	Level
114	msdc3_irq_b	L	Level
115	md2spm_dvfs_con[5]	H	Level
116	i2c0_irqb	L	Level
117	i2c1_irqb	L	Level
118	i2c2_irqb	L	Level
119	i2c3_irqb	L	Level
120	i2c4_irqb	L	Level
121	md2spm_dvfs_con[6]	H	Level
122	md2spm_dvfs_con[7]	H	Level
123	uart0_irq_b	L	Level
124	uart1_irq_b	L	Level
125	uart2_irq_b	L	Level

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GIC ID	Interrupt source/name	Polarity	Trigger type
126	uart3_irq_b	L	Level
127	uart4_irq_b	L	Level
128	1'b1	L	Level
129	dma_irq[0]	L	Level
130	dma_irq[1]	L	Level
131	dma_irq[2]	L	Level
132	dma_irq[3]	L	Level
133	dma_irq[4]	L	Level
134	dma_irq[5]	L	Level
135	dma_irq[6]	L	Level
136	dma_irq[7]	L	Level
137	dma_irq[8]	L	Level
138	dma_irq[9]	L	Level
139	dma_irq[10]	L	Level
140	dma_irq[11]	L	Level
141	dma_irq[12]	L	Level
142	dma_irq[13]	L	Level
143	dma_irq[14]	L	Level
144	btif_irq_b	L	Level
145	cq_gdma_irq_b[0]	L	Level
146	cq_gdma_irq_b[1]	L	Level
147	cq_gdma_irq_b[2]	L	Level
148	dma_irq[15]	L	Level
149	emi_bw_int	H	Level
150	spi0_irq_b	L	Level
151	msdc0_wakeup_ps	H	Edge
152	msdc1_wakeup_ps	H	Edge
153	msdc2_wakeup_ps	H	Edge
154	spi1_irq_b	L	Level
155	(Reserved)	-	-
156	msdc3_wakeup_ps	H	Edge
157	ptp_fsm_irq_b	L	Level
158	disppwm_irq_b	L	Level
159	irtx_irq_b	L	Level
160	wdt_irq_b	L	Edge
161	1'b1	L	Level
162	1'b1	L	Level
163	dcc_aparm_irq	L	Level
164	bus_dbg_tracker_irq_b	L	Level

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GIC ID	Interrupt source/name	Polarity	Trigger type
165	aparm_domain_irq_b	L	Level
166	aparm_decerr_irq_b	L	Level
167	domain_abort[0]	L	Edge
168	apmixedsys_tx_irq	H	Edge
169	efuse_tx_irq	H	Edge
170	mipi_apb_tx_irq	H	Edge
171	ccif0_ap_irq_b	L	Level
172	trng_irq_b	L	Level
173	ccif1_ap_irq_b	L	Level
174	audio_irq_mcu_b	L	Level
175	gce_irq_b	L	Level
176	gce_secure_irq_b	L	Level
177	1'b1	L	Level
178	1'b1	L	Level
179	mm_iommu_irq_b	L	Level
180	mm_iommu_sec_irq_b	L	Level
181	refresh_rate_int_pulse	L	Edge
182	gcpu_irq_b	L	Level
183	gcpu_dmx_irq_b	L	Level
184	dvfsp_irq_b[0]	L	Level
185	dvfsp_irq_b[1]	L	Level
186	irq_apxgpt	L	Level
187	eint_irq	H	Level
188	eint_irq_secure	H	Level
189	eint_event_b	L	Level
190	eint_event_secure_b	L	Level
191	eint_direct_irq[0]	H	Level
192	eint_direct_irq[1]	H	Level
193	eint_direct_irq[2]	H	Level
194	eint_direct_irq[3]	H	Level
195	pmic_wrap_int	H	Level
196	kp_irq_b	L	Edge
197	spm_irq_b[0]	L	Level
198	spm_irq_b[1]	L	Level
199	spm_irq_b[2]	L	Level
200	spm_irq_b[3]	L	Level
201	spm_irq_b[4]	L	Level
202	spm_irq_b[5]	L	Level
203	spm_irq_b[6]	L	Level
204	spm_irq_b[7]	L	Level

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GIC ID	Interrupt source/name	Polarity	Trigger type
205	sej_apxgpt_rq_b	L	Level
206	sej_wdt_irq_b	L	Level
207	apb_async_scpsys_fhctl_irq	H	Edge
208	md32_ipc_md2host	H	Level
209	mm_mutex_irq_b	L	Level
210	mdp_rdma_irq_b	L	Level
211	mdp_rsz0_irq_b	L	Level
212	mdp_rsz1_irq_b	L	Level
213	mdp_tdshp_irq_b	L	Level
214	mdp_wdma_irq_b	L	Level
215	mdp_wrot_irq_b	L	Level
216	disp_ovl0_irq_b	L	Level
217	disp_ovl1_irq_b	L	Level
218	disp_rdma0_irq_b	L	Level
219	disp_rdma1_irq_b	L	Level
220	disp_wdma0_irq_b	L	Level
221	disp_color_irq_b	L	Level
222	disp_ccorr_irq_b	L	Level
223	disp_aal_irq_b	L	Level
224	disp_gamma_irq_b	L	Level
225	disp_dither_irq_b	L	Level
226	dsi0_irq_b	L	Level
227	dpi0_irq_b	L	Level
228	mmsys_apb_error_int_b	L	Level
229	disp_wdma1_irq_b	L	Level
230	mdp_color_irq_b	L	Level
231	disp_2L_ovl0_irq_b	L	Level
232	disp_2L_ovl1_irq_b	L	Level
233	larb0_irq_b	L	Level
234	venc_irq_b	L	Level
235	larb3_irq_b	L	Level
236	jpgenc_irq_b	L	Level
237	jpgdec_irq_b	L	Level
238	vdec_irq_b	L	Level
239	larb1_irq_b	L	Level
240	larb2_irq_b	L	Level
241	seninf_irq_b	L	Level
242	cam_irq_b	L	Level
243	cam_irq1_b	L	Level

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GIC ID	Interrupt source/name	Polarity	Trigger type
244	cam_irq2_b	L	Level
245	cam_sv_irq_b	L	Level
246	cam_sv_irq1_b	L	Level
247	fd_irq_b	L	Level
248	mali_irq_gpu_b	L	Level
249	mali_irq_mmu_b	L	Level
250	mali_irq_job_b	L	Level
251	mfg_dfsoc_irq	H	Level
252	c2k_wdt_irq_b	L	Edge
253	c2k_sdio_host_fn1_int_b	L	Level
254	cldma_ap_irq_b	H	Level
255	md_wdt_irq_b	H	Edge
256	i2c_int_lv_b	L	Level
257	usim1_irq_b	L	Level
258	usim2_irq_b	L	Level
259	l12ps_rccif_wake_b	L	Level
260	ps_wakeup_l1_b	L	Level
261	ccif_ps_irq_b	L	Level
262	md_ipsec_so_int_lv_b	L	Level
263	md2spm_dvfs_con[0]	H	Level
264	md2spm_dvfs_con[1]	H	Level
265	md2spm_dvfs_con[2]	H	Level
266	md2spm_dvfs_con[3]	H	Level
267	md2spm_dvfs_con[4]	H	Level
268	bt_cvsd_int_b	L	Level
269	conn2ap_btif_wakeup_out_b	L	Level
270	wf_hif_int_b	L	Level
271	conn_wdt_irq_b	L	Edge
272	cirq_event_b	L	Edge

3.1.5 Register Definition

This section describes the registers defined in the MCUCFG_REG block in the MCU system.

See chapter 1.1 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

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3.2 On-chip Memory Controller

3.2.1 Introduction

The on-chip memory controller provides the boot ROM and SRAM resources.

3.2.2 Features

The memory controller has the following features

- 64KB on-chip ROM, with memory access protection and detection
- 128 KB on-chip SRAM, with memory access protection and detection
- 128 KB L2 share SRAM
- Chip ID

The following table is the memory map of on-chip ROM and SRAM.

Table 3-2. Memory map of on-chip memory controller

Bank	Start address	End address	Size	Device
0	0x0000_0000	0x0000_FFFF	64KB	ROM
	0x0010_0000	0x0011_FFFF	128KB	SRAM

3.2.3 Block Diagram

The on-chip memory controller consists of a SRAM controller, a ROM controller, an AXI-FPC bus bridge, a bus interface unit, setting register and chip ID unit (see Figure 3-1). Detailed functionality is described in the following sections.

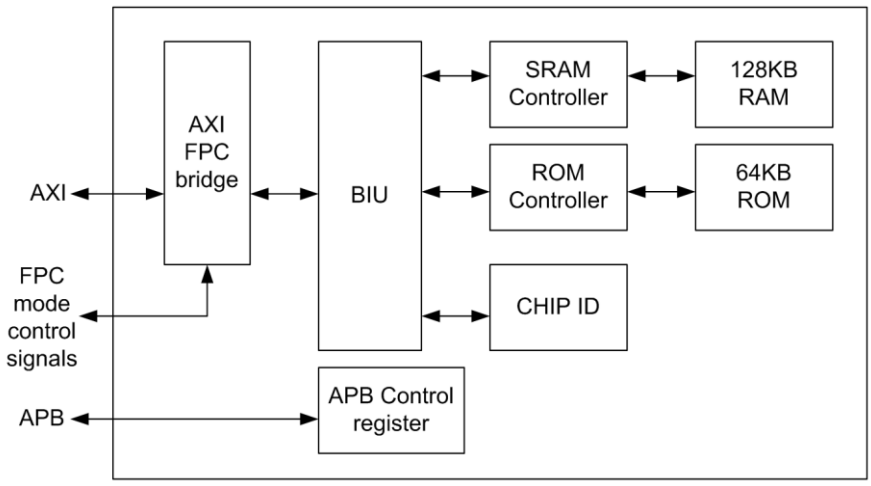

Figure 3-1. Block diagram of on-chip memory controller

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3.2.3.1 BOOT ROM Power Down Mode

Boot ROM power down mode is used in the following scenarios:

1. After system boot, boot ROM will be powered down and prevented from any probe of ROM content
2. In MCDI (multi-core-deep-idle), it is the bootstrap for suspend/resume CPU.

The power down mode can be entered by setting *SRAMROM_SEC_CTRL.sramrom_sw_rom_pd* = 1. The bus interface unit will return a far jump instruction when receiving the read transactions. The jump address can be configurable by the *SRAMROM_BOOT_ADDR* register.

3.2.3.2 BOOT ROM FPC Mode

Boot ROM FPC mode is mainly used in Function Pattern mode. When the chip is trapped into FPC mode, the AXI-FPC bridge will block all the transactions to ROM address by returning a far jump instruction, with jump address specified in SRAMROM_FPC_BOOT_ADDR. The default value of SRAMROM_FPC_BOOT_ADDR is 0. The AXI-FPC bridge will automatically unblock the transaction when the FPC program is downloaded to SRAM memory address space.

3.2.3.3 On-chip SRAM Security Protection

The on-chip SRAM can be partitioned into 2 regions with different security protection configurations. The bus interface unit performs permission check based on the settings, records the first violated address in the *SEC_VIO_ADDR* register and issues interrupts to the host processor. The violation interrupt can be cleared by a write to *SEC_VIO_ACK*.

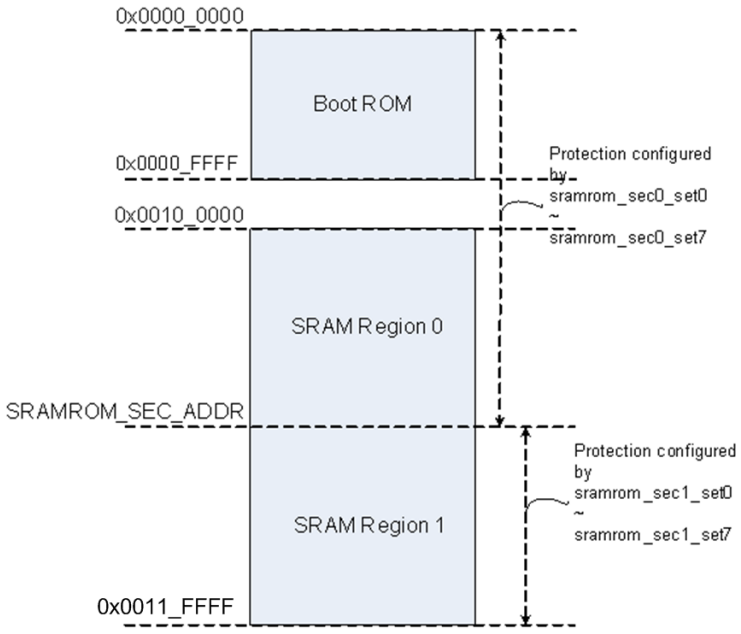

Figure 3-2. Security memory protection scheme

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3.2.4 Register Definition

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3.3 External Interrupt Controller

3.3.1 Introduction

The external interrupt controller (EINTC) processes all off-chip interrupt sources and forwards interrupt request signals to AP MCU.

3.3.2 Features

EINTC supports up to 160 external interrupt signals and performs the following processes to the interrupt signals coming from external sources:

Polarity inversion
Edge/level trigger selection
De-bounce with a configurable 32kHz clock (optional)

According to the register configuration, the external interrupt source will be forwarded to the Cortex-A7 built-in interrupt controller with different IRQ signals, eint_irq or eint_direct_irq. EINTC generates wakeup events to AP MCU.

3.3.3 Block Diagram

Figure 3-3 is the block diagram of the external interrupt controller in MT6750. Every functional block is controlled by the corresponding control registers defined in next section.

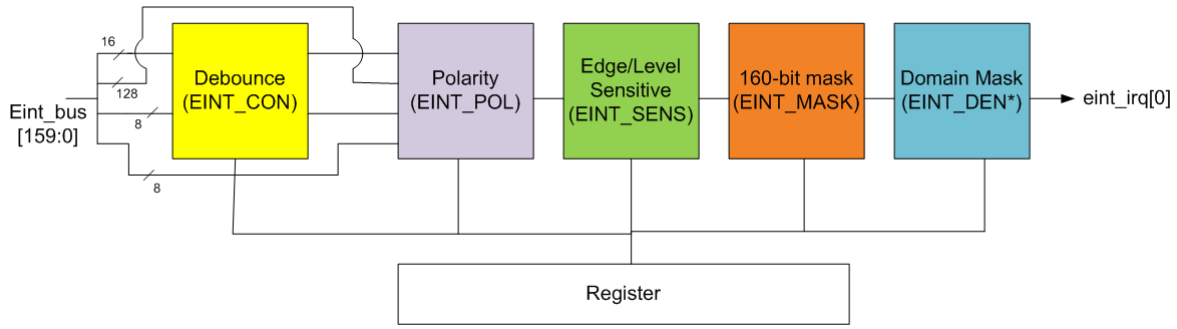

Figure 3-3. Block diagram of external interrupt controller

Normally the external interrupt source goes through the de-bounce unit which is driven by 32kHz clock and triggers the corresponding CPU with eint_irq. Therefore, the minimum latency from eint_bus to eint_irq is 30.52μs.

The following tables list the signal connections to the interrupt controller of CPU.

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Table 3-3. External interrupt request signal connection

IRQ name	AP MCU INTC
eint_irq	IRQ[187]
eint_event_b	IRQ[189]
deint_irq[0]	IRQ[191]
deint_irq[1]	IRQ[192]
deint_irq[2]	IRQ[193]
deint_irq[3]	IRQ[194]

Table 3-4. Definitions of domains

Domain number	Target CPU/DSP
0	Application CPU

Table 3-5. EINT table

EINT Name	EINT number	Support HW debounce?
GPIO[138:0]	138~0	Only 15~0 support debounce.
C2K_eint[4:0]	143~139	No
icusb_vbusvalid	149	Yes
PMIC[1:0]	151~150	Yes

3.3.4 Register Definition

See chapter 1.3 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

3.3.5 Programming Guide

3.3.5.1 Register Bit Set/Clear

For efficient bit set up/clear operation, the following registers have specific bit set/clear registers:

- EINT_MASK
- EINT_SOFT
- EINT_DBNC
- EINT_POL

Write 1 to the specified bit of the set/clear register to set up or clear the corresponding bit in the status register.

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3.3.5.2 Domain Control

For instance, if you would like int_bus[3] to trigger eint_irq[0], bit 3 in the EINT_DOEN register should be set.

3.3.5.3 EINT De-bounce Control Sequence

1. Set up EINT_CON (PRESCALER, POL, CNT) and enable de-bounce (EN).
2. Wait for 3*32K (~100us).
3. Write RSTDBC (self-clear).
4. Wait for 3*32K (~100us).
5. Write EINT_INTACK to ack/clear all statuses.
6. Unmask EINT_MASK.

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3.4 System Interrupt Controller

3.4.1 Introduction

For processors which have embedded interrupt controllers (GIC) in it, the part of MCUSYS should keep feeding clock and power to make the interrupt functional. However, due to power/leakage overhead introduced by higher clock ratio and deep submicron processes, reserving an always on (or frequently turned on) domain in MCUSYS has become power ineffective. The system interrupt controller (SYS_CIRQ) is a low power interrupt controller designed to work outside MCUSYS as a second level interrupt controller. With SYS_CIRQ, MCUSYS can be completely turned off to improve system power consumption without losing interrupts.

3.4.2 Features

SYS_CIRQ supports up to 168 interrupts which can configure following attributes individually.

Polarity inversion
Edge/level trigger selection

The 168 interrupts feed through SYS_CIRQ and connect to GIC in MCUSYS. When SYS_CIRQ is enabled, it will record the edge-sensitive interrupts and generate a pulse signal to CPU GIC when the flush command is executed.

3.4.3 Block Diagram

Figure 3-4 is the system level block diagram of the system interrupt controller.

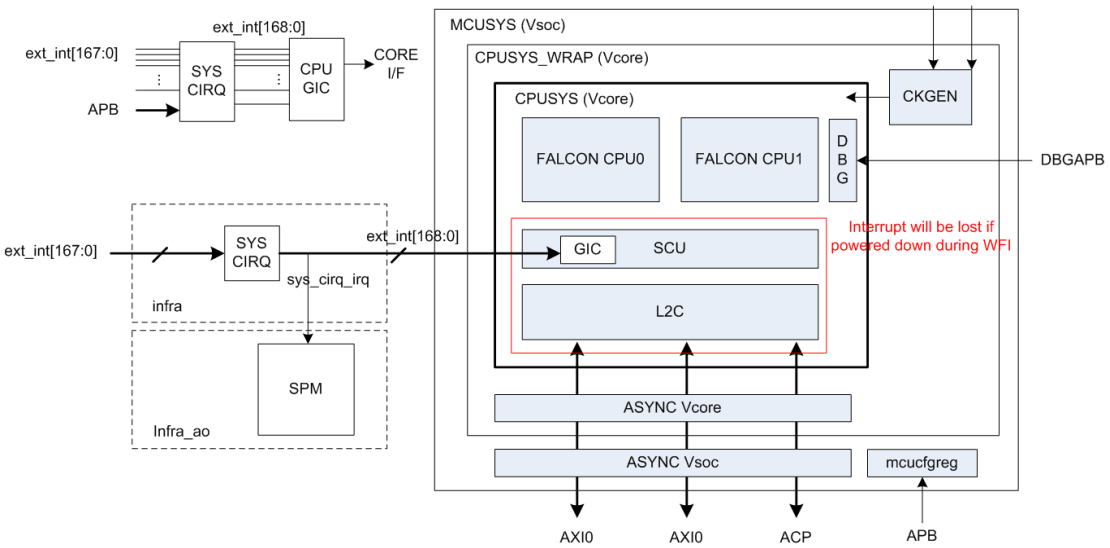

Figure 3-4. System level block diagram of system interrupt controller

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The SYS_CIRQ controller is integrated in between MCUSYS and other interrupt sources as the second level interrupt controller. All interrupts are fed through SYS_CIRQ controller then bypassed to MCUSYS. In normal mode (where MCUSYS GIC is active), SYS_CIRQ is disabled and interrupts will be directly issued to MCUSYS. When MCUSYS enters the sleep mode, where GIC is power downed, the SYS_CIRQ controller will be enabled and monitor all edge-trigger interrupts (only edge-triggered interrupt will be lost in this scenario). When an edge-trigger interrupt is triggered, it will be recorded in SYS_CIRQ_STA register and can be restored to GIC by SW context restore or the SYS_CIRQ flush function.

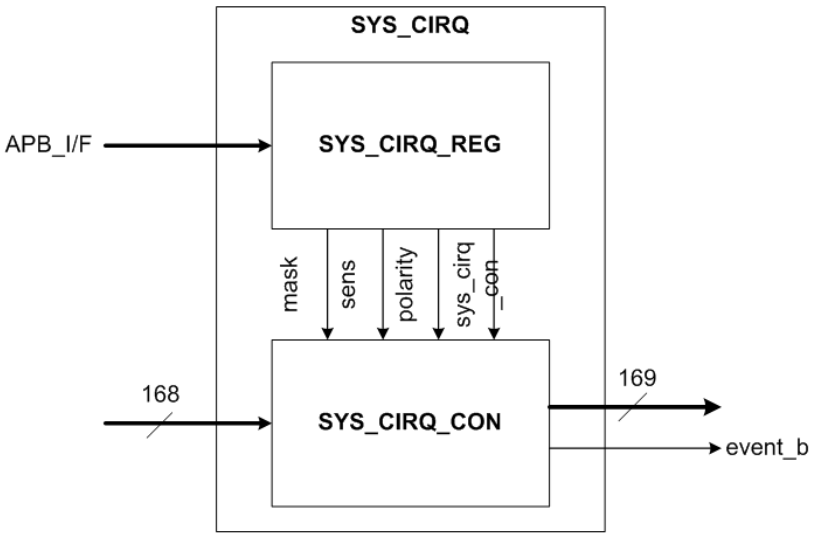

Figure 3-5. Block diagram of system interrupt controller

Figure 3-5 is the architecture of SYS_CIRQ. SYS_CIRQ_REG stores the mask/sensitivity/polarity attributes of each interrupt signal, and SYS_CIRQ_CON is used to mask and detect edge-triggered interrupts.

3.4.4 Register Definition

See chapter 1.4 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

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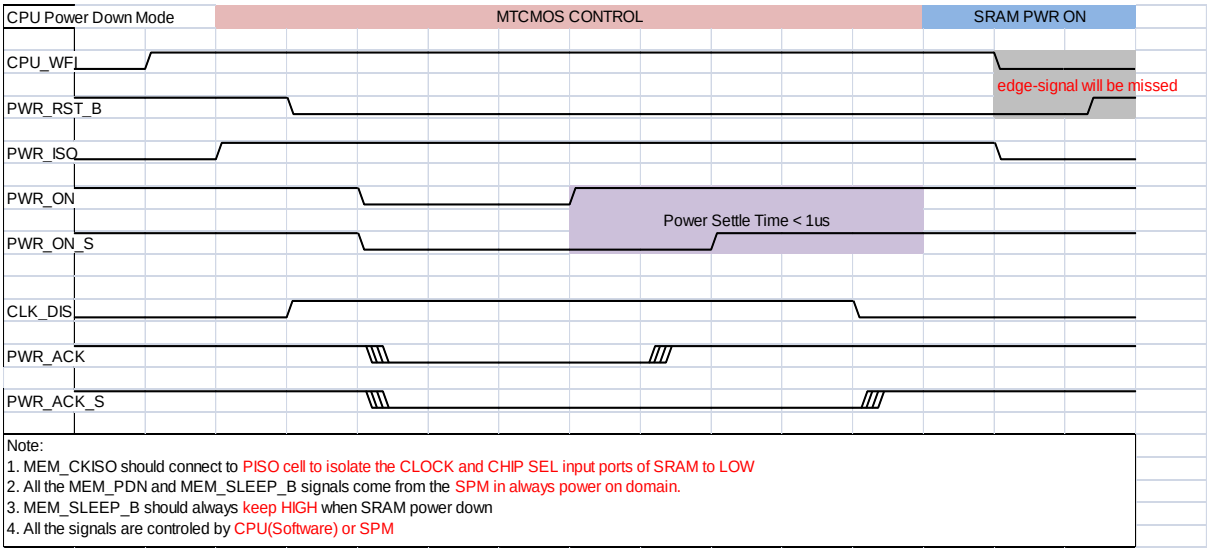
3.4.5 Programming Guide

3.4.5.1 MCUSYS MTCMOS Sequence



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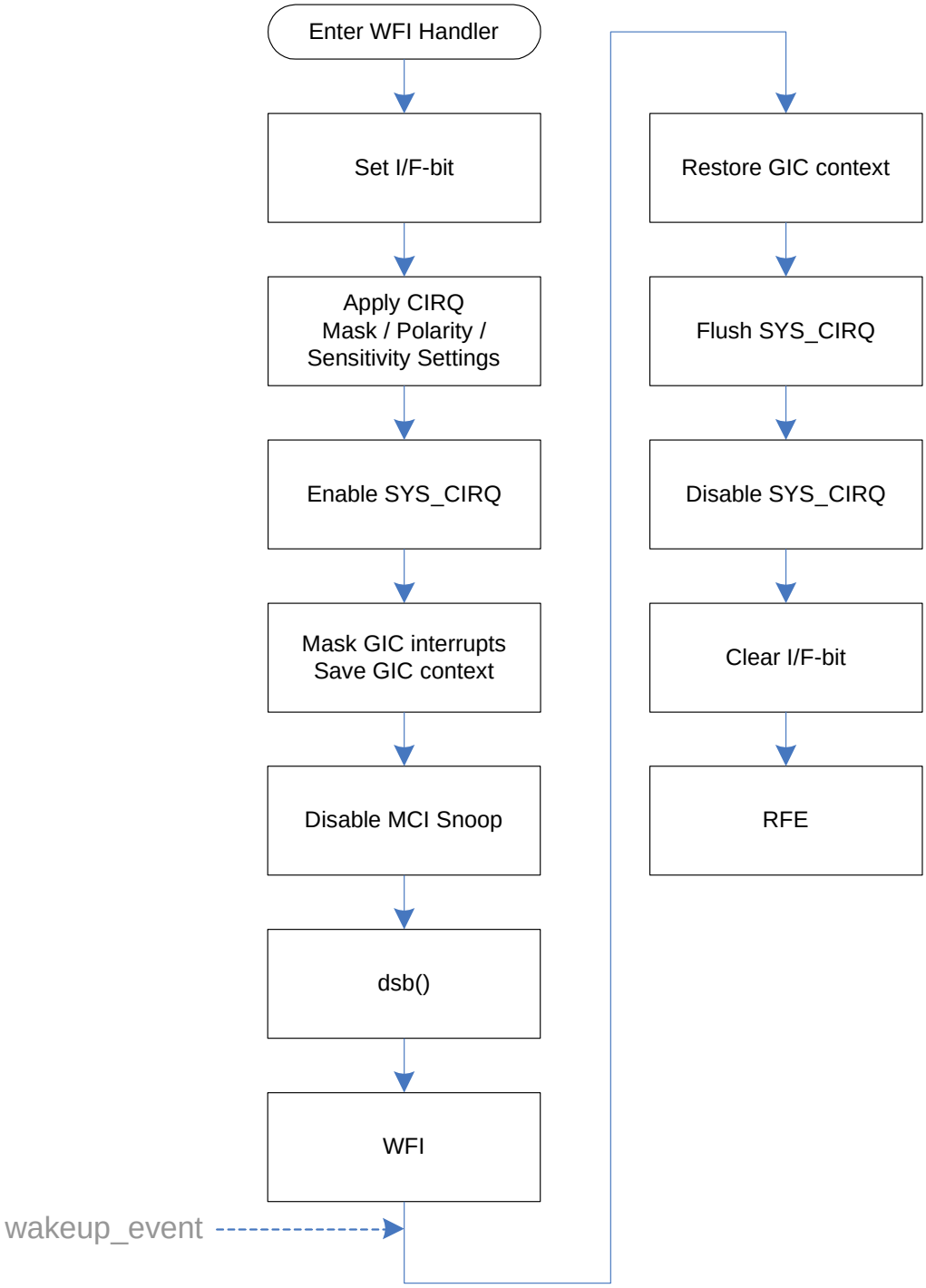
3.4.5.2 SW Flow



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3.5 Infrastructure System Configuration Module

3.5.1 Introduction

The infrastructure system configuration module (INFRACFG) provides reset, clock and miscellaneous control signals in the infrastructure system.

3.5.2 Features

INFRACFG provides the following control signals to the functional blocks inside the infrastructure system:

- Software reset signals
- Clock gating control signals
- Dynamic clock management control signals
- Top AXI bus fabric control signals
- Dynamic clock management function

3.5.2.1 DCM in Details

The dynamic clock management function is used to slow down the clock frequency for power saving when the system is in idle state automatically.

Figure 3-6 is a sample clock waveform when DCM is activated. In this example, the clock frequency in DCM mode is set to quarter of the original clock. The ratio of clock frequency slow-down is controlled by the INFRA_DCMFSEL register.

After the bus idle signal is low, it will take several cycles of latency to make the slow-down clock return to the normal frequency. The cycle number varies with the runtime status of the clock gating logic and will somehow cause minor performance impact. In order to minimize the impact when the system is in heavy load status, the INFRA_DCMDBC register controls the cycle count once the bus idle signal is asserted. Setting the de-bounce cycle to be longer and enabling the function will reduce the probability of the system entering the DCM mode.

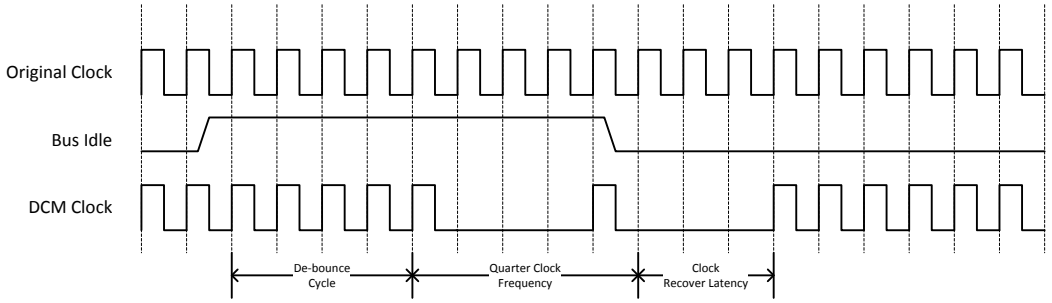

Figure 3-6. DCM in action

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3.5.3 Register Definition

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3.6 External Memory Interface

3.6.1 Introduction

The EMI (External Memory Interface) controller schedules requests from the masters and issues commands to DRAMC in an efficiency way. The block conducts flow control for DRAMC and masters to avoid DRAM stall or data overflow or underflow. It also minimizes the latency of processor path to enhance the performance and tries to increase the DRAM efficiency. The block also informs clock control to gate the clock when it does not find any transaction right now. This block is designed to supply 325MHz bus clock frequency.

3.6.2 Features

The EMI controller receives AXI master commands and issues them to the DRAM controller. It supports all AXI transaction type commands except for the fixed and cache commands. There are plenty of schedule options to schedule the command, which are:

- Starvation control
- Bandwidth limiter
- High priority
- Page hit control
- Read/write turn around prevent control
- Memory protect unit (DRAM & APB)

3.6.3 Block Diagram

In MT6750, the DRAM controller connects three systems via six AXI ports and supports connecting two rank DRAM devices at the same time. For cortex APMCU system, a 128-bit AXI port is provided for the connection. For the multimedia system, a 128-bit AXI port is provided for the connection. Besides, there are three 64-bit AXI ports for connecting to modem MCU, modem 2G/3G/4G HW and peripheral system. In the DRAM controller, the APB interface is for programming registers. Then you can initialize DRAM or other parameter settings.

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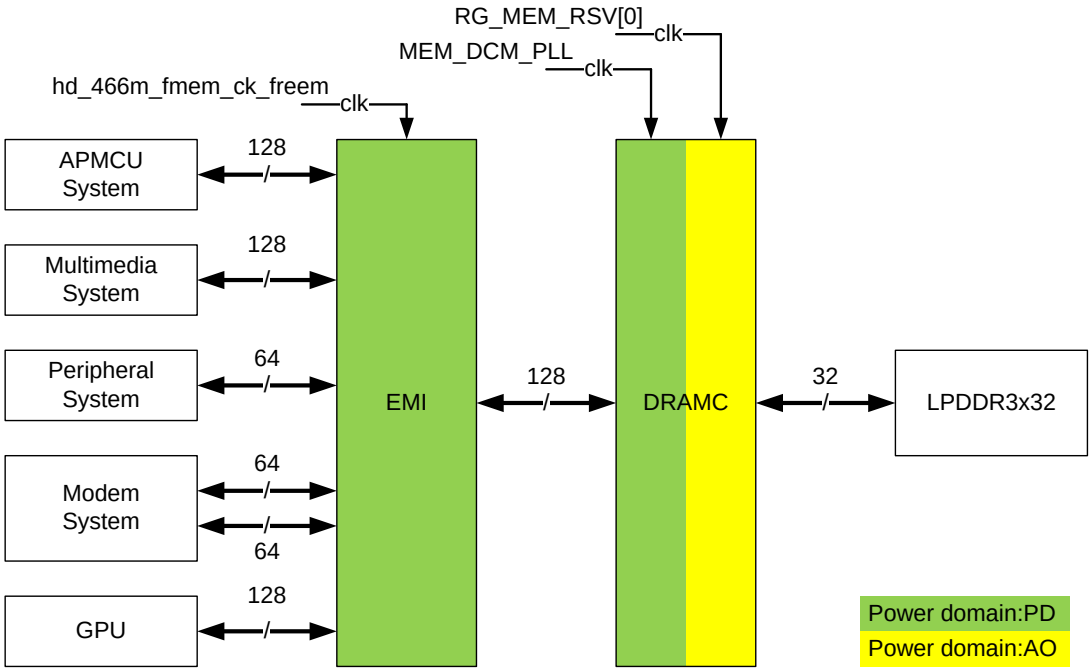

Figure 3-7. EMI/DRAM controller top connection

3.6.4 Register Definition

See chapter 1.6 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

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3.7 DRAM Controller

3.7.1 Overview

DRAM controller supports the following DRAM bus configuration:
LPDDR3 32-bit @ 1800MHz (1,800M bps/per bit channel)

See the table below for the DRAM bus signals:

Table 3-6. DRAM bus signal list (refer to DRAMC side)

Signal name	Type	Description
CK0/CK1	Input	DRAM clock signal
CK0#/CK1#	Input	DRAM clock invert signal
MA[9:0]	Input	Address for all memories/CA bus for LPDDR3
CKE	Input	Clock enable signal for DRAM
CS# [1:0]	Input	RANK1~RANK0 selection signal
DQ[31:0]	I/O	Data bus for LPDDR3
DQM[1:0]	Input	Data mask
DQS[3:0]	I/O	Data strobe
DQS#[3:0]	I/O	Differential data strobe in LPDDR3
REXTDN	I/O	Output driving calibration

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See below for the DRAM bus command truth table:

Table 3-7. DRAM bus command truth table (LPDDR3)

		SDR Command Pins			DDR CA pins (10)										
SDRAM Command	NVM Command	CKE		CS_N	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CK_t EDGE
		CK_t(n-1)	CK_t(n)												
MRW	MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	↑
				X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	↓
MRR	MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	↑
				X	MA6	MA7	X								↓
Refresh (per bank)[11]	-	H	H	L	L	L	H	L	X						↑
				X	X										↓
Refresh (all bank)	-	H	H	L	L	L	H	H	X						↑
				X	X										↓
Enter Self Refresh	Enter Power Down	H	L	L	L	L	H	X							↑
		X		X	X										↓
Activate (bank)	Activate (row buffer)	H	H	L	L	H	R8/a15	R9/a16	R10/a17	R11/a18	R12/a19	BA0	BA1	BA2	↑
				X	R0/a5	R1/a6	R2/a7	R3/a8	R4/a9	R5/a10	R6/a11	R7/a12	R13/a13	R14/a14	↓
Write (bank)	Write (RDB)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
				X	AP[3,4]	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
Read (bank)	Read (RDB)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
				X	AP[3,4]	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
Precharge (pre bank, all bank)	Preactive (RAB)	H	H	L	H	H	L	H	AB/a30	X/a31	X/a32	BA0	BA1	BA2	↑
				X	X/a20	X/a21	X/a22	X/a23	X/a24	X/a25	X/a26	X/a27	X/a28	X/a29	↓
BST	BST	H	H	L	H	H	L	L	X						↑
				X	X										↓
Enter Deep Power Down	Enter Power Down	H	L	L	H	H	L	X							↑
		X		X	X										↓
NOP	NOP	H	H	L	H	H	H	X							↑
				X	X										↓
Maintain PD, SREF, DPD (NOP)	Maintain Power Down (NOP)	L	L	L	H	H	H	X							↑
				X	X										↓
NOP	NOP	H	H	H	X										↑
				X	X										↓
Maintain PD, SREF, DPD (NOP)	Maintain Power Down (NOP)	L	L	H	X										↑
				X	X										↓
Enter Power Down	Enter Power Down	H	L	H	X										↑
		X		X	X										↓
Exit PD, SREF, DPD	Exit Power Down	L	H	H	X										↑
		X		X	X										↓

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These tables are applied when CKE is asserted at the clock cycle before CS# is asserted. Read and write accesses to the DDR SDRAM are burst oriented. The accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. The accesses begin with the registration of an ACTIVE command, followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

As with standard SDRAMs, the pipelined, multi-bank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

The DDR SDRAM operates from a differential clock (CK and CK#). Commands (address and control signals) are registered at every positive and negative edges of CK for LPDDR3. The input data are registered on both edges of DQS, and the output data are referenced to both edges of DQS, as well as to both edges of CK. DQS is center-aligned with data for WRITEs. Without DLL inside mobile DRAM's (LPDDR3), DQS is not edge-aligned with data for READs.

The commands for LPDDR3 SDRAM are encoded in MA0 ~ MA9 and transfer at double rate of clock frequency such as DQ.

Other key points of Denali DRAM controller:
- Supports column address bit number from 8 to 11
- Supports DRAM burst length 4 and 8
- Supports maximum LPDDR3 8G-bit device

3.7.2 Features

- 128-bit data bus interface with BE[15:0] for write data mask
- LEN has 4-bit, 0 ~ 15 DLE's/WDLE's
- Supports END_SIZE for optimize utilization rate
- Supports WDLE for split transaction
- Supports HDLE (DLE64) side band signal for early responses
- Supports high-priority side band signal for reducing request latency
- A request cannot cross page boundary
- Supports 2X frequency mode (frequency ratio of DRAMC:DRAM = 1:2) for timing optimization
- Supports dual-scheduler function for 1T command rate under 2X frequency mode for performance optimization
- Supports power-down and self-refresh for power saving
- Supports clock stop for power saving
- Supports input DQS/DQ timing calibration for PVT variation
- Supports read/write command out of order control

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3.7.2.1 Reference

LPDDR2 spec: http://www.jedec.org/download/search/JESD209-2.pdf

3.7.3 Block Diagram

The major blocks of DRAM controller are command decoder, command pool, bus scheduler, timing controller DDR PHY and response generator.

The requests from Arbiter are pushed to command pool to wait for execution in order. The bus scheduler inspects the precharge/active pool and command FIFO and decides which DRAM bus command, e.g. PRECHARGE, ACTIVE, READ or WRITE, is issued to the DRAM bus. The goals of bus scheduler are to raise the bus utilization rate and lower the response latency. The timing control unit is responsible for the integrity of DRAM bus timing such as pre-charge to active delay (tRP), active to command delay (tRCD) and bus turnaround time. The bus scheduler refers to the information and choose the next DRAM bus command. The DRAM interface unit is responsible for generating DRAM bus commands, transmitting data and DQS to DDR DRAM and receiving data and DQS from DDR DRAM. The response generator produces the response signals for all DRAM agents such as DLE and RDAT.

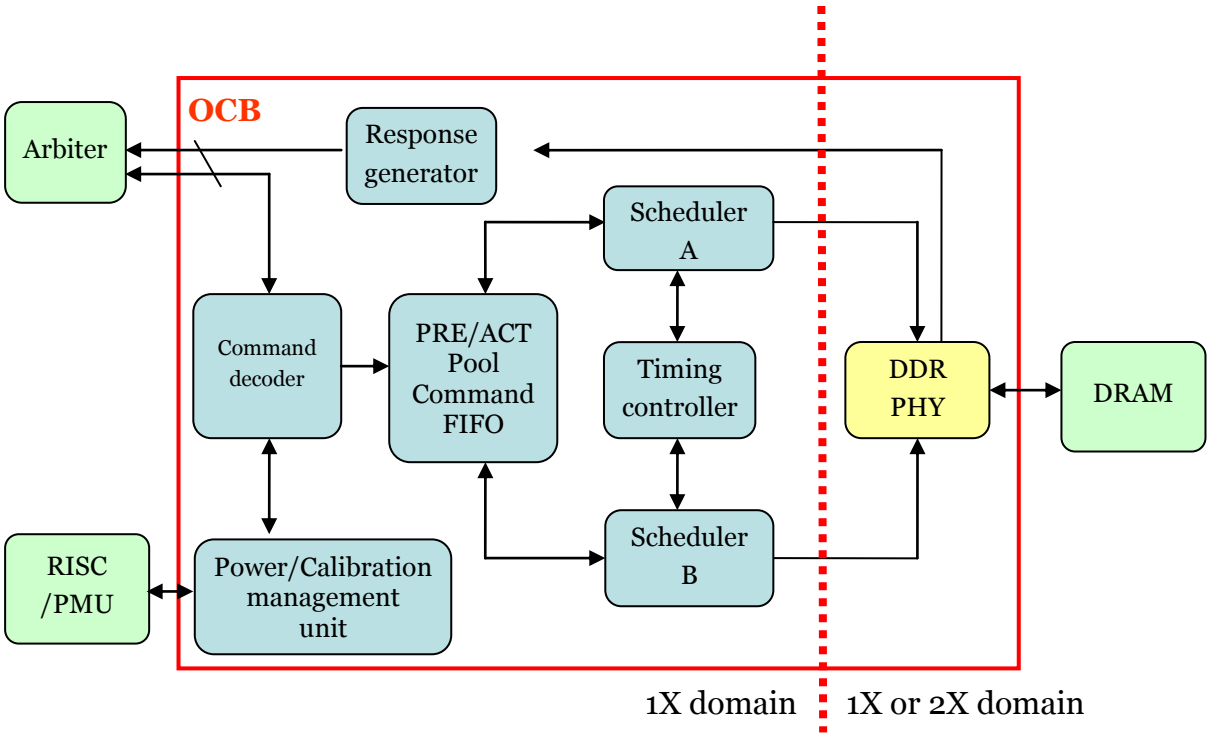

Figure 3-8. Block diagram of DRAM controller

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3.7.4 Register Definition

See chapter 1.7 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

3.7.5 Programming Guide

Steps of DRAM initialization

1. Set up DRAM AC timing parameter.
2. Follow DRAM spec to complete DRAM initialization including mode register programming.
3. Enable calibration for DQ/DQS window.
4. Set up refresh rate counter.
5. Normal operation.

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3.8 AP_DMA

3.8.1 Introduction

There is always a DMA in a platform. The purpose of DMA is performing data transfer between different slaves. There are several slaves in a platform, and the major one is external memory, e.g. DRAM. There are also internal SRAM and some slave ports for the peripheral to transfer data. For saving software efforts, DMA delivers a virtual FIFO concept to help the software maintain read and write pointer when the software accesses data from a ring buffer. As the bus goes more and more efficient, the old DMA still utilizes the AHB bus protocol and may decrease its performance. Another problem is that when the old DMA meets byte alignment addresses or byte alignment sizes, it will need some software efforts to help solve head and tail non word alignment problems or let DMA to simply issue single-1-byte requests to conquer the byte-alignment problem. This will harm the overall system because the single-1-byte transaction is quite inefficient. The DMA efficiency is now improved by increasing its bus efficiency, including data buffering and overcoming byte alignment problems.

3.8.2 Features

APDMA has the following DMA engines.

- I2C DMA engine*5
- BTIF TX DMA engine*1
- BTIF RX DMA engine*1
- UART TX DMA engine*4
- UART RX DMA engine*4
- HIF DMA engine*1

The DMA engines and corresponding peripheral devices are listed below.

Table 3-8. Relationship between engines and devices

Engine	Peripheral device
HIF0	Connsys(sdctl)
I2C_0 ~ I2C_4	I2C_0 ~ I2C_4
UART0 ~ UART3	UART0 ~ UART3
BTIF	BTIF

3.8.3 Block Diagram

Figure 3-9 is the basic block diagram of AP_DMA. There are total 12 channels in DMA. The external AXI interface is connected to the peripheral AXI bus fabric to provide external memory access ability. The internal AXI interface is also connected to the peripheral AXI bus fabric and is re-directed to related peripherals, e.g. HIF, I2C, BTIF and UART. A memory block is used as a buffer which makes the transfer on the AXI bus interface more efficient. An APB interface is used to program registers for both global registers and local registers existing in every individual DMA channel.

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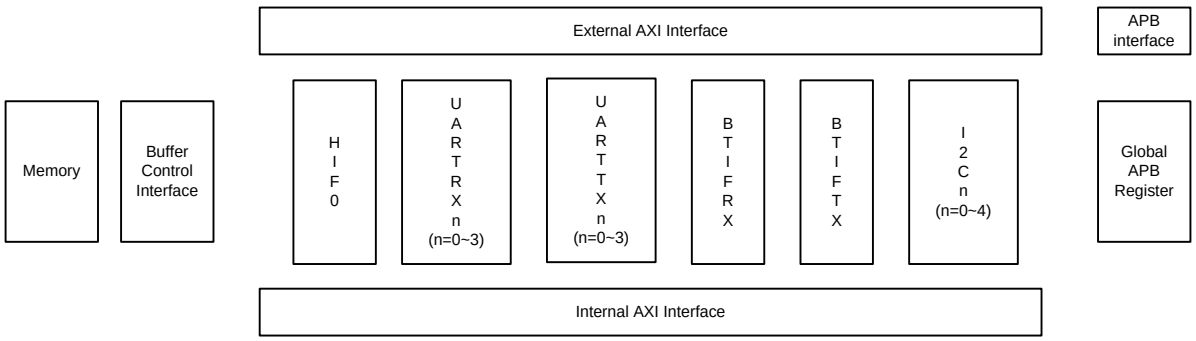

Figure 3-9. APDMA block diagram

3.8.4 Programming Guide

3.8.4.1 Warm Reset and Hard Reset

Warm reset and hard reset exist in DMA global control and each DMA engine. When warm reset is set, the engine will be reset after the current transaction is finished, and therefore the warm reset will not cause any bus hang. Conversely, when hard reset is set, the engine will be reset immediately, and therefore the bus may go down due to unfinished (and will never finish) transaction.

Mechanism of global warm reset

When the software is to re-start all engines or re-clear all engines in DMA, it can set the global WARM_RST to 1 and wait for (poll) all global running status to be 0. Next, set WARM_RST back to 0 to finish the global warm reset.

Mechanism of global hard reset

When the software is to re-start all engines or re-clear all engines in DMA without waiting for any period of time, it can set the global HARD_RST to 1 then back to 0 to finish the global hard reset. Note that this may break the bus protocol and cause system hang.

3.8.4.2 Pause and Resume

There are pause and resume functions available for general DMA and peripheral DMA. The mechanism is as the following:

1. Start DMA. (Program necessary settings, then set EN = 1.)
2. Pause DMA. (Set PAUSE = 1.)
3. Resume DMA. (Set PAUSE = 0.)
4. Wait for DMA to finish. (EN will become 0, and flag will be set to 1.)

The software can repeat step 2 and 3 many times when DMA is running and monitor the idle bit to see if DMA is stopped. DMA will not pause immediately and will wait for the last transaction to be finished.

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3.8.4.3 Access Security Region

To access the memory security region, the security and domain bits must be specified before channel configuration and DMA is enabled. After SEC_EN and GSEC are set, access DMA registers with APB secure access. When DMA finishes the transmission, the secure and domain bits will become default value. Configure the bits again if DMA transmission is going to start.

1. Set register DOMAIN_CFG as the AP domain.
2. Set register SEC_EN=1 and GSEC=1.

3.8.5 Programmed Sequence for Different Types of Channels

3.8.5.1 Peripheral DMA with Burst Length equals 1 (e.g. I2C)

1. Configure DMA registers.
   AP_DMA_I2C_*_CON (dir)
   AP_DMA_I2C_*_TX_MEM_ADDR, AP_DMA_I2C_*_TX_LEN (Tx)
   AP_DMA_I2C_*_RX_MEM_ADDR, AP_DMA_I2C_*_RX_LEN (Rx)
2. Set interrupt enable=1 .
   AP_DMA_I2C_*_INT_EN
3. Wait for interrupt.
4. Clear interrupt flag.
   AP_DMA_I2C_*_INT_FLAG

3.8.5.2 Peripheral DMA with Configurable Burst Length (e.g. HIF)

1. Configure DMA registers.
   AP_DMA_HIF_*_CON (dir, burst_length)
   AP_DMA_HIF_*_MEM_ADDR
   AP_DMA_HIF_*_LEN
2. Set interrupt enable=1 .
   AP_DMA_HIF_*_INT_EN
3. Set enable=1.
   AP_DMA_HIF_*_EN
4. Wait for interrupt.
5. Clear interrupt flag.
   AP_DMA_HIF_*_INT_FLAG

3.8.5.3 Virtual FIFO DMA TX (e.g. UART_TX, BTIF_TX)

1. Configure registers.
   AP_DMA_UART_*_TX_VFF_ADDR
   AP_DMA_UART_*_TX_VFF_LEN, AP_DMA_UART_*_TX_VFF_THRE

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AP_DMA_UART_*_TX_VFF_WPT
2. Write data to EMI and update SW write_pointer.
   AP_DMA_UART_*_TX_VFF_WPT
3. Clear interrupt (repeat step 3-6 till finished).
   AP_DMA_UART_*_TX_INT_FLAG
4. Set interrupt enable =1.
   AP_DMA_UART_*_TX_INT_EN
5. Set enable=1 (first time).
   AP_DMA_UART_*_TX_EN
6. Wait for interrupt.
7. Set stop=1 if finished.
   AP_DMA_UART_*_STOP

3.8.5.4 Virtual FIFO DMA RX (e.g. UART_RX, BTIF_RX)

1. Configure registers.
   AP_DMA_UART_*_RX_VFF_ADDR
   AP_DMA_UART_*_RX_VFF_LEN, AP_DMA_UART_*_RX_VFF_THRE
   AP_DMA_UART_*_RX_VFF_RPT
   AP_DMA_UART_*_RX_FLOW_CTRL_THRE
2. Set interrupt enable =1.
   AP_DMA_UART_*_RX_INT_EN
3. Set enable=1 (first time).
   AP_DMA_UART_*_RX_EN
4. Wait for interrupt (repeat step 4-6 till finished).
5. Read data from EMI; update SW read_pointer.
   AP_DMA_UART_*_RX_VFF_RPT
6. Clear interrupt flag.
   AP_DMA_UART_*_RX_INT_FLAG
7. Set stop=1 if finished.
   AP_DMA_UART_*_RX_STOP

3.8.6 Register Definition

There are several registers put together for the software to monitor. However, if the software is to change them, they can only be written through individual DMA registers. The global register is only for the software to watch all DMA running statuses and interrupt flags together. Note that the security ability of all global registers belongs to the GSEC_EN bit. When this bit is set to 1, only the security transaction can write the global register (global reset and global slow-down). If a non-security read transaction is issued to read the interrupt flag or running status, only statuses of non-security engines can be reported, and others will always be 0.

For register tables, see chapter 1.8 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

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3.9 CQ_DMA

3.9.1 Introduction

There is always a DMA in a platform. The purpose of DMA is performing data transfer between different slaves. There are several slaves in a platform, and the major one is external memory, e.g. DRAM. There are also internal SRAM and some slave ports for the peripheral to transfer data. For saving software efforts, DMA delivers a virtual FIFO concept to help the software maintain read and write pointer when the software accesses data from a ring buffer. As the bus goes more and more efficient, the old DMA still utilizes the AHB bus protocol and may decrease its performance. Another problem is that when the old DMA meets byte alignment addresses or byte alignment sizes, it will need some software efforts to help solve head and tail non word alignment problems or let DMA to simply issue single-1-byte requests to conquer the byte-alignment problem. This will harm the overall system because the single-1-byte transaction is quite inefficient. The DMA efficiency is now improved by increasing its bus efficiency, including data buffering and overcoming byte alignment problems.

3.9.2 Features

CQDMA has the following DMA engines.

- GDMA0 DMA
- GDMA1 DMA
- Audio DMA
- FPC DMA

3.9.3 Programming Guide

3.9.3.1 Warm Reset and Hard Reset

Warm reset and hard reset exist in DMA global control and each DMA engine. When warm reset is set, the engine will be reset after the current transaction is finished, and therefore the warm reset will not cause any bus hang. Conversely, when hard reset is set, the engine will be reset immediately, and therefore the bus may go down due to unfinished (and will never finish) transaction.

3.9.3.2 Pause and Resume

There are pause and resume functions available for general DMA and peripheral DMA. The mechanism is as the following:

1. Start DMA. (Program necessary settings, then set EN = 1.)
2. Pause DMA. (Set PAUSE = 1.)
3. Resume DMA. (Set PAUSE = 0.)
4. Wait for DMA to finish. (EN will become 0, and flag will be set to 1.)

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The software can repeat step 2 and 3 many times when DMA is running and monitor the idle bit to see if DMA is stopped. DMA will not pause immediately and will wait for the last transaction to be finished.

3.9.3.3 Access Security Region

To access the memory security region, the security and domain bits must be specified before channel configuration and DMA is enabled. After SEC_EN and GSEC are set, access DMA registers with APB secure access. When DMA finishes the transmission, the secure and domain bits will become default value. The bits should be configured again if DMA transmission is going to start.

1. Set register DOMAIN_CFG as AP domain.
2. Set register SEC_EN=1 and GSEC=1.

3.9.4 Register Definition

There are several registers put together for the software to monitor. However, if the software is to change them, they can only be written through individual DMA registers. The global register is only for the software to watch all DMA running statuses and interrupt flags together. Note that the security ability of all global registers belongs to the GSEC_EN bit. When this bit is set to 1, only the security transaction can write the global register (global reset and global slow-down). If a non-security read transaction is issued to read the interrupt flag or running status, only statuses of non-security engines can be reported, and others will always be 0.

For register tables, see chapter 1.9 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

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4 Clock and Power Control

4.1 Top Clock Generator

4.1.1 Introduction

This chapter introduces the top clock generator (TOPCKGEN) and the clock architecture.

4.1.2 Features

TOPCKGEN is responsible for generating the following clock signals:

- Free clock generation for whole chip
- Infrastructure and peripheral system clock, including the top level AXI fabric clock
- Multimedia system clock
- Pad macro clocks to be synchronized with one of the above system

The module TOPCKGEN provides clock source selection. Each clock has several clock source selection and can be turned off as well. When switching certain clock from frequency A to frequency B, make sure frequency A and B are available.

It comprises glitch-free clock MUX and digital clock divider to generate various clock frequencies.

4.1.3 Block Diagram

4.1.3.1 Clock Architecture

There are clock generators not only in the top level hierarchy but also in every partition/system. Figure 4-1 shows the location of the top level clock generator.

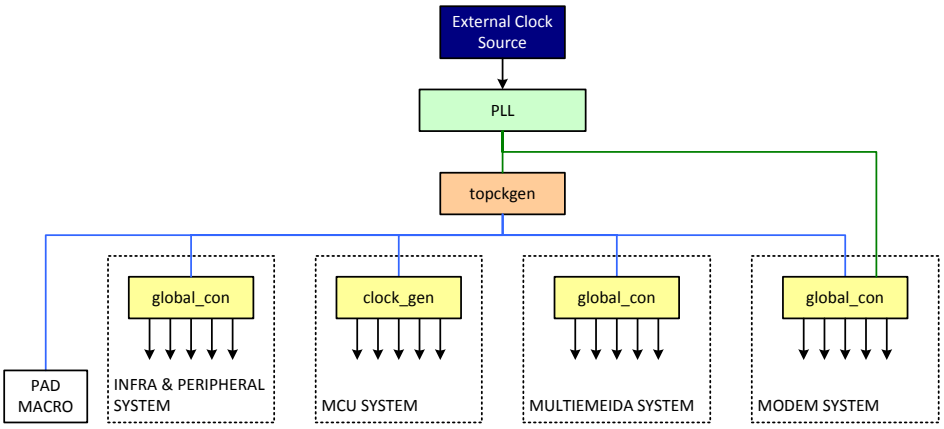

Figure 4-1. Block diagram of clock architecture

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4.1.3.2 Clock Multiplier

Clock selection and generation have similar structure (see Figure 4-2). Several clock sources are provided. Choose one by specified register setting. The turn-off bit is provided as well to stop the clock output.

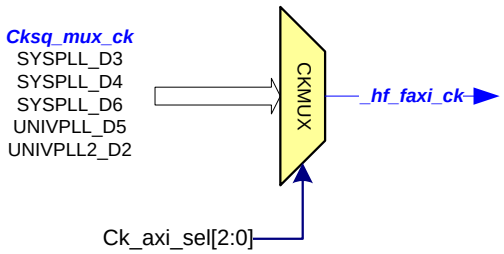

Figure 4-2. Example of clock multiplier

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4.1.4 Clock PLL

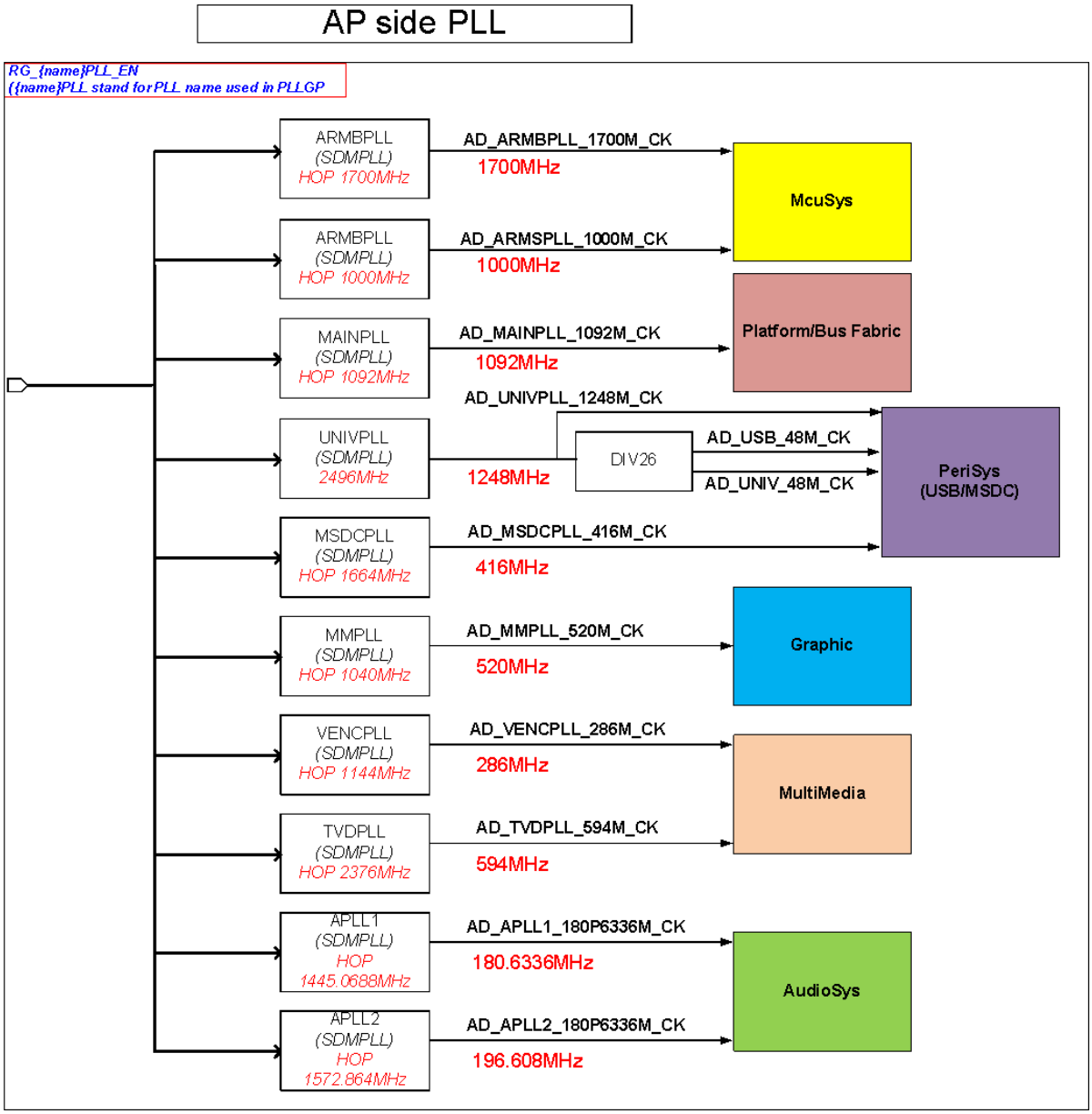

Figure 4-3. PLL block diagram

4.1.5 PLL Related Control

The following table lists all PLLs inside the application system.

The enabling of PLL can be switched between software control and hardware control. The hardware control is from SCPSYS.

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The hopping and SSC features can be switched between software control and hardware control. The hardware control is from FHCTL.

Table 4-1. PLL related control

PLL	Capability	Control by FHCTL	Control by SPM
ARMBPLL	Hopping, SSC	Y	Y
ARMSPLL	Hopping, SSC	Y	N
MAINPLL	Hopping, SSC	Y	Y
UNIVPLL	Fix	N	Y
MSDCPLL	Hopping, SSC	Y	N
MMPLL	Hopping, SSC	Y	N
TVDPLL	Hopping, SSC	Y	N
VENCPLL	Hopping, SSC	Y	N
APLL1	Fix	N	N
APLL2	Fix	N	N
MIPI	SSC	N	N
MEMPLL	Hopping, SSC	Y	N

4.1.6 Clock Gating

The clock gating for module TOPCKGEN is listed in the table below where DCM and turn-off settings are provided.

Table 4-2. Clock gating settings

Register name	Bit	Default	Function name	Description
CLK_MODE	8	1'b0	pdn_md_32k	Turns off 32K clock source to MD
CLK_SCP_CFG_0	[0]	1'b0	sc_26ck_off_en	Turns on scpsys control path to gate 26MHz
	[1]	1'b0	sc_mem_ck_off_en	Turns on scpsys control path to gate DDRPHY
	[2]	1'b0	sc_axick_off_en	Turns on scpsys control path to gate hf_faxi_ck
	[5]	1'b0	sc_md_32k_off_en	Turns on scpsys control path to gate MD 32KHz
	[9]	1'b0	sc_mac_26m_off_en	Turns on scpsys control path to gate MIPI 26MHz
	[16]	1'b0	sc_armck_off_en_bus	Turns on scpsys control path to gate bus hf_farm_ck
	[17]	1'b0	sc_armck_off_en_sml	Turns on scpsys control path to gate sml hf_farm_ck
	[18]	1'b0	sc_armck_off_en_big	Turns on scpsys control path to gate big hf_farm_ck
CLK_SCP_CFG_1	[0]	1'b0	sc_axi_26m_sel_en	Turns on scpsys control path to switch hf_faxi_ck to 26MHz
	[3]	1'b0	sc_pmicspick_26m_sel_en	Turns on scpsys control path to switch hf_fpmicspi_ck to 26MHz

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4.1.7 Frequency Meter

There is one frequency meter inside TOPCKGEN. There are two input clock sources: one is for PLLs and TEST clock, the other is for clocks generated from TOPCKGEN.

It has PAD output that can observe frequency directly instead of reading results from the frequency meter through DEBUG_MON[0].

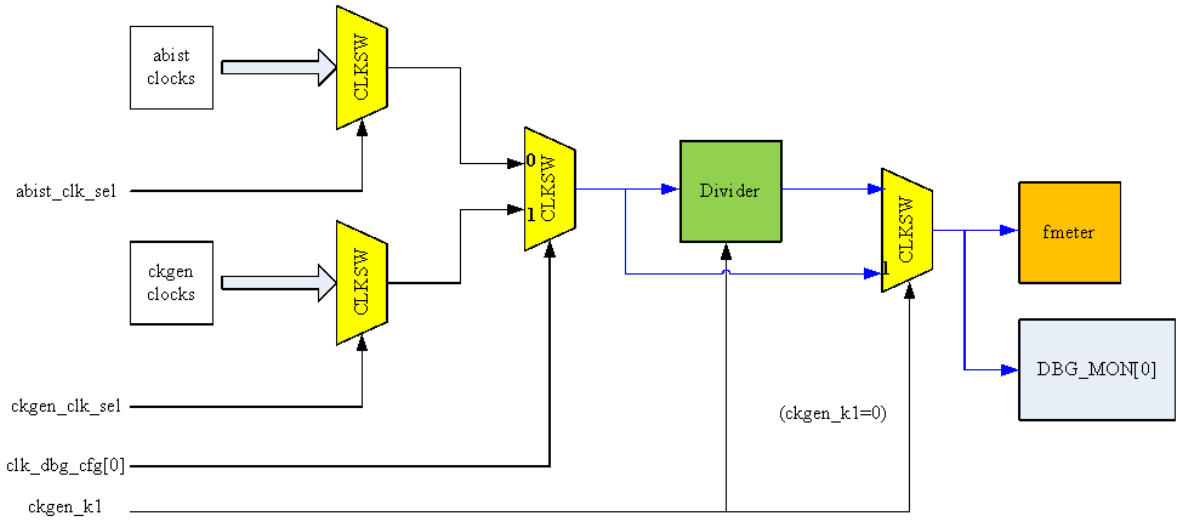

Figure 4-4. TOPCKGEN FMETER structure

4.1.8 Register Definition

See chapter 2.1 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

4.1.9 Programming Guide

4.1.9.1 Clock Off

- The clock can be turned on/off through changing the value of pdn_*. However, this control cannot be switched along with clk_*_sel and clk_*_inv.
- It is recommended to change pdn_* with SET and CLEAR function provided by CLK_CFG_*_SET and CLK_CFG_*_CLR. Because there may be clock with multi-bit pdn_* which are planned to avoid read modify write from different sub-systems (APSYS, MDSYS) at the same time.
- SET and CLEAR function of CLK_CFG_* is a solution to avoid read modify write from different sub-systems.

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4.1.9.2 Clock Switching

- Make sure clock A and clock B are available before changing the setting of clk_*_sel. If switched to a non-exist clock, the clock switch will be stuck until non-exist clock is turned on to free the clock switch.
- Supports multi-clock switching at the same time (without changing pdn_*)

Switching from clock A to clock B

1. Make sure clock B is ready.
2. Change clk_*_sel.
3. Write *_ck_update
4. Wait until chg_sta = 1'b0 (optional).
5. Turn off clock A (optional).

4.1.9.3 Switch AXI to 26MHz by SCPSYS

The reflection time is about 17T 26MHz if all clocks are counted as 26MHz. Refer to the following formula:

$$4T\ Bus\ Clock_{(*1)} + 4T\ Current\ Clock_{(*2)} + 5T\ Reference\ Clock_{(*3)} + 1T\ Bus\ Clock_{(*4)} + 3T\ Target\ Clock_{(*5)}$$

Comment	Description
Bus clock	26MHz (in current project)
Ref clock	26MHz, balance with bus clock
*1	2T Sync + 1 T Control
*2	3T sync
*3	4T sync
*4	1T control. For async CLKSW like hf_fmem_ck used, it will be 2T sync.
*5	2T sync

4.1.9.4 Frequency Meter

There are two frequency meters embedded inside TOPCKGEN.

1. Set fmeter_en to 1'b1.
2. Choose frequency meter source by clk_dbg_cfg[0]
3. Choose target clock by changing abist_clk_sel / ckgen_clk_sel.
4. Change ckgen_k1 for dividing target clock (optional).
5. Change reference clock by changing clk_exc (optional).
6. Change ckgen_load_cnt (optional).
7. Trigger frequency meter by set ckgen_tri_cal = 1b'1.
8. Wait until ckgen_tri_cal = 1'b0.
9. Read frequency meter result from ckgen_cal_cnt.
    - freq(target) = (ckgen_k1 + 1)*[freq(reference clock)*ckgen_cal_cnt]/(ckgen_load_cnt + 1)

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4.2 Top Reset Generator Unit

4.2.1 Introduction

The top reset generator unit (TOPRGU) generates reset signals and distributes to each system. A watchdog timer is also included in this module.

4.2.2 Features

- Hardware reset signals for the whole chip
- Software controllable reset for each system (except for infrastructure and apmixedsys system)
- Watchdog timer
- Reset output signals for companion chips

4.2.3 Block Diagram

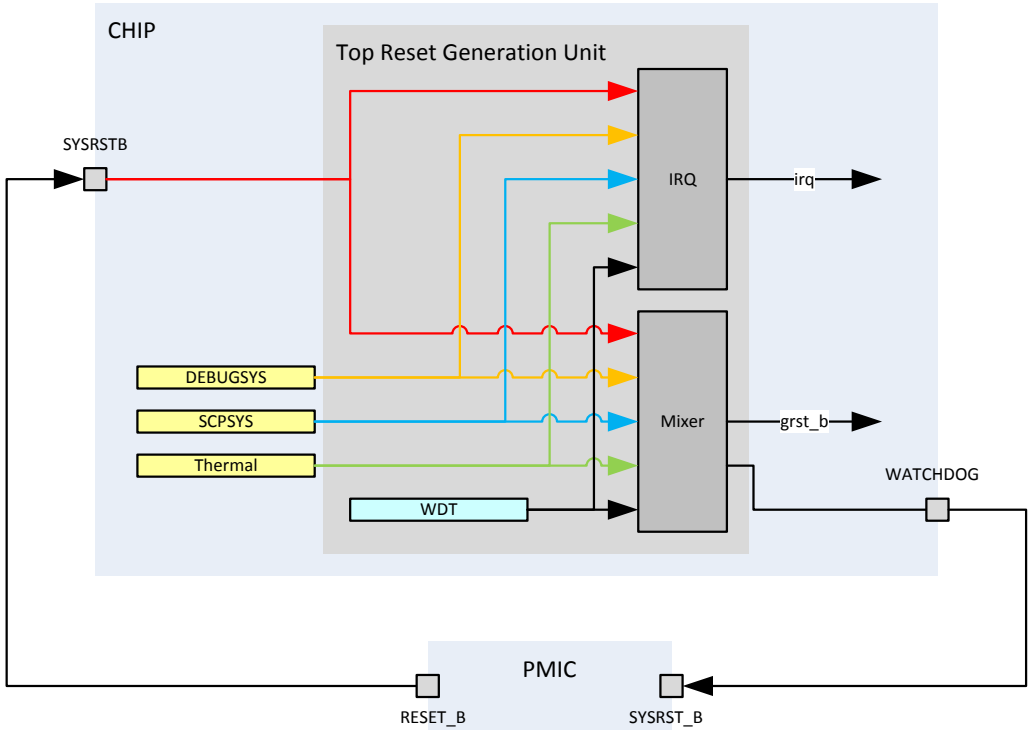

Figure 4-5. Block diagram of top reset generation unit

4.2.4 Register Definition

See chapter 2.2 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

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4.2.5 Programming Guide

4.2.5.1 TOPRGU Initialization

Enable dual mode reset when TOPRGU is first initialized. Because WDT_MODE will not be reset and the dual mode will be disabled if system reset is triggered through WDT_SWRST, these registers will only be reset by SYSRSTB.

The following registers will not be reset by TOPRGU.

- WDT_MODE
- WDT_STA
- WDT_NONRST_REG
- WDT_NONRST_REG2
- WDT_REQ_MODE
- WDT_REQ_IRQ_EN
- WDT_DEBUG_CTL

4.2.5.2 Watchdog Timer

- Trigger WDT_RESTART right after WDT_LENGTH is updated.
- WDT_SWRST can be triggered without wdt_en set to 1'b1.
- It is recommended to trigger WDT_RESTART before setting wdt_en to 1'b1.

4.2.5.3 IRQ Mode

Dual mode reset is default on. Therefore, all reset requests are default with IRQ mode enabled. This means the interrupt is triggered instead of triggering system reset immediately. To trigger system reset instead of interrupt, change the corresponding configuration of each reset request.

Each reset request can be configured as reset or IRQ separately.

4.2.5.4 MDSYS and CONNSYS Watchdog Timeout

MDSYS and CONNSYS have their own watchdog timer. When their watchdog timers expire, they notify AP through interrupts. AP then asserts software reset to MDSYS or CONNSYS.

- MDSYS
  - Enable bus protection to/from MDSYS.
  - Set md_rst = 1'b1.
  - Wait for 2T 32kHz then set md_rst = 1'b0.
  - Disable bus protection to/from MDSYS.
  - Set up MDSYS boot slave.
  - Inform MDSYS abnormal reset via CCIF after MDSYS is ready.

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- CONSYS
  - conn_rst = 1'b1
  - Wait for 2T 32kHz then set conn_rst = 1'b0.

4.2.5.5 Dual Mode Reset

Dual mode reset is system reset after TOPRGU triggers interrupt. The watchdog timer needs to be enabled to complete this function.

In this mode, the watchdog timer will be ***AUTO-RESTART*** after interrupt is triggered. AP should clear WDT_STA after receiving interrupt from TOPRGU, or system reset will be triggered after watchdog timer expires.

- Set wdt_en = 1'b1.
- Set dual_mode = 1'b1.
- Set wdt_irq, thermal_irq, scpsys_irq or debug_irq to 1'b1.

4.2.5.6 DDR Protect

DDR protect (rg_ddr_protect_en) is useless when DDR reserved mode is enabled.

4.2.5.7 DDR Reserved Mode Reset

DDR reserved mode keeps data in DDR during system reset. In order to complete this function, DRAMC, DRMC_CONF, DDRPHY_CONF and EMI_CONF (optional) will not be reset.

- Enable DDR reserved mode when initializing TOPRGU.
- Wait for system reset to be triggered.
- [Optional] Check DDR reserved mode status (ddr_reserve_sta).
- After system reset, release DRAMC_CONF protect (set rg_dramc_conf_iso = 1'b0).
- Ensure related clocks of EMI, DRAMC, DDRPHY are ready (including PLL).
- Wait for dramc_sref_sta = 1'b1.
- Release DRAMC protect (set rg_dramc_iso = 1'b0).
- Release DRAMC self-refresh control (set rg_dramc_sref = 1'b0).
- Wait for dramc_sref_sta = 1'b0.

4.2.5.8 History

- EXT RESET is for NAND and PMIC, but there is exception.
  - MT6329 needs to disable WDT_MODE[2].
- WDT_LENGTH needs to be reset, or SYSTEM will enter RESET loop if WDT_LENGTH has been set to very short before reset trigger.

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4.3 PMIC Wrapper

4.3.1 Introduction

The PMIC wrapper is the bridge for communication between AP and PMIC.

4.3.2 Feature

- Fast auto SPI format generator for PMIC register read/write
- APB3.0 bus lock scheme when SPI is busy
- Manual SPI format generator
- Supports access to dual PMICs
- Single and dual I/O SPI mode support for PMIC
- Single IO mode support only for Switching Charger
- Separated frequency between controller and SPI

4.3.3 Block Diagram

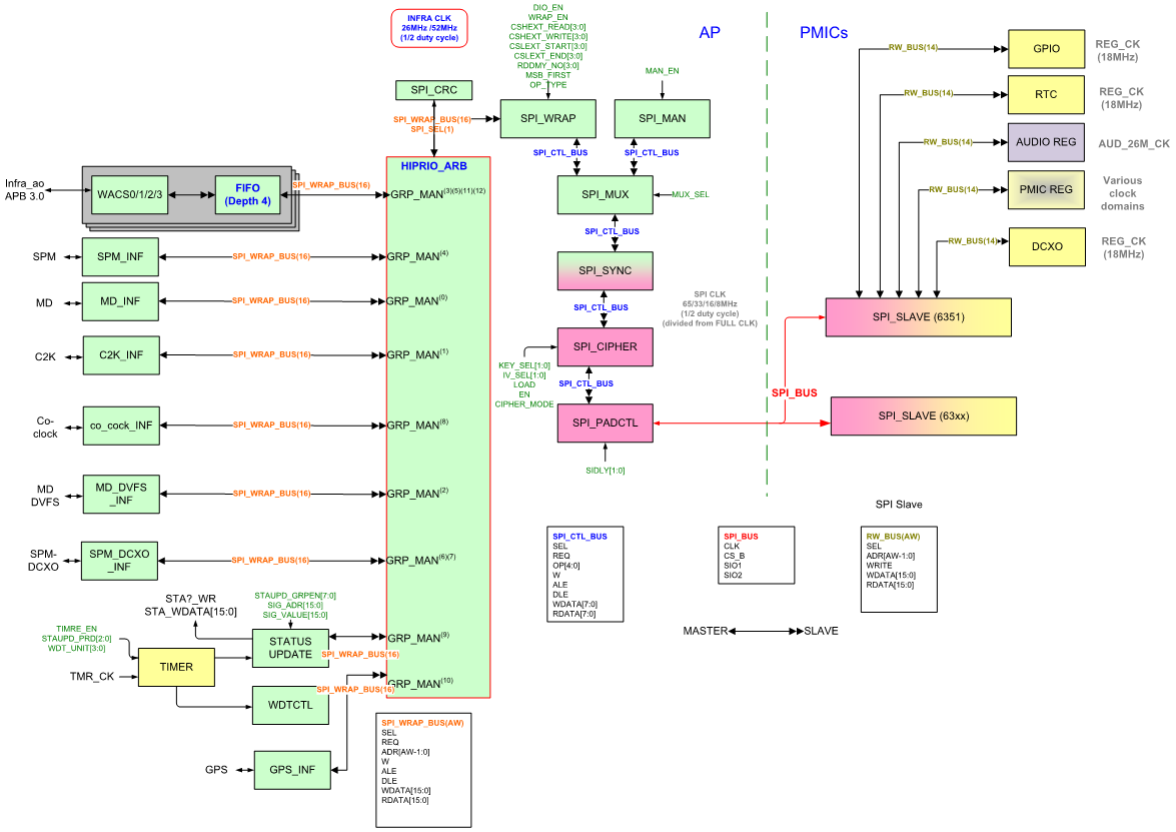

Figure 4-6. PMIC_WRAP architecture

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4.3.4 Register Definition

See chapter 2.3 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

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4.4 Frequency Hopping Controller

4.4.1 Introduction

The frequency hopping controller helps AP resolve de-sense issues. The RF victims are 2G, 3G, BT, FM, Wi-Fi, GPS, etc. The aggressors in AP are the clocks generated from PLL in ABB. The harmonic of all clock frequencies may de-sense the band of RF system.

4.4.2 Features

The frequency hopping controller receives commands from CPU to trigger two mechanisms:

- Spread spectrum clocking
- Frequency hopping

4.4.3 Block Diagram

Whenever MCUSYS enters sleep mode, SRCLKENA from the sleep controller is de-asserted. The SRCLKENA from MCUSYS controls the power supply for the 13MHz/26MHz TCVCXO via the on-chip PMU. When the signal is de-asserted, the LDO for TCVCXO in the PMU will be turned off then 13MHz/26MHz clock will stop.

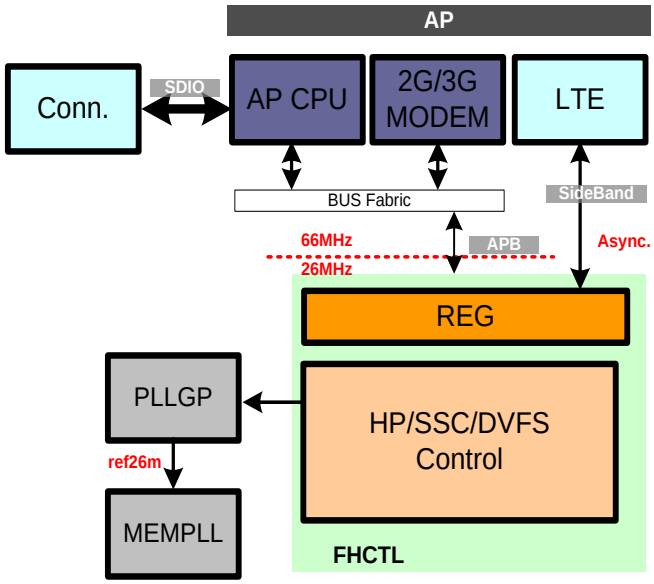

Figure 4-7. Block diagram of frequency hopping controller

4.4.4 Register Definition

See chapter 2.4 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

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5 Peripherals

5.1 Pericfg Controller

5.1.1 Introduction

The pericfg controller controls the reset, clock and bus setting of peripheral subsys. Each module inside the peripheral subsys has its own software reset and clock gated control (power-down control). The hardware DCM (Dynamic Clock Management) of the peripheral subsys is also controlled in the pericfg controller. Beside AP MCU, the modem MCU can also use this pericfg controller to control specific modules clock gated control (power-down control).

5.1.2 Features

- Supports software reset control of each module inside peripheral subsys
- Supports clock gated control of the modules insider peripheral subsys by AP MCU
- Supports clock gated control of the modules insider peripheral subsys by Modem1 MCU
- Supports clock gated control of the modules insider peripheral subsys by Modem2 MCU
- Supports DCM control of peripheral subsys
- Supports bus setting (bandwidth limit/way enable/...) of peripheral subsys

5.1.3 Block Diagram

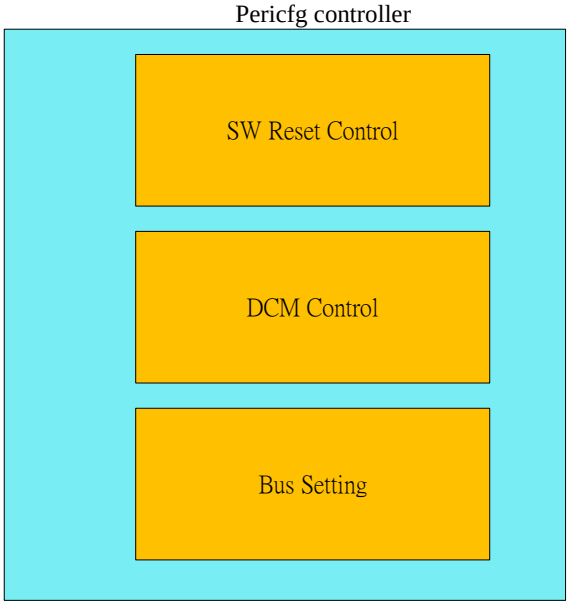

Figure 5-1. Block diagram of pericfg controller

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5.1.4 Register Definition

See chapter 3.1 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

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5.2 GPIO Control

5.2.1 General Descriptions

There are 190 I/O pins that can be programmed as multiple-purpose pins, which are GPIO, NAND, SPI, etc. By setting up the GPIO_MODE register, specific IO can be selected for specific function.

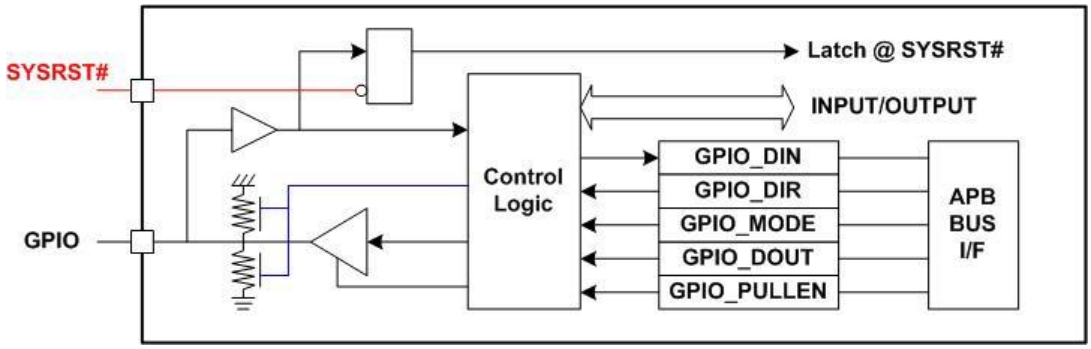

Figure 5-2. GPIO block diagram

All functions should comply with the priority rule. When there are more than one IO set as the same output function, all of the selected IOs are able to output specific signals. When there are more than one IO set as the same input (or bi-directional) function, only the IO with the largest GPIO index can work functionally.

When the MIPI function is not used, related IOs can be switched to non-MIPI input-only function, like EINT. To enable the GPI function of MIPI, there are some configurations to be done before the related GPIO_MODE is set.

Table 5-1. Summary of configuration registers of GPIOs

Name	IES	SMT	Pullen	Pullsel	PUPD
PAD_EINT0	0x1000_2600[5]	0x1000_2610[5]	0x1000_2660[14]	0x1000_2680[14]	FALSE
PAD_EINT1	0x1000_2600[5]	0x1000_2610[5]	0x1000_2660[15]	0x1000_2680[15]	FALSE
PAD_EINT2	0x1000_2600[5]	0x1000_2610[5]	0x1000_2660[16]	0x1000_2680[16]	FALSE
PAD_EINT3	0x1000_2600[5]	0x1000_2610[5]	0x1000_2660[17]	0x1000_2680[17]	FALSE
PAD_EINT4	0x1000_2600[6]	0x1000_2610[6]	0x1000_2660[18]	0x1000_2680[18]	FALSE
PAD_EINT5	0x1000_2600[6]	0x1000_2610[6]	0x1000_2660[19]	0x1000_2680[19]	FALSE
PAD_EINT6	0x1000_2600[6]	0x1000_2610[6]	0x1000_2660[20]	0x1000_2680[20]	FALSE
PAD_EINT7	0x1000_2600[6]	0x1000_2610[6]	0x1000_2660[21]	0x1000_2680[21]	FALSE
PAD_EINT8	0x1000_2600[12]	0x1000_2610[12]	0x1000_2660[30]	0x1000_2680[30]	FALSE
PAD_EINT9	0x1000_2600[13]	0x1000_2610[13]	0x1000_2660[31]	0x1000_2680[31]	FALSE
PAD_EINT10	0x1000_2600[13]	0x1000_2610[13]	0x1000_2670[0]	0x1000_2690[0]	FALSE
PAD_EINT11	0x1000_2000[3]	0x1000_2010[3]	0x1000_2060[5]	0x1000_2080[5]	FALSE
PAD_EINT12	0x1000_2000[7]	0x1000_2010[7]	0x1000_2060[12]	0x1000_2080[12]	FALSE
PAD_DPI_D0	0x1000_2200[5]	0x1000_2210[5]	0x1000_2260[11]	0x1000_2280[11]	FALSE
PAD_DPI_D1	0x1000_2200[5]	0x1000_2210[5]	0x1000_2260[12]	0x1000_2280[12]	FALSE

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Name	IES	SMT	Pullen	Pullsel	PUPD
PAD_DPI_D2	0x1000_2200[5]	0x1000_2210[5]	0x1000_2260[13]	0x1000_2280[13]	FALSE
PAD_DPI_D3	0x1000_2200[5]	0x1000_2210[5]	0x1000_2260[14]	0x1000_2280[14]	FALSE
PAD_DPI_D4	0x1000_2200[6]	0x1000_2210[6]	0x1000_2260[15]	0x1000_2280[15]	FALSE
PAD_DPI_D5	0x1000_2200[6]	0x1000_2210[6]	0x1000_2260[16]	0x1000_2280[16]	FALSE
PAD_DPI_D6	0x1000_2200[6]	0x1000_2210[6]	0x1000_2260[17]	0x1000_2280[17]	FALSE
PAD_DPI_D7	0x1000_2200[6]	0x1000_2210[6]	0x1000_2260[18]	0x1000_2280[18]	FALSE
PAD_DPI_D8	0x1000_2200[7]	0x1000_2210[7]	0x1000_2260[19]	0x1000_2280[19]	FALSE
PAD_DPI_D9	0x1000_2200[7]	0x1000_2210[7]	0x1000_2260[20]	0x1000_2280[20]	FALSE
PAD_DPI_D10	0x1000_2200[7]	0x1000_2210[7]	0x1000_2260[21]	0x1000_2280[21]	FALSE
PAD_DPI_D11	0x1000_2200[7]	0x1000_2210[7]	0x1000_2260[22]	0x1000_2280[22]	FALSE
PAD_DPI_HSYNC	0x1000_2200[8]	0x1000_2210[8]	0x1000_2260[23]	0x1000_2280[23]	FALSE
PAD_DPI_VSYNC	0x1000_2200[8]	0x1000_2210[8]	0x1000_2260[24]	0x1000_2280[24]	FALSE
PAD_DPI_DE	0x1000_2200[8]	0x1000_2210[8]	0x1000_2260[25]	0x1000_2280[25]	FALSE
PAD_DPI_CK	0x1000_2200[8]	0x1000_2210[8]	0x1000_2260[26]	0x1000_2280[26]	FALSE
PAD_SRCLKENA1	0x1000_2000[6]	0x1000_2010[6]	0x1000_2060[11]	0x1000_2080[11]	FALSE
PAD_MSDC1_CLK	0x1000_2000[8]	0x1000_2010[8]	FALSE	FALSE	0x100020C0[2:0]
PAD_MSDC1_DAT3	0x1000_2000[9]	0x1000_2010[9]	FALSE	FALSE	0x100020C0[6:4]
PAD_MSDC1_CMD	0x1000_2000[10]	0x1000_2010[10]	FALSE	FALSE	0x100020C0[10:8]
PAD_MSDC1_DAT0	0x1000_2000[9]	0x1000_2010[9]	FALSE	FALSE	0x100020C0[14:12]
PAD_MSDC1_DAT2	0x1000_2000[9]	0x1000_2010[9]	FALSE	FALSE	0x100020C0[18:16]
PAD_MSDC1_DAT1	0x1000_2000[9]	0x1000_2010[9]	FALSE	FALSE	0x100020C0[22:20]
PAD_SIM2_SIO	0x1000_2000[11]	0x1000_2010[11]	FALSE	FALSE	0x100020D0[3:0]
PAD_SIM2_SRST	0x1000_2000[11]	0x1000_2010[11]	FALSE	FALSE	0x100020D0[7:4]
PAD_SIM2_SCLK	0x1000_2000[11]	0x1000_2010[11]	FALSE	FALSE	0x100020D0[11:8]
PAD_SIM1_SCLK	0x1000_2000[12]	0x1000_2010[12]	FALSE	FALSE	0x100020D0[15:12]
PAD_SIM1_SRST	0x1000_2000[12]	0x1000_2010[12]	FALSE	FALSE	0x100020D0[19:16]
PAD_SIM1_SIO	0x1000_2000[12]	0x1000_2010[12]	FALSE	FALSE	0x100020D0[23:20]
PAD_IDDIG	0x1000_2200[0]	0x1000_2210[0]	FALSE	FALSE	0x100022C0[2:0]
PAD_DRVBUS	0x1000_2200[0]	0x1000_2210[0]	FALSE	FALSE	0x100022C0[6:4]
PAD_DSI_TE	0x1000_2200[1]	0x1000_2210[1]	0x1000_2260[3]	0x1000_2280[3]	FALSE
PAD_INT_SIM2	0x1000_2200[2]	0x1000_2210[2]	0x1000_2260[5]	0x1000_2280[5]	FALSE
PAD_INT_SIM1	0x1000_2200[2]	0x1000_2210[2]	0x1000_2260[6]	0x1000_2280[6]	FALSE
PAD_SCL_APPM	0x1000_2200[3]	0x1000_2210[3]	0x1000_2260[7]	0x1000_2280[7]	FALSE
PAD_SDA_APPM	0x1000_2200[3]	0x1000_2210[3]	0x1000_2260[8]	0x1000_2280[8]	FALSE

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Name	IES	SMT	Pullen	Pullsel	PUPD
PAD_SCL3	0x1000_2200[4]	0x1000_2210[4]	0x1000_2260[9]	0x1000_2280[9]	FALSE
PAD_SDA3	0x1000_2200[4]	0x1000_2210[4]	0x1000_2260[10]	0x1000_2280[10]	FALSE
PAD_BPI_ANT3	0x1000_2200[9]	0x1000_2210[9]	0x1000_2260[27]	0x1000_2280[27]	FALSE
PAD_BPI_ANT2	0x1000_2200[9]	0x1000_2210[9]	0x1000_2260[28]	0x1000_2280[28]	FALSE
PAD_BPI_ANT1	0x1000_2200[9]	0x1000_2210[9]	0x1000_2260[29]	0x1000_2280[29]	FALSE
PAD_BPI_ANT0	0x1000_2200[9]	0x1000_2210[9]	0x1000_2260[30]	0x1000_2280[30]	FALSE
PAD_BPI_BUS11	0x1000_2200[9]	0x1000_2210[9]	0x1000_2260[31]	0x1000_2280[31]	FALSE
PAD_BPI_BUS10	0x1000_2200[9]	0x1000_2210[9]	0x1000_2270[0]	0x1000_2290[0]	FALSE
PAD_BPI_BUS9	0x1000_2200[9]	0x1000_2210[9]	0x1000_2270[1]	0x1000_2290[1]	FALSE
PAD_BPI_BUS8	0x1000_2200[9]	0x1000_2210[9]	0x1000_2270[2]	0x1000_2290[2]	FALSE
PAD_BPI_BUS7	0x1000_2200[9]	0x1000_2210[9]	0x1000_2270[3]	0x1000_2290[3]	FALSE
PAD_BPI_BUS6	0x1000_2200[9]	0x1000_2210[9]	0x1000_2270[4]	0x1000_2290[4]	FALSE
PAD_BPI_BUS5	0x1000_2200[9]	0x1000_2210[9]	0x1000_2270[5]	0x1000_2290[5]	FALSE
PAD_BPI_BUS4	0x1000_2200[9]	0x1000_2210[9]	0x1000_2270[6]	0x1000_2290[6]	FALSE
PAD_MISC_BSI_DO_1	0x1000_2200[10]	0x1000_2210[10]	0x1000_2270[7]	0x1000_2290[7]	FALSE
PAD_MISC_BSI_CK_1	0x1000_2200[10]	0x1000_2210[10]	0x1000_2270[8]	0x1000_2290[8]	FALSE
PAD_MISC_BSI_DO_0	0x1000_2200[10]	0x1000_2210[10]	0x1000_2270[9]	0x1000_2290[9]	FALSE
PAD_MISC_BSI_CK_0	0x1000_2200[10]	0x1000_2210[10]	0x1000_2270[10]	0x1000_2290[10]	FALSE
PAD_RFIC0_BSI_D2	0x1000_2200[11]	0x1000_2210[11]	0x1000_2270[11]	0x1000_2290[11]	FALSE
PAD_RFIC0_BSI_D1	0x1000_2200[11]	0x1000_2210[11]	0x1000_2270[12]	0x1000_2290[12]	FALSE
PAD_RFIC0_BSI_D0	0x1000_2200[11]	0x1000_2210[11]	0x1000_2270[13]	0x1000_2290[13]	FALSE
PAD_AUXIN0	NA	NA	NA	NA	FALSE
PAD_AUXIN1	NA	NA	NA	NA	FALSE
PAD_AUXIN2	NA	NA	NA	NA	FALSE
PAD_AUXIN3	NA	NA	NA	NA	FALSE
PAD_AUXIN4	NA	NA	NA	NA	FALSE
PAD_MISC_BSI_DO_3	0x1000_2400[0]	0x1000_2410[0]	0x1000_2460[0]	0x1000_2480[0]	FALSE
PAD_MISC_BSI_CK_3	0x1000_2400[0]	0x1000_2410[0]	0x1000_2460[1]	0x1000_2480[1]	FALSE
PAD_MISC_BSI_DO_2	0x1000_2400[0]	0x1000_2410[0]	0x1000_2460[2]	0x1000_2480[2]	FALSE
PAD_MISC_BSI_CK_2	0x1000_2400[0]	0x1000_2410[0]	0x1000_2460[3]	0x1000_2480[3]	FALSE
PAD_BPI_BUS3	0x1000_2400[1]	0x1000_2410[1]	0x1000_2460[4]	0x1000_2480[4]	FALSE

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Name	IES	SMT	Pullen	Pullsel	PUPD
PAD_BPI_BUS2	0x1000_2400[1]	0x1000_2410[1]	0x1000_2460[5]	0x1000_2480[5]	FALSE
PAD_BPI_BUS1	0x1000_2400[1]	0x1000_2410[1]	0x1000_2460[6]	0x1000_2480[6]	FALSE
PAD_BPI_BUS0	0x1000_2400[1]	0x1000_2410[1]	0x1000_2460[7]	0x1000_2480[7]	FALSE
PAD_DET_BPI1	0x1000_2400[2]	0x1000_2410[2]	0x1000_2460[8]	0x1000_2480[8]	FALSE
PAD_DET_BPI0	0x1000_2400[2]	0x1000_2410[2]	0x1000_2460[9]	0x1000_2480[9]	FALSE
PAD_TX_SWAP3	0x1000_2400[2]	0x1000_2410[2]	0x1000_2460[10]	0x1000_2480[10]	FALSE
PAD_TX_SWAP2	0x1000_2400[2]	0x1000_2410[2]	0x1000_2460[11]	0x1000_2480[11]	FALSE
PAD_TX_SWAP1	0x1000_2400[3]	0x1000_2410[3]	0x1000_2460[12]	0x1000_2480[12]	FALSE
PAD_TX_SWAP0	0x1000_2400[3]	0x1000_2410[3]	0x1000_2460[13]	0x1000_2480[13]	FALSE
PAD_PA_VM1	0x1000_2400[3]	0x1000_2410[3]	0x1000_2460[14]	0x1000_2480[14]	FALSE
PAD_PA_VM0	0x1000_2400[3]	0x1000_2410[3]	0x1000_2460[15]	0x1000_2480[15]	FALSE
PAD_SDA1	0x1000_2600[0]	0x1000_2610[0]	0x1000_2660[0]	0x1000_2680[0]	FALSE
PAD_SDA0	0x1000_2600[1]	0x1000_2610[1]	0x1000_2660[1]	0x1000_2680[1]	FALSE
PAD_SCL0	0x1000_2600[1]	0x1000_2610[1]	0x1000_2660[2]	0x1000_2680[2]	FALSE
PAD_SCL1	0x1000_2600[0]	0x1000_2610[0]	0x1000_2660[3]	0x1000_2680[3]	FALSE
PAD_SPI_MI	0x1000_2600[2]	0x1000_2610[2]	0x1000_2660[4]	0x1000_2680[4]	FALSE
PAD_SPI_CSB	0x1000_2600[2]	0x1000_2610[2]	0x1000_2660[5]	0x1000_2680[5]	FALSE
PAD_SPI_MO	0x1000_2600[2]	0x1000_2610[2]	0x1000_2660[6]	0x1000_2680[6]	FALSE
PAD_SPI_CLK	0x1000_2600[2]	0x1000_2610[2]	0x1000_2660[7]	0x1000_2680[7]	FALSE
PAD_SRCLKENAI	0x1000_2600[3]	0x1000_2610[3]	0x1000_2660[8]	0x1000_2680[8]	FALSE
PAD_PWM_A	0x1000_2600[3]	0x1000_2610[3]	0x1000_2660[9]	0x1000_2680[9]	FALSE
PAD_KPROW1	0x1000_2600[4]	0x1000_2610[4]	FALSE	FALSE	0x100026C0[2:0]
PAD_KPROW0	0x1000_2600[4]	0x1000_2610[4]	FALSE	FALSE	0x100026C0[6:4]
PAD_KPCOL0	0x1000_2600[4]	0x1000_2610[4]	FALSE	FALSE	0x100026C0[18:16]
PAD_KPCOL1	0x1000_2600[4]	0x1000_2610[4]	FALSE	FALSE	0x100026C0[22:20]
PAD_URXD0	0x1000_2600[7]	0x1000_2610[7]	0x1000_2660[22]	0x1000_2680[22]	FALSE
PAD_UTXD0	0x1000_2600[7]	0x1000_2610[7]	0x1000_2660[23]	0x1000_2680[23]	FALSE
PAD_CAM_PDN0	0x1000_2600[8]	0x1000_2610[8]	0x1000_2660[24]	0x1000_2680[24]	FALSE
PAD_CAM_PDN1	0x1000_2600[8]	0x1000_2610[8]	0x1000_2660[25]	0x1000_2680[25]	FALSE
PAD_CAM_CLK1	0x1000_2600[10]	0x1000_2610[10]	0x1000_2660[27]	0x1000_2680[27]	FALSE
PAD_CAM_RST0	0x1000_2600[11]	0x1000_2610[11]	0x1000_2660[28]	0x1000_2680[28]	FALSE
PAD_CAM_RST1	0x1000_2600[11]	0x1000_2610[11]	0x1000_2660[29]	0x1000_2680[29]	FALSE
PAD_SCL2	0x1000_2600[14]	0x1000_2610[14]	0x1000_2670[1]	0x1000_2690[1]	FALSE
PAD_SDA2	0x1000_2600[14]	0x1000_2610[14]	0x1000_2670[2]	0x1000_2690[2]	FALSE
PAD_ANT_SEL0	0x1000_2800[0]	0x1000_2810[0]	FALSE	FALSE	0x100028C0[2:0]

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Name	IES	SMT	Pullen	Pullsel	PUPD
PAD_ANT_SEL1	0x1000_2800[0]	0x1000_2810[0]	FALSE	FALSE	0x100028C0[6:4]
PAD_ANT_SEL2	0x1000_2800[0]	0x1000_2810[0]	FALSE	FALSE	0x100028C0[10:8]
PAD_F2W_DATA	0x1000_2800[1]	0x1000_2810[1]	0x1000_2860[3]	0x1000_2880[3]	FALSE
PAD_F2W_CLK	0x1000_2800[1]	0x1000_2810[1]	0x1000_2860[4]	0x1000_2880[4]	FALSE
PAD_WB_RSTB	0x1000_2800[2]	0x1000_2810[2]	0x1000_2860[5]	0x1000_2880[5]	FALSE
PAD_WB_SCLK	0x1000_2800[2]	0x1000_2810[2]	0x1000_2860[6]	0x1000_2880[6]	FALSE
PAD_WB_SDATA	0x1000_2800[2]	0x1000_2810[2]	0x1000_2860[7]	0x1000_2880[7]	FALSE
PAD_WB_SEN	0x1000_2800[2]	0x1000_2810[2]	0x1000_2860[8]	0x1000_2880[8]	FALSE
PAD_GPS_RXQN	NA	NA	NA	NA	FALSE
PAD_GPS_RXQP	NA	NA	NA	NA	FALSE
PAD_GPS_RXIN	NA	NA	NA	NA	FALSE
PAD_GPS_RXIP	NA	NA	NA	NA	FALSE
PAD_WB_RXQN	NA	NA	NA	NA	FALSE
PAD_WB_RXQP	NA	NA	NA	NA	FALSE
PAD_WB_RXIN	NA	NA	NA	NA	FALSE
PAD_WB_RXIP	NA	NA	NA	NA	FALSE
PAD_WB_CTRL0	0x1000_2800[3]	0x1000_2810[3]	FALSE	FALSE	0x100028C0[14:12]
PAD_WB_CTRL1	0x1000_2800[4]	0x1000_2810[4]	FALSE	FALSE	0x100028C0[18:16]
PAD_WB_CTRL2	0x1000_2800[5]	0x1000_2810[5]	FALSE	FALSE	0x100028C0[22:20]
PAD_WB_CTRL3	0x1000_2800[3]	0x1000_2810[3]	FALSE	FALSE	0x100028C0[26:24]
PAD_WB_CTRL4	0x1000_2800[3]	0x1000_2810[3]	FALSE	FALSE	0x100028C0[30:28]
PAD_WB_CTRL5	0x1000_2800[3]	0x1000_2810[3]	FALSE	FALSE	0x100018D0[2:0]
PAD_TDP0	NA	NA	NA	NA	FALSE
PAD_TDN0	NA	NA	NA	NA	FALSE
PAD_TDP1	NA	NA	NA	NA	FALSE
PAD_TDN1	NA	NA	NA	NA	FALSE
PAD_TCP	NA	NA	NA	NA	FALSE
PAD_TCN	NA	NA	NA	NA	FALSE
PAD_TDP2	NA	NA	NA	NA	FALSE
PAD_TDN2	NA	NA	NA	NA	FALSE
PAD_TDP3	NA	NA	NA	NA	FALSE
PAD_TDN3	NA	NA	NA	NA	FALSE

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Name	IES	SMT	Pullen	Pullsel	PUPD
PAD_RTC32K_CK	0x1000_2000[0]	0x1000_2010[0]	0x1000_2060[0]	0x1000_2080[0]	FALSE
PAD_WATCHDOG	0x1000_2000[1]	0x1000_2010[1]	0x1000_2060[1]	0x1000_2080[1]	FALSE
PAD_AUD_CLK_MOSI	0x1000_2000[2]	0x1000_2010[2]	0x1000_2060[2]	0x1000_2080[2]	FALSE
PAD_AUD_DAT_MOSI	0x1000_2000[2]	0x1000_2010[2]	0x1000_2060[3]	0x1000_2080[3]	FALSE
PAD_AUD_DAT_MISO	0x1000_2000[2]	0x1000_2010[2]	0x1000_2060[4]	0x1000_2080[4]	FALSE
PAD_PWRAP_SPI0_MI	0x1000_2000[4]	0x1000_2010[4]	0x1000_2060[6]	0x1000_2080[6]	FALSE
PAD_PWRAP_SPI0_CSN	0x1000_2000[4]	0x1000_2010[4]	0x1000_2060[7]	0x1000_2080[7]	FALSE
PAD_PWRAP_SPI0_MO	0x1000_2000[4]	0x1000_2010[4]	0x1000_2060[8]	0x1000_2080[8]	FALSE
PAD_PWRAP_SPI0_CK	0x1000_2000[4]	0x1000_2010[4]	0x1000_2060[9]	0x1000_2080[9]	FALSE
PAD_SRCLKENA0	0x1000_2000[5]	0x1000_2010[5]	0x1000_2060[10]	0x1000_2080[10]	FALSE
PAD_DISP_PWM	0x1000_2200[1]	0x1000_2210[1]	0x1000_2260[2]	0x1000_2280[2]	FALSE
PAD_LCM_RST	0x1000_2200[1]	0x1000_2210[1]	0x1000_2260[4]	0x1000_2280[4]	FALSE
PAD_RFIC0_BSI_EN	0x1000_2200[11]	0x1000_2210[11]	0x1000_2270[14]	0x1000_2290[14]	FALSE
PAD_RFIC0_BSI_CK	0x1000_2200[11]	0x1000_2210[11]	0x1000_2270[15]	0x1000_2290[15]	FALSE
PAD_CAM_CLK0	0x1000_2600[9]	0x1000_2610[9]	0x1000_2660[26]	0x1000_2680[26]	FALSE
PAD_RDN0	NA	NA	NA	NA	FALSE
PAD_RDP0	NA	NA	NA	NA	FALSE
PAD_RDN1	NA	NA	NA	NA	FALSE
PAD_RDP1	NA	NA	NA	NA	FALSE
PAD_RCN	NA	NA	NA	NA	FALSE
PAD_RCP	NA	NA	NA	NA	FALSE
PAD_RDN2	NA	NA	NA	NA	FALSE
PAD_RDP2	NA	NA	NA	NA	FALSE
PAD_RDN3	NA	NA	NA	NA	FALSE
PAD_RDP3	NA	NA	NA	NA	FALSE
PAD_RDN0_A	NA	NA	NA	NA	FALSE
PAD_RDP0_A	NA	NA	NA	NA	FALSE
PAD_RDN1_A	NA	NA	NA	NA	FALSE
PAD_RDP1_A	NA	NA	NA	NA	FALSE
PAD_RCN_A	NA	NA	NA	NA	FALSE
PAD_RCP_A	NA	NA	NA	NA	FALSE
PAD_MSDC0_DAT0	0x1000_2A00[0]	0x1000_2A10[0]	FALSE	FALSE	0x10002AC0[2:0]
PAD_MSDC0_CLK	0x1000_2A00[1]	0x1000_2A10[1]	FALSE	FALSE	0x10002AC0[6:4]
PAD_MSDC0_CMD	0x1000_2A00[2]	0x1000_2A10[2]	FALSE	FALSE	0x10002AC0[10:8]

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Name	IES	SMT	Pullen	Pullsel	PUPD
PAD_MSDC0_DAT1	0x1000_2A00[0]	0x1000_2A10[0]	FALSE	FALSE	0x10002AC0[14:12]
PAD_MSDC0_DAT5	0x1000_2A00[0]	0x1000_2A10[0]	FALSE	FALSE	0x10002AC0[18:16]
PAD_MSDC0_DAT6	0x1000_2A00[0]	0x1000_2A10[0]	FALSE	FALSE	0x10002AC0[22:20]
PAD_MSDC0_DAT4	0x1000_2A00[0]	0x1000_2A10[0]	FALSE	FALSE	0x10002AC0[26:24]
PAD_MSDC0_RSTB	0x1000_2A00[3]	0x1000_2A10[3]	FALSE	FALSE	0x10002AC0[30:28]
PAD_MSDC0_DAT2	0x1000_2A00[0]	0x1000_2A10[0]	FALSE	FALSE	0x10001AD0[2:0]
PAD_MSDC0_DAT3	0x1000_2A00[0]	0x1000_2A10[0]	FALSE	FALSE	0x10001AD0[6:4]
PAD_MSDC0_DAT7	0x1000_2A00[0]	0x1000_2A10[0]	FALSE	FALSE	0x10001AD0[10:8]
PAD_MSDC0_DSL	0x1000_2A00[4]	0x1000_2A10[4]	FALSE	FALSE	0x10001AD0[14:12]

5.2.2 Register Definition

See chapter 3.2 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

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5.3 Keypad Scanner

5.3.1 General Description

The keypad supports two types of keypads: 3*3 single keys and 3*3 configurable double keys.

The 3*3 keypad can be divided into two parts: 1) The keypad interface including 8 columns and 8 rows (see Figure 5-3 and Figure 5-4); 2) The key detection block provides key pressed, key released and de-bounce mechanisms.

Each time the key is pressed or released, i.e. something different in the 8x8 matrix, the key detection block senses the change and recognizes if a key has been pressed or released. Whenever the key status changes and is stable, a KEYPAD IRQ will be issued. The MCU can then read the key(s) pressed directly in the KP_MEM1, KP_MEM2, KP_MEM3, KP_MEM4 and KP_MEM5 registers. To ensure the key pressed information is not missed, the status register in keypad will not be read-cleared by the APB read command. The status register can only be changed by the key-pressed detection FSM.

This keypad detects one or two keys pressed simultaneously with any combination. Figure 5-7 shows the one key pressed condition. Figure 5-8 (a) and Figure 5-8 (b) illustrate the cases of two keys pressed. Since the key pressed detection depends on the HIGH or LOW level of the external keypad interface, if the keys are pressed at the same time, and there exists a key that is on the same column and the same row with other keys, the pressed key cannot be correctly decoded. For example, if there are three key pressed: key1 = (x1, y1), key2 = (x2, y2), and key3 = (x1, y2), both key3 and key4 = (x2, y1) will be detected, and therefore they cannot be distinguished correctly. Hence, the keypad detects only one or two keys pressed simultaneously in any combination. More than two keys pressed simultaneously in a specific pattern will retrieve the wrong information.

The 3*3 keypad supports a 3*3*2 = 18 keys matrix. The 18 keys are divided into 9 sub groups, and each group consists of 2 keys and a 20 ohm resistor. Besides the limitation of the 3*3 keypad, 3*3 keypad has another limitation, which is it cannot detect two keys pressed simultaneously when the two keys are in one group, i.e. the 3*3 keypad cannot detect key 0 and key 1 pressed simultaneously or key 14 and key 15 pressed simultaneously.

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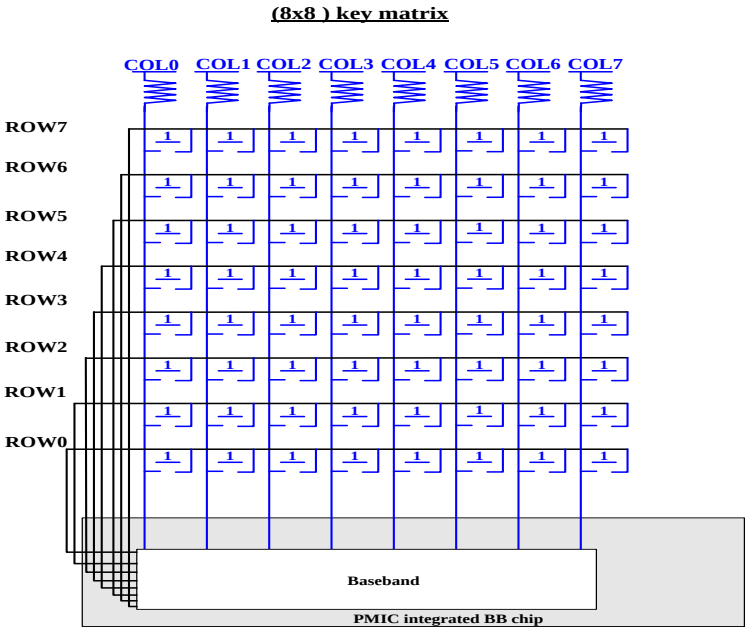

Figure 5-3. 3x3 keypad matrix (9 keys)

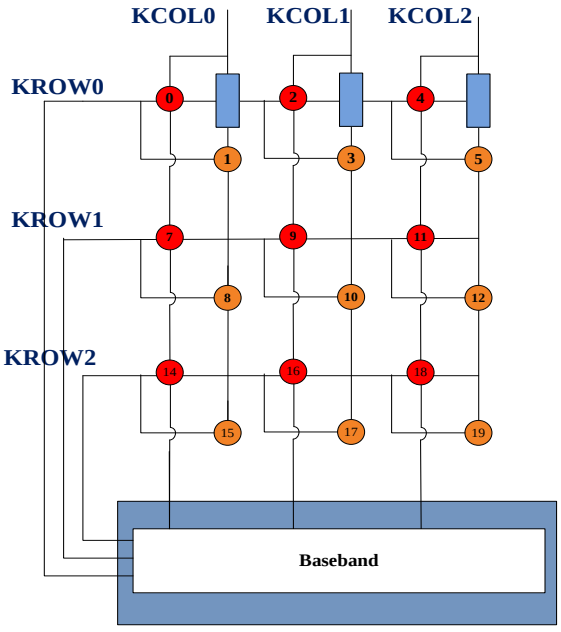

Figure 5-4. 3x3 keypad matrix (18 keys)

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5.3.2 Waveform

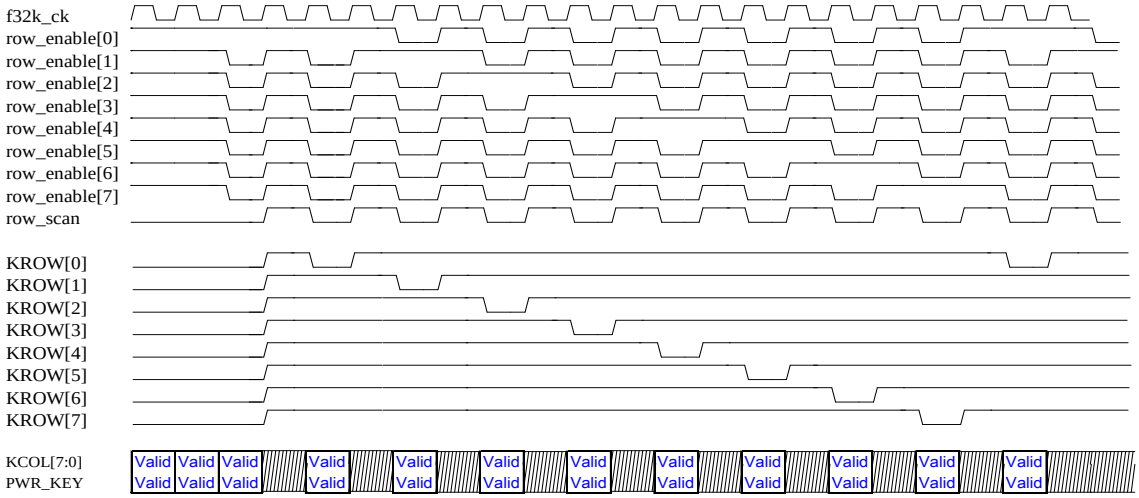

Figure 5-5. 3x3 single keypad scan waveform

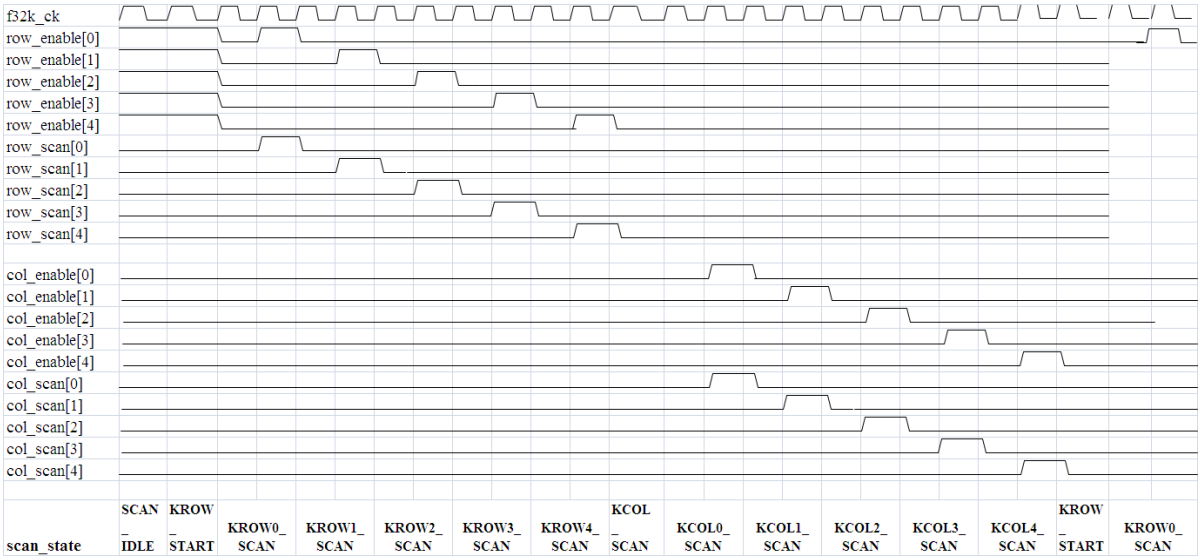

*Figure 5-6. 3*3 double keypad scan waveform*

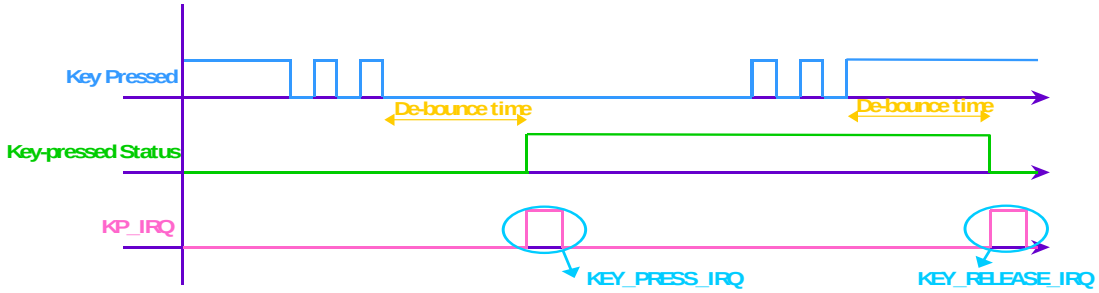

Figure 5-7. One key pressed with de-bounce mechanism denoted

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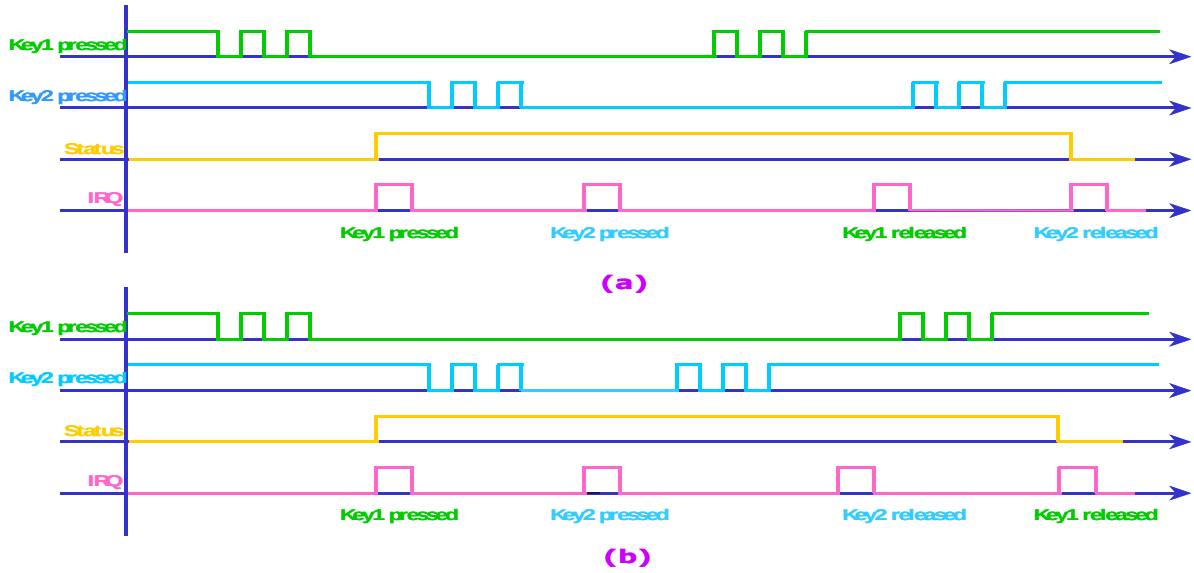

Figure 5-8 (a) Two keys pressed, case 1; (b) Two keys pressed, case 2

5.3.3 Register Definition

See chapter 3.3 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

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5.4 UART

5.4.1 Introduction

The baseband chipset houses four UARTs. UARTs provide full duplex serial communication channels between the baseband chipset and external devices.

UART has both M16C450 and M16550A modes of operation, which are compatible with a range of standard software drivers. The extensions are designed to be broadly software compatible with 16550A variants, but certain areas offer no consensus.

In common with M16550A, the UART supports word lengths from 5 to 8 bits, an optional parity bit and one or two stop bits and is fully programmable by an 8-bit CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmit and receive FIFOs. Two modem control lines and a diagnostic loop-back mode are provided. UART also includes two DMA handshake lines, indicating when the FIFOs are ready to transfer data to the CPU. Interrupts can be generated from any of the ten sources.

Note that UART is designed so that all internal operation is synchronized by the CLK signal. This synchronization results in minor timing differences between the UART and industry standard 16550A device, which means that the core is not clock for clock identical to the original device.

After hardware reset, UART will be in M16C450 mode; its FIFOs can then be enabled and UART can enter M16550A mode. UART has further additional functions beyond the M16550A mode. Each of the extended functions can be selected individually under software control.

UART provides more powerful enhancements than the industry-standard 16550:

Hardware flow control
This feature is very useful when the ISR latency is hard to predict and control in the embedded applications. The MCU is relieved of having to fetch the received data within a fixed amount of time.

Note that in order to enable the enhancements, the enhanced mode bit, EFR[4], must be set. If EFR[4] is not set, IER[7:4], FCR[5:4], cannot be written and MCR[7] cannot be read. The enhanced mode bit ensures that UART is backward compatible with the software that has been written for 16C450 and 16550A devices.

5.4.2 Features

- Provides four channels
- DMA, polling or interrupt operation
- Supports word lengths from five to eight bits, with an optional parity bit and one or two stop bits
- Four UART ports for hardware automatic flow control (UART0, UART1, UART2, UART3)
- Supports baud rates from 110bps up to 961,200bps
- Baud rate auto detection function

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5.4.3 Block Diagram

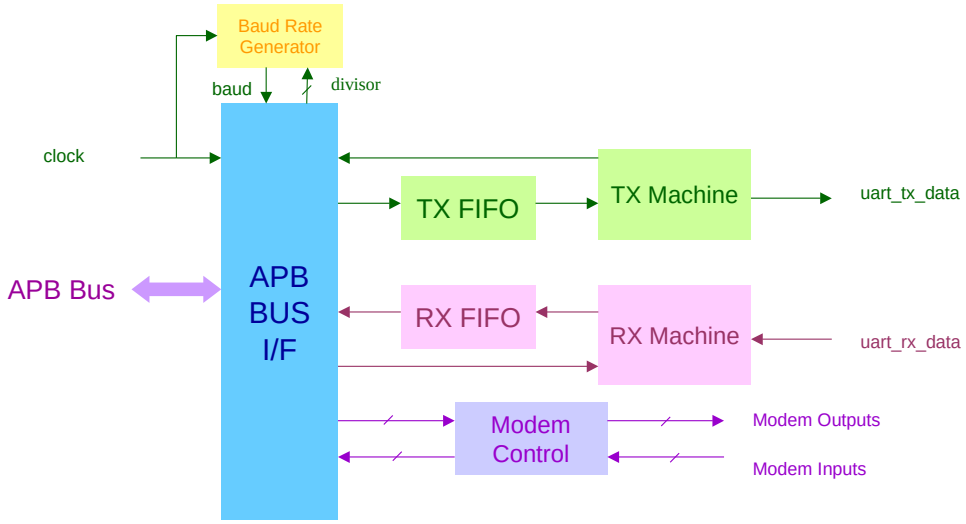

Figure 5-9. Block diagram of UART

5.4.4 Register Definition

UART number	Base address	Feature
UART0	0x11002000	Supports DMA, HW flow control
UART1	0x11003000	Supports DMA, HW flow control
UART2	0x11004000	Supports DMA, HW flow control

There are three UART IPs in this SOC. The usage of the registers is the same except that the base address must be changed to respective one. Note that UART2 is connected to C2KSYS in the SOC, and do not connect to pin-mux.

See chapter 3.4 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

5.4.5 Programming Guide

5.4.5.1 Auto Baud Rate Detection

UART detects the baud rate used automatically. Follow the steps below:

1. Set up register autobaud_en to start detecting the data.
2. Send data of ASCII code "AT" or "at" to UART from the connected host, e.g. the PC.
3. Check if the "AT" or "at" is received. If received, the setting is now already set for further transmission.

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5.4.5.2 Transmission

Follow the steps below for UART transmission:

1. Use the autobaud function to set up the baud rate or set up the parameters by yourself. The settings needed can be found in register DLL, DLM ,HIGH SPEED.
2. After setting up the baud rate, start the transmission by filling the TX FIFO and receiving data from RX FIFO.
3. Virtual FIFO can also be used for the transmission. To use the virtual FIFO, you need APDMA settings (refer to details in the APDMA section).

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5.5 USB

5.5.1 Introduction

The super speed universal serial bus (SSUSB) IP provides USB2.0 dual role capability. It contains a pair of U2 PHY and U2 MAC for high-, full- and low-speed connection. The USB2.0 dual role capability allows the port to support On-The-Go (OTG) host and peripheral. When acting as USB2.0 host, this port is controlled by the host controller (xHC) which is used to manage all devices connected through its root hub ports. When acting as peripheral, the port is controlled by the Device (DEV) controller.

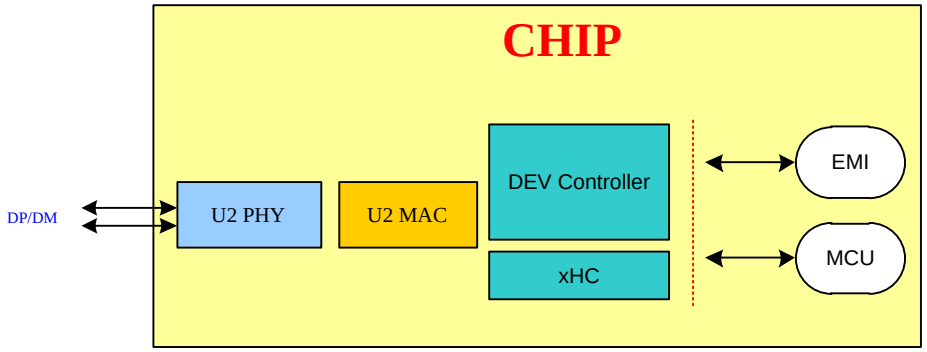

Figure 5-10. Block diagram of SSUSB IP

5.5.2 Features

- Configurable to be USB2.0 peripheral role
- Configurable to be USB2.0 host role
- Shared hardware on dual function
- Proprietary application layer device controller with linked list queue and scatter/gather DMA
- Extensible Host Controller Interface (xHCI) based host controller
- Embedded USB2 PHY with 16-bit/30MHz UTMI interface
- High-/Full-speed OTG host and peripheral compliant with OTG Supplement Version 2.0

5.5.3 Register Definition

The following table illustrates the register of SSUSB IP. See chapter 3.5 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

Base address	SSUSB MAC coda file
0x11270000	ssusb_xhci_exclude_port_csr_ssusb_host
0x11270440	ssusb_xhci_u2_port_csr_xhci_u2_port
0x11271000	ssusb_device
0x11271800	ssusb_epctl_csr

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Base address	SSUSB MAC coda file
0x11273400	ssusb_usb2_csr
0x11280700	ssusb_sifslv_ippc

Base Address	SSUSB PHY coda file
0x11290100	ssusb_sifslv_fmreg
0x11290300	ssusb_sifslv_chip
0x11290800	ssusb_sifslv_u2_phy_com_T28HPM

5.5.4 Host Function Architecture

5.5.4.1 Host Features

- Supports linkage with high-, full- and low-speed device
- Lower Power Management (LPM) on U2 port
- Hardware configurable up to 2 USB2 port with dedicated 480-Mbs bandwidth and shared DMA
- Control/Bulk/Interrupt/Isochronous PIPE type (currently no stream support)
- Compatible with connect to U2 hub
- Smart scheduling algorithm
- Up to 15 devices
- Up to 32 endpoints configuration

5.5.5 Architecture Overview

The architecture of USB2.0 host is illustrated in Figure 5-11. It includes one U2PHY and one MAC to handle protocol packets. All resources of endpoint and device are handled by xHCI controller. Firmware can dynamically allocate resource for different endpoints. The DMA channel of U2 port can be multiplexed in the system.

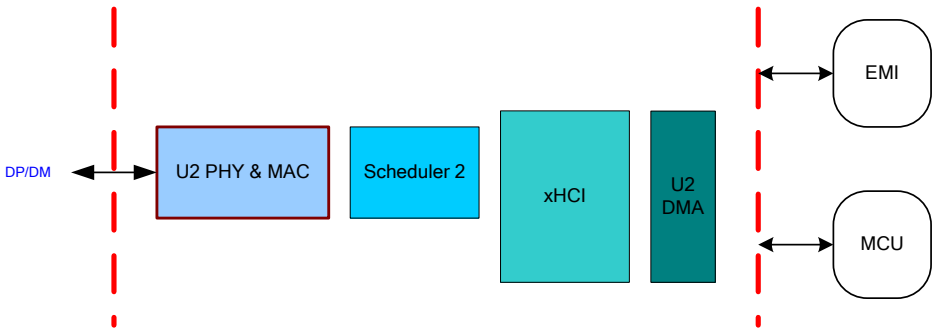

Figure 5-11. USB2.0 host architecture

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5.5.6 Device Function Architecture

5.5.6.1 Device Features

- Supports linkage with high- and full-speed host
- Embedded queue management function with scatter/gather DMA capability
- Lower Power Management (LPM) on U2 port
- L0/L1/L2/L3 state on U2 port
- 24KB of on-chip data RAM
- Hardware configurable up to 8 OUT endpoints and 8 IN endpoints
- Hardware configurable up to 4 packet slots for each endpoint separately
- Firmware configurable FIFO size allocation for each endpoint separately
- Firmware configurable transfer type to Bulk/Interrupt/Isochronous for each endpoint

5.5.6.2 Architecture Overview

The architecture of device is illustrated in Figure 5-12. The linked-list queue of device is basically inherited from MTK Unified USB IP with similar descriptor definition.

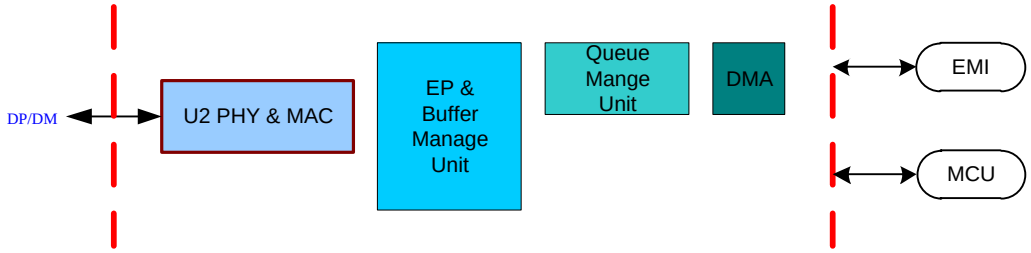

Figure 5-12. USB2.0 device architecture

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5.6 USB 2.0 High Speed Dual-Role Controller

5.6.1 Introduction

The USB controller is configured for supporting 5 endpoints to receive packets and 4 endpoints to send packets except for endpoint 0. These endpoints can be individually configured in the software to handle either Bulk transfers, Interrupt transfers or Isochronous transfers. There are 8 DMA channels and the embedded RAM size is configurable size up to 8K bytes. The embedded RAM can be dynamically configured to each endpoint. As the host for point-to-point communications, the controller maintains a frame counter and automatically schedules SOF, Isochronous, Interrupt and Bulk transfers.

5.6.2 Features

The following table lists the unified USB IP features.

Feature	Description
USB specifications	USB2.0 Host USB2.0 Dev USB2.0 OTG USB2.0 Hub USB1.1 Host USB1.1 Dev USB1.1 OTG
Enhanced feature	WiMAX Specific QMU Generic Host QMU Generic Dev QMU
Endpoint	15 Tx 15 Rx EP0
DMA channel	8
Embedded RAM	Up to 8KB
UTMI+ interface	UTMI+ 16b UTMI+ 8b
CPU slave interface	AHB asynchronous design AXI Asynchronous design RISC CPU asynchronous design
DMA master interface	AHB busy free asynchronous design AXI busy free asynchronous design RAMC busy free asynchronous design

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5.6.3 USB Controller Block Diagram

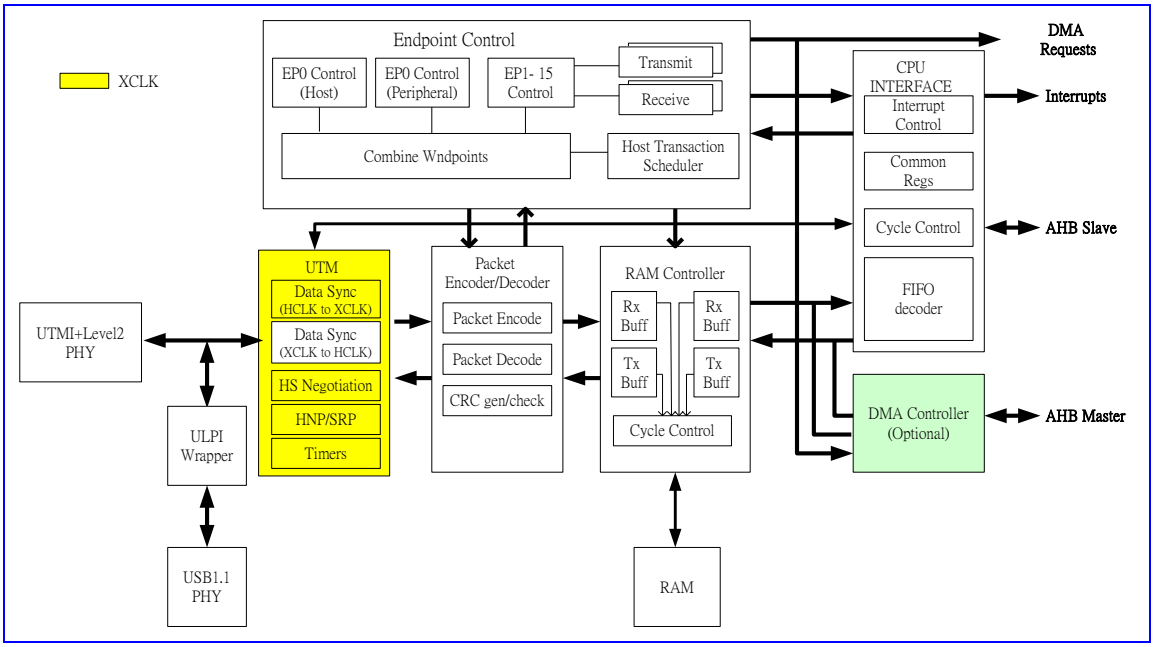

Figure 5-13. USB controller block diagram

5.6.4 Register Definition

Registers accessed using byte manipulation are marked in blue columns. Byte accessing registers can be accessed using word manipulation. Word accessing registers cannot be accessed using the byte manipulation.

Register address	Register name	Manipulation (Byte/Word)	Acronym
Common Registers			
USB + 0000h	Function address register	Byte	FADDR
USB + 0001h	Power management register	Byte	POWER
USB + 0002h	Tx interrupt status register	Byte	INTRTX
USB + 0004h	Rx interrupt status register	Byte	INTRRX
USB + 0006h	Tx interrupt enable register	Byte	INTRTXE
USB + 0008h	Rx interrupt enable register	Byte	INTRRXE
USB + 000Ah	Common USB interrupts register	Byte	INTRUSB
USB + 000Bh	Common USB interrupts enable register	Byte	INTRUSBE
USB + 000Ch	Frame number register	Byte	FRAME
USB + 000Eh	Endpoint selecting index register	Byte	INDEX
USB + 000Fh	Test mode enable register	Byte	TESTMODE
Indexed EndPoint CSR Region *n stands for endpoint number.* *For example, endpoint 1's n = 1. Valid n = 1 ~ MaxEndPoint.*			

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Register address	Register name	Manipulation (Byte/Word)	Acronym
MaxEndPoint is hardware configured and the maximum is 15.			
USB + 0010h ~ USB + 001Fh	It maps to CSR EP0 ~ EPx depending on the INDEX register. For example, if INDEX is n, address 0010h ~ 001Fh are mapped to 0x(100+10*n)h ~ 0x(100+10*n+F)h.	Byte	Indexed CSR
USB + 0020h	USB endpoint 0 FIFO register	Byte	FIFO0
USB + 0020h +(n)*4 h	USB endpoint n FIFO register	Byte	FIFOn
OTG, Dynamic FIFO, Version Registers			
USB + 0060h	OTG device control register	Byte	DEVCTL
USB + 0061h	Power up counter register	Byte	PWRUPCNT
USB + 0062h	Tx FIFO size register	Byte	TXFIFOSZ
USB + 0063h	Rx FIFO size register	Byte	RXFIFOSZ
USB + 0064h	Tx FIFO address register	Byte	TXFIFOADD
USB + 0066h	Rx FIFO address register	Byte	RXFIFOADD
USB + 006Ch	Hardware capability register	Byte	HWCAPS
USB + 006Eh	Hardware sub version register	Byte	HWSVERS
Hardware Configuration, Special Setting Registers			
USB + 0070h	USB bus performance register 1	Byte	BUSPERF1
USB + 0072h	USB bus performance register 2	Byte	BUSPERF2
USB + 0074h	USB bus performance register 3	Byte	BUSPERF3
USB + 0078h	Information about number of Tx and Rx register	Byte	EPINFO
USB + 0079h	Information about the width of RAM and the number of DMA channel register	Byte	RAMINFO
USB + 007Ah	Info. about delay to be applied register	Byte	LINKINFO
USB + 007Bh	Vbus pulsing charge register	Byte	VPLEN
USB + 007Ch	Time buffer available on HS transactions register	Byte	HS_EOF1
USB + 007Dh	Time buffer available on FS transactions register	Byte	FS_EOF1
USB + 007Eh	Time buffer available on LS transactions register	Byte	LS_EOF1
USB + 007Fh	Reset information register	Byte	RST_INFO
USB + 0080h	Rx data toggle set/status register	Word	RXTOG
USB + 0082h	Rx data toggle enable register	Word	RXTOGEN
USB + 0084h	Tx data toggle set/status register	Word	TXTOG
USB + 0086h	Tx data toggle enable register	Word	TXTOGEN
Level1 interrupt Control/Status registers			
USB + 00A0h	USB Level 1 interrupt status register	Byte	USB_L1INTS
USB + 00A4h	USB Level 1 interrupt unmask register	Byte	USB_L1INTM
USB + 00A8h	USB Level 1 interrupt polarity register	Byte	USB_L1INTP
USB + 00ACh	USB Level 1 interrupt control register	Byte	USB_L1INTC
Non-indexed EndPoint CSR Region *n stands for endpoint number.* *For example, endpoint 1's n = 1. Valid n = 1 ~ MaxEndPoint.* *MaxEndPoint is hardware configured and the maximum is 15.*			
USB + 0102h	EP0 control status register	Byte	CSR0

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Register address	Register name	Manipulation (Byte/Word)	Acronym
USB + 0108h	EP0 received bytes register	Byte	COUNT0
USB + 010Bh	NAK limit register	Byte	NAKLIMT0
USB + 010Fh	Core configuration register	Byte	CONFIGDATA
USB + 0100h +(n)*10h	TXMAP register	Byte	TXMAP(n)
USB + 0102h +(n)*10h	Tx CSR register	Byte	TXCSR(n)
USB + 0104h +(n)*10h	RXMAP register	Byte	RXMAP(n)
USB + 0106h +(n)*10h	Rx CSR register	Byte	RXCSR(n)
USB + 0108h +(n)*10h	Rx Count register	Byte	RXCOUNT(n)
USB + 010Ah +(n)*10h	TxType register	Byte	TXTYPE(n)
USB + 010Bh +(n)*10h	TxInterval register	Byte	TXINTERVAL(n)
USB + 010Ch +(n)*10h	RxType register	Byte	RXTYPE(n)
USB + 010Dh +(n)*10h	RxInterval register	Byte	RXINTERVAL(n)
USB + 010Fh +(n)*10h	Configured FIFO size register	Byte	FIFOSIZE(n)
DMA Channels Control Registers *M stands for DMA channel number.* *For example, DMA channel 1's M = 1. Valid M = 1 ~ MaxDMAChannel.* *MaxDMAChannel is hardware configured and the maximum is 8.*			
USB + 0200h	DMA interrupt status register (word access only)	Word	DMA_INTR
USB + 0210h	DMA limiter register (word access only)	Word	DMA_LIMITER
USB + 0220h	DMA configuration register (word access only)	Word	DMA_CONFIG
USB + 0204h +(M-1)*10h	DMA channel M control register (word access only)	Word	DMA_CNTL_M
USB + 0208h +(M-1)*10h	DMA channel M address register (word access only)	Word	DMA_ADDR_M
USB + 020Ch +(M-1)*10h	DMA channel M byte count register (word access only)	Word	DMA_COUNT_M
EndPoint RX Packet Count Register *n stands for endpoint number. For example, endpoint 1's n = 1. Valid n = 1 ~ MaxEndPoint.* *MaxEndPoint is hardware configured and the maximum is 15.*			
USB + 0300h +(n)*4h	EPn RxPktCount register	Word	EPnRXPKTCOUNT
Host/Hub Control Registers (Host mode only registers) *n stands for endpoint number. For example, endpoint 1's n = 1. Valid n = 1 ~ MaxEndPoint.* *MaxEndPoint is hardware configured and maximum is 15.*			
USB + 0480h +8*n h	Transmit endpoint n function address	Word	TXFUNCADDR

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Register address	Register name	Manipulation (Byte/Word)	Acronym
USB + 0482h +8*n h	Transmit endpoint n hub/port address	Word	TXHUBADDR
USB + 0484h +8*n h	Receive endpoint n function address	Word	RXFUNCADDR
USB + 0486h +8*n h	Receive endpoint n hub/port address	Word	RXHUBADDR
Debug Function Registers			
USB + 0600h	Debug flag selection control (byte 0, 1, 2, 3)	Word	DFC0R, DFC1R
USB + 0604h	Timing test mode	Word	TM1
USB + 0605h	No response error count	Word	TM1
USB + 0606h	Debug flag UTMI11 sub group selection	Word	DFC2R
USB + 0608h	Hardware version control register	Word	HWVER_DATE
USB + 0610h	Packet sequence record control/OpState record control	Word	PSR_CTRL/ OSR_CTRL
USB + 0611h ~ 0616h	Packet sequence record filter and trigger setting	Word	PSR_CTRL
USB + 0620h ~ 0637h	Debug register	Word	DBG_PRB
USB + 0640h ~ 065fh	Packet sequence PID data/OpState record Data	Word	PSR_DATA/ OSR_DATA
USB + 0684h	SRAM address register	Word	SRAMA
USB + 0688h	SRAM data register (word access only)	Word	SRAMD
USB + 0690h	RISC_SIZE register	Word	RISC_SIZE
USB + 0700h	Reserved register	Word	RESREG
USB + 0704h	HW TxPktRdy	Word	HWTPR
USB + 0708h	HW TxPktRdy enable register	Word	HWTPR_EN
USB + 070Ch	HW TxPktRdy error detection register	Word	HWTPR_ERR

5.6.4.1 Function Address Register

See chapter 3.6 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

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5.7 USBPHY Register File

The full features include USB2.0 PHYD and PHYA macro control registers. A frequency meter for USB2.0 PHYA monitor clock is also included. The registers can be accessed by I2C interface (FT). The default mode is accessing registers by AHB. After 0xfe (I2C access only) is configured to 8'h01, the register file will be in the I2C mode (accessing registers by I2C).

5.7.1 Features

- USB2.0
  - USB2.0 PHYD control registers for PHYD macro setting
  - USB2.0 PHYA control registers for PHYA characteristic tuning
  - Force USB2.0 UTMI interface for FT tests
  - Force USB2.0 PHY analog power-down in ATPG mode
  - Frequency meter for USB2.0 PHYA monitor clock
- USB1.1
  - USB1.1 PHYA control registers for PHYA characteristic tuning
  - Force USB1.1 PHY interface for FT tests
  - Force USB1.1 PHY analog power-down in ATPG mode
- Accessing PHY registers by AHB slave interface
- Accessing PHY registers by I2C interface

5.7.2 USBPHY Register File Block Diagram

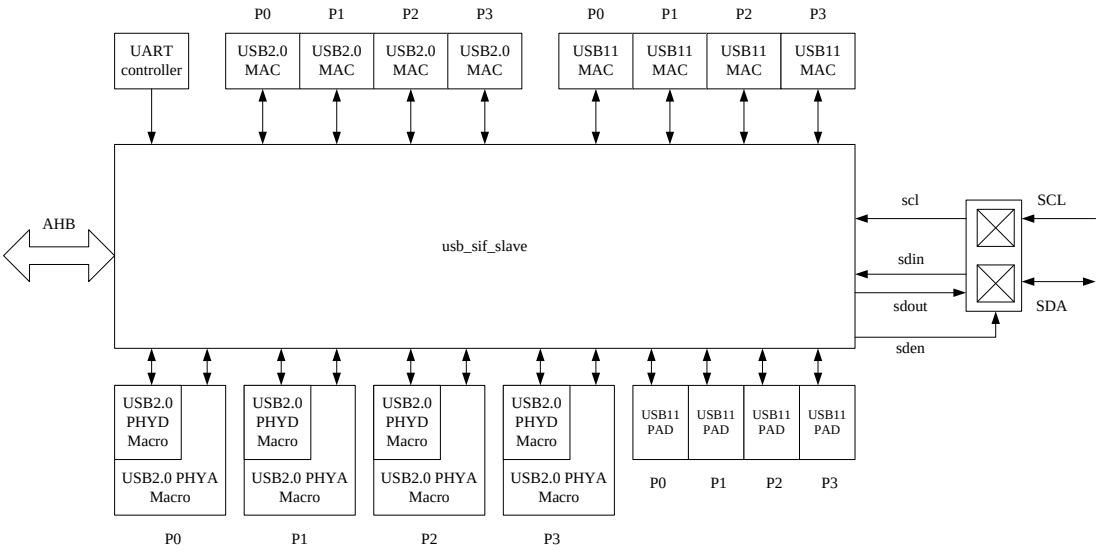

Figure 5-14. USBPHY RegFile block diagram

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5.7.3 Register Definition

- Page base
  - Every page register contains 0x00h ~ 0xefh (USB2.0+ USB1.1)
  - Frequency meter registers in one page (@ 0xff = 8'h0f)
  - 0xf0~0xff: Global register
  - 0xfe[0]: I2C mode, the default value is 0 (accessing register by AHB interface)
    - If switched to I2C mode, configuring 0xfe[0] to be 1'h1 is required.
    - I2C access only
  - 0xffh (RG_PAGE): I2C page register
    - I2C access only
- I2C
  - Accessing different pages by setting up RG_PAGE
  - Default device number: 7'h60
    (*If there are more than one hier, the device number of the second hier. will be 7'h61.)
  - Accessing different pages by setting up RG_PAGE (0xff)
  - Port 0 USB PHY register page: RG_PAGE value: 8'h00
  - Port 1 USB PHY register page: RG_PAGE value: 8'h01
  - Port 2 USB PHY register page: RG_PAGE value: 8'h02
  - Port 3 USB PHY register page: RG_PAGE value: 8'h03
  - Frequency meter register page: RG_PAGE value: 8'h0f
- AHB
  - Accessing different pages by different base addresses
  - Supports max. four ports. Base address: 800h, 900h, a00h, b00h
    - Port 0 register base address: 800h
    - Port 1 register base address: 900h
    - Port 2 register base address: a00h
    - Port 3 register base address: b00h
    - Frequency meter registers base address: f00h

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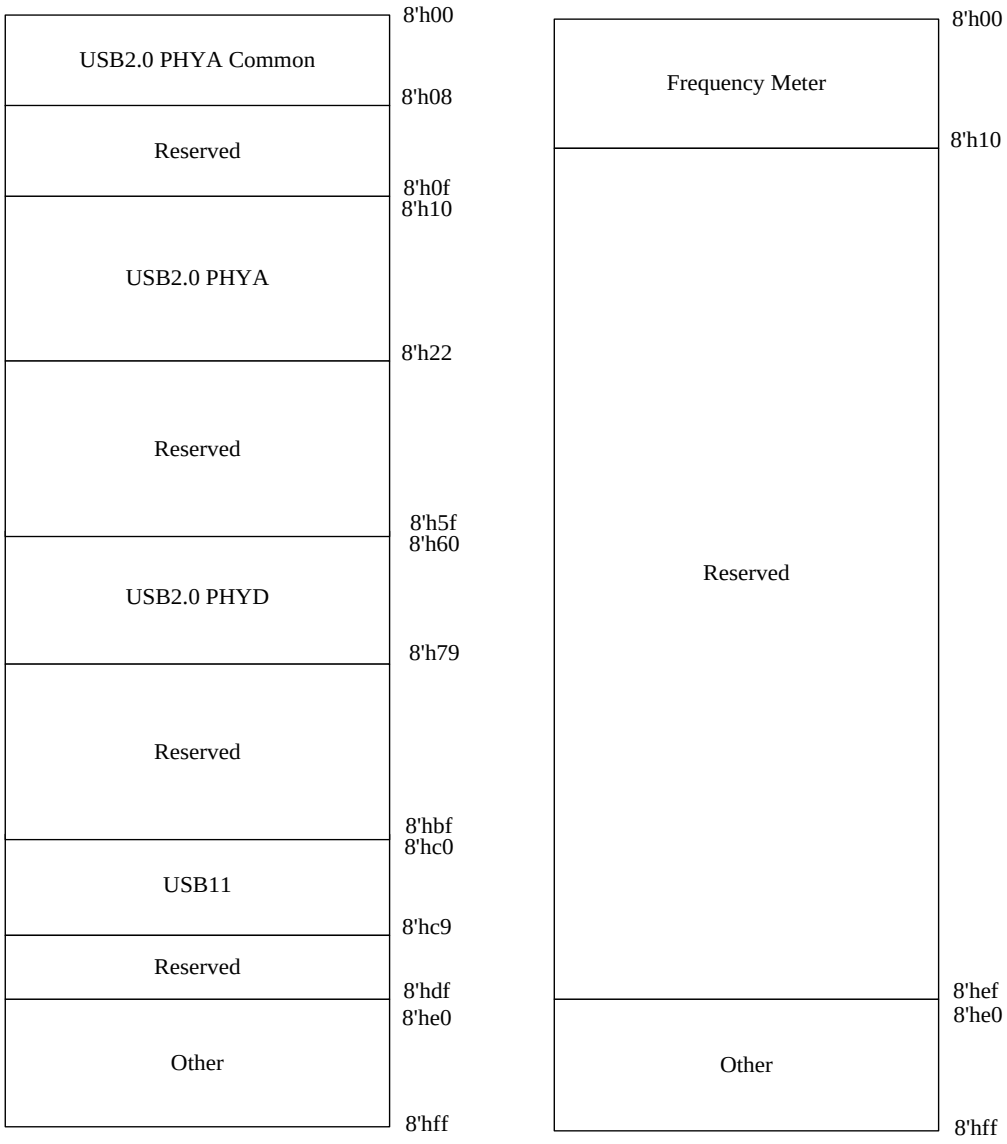

5.7.3.1 Function Address Register

See chapter 3.7 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

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5.8 SPI Interface Controller

5.8.1 Introduction

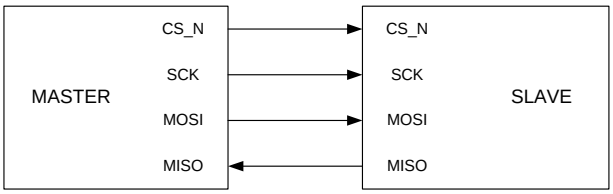

Figure 5-15. Pin connection between SPI master and SPI slave

The SPI interface is a bit-serial, four-pin transmission protocol. Figure 5-15 is an example of the connection between the SPI master and SPI slave. The SPI interface controller is a master responsible of the data transmission with the slave.

5.8.2 Pin Description

Table 5-2. SPI controller interface

Signal name	Type	Description
CS_N	O	Low active chip selection signal
SCK	O	The (bit) serial clock
MOSI	O	Data signal from master output to slave input
MISO	I	Data signal from slave output to master input

5.8.3 Transmission Formats

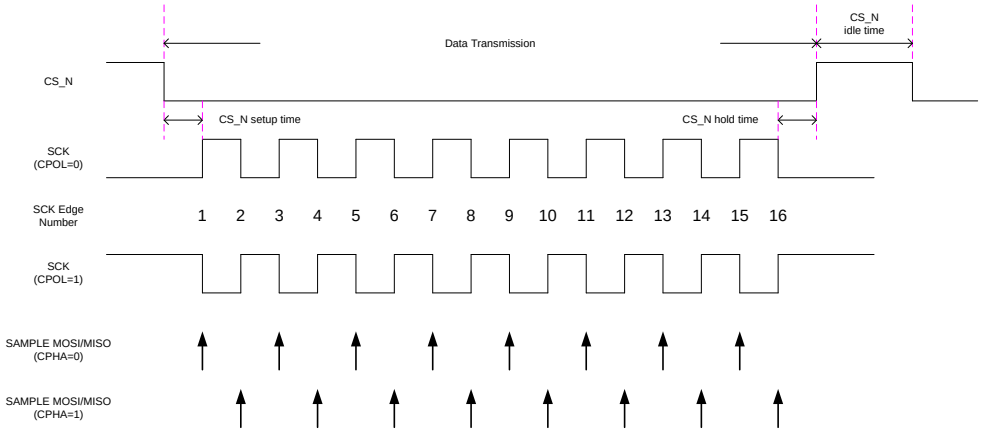

Figure 5-16. SPI transmission formats

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Figure 5-16 shows the waveform during the SPI transmission. The low active CS_N determines the start point and end point of one transaction. The CS_N setup time, hold time and idle time are also depicted.

CPOL defines the clock polarity in the transmission. Two types of polarity can be adopted, i.e. polarity 0 and polarity 1. Figure 5-16 is an example of both clock polarities (CPOL).

CPHA defines the legal timing to sample MOSI and MISO. Two different methods can be adopted.

5.8.4 Features

The features of the SPI controller (master) are:

- Configurable CS_N setup time, hold time and idle time
- Programmable SCK high time and low time
- Configurable transmitting and receiving bit order
- Two configurable modes for the source of the data to be transmitted. 1) In TX DMA mode, the SPI controller automatically fetches the transmitted data (to be put on the MOSI line) from memory; 2) In TX FIFO mode, the data to be transmitted on the MOSI line are written to FIFO before the start of the transaction.
- Two configurable modes for destination of the data to be received. 1) In RX DMA mode, the SPI controller automatically stores the received data (from MISO line) to memory; 2) In RX FIFO mode, the received data keep being in RX FIFO of the SPI controller. The processor must read back the data by itself.
- Adjustable endian order from/to memory system
- Programmable byte length for transmission
- Unlimited length for transmission. This is achieved by the operation of PAUSE mode. In PAUSE mode, the CS_N signal will keep being active (low) after the transmission. At this time, the SPI controller is in PAUSE_IDLE state, ready to receive the resume command. The state transition is shown in Figure 5-17.
- Configurable option to control CS_N de-assert between byte transfers. The controller supports a special transmission format called CS_N de-assert mode. Figure 5-18 illustrates the waveform in this transmission format.

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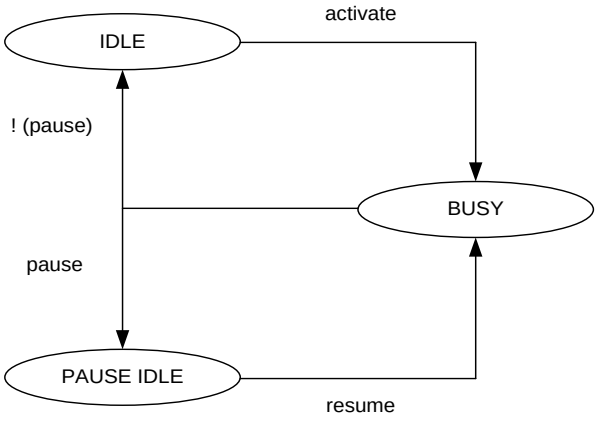

Figure 5-17. Operation flow with or without PAUSE mode

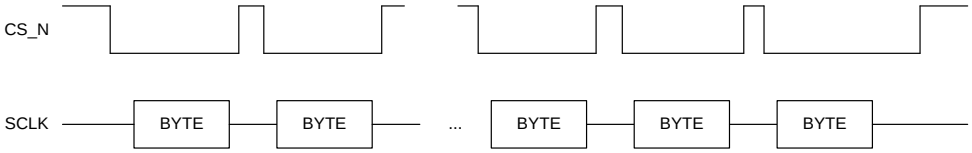

Figure 5-18. CS_N de-assert mode

5.8.5 Block Diagram

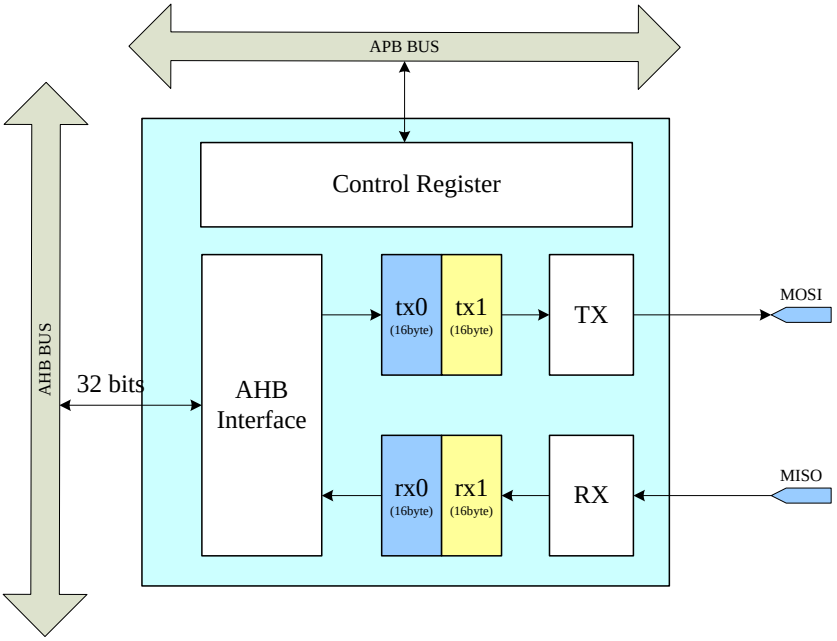

Figure-5-19. Block diagram of SPI

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5.8.6 Register Definition

See chapter 3.8 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

5.8.7 Programming Guide

Follow the steps below to perform SPI transmission:

1. Prepare the data in the memory with its start address to be the "source address".
2. Set up the timing and protocol for the SPI transmission (see Figure 5-16 for detailed setup parameters).
3. Fill the "destination address", which is the start address that you would like to place the received data, and "source address", which is the start address to place the data to be transmitted, into register SPI_RX_DST and SPI_TX_SRC, respectively.
4. Write 1 to CMD_ACT to start the transfer
5. Get the data received from the buffer prepared starting from "destination address".

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5.9 Memory Stick and SD card Controller

5.9.1 MSDC0

5.9.1.1 Introduction

This MSDC (memory stick and SD card controller) fully supports

- SD memory card specification version 3.0
- SDIO card specification version 3.0
- MMC/eMMC5.0

5.9.1.2 Features

Unified MSDC0 IP features:

- Interface with MCU by AHB bus
- 32-bit access on AHB bus
- 32-bit access for control registers
- 8-bit/16-bit/32-bit access for FIFO in PIO mode
- Built-in 128 bytes FIFO buffers for transmission and reception
- Built-in CRC circuit
- Supports Basic DMA mode, Basic Descriptor mode, and Enhanced Descriptor mode for SD/MMC
- Interrupt capabilities
- Does not support SPI mode for SD/MMC memory card
- Does not support suspend/resume for SD/MMC memory card
- Supports SD3.0 SDR104, data rate up to 208*4Mbps
- Supports SD3.0 DDR50, data rate up to 50x4*2Mbps(4-bit with clock dual edge)
- Supports eMMC HS400, data rate up to 200*8*2Mbps(8-bit with clock dual edge)
- Supports eMMC boot-up mode
- 256 programmable serial clock rates on MS/SD/MMC bus from 100kHz to 208MHz
- Card detection capabilities

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5.9.1.3 Block Diagram

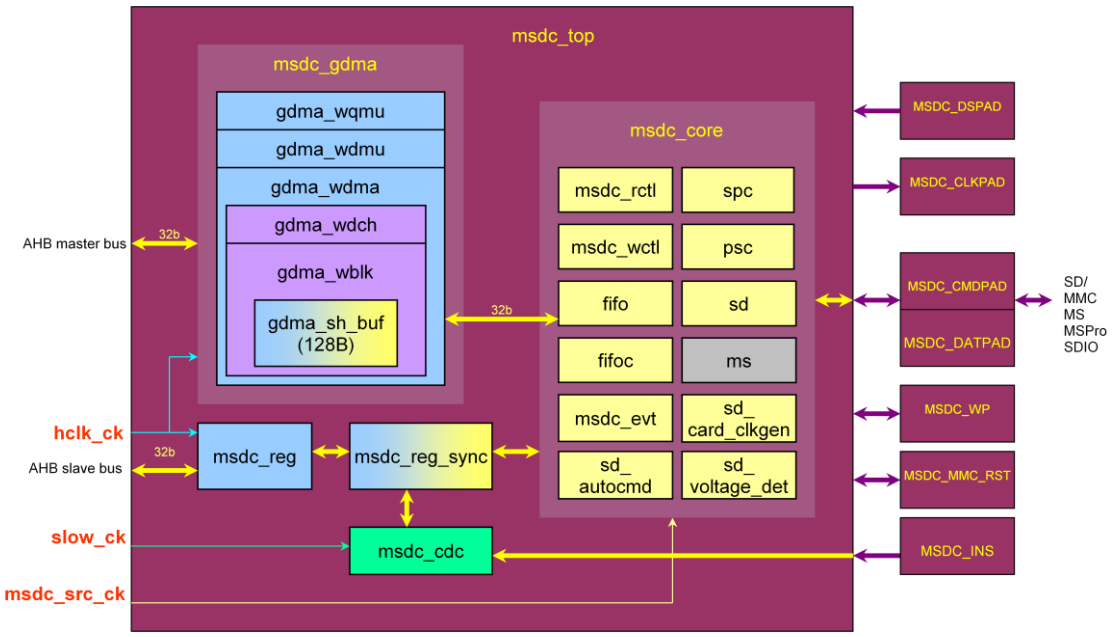

Figure 5-20. MSDC0 controller block diagram

5.9.1.4 Register Definition

See chapter 3.9 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

5.9.2 MSDC1

5.9.2.1 Introduction

This MSDC (memory stick and SD card controller) fully supports

- SD memory card specification version 3.0
- SDIO card specification version 3.0
- MMC/eMMC4.5

5.9.2.2 Features

Unified MSDC1 IP features:

- Interface with MCU by AHB bus
- 32-bit access on AHB bus
- 32-bit access for control registers
- 8-bit/16-bit/32-bit access for FIFO in PIO mode
- Built-in 128 bytes FIFO buffers for transmission and reception
- Built-in CRC circuit
- Supports Basic DMA mode, Basic Descriptor mode, and Enhanced Descriptor mode for SD/MMC

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- Interrupt capabilities
- Does not support SPI mode for SD/MMC memory card
- Does not support suspend/resume for SD/MMC memory card
- Supports SD3.0 SDR104, data rate up to 208*4Mbps
- Supports SD3.0 DDR50, data rate up to 50*4*2Mbps(4-bit with clock dual edge)
- Supports eMMC HS200, data rate up to 200*8Mbps(4-bit with clock dual edge)
- Supports SD boot-up mode
- 256 programmable serial clock rates on MS/SD/MMC bus from 100kHz to 208MHz
- Card detection capabilities

5.9.2.3 Block Diagram

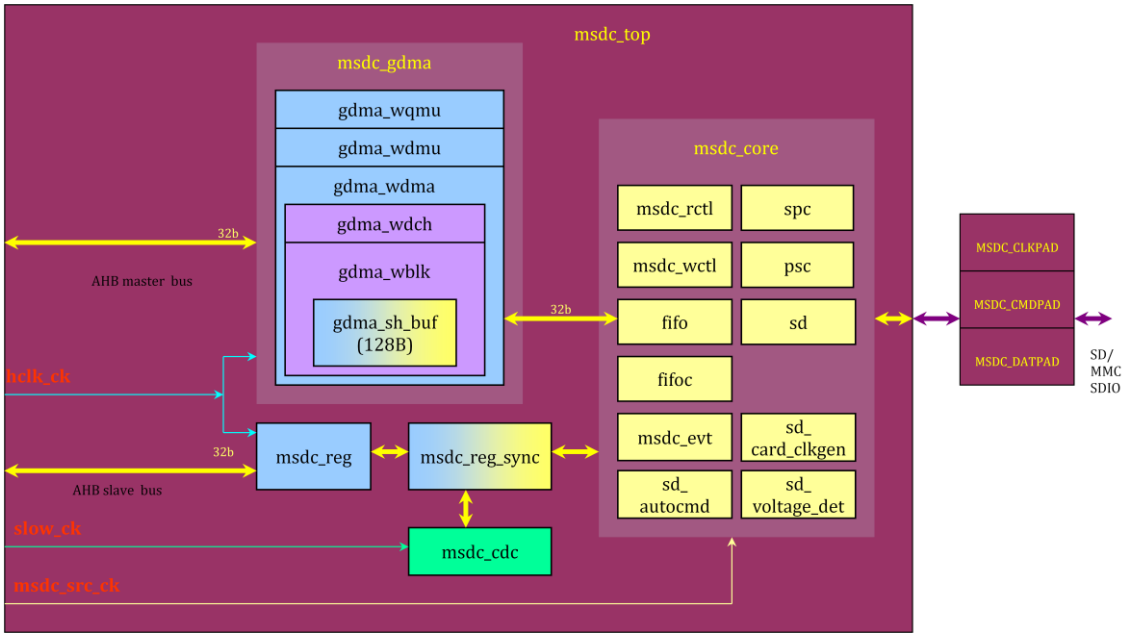

Figure 5-21. MSDC1 controller block diagram

5.9.2.4 Register Definition

See chapter 3.9 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

5.9.3 MSDC2

5.9.3.1 Introduction

This MSDC (memory stick and SD card controller) fully supports

- SD memory card specification version 3.0
- SDIO card specification version 3.0

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5.9.3.2 Features

Unified MSDC2 IP features:

- Interface with MCU by AHB bus
- 32-bit access on AHB bus
- 32-bit access for control registers
- 8-bit/16-bit/32-bit access for FIFO in PIO mode
- Built-in 128 bytes FIFO buffers for transmission and reception
- Built-in CRC circuit
- Supports Basic DMA mode, Basic Descriptor mode, and Enhanced Descriptor mode for SD/MMC
- Interrupt capabilities
- Does not support SPI mode for SD/MMC memory card
- Does not support suspend/resume for SD/MMC memory card
- Supports SD3.0 SDR104, data rate up to 208*4Mbps
- Supports SD3.0 DDR50, data rate up to 50*4*2Mbps(4-bit with clock dual edge)
- 256 programmable serial clock rates on MS/SD/MMC bus from 100kHz to 208MHz
- Card detection capabilities

5.9.3.3 Block Diagram

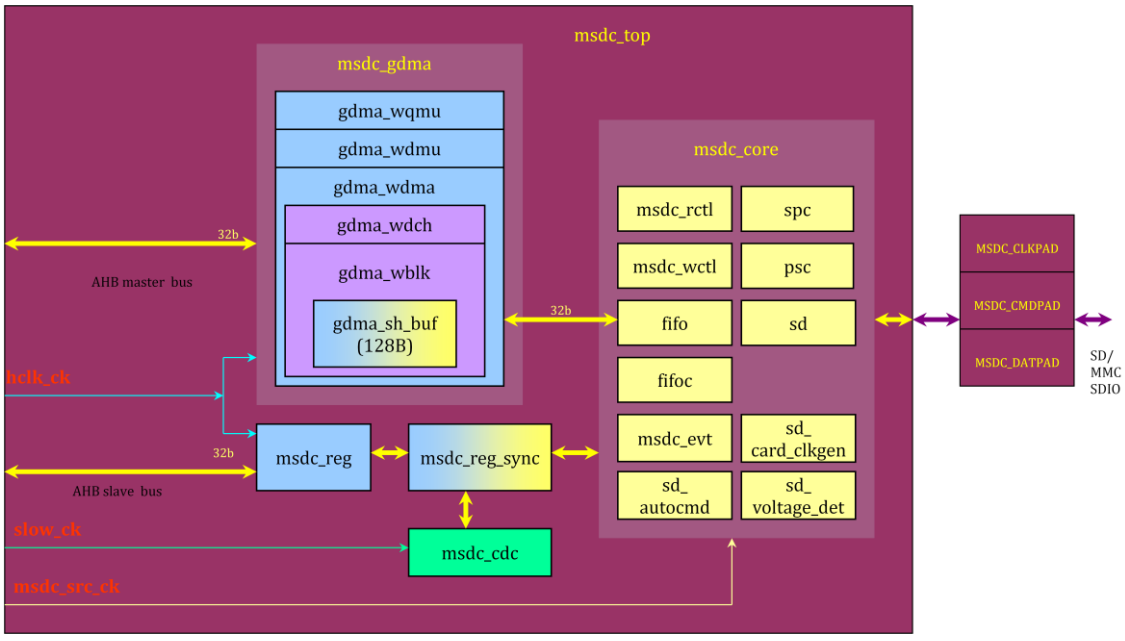

Figure 5-22. MSDC2 controller block diagram

5.9.3.4 Register Definition

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5.9.4 MSDC3

5.9.4.1 Introduction

This MSDC (memory stick and SD card controller) fully supports

- SD memory card specification version 3.0
- SDIO card specification version 3.0

5.9.4.2 Features

Unified MSDC3 IP features:

- Interface with MCU by AHB bus
- 32-bit access on AHB bus
- 32-bit access for control registers
- 8-bit/16-bit/32-bit access for FIFO in PIO mode
- Built-in 128 bytes FIFO buffers for transmit and receive
- Built-in CRC circuit
- Supports Basic DMA mode, Basic Descriptor mode, and Enhanced Descriptor mode for SD/MMC
- Interrupt capabilities
- Does not support SPI mode for SD/MMC memory card
- Does not support suspend/resume for SD/MMC memory card
- Supports SD3.0 SDR104, data rate up to 208*4Mbps
- Supports SD3.0 DDR50, data rate up to 50*4*2Mbps(4-bit with clock dual edge)
- 256 programmable serial clock rates on MS/SD/MMC bus from 100kHz to 208MHz
- Card detection capabilities

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5.9.4.3 Block Diagram

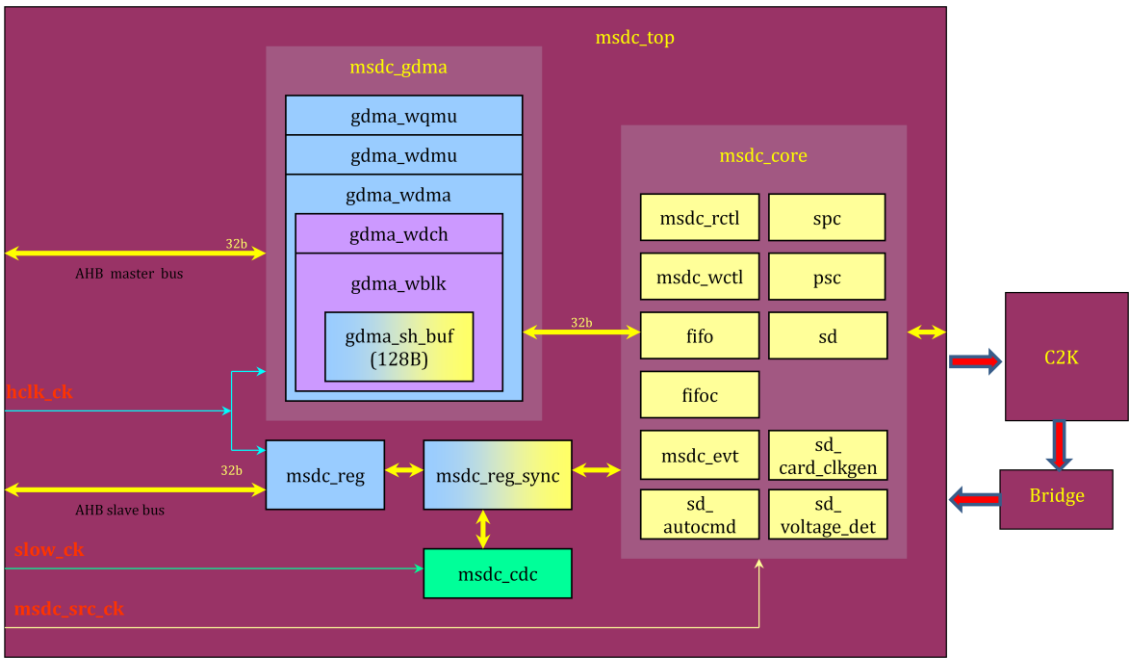

Figure 5-23. MSDC3 controller block diagram

5.9.4.4 Register Definition

See chapter 3.9 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

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5.10 AUXADC

5.10.1 Introduction

The auxiliary ADC unit is used to identify the plugged peripheral and perform temperature measurement. There are 16 input channels allowing diverse applications, such as temperature measurement and light sensor.

Each channel only operates in the immediate mode. The time-trigger mode is removed now. In the immediate mode, the A/D converter samples the value once only when the flag in the AUXADC_CON1 register is set. For example, if the flag IMM0 in AUXADC_CON1 is set, the A/D converter will sample the data for channel 0. The IMM flags have to be cleared and set again to initialize another sampling. The value sampled for channel 0 is stored in register AUXADC_DAT0, and the value for channel 1 is stored in register AUXADC_DAT1 and so on. If the AUTOSET(x) flag in the register AUXADC_CON0 is set, the auto-sampling function will be enabled in channel(x). The A/D converter samples the data for the channel(x) in which the corresponding data register is read. For example, in the case the AUTOSET0 flag is set. When the data register AUXADC_DAT0 is read, the A/D converter will sample the next value for channel 0 immediately.

If multiple channels are selected at the same time, the task will be performed sequentially on every selected channel from high to low channel. For example, if AUXADC_CON1 is set to 0x7f, i.e. all 7 channels are selected, the state machine in the unit will start sampling from channel 6 to channel 0 and saves the values of each input channel in respective registers. The same process also applies to the timer-triggered mode.

The PUWAIT_EN bit in register AUXADC_CON3 is used to power up the analog port in advance, ensuring that the power is ramped up to the stable state before A/D converter starts the conversion. The analog part is automatically powered down after the conversion is completed.

Besides, there are several embedded temperature sensors. The module accepts signals from module of thermal controller to measure the temperature of the embedded sensors. The measurement result is able to be read in the command registers in the module of thermal controller.

5.10.2 Features

Table 5-3 lists the features in the AUXADC module.

Table 5-3. AUXADC features

Item	Main function	Description
1	Immediate analog-digital conversion	In immediate mode, it supports auto-set option. In time-trigger mode, it supports auto-clear option.
2	Background detection and interrupt	The related command registers: AUXADC_DET_VOLT, AUXADC_PERIOD, AUXADC_DEBT, AUXADC_SEL
3	Temperature measurement	

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Table 5-4. AUXADC channel description

AUXADC channel ID	Description
Channel 0	External use (AUXIN 0)
Channel 1	External use (AUXIN 1)
Channel 2	Internal use
Channel 3	Internal use
Channel 4	Internal use
Channel 5	Internal use
Channel 6	Internal use
Channel 7	Internal use
Channel 8	Internal use
Channel 9	Internal use
Channel 10	Internal use
Channel 11	Internal use
Channel 12	External use (AUXIN 2)
Channel 13	External use (AUXIN 3)
Channel 14	External use (AUXIN 4)
Channel 15	N/A

5.10.3 Block Diagram

SW controls the AUXADC through the APB bus. Once the hardware receives the command, it will trigger AUXADC channel sampling automatically. SW polls the status register or waits for interrupts from the CPU.

5.10.4 Theory of Operation

5.10.4.1 SAR ADC

Successive-approximation-register (SAR) ADC provides low power consumption, cost-effective and medium resolution. The AUXADC is SAR ADC architecture.

Here is an 8-bit conversion example. V_{REF} is the reference voltage of AUXADC.

The AUXADC implements a binary search algorithm. An initial register V_{DA} value compared to the input voltage V_{IN} is the mid-value between (2^8-1) and 0. The value represents $V_{REF}/2$. If V_{IN} is bigger than V_{DA}, the output of comparison will be 1, and the MSB-bit will be 1. On the contrary, the MSB bit will be 0. Subsequently, bit 7 will be set to 1, and another comparison is done. Bit 6 to bit 0 will be executed as the previous action. Then, the 8-bit digital value will be available.

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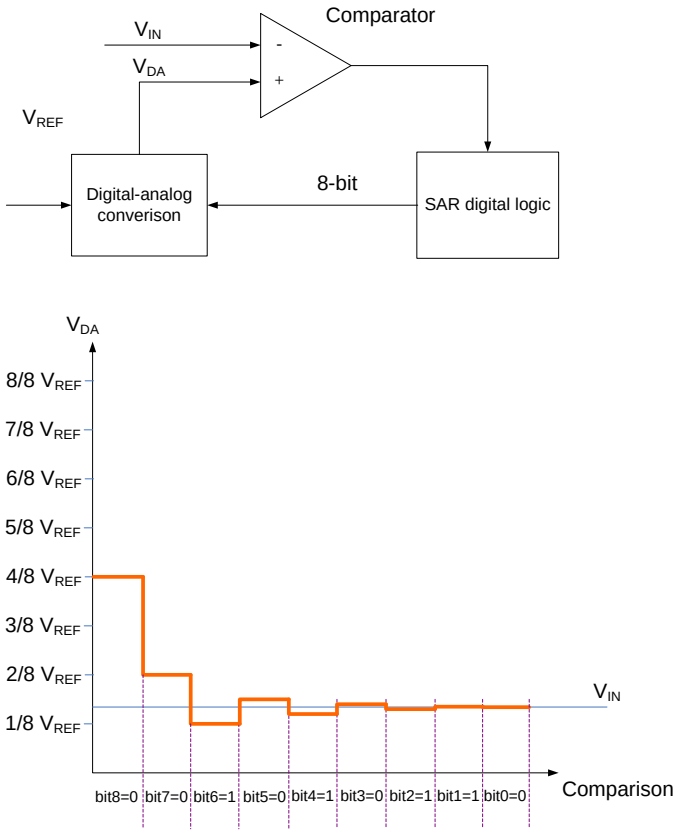

Figure 5-24. SAR ADC architecture and conversion

5.10.4.2 Design Partition

Table 5-5 shows the design partition.

Table 5-5. AUXADC design partition

Sub module name (hier1)	Description
AUXADC	Top module
AUXADC_REG	APB command registers
AUXADC_SIF	ADC serial interface with the module SADC_SIF
AUXADC_DEBUG	Debugging signal selection
AUXADC_MONITOR	Background detection and generate interrupt
AUXADC_CORE	AUXADC state machine and handle sampling sequence
SADC_SIF	Generate signals to analog part and transfer ADC result to the module AUXADC

5.10.5 Register Definition

See chapter 3.10 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

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5.11 I2C/SCCB Controller

5.11.1 Introduction

I2C (Inter-IC)/SCCB (Serial Camera Control Bus) is a two-wire serial interface. The two signals are SCL and SDA. SCL is a clock signal that is driven by the master. SDA is a bi-directional data signal that can be driven by either the master or the slave. This generic controller supports the master role and conforms to the I2C specification.

5.11.2 Features

- I2C compliant master mode operation
- Adjustable clock speed for LS/FS mode operation
- Supports 7-bit/10-bit addressing
- Supports high-speed mode
- Supports slave clock extension
- START/STOP/REPEATED START condition
- Manual transfer mode
- Multi-write per transfer
- Multi-read per transfer
- Multi-transfer per transaction
- Combined format transfer with length change capability.
- Active drive/wired-and I/O configuration
- Repeated start multiple transfer

5.11.2.1 Manual Transfer Mode

The controller offers manual mode.

When the manual mode is selected, in addition to the slave address register, the controller has a built-in 8-byte deep FIFO which allows MCU to prepare up to eight bytes of data for a write transfer, or read up to eight bytes of data for a read transfer.

5.11.2.2 Transfer Format Support

This controller is designed to be as generic as possible in order to support a wide range of devices that may utilize different combinations of transfer formats. Here are the transfer format types supported through different software configurations:

Wording convention note
Transfer = Anything encapsulated within a Start and Stop or Repeated Start.
Transfer length = Number of bytes within the transfer
Transaction = This is the top unit. Everything combined equals 1 transaction.

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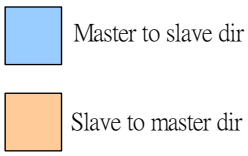
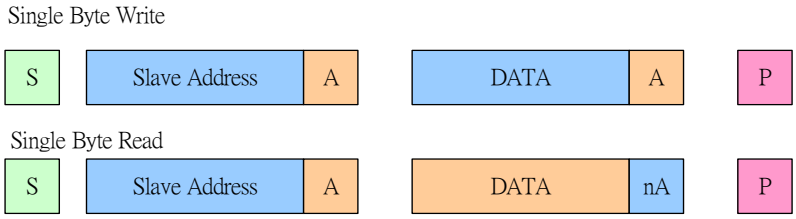
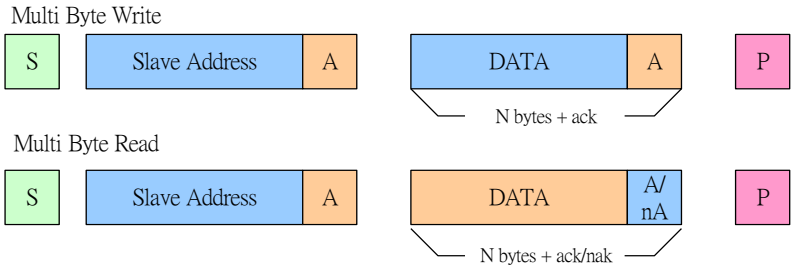
Transaction length = Number of transfers to be conducted.



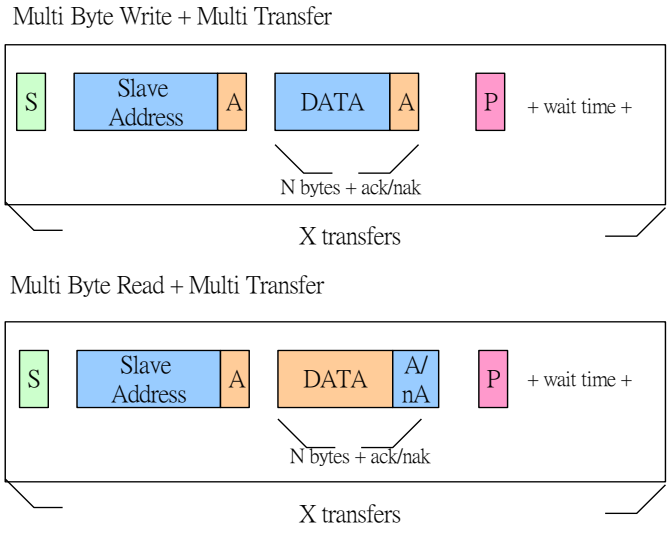
Single byte access



Multi byte access



Multi-byte transfer + multi-transfer (same direction)



Multi-byte transfer + multi-transfer w RS (same direction)

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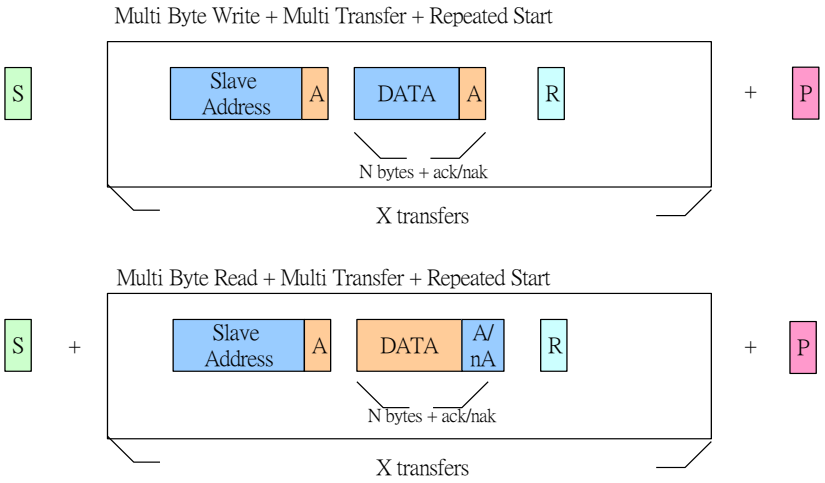
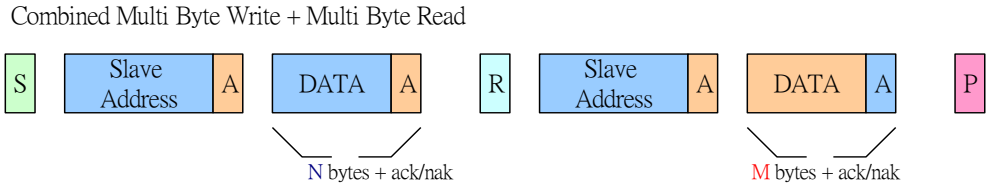
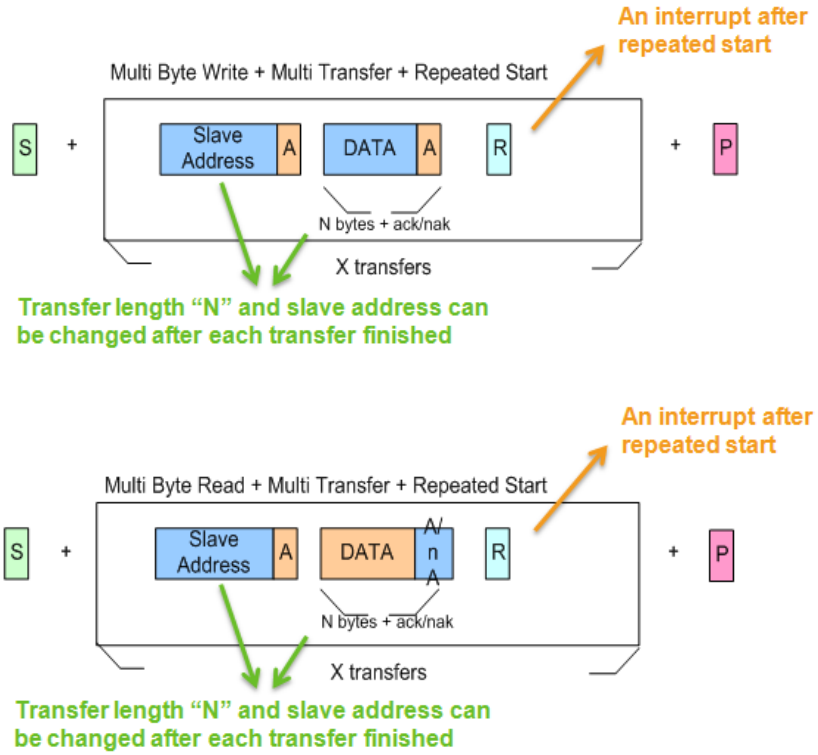


Combined write/read with Repeated Start (direction change)

Note: Only supports write and then read sequence. Read and then write is not supported.



Repeated start multiple transfer (write/read)



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5.11.3 Block Diagram

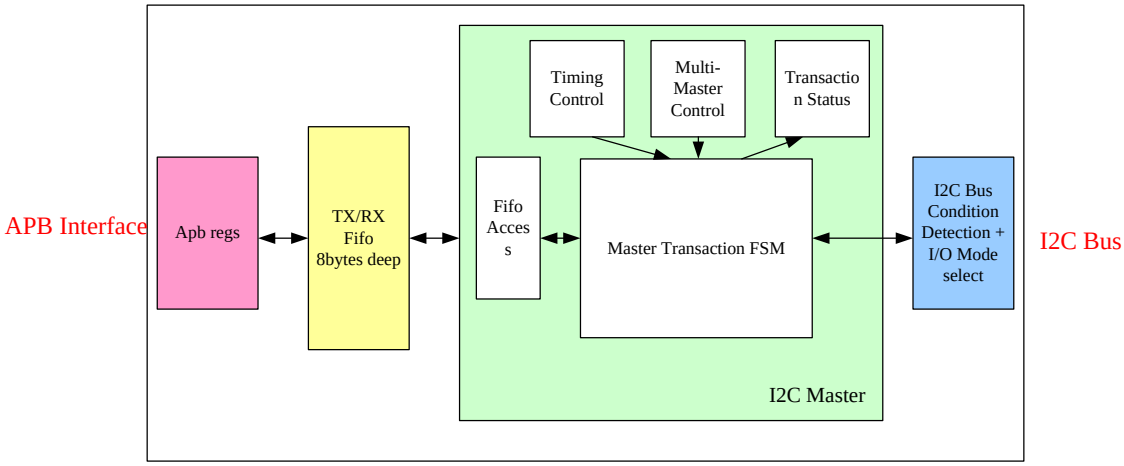

Figure 5-25. Block diagram of I2C

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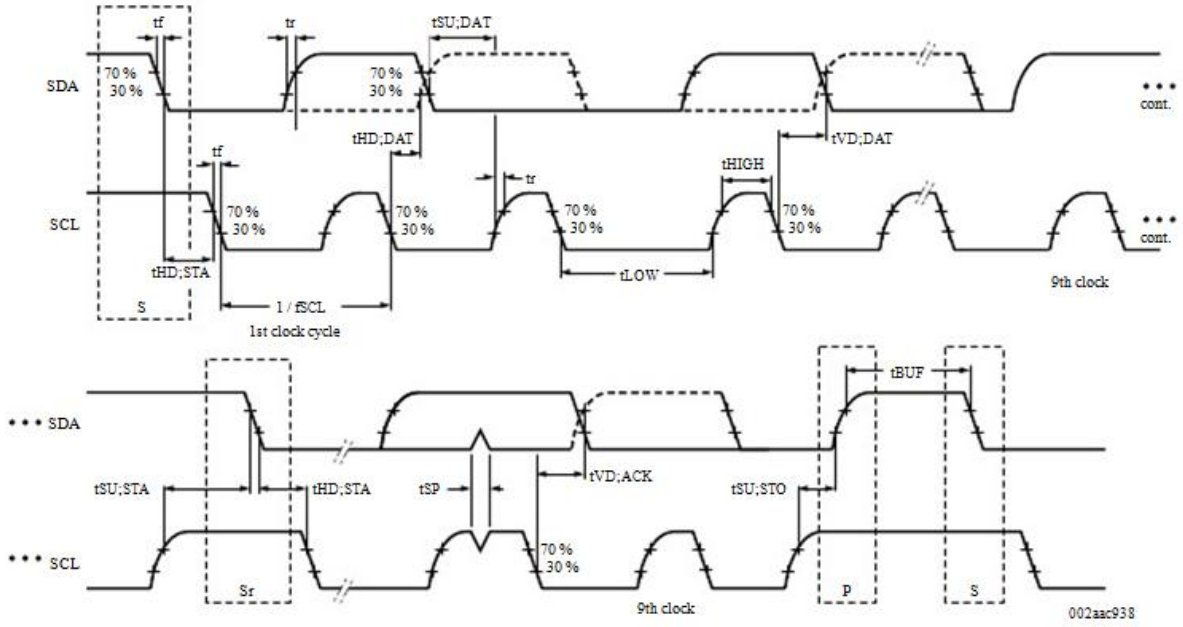
5.11.4 Timing Characteristic

Standard mode (100kHz) and fast mode (400kHz)



Symbol	Standard mode	Fast mode	Unit	Note
$t_{HD;STA}$	2.5	0.625	µs	Can be extended by 0x28, extension configuration register.
t_{LOW}	5	1.25	µs	
t_{HIGH}	5	1.25	µs	
$t_{SU;STA}$	2.5	0.625	µs	
$t_{HD;DAT}$	2.5	0.625	µs	
$t_{SU;DAT}$	2.5	0.625	µs	
$t_{SU;STO}$	2.5	0.625	µs	Can be extended by 0x28, extension configuration register.

5.11.5 Register Definition

I2C number	Base address	Feature
I2C0	0x11007000	Supports DMA
I2C1	0x11008000	Supports DMA
I2C2	0x11009000	Supports DMA
I2c3	0x1100F000	Supports DMA
I2c4	0x11011000	Supports DMA

There are five I2C IPs in this SOC. The usage of the registers is the same except that the base address must be changed to respective one.

See chapter 3.11 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

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5.12 Pulse-Width Modulation (PWM)

5.12.1 Introduction

Seven generic pulse-width modulators are implemented to generate pulse sequences with programmable frequency and duration for LCD backlight, charging or other purposes. Before enabling PWM, the pulse sequences must be prepared in the memory or registers. Then PWM will read the pulse sequences to generate random waveform to meet all kinds of applications (see Figure 5-26).

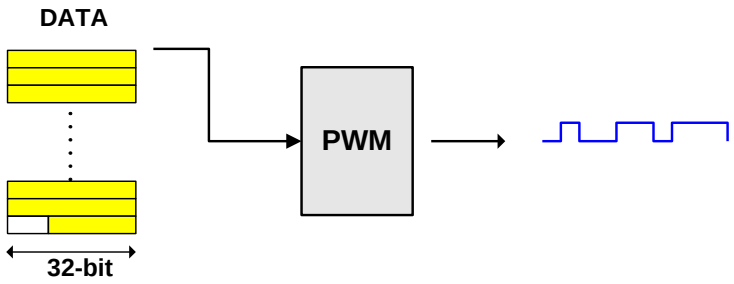
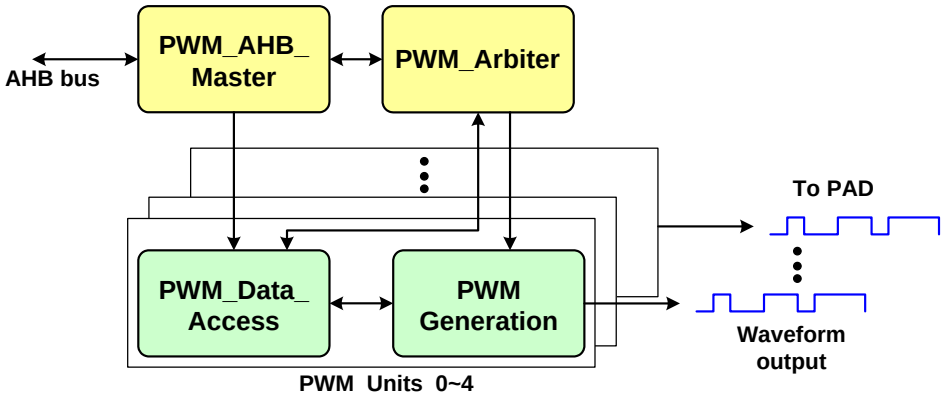


Figure 5-26. Generation procedure of PWM

5.12.2 Features

- Old mode, FIFO mode
- Periodical memory and random mode
- Sequential output mode and 3DLCM mode

5.12.3 Block Diagram



5.12.4 Register Definition

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5.12.5 Clock Source Selection

Mode	OLD_MODE	CLKSEL_OLD	CLKSEL	CLKSRC
Old mode	1	Don't care	0	bclk
Old mode	1	1	1	32kHz (used in old mode only)
Old mode	1	0	1	bclk/1625
FIFO mode	0	Don't care	0	bclk
FIFO mode	0	Don't care	1	bclk/1625

5.12.6 Output Frequency and Duty Cycle

Mode	Duty cycle	Output frequency
Old mode	PWM_THRESH/(PWM_DATA_WIDTH + 1)	SRCLK/[CLK_DIV*(PWM_DATA_WIDTH + 1)]
FIFO mode	Output freq. = (SRCLK*duty cycle)/4	

Note: bclk can be selected as 26MHz or 66MHz(bus clock) by PWM_CK_26M_SEL.

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5.13 General-Purpose Timer (GPT)

5.13.1 Introduction

The GPT includes five 32-bit timers and one 64-bit timer. Each timer has four operation modes, which are ONE-SHOT, REPEAT, KEEP-GO and FREERUN, and can operate on one of the two clock sources, RTC clock (32.768kHz) and system clock (13MHz).

5.13.2 Features

The four operation modes for GPT are ONE-SHOT, REPEAT, KEEP-GO and FREERUN. See Table 5-6 ffor the functions of each mode.

Table 5-6. Operation mode of GPT

Mode	Auto stop	Interrupt	Increases when EN=1 and ...	When COUNTn equals COMPAREn	Example: Compare is set to 2 **Bold means interrupt*
ONE-SHOT	Yes	Yes	Stops when COUNTn equals to COMPAREn	EN is reset to 0.	0,1,**2**,2,2,2,2,2,2,2,2,2,...
REPEAT	No	Yes		Count is reset to 0.	0,1,**2**,0,1,**2**,0,1,**2**,0,1,**2**...
KEEP-GO	No	Yes	Reset to 0 when overflow		0,1,**2**,3,4,5,6,7,8,9,10,...
FREERUN	No	No	Reset to 0 when overflow		0,1,2,3,4,5,6,7,8,9,10,...

Each timer can be programmed to select the clock source, RTC clock (32.76kHz) or system clock (13MHz). After the clock source is determined, the division ratio of the selected clock can be programmed. The division ratio can be fine-granulated as 1, 2, 3, 4 to 13 and coarse-granulated as 16, 32 and 64.

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5.13.3 Block Diagram

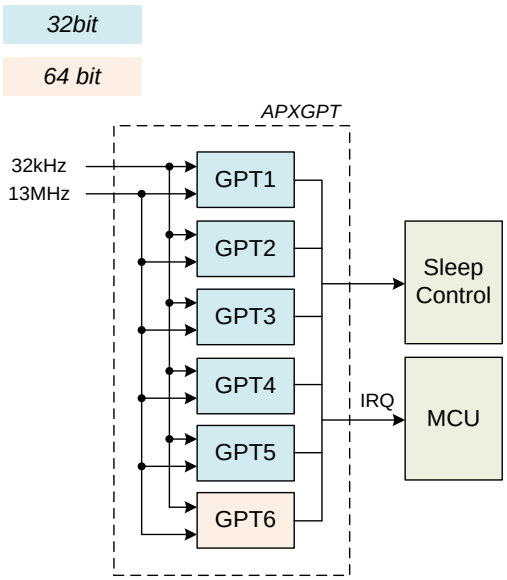

Figure 5-27. Block diagram of APXGPT

5.13.4 Register Definition

See chapter 3.13 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

5.13.5 Programming Guide

To program and use GPT, note that:

- The counter value can be read any time even when the clock source is RTC clock.
- The compare value can be programmed any time.

For the GPT6 64-bit timer, the read operation of the 64-bit timer value will be separated into two APB reads since an APB read is of 32-bit width. To perform the read of 64-bit timer value, the lower word should be read first then the higher word. The read operation of lower word freezes the "read value" of the higher word but does not freeze the timer counting. This ensures that the separated read operation acquires the correct timer value. If both two tasks, e.g. task A and task B, perform the read of 64-bit timer value, task A first reads the lower word of the value, and task B reads the lower word of the value. Either of the tasks reads the higher word of timer value, and the obtained value will be the time when task B reads the lower word of timer value. To guarantee task A reads the correct 64-bit timer value, some software procedures are required, e.g. the semaphore.

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5.14 Thermal Controller

5.14.1 Introduction

On mobile platform, thermal management is very fundamental. The thermal management controls the platform computing performance to achieve the requirement and maintain the Raven within the temperature constraints. Operation under over-high temperature for a long time will have a risk of damage for Raven reliability.

In MT6750, it embeds several temperature sensors in possible hot spots on the die. The thermal controller module executes a periodic measurement for each hot spot. The temperature readings are readable for software.

In order to minimize the software effort of temperature monitoring, the thermal controller generates interrupts to microprocessors which informs the abnormal condition.

5.14.2 Features

- Supports up to four thermal sensors
- Periodic temperature measurement
- Temperature monitoring
- Different types of low pass filters for thermal sensor reading

5.14.3 Block Diagram

Figure 5-28 is a basic sketch of the connection between thermal controller, AUXADC, and the thermal sensors (on-die PNP). In this example, there are two thermal sensors, one inside ABB and the other placed nearby CPUSYS.

You can specify some pre-defined parameters to thermal controller through APB bus by software. The pre-defined parameters include the information like the interval to periodic measure thermal sensors, the MUX address of thermal sensors, etc. After the temperature monitor enable command is specified, the thermal controller will be triggered and start to ask AUXADC to sample thermal sensor readings. The thermal controller sends the polling temperature requests and receives the measurement data to/from AUXADC through AHB bus. Since the thermal sensor is an analog design, the measurement results are transferred from thermal sensor to AUXADC by SADC_SIF. Refer to AUXADC documents for further information on the AUXADC mechanism.

The thermal controller is also designed with a thermal protection mechanism. Several thresholds can be pre-defined as shown in Figure 5-29. Once the measurement temperature exceeds certain threshold, the thermal controller will issue interrupt to inform the system, so that the system temperature can be monitored and thus help prevent the system from abnormal condition.

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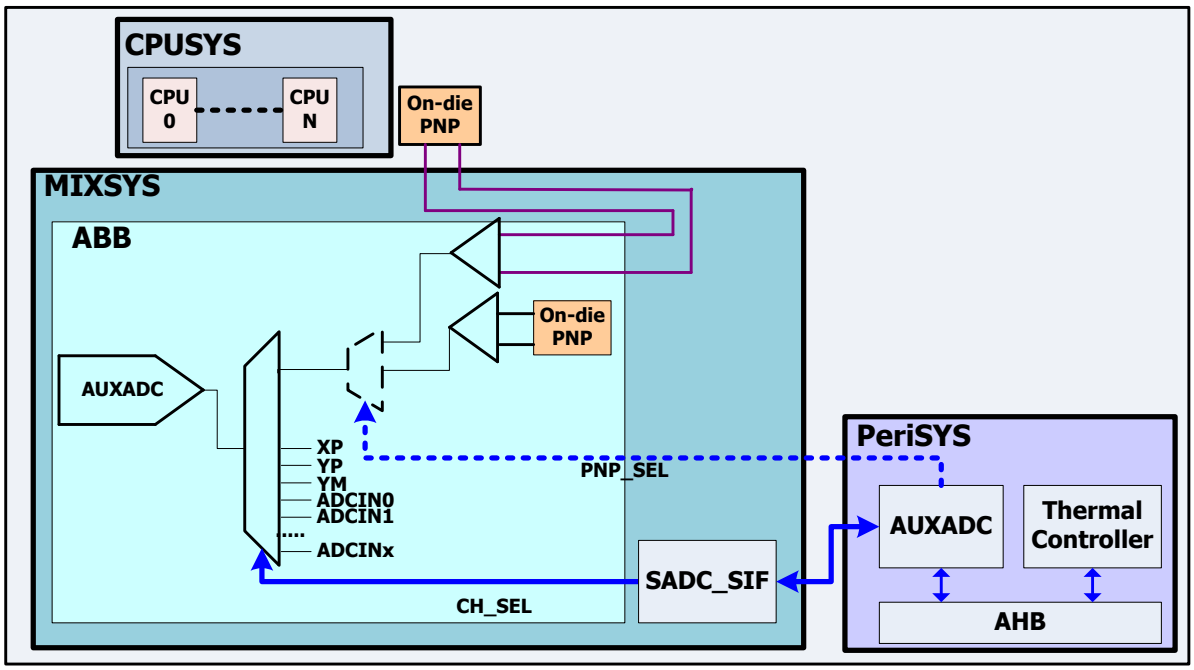

Figure 5-28. Block diagram of system temperature measurement

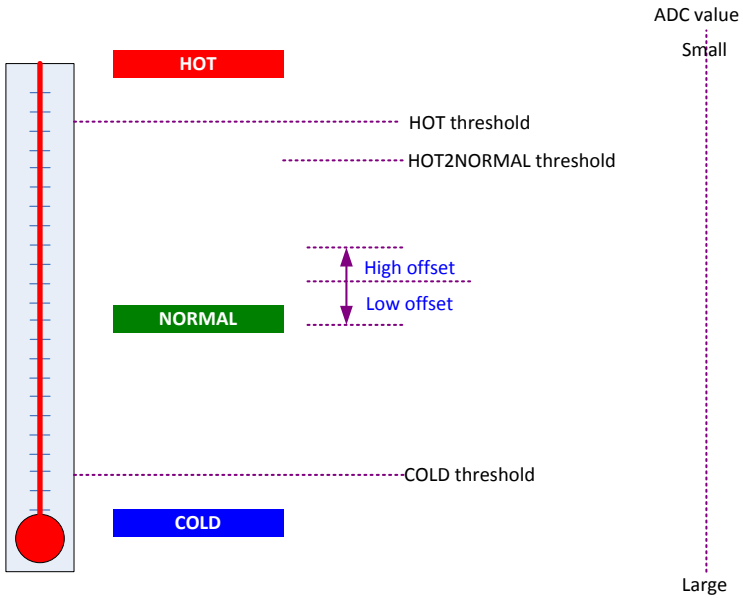

Figure 5-29. Block diagram of system temperature measurement

5.14.4 Register Definition

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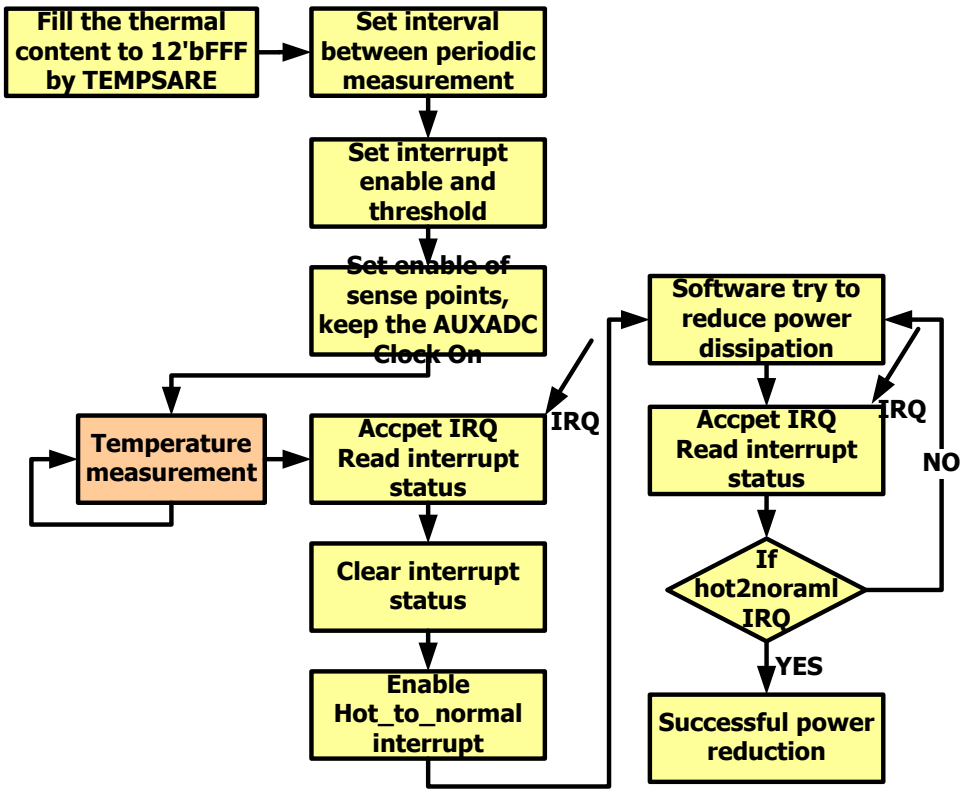
5.14.5 Programming Guide



:

Figure 5-30. Programming flow

1. Fill the thermal content to 12'bFFF by accessing TEMPSPARE.

```
vWriteREG(TEMPMONCTL1, 'h0);
vWriteREG(TEMPMONCTL2, 'h0);
vWriteREG(TEMPAHBPOLL, 'h0); // polling interval to check if temp sense is ready
vWriteREG(TEMPAHBTO, 'hFF); // Exceed this polling time, IRQ would be inserted
vWriteREG(TEMPSPARE0, 'h1FFF); // fill the TEMPSPARE0 register as 'h1FFF
vWriteREG(TEMPPNPMUXADDR, 32'hTS_CON1); // The adxadc mux address to select to Thermal channel, and please reference mixsys.doc
vWriteREG(TEMPADCENADDR, 32'TEMPSPARE1); // The adxadc enable address to trigger Thermal senser, please reference auxadc.doc
vWriteREG(TEMPADCVALIDADDR, 32'hTEMPSPARE1); // The adxadc status address to check if Thermal senser reading is valid, please reference auxadc.doc
vWriteREG(TEMPADCVOLTADDR, 32'hTEMPSPARE0); // The adxadc temperature address for the value read back from temp senser, please reference auxadc.doc
vWriteREG(TEMPRDCTRL, 'h0); // use TEMPSPARE0 as valid address
vWriteREG(TEMPADCVALIDMASK, 'h2c); // set adxadc valid polarity to 0
vWriteREG(TEMPMONCTL0, 'h0F); // enable all sense points include the debug one
Wait until the content of TEMPIMMD are filled by 'hFFF
```

2. Set up interval between periodic temperature measurements if the MODULE clock is 66MHz.

```
vWriteREG(TEMPMONCTL1, 'h3FF); // counting unit is 1024*15.15ns=15.5 us
vWriteREG(TEMPMONCTL2, 'h3FF); // sensing interval is 1024*15.5us=15.87 ms
vWriteREG(TEMPAHBPOLL, 'h0F); // polling interval to check if temp sense is ready
```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```
vWriteREG(TEMPAHBTO, 'hFF); // Exceed this polling time, IRQ would be inserted
vWriteREG(TEMPPNPMUXADDR, 32'hTS_CON1); // The adxadc mux address to select to Thermal channel, and please reference mixsys.doc
vWriteREG(TEMPADCENADDR, 32'hAUXADC_CON1); // The adxadc enable address to trigger Thermal senser, please reference auxadc.doc
vWriteREG(TEMPADCVALIDADDR, 32'hAUXADC_CON3); // The adxadc status address to check if Thermal senser reading is valid, please reference auxadc.doc
vWriteREG(TEMPADCVOLTADDR, 32'hAUXADC_DAT11); // The adxadc temperature address for the value read back from temp senser, please reference auxadc.doc
vWriteREG(TEMPRDCTRL, 'h0); // use AUXADC_DAT11 as valid address
vWriteREG(TEMPADCVALIDMASK, 'h2c); // set adxadc valid polarity to 0
```

3. Set up monitoring threshold and SPM wake-up event.

```
vWriteREG(TEMPHTHRE, 'hxxx); // set hot threshold
vWriteREG(TEMPCTHRE, 'hxxx); // set cold threshold
vWriteREG(TEMPCTHRE, 'hxxx); // set hot to normal threshold
vWriteREG(TEMPPROTCTL, 'h20xxx); // set hot to wakeup event control
vWriteREG(TEMPPROTTC, 'hxxx); // set hot to HOT wakeup event
vWriteREG(TEMPMONINT, 'h8000001F); // enable interrupt
```

4. Enable sensing points.

```
vWriteREG(TEMPMONCTL0, 'h07); // enable all three sense points
```

5. Accept IRQ.

```
vReadREG(TEMPMONINTSTS); // read interrupt and clear interrupt status
```

6. Read temperature readings (optional).

```
vReadREG(TEMPMSR0); // read temperature reading of sense point 0
vReadREG(TEMPMSR1); // read tempe
rature reading of sense point 1
vReadREG(TEMPMSR2); // read temperature reading of sense point 1
```

7. Release pause of periodic temperature measurement.

```
vWriteREG(TEMPMSRCTL1, vReadREG(TEMPMSRCTL1) & 0xFFFE);
```

Immediate temperature measurement:

After each immediate is done, the software should disable the immediate mode.

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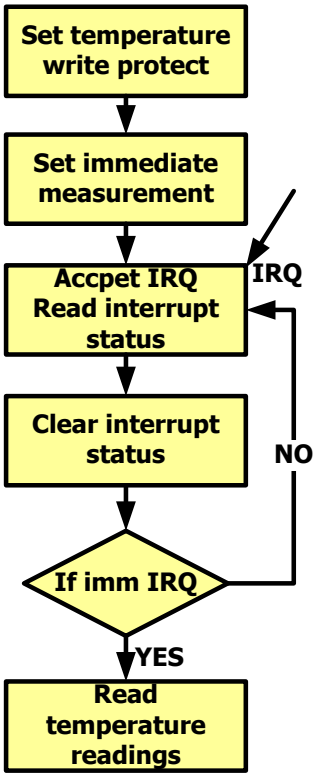

Figure 5-31. Immediate measurement programming flow

5.14.5.1 Interrupt Control Flow

The interrupt condition of high and low temperature monitoring is shown in Figure 5-32.

The software will accept interrupts when the following three conditions occur. The software determines which temperature sensor is to be monitored. Once the condition in any of the three temperature sensors occurs, the interrupt will be issued.

The state machine is shown in Figure 5-33.

- Cold interrupt: When the temperature decreases to lower than the cold threshold form the normal temperature range, it means when the state of NORMAL is transferred into the state of COLD.
- Hot interrupt: When the temperature increases to higher than the hot threshold from the temperature below the hot threshold.

The state of VERY_HOT indicates that temperature is higher than the hot threshold. The state of HOT1 indicates that the temperature is higher than the hot_to_normal threshold. NORAML state cannot be transferred into VERY_HOT directly.

- Hot to normal temperature interrupt: When HOT2 state is transferred into the NORMAL state.

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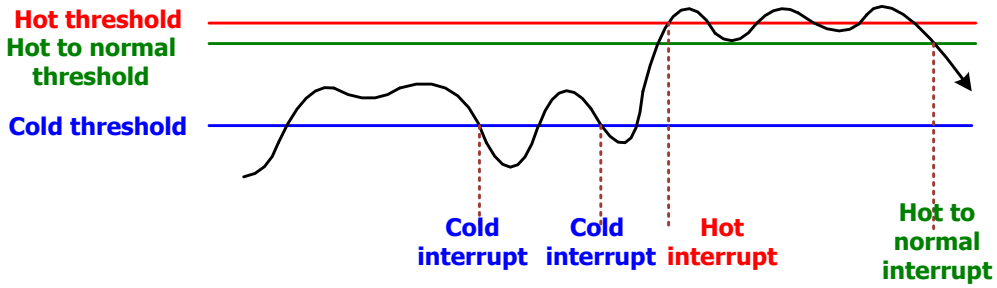

Figure 5-32. Interrupt condition of high/low temperature monitoring

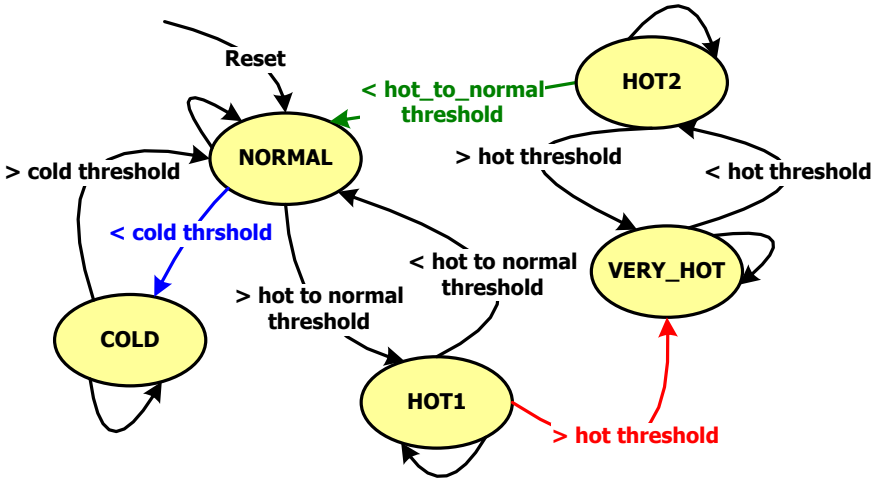

Figure 5-33. Finite state machine of high/low temperature monitoring

In Figure 5-33, when the software immediate measurement is enabled, the state will maintain the current state until the software disables the immediate mode. It is shown as the "*" mark.

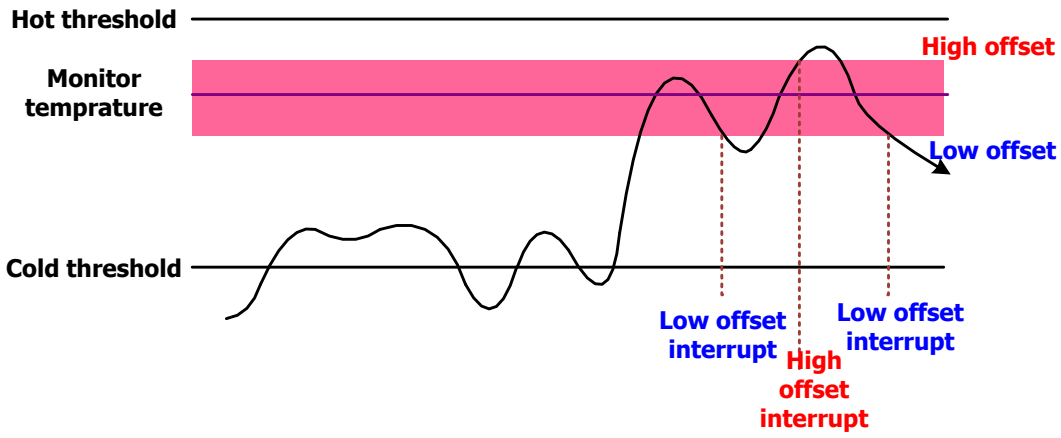

Figure 5-34. Interrupt condition of high/low offset monitoring

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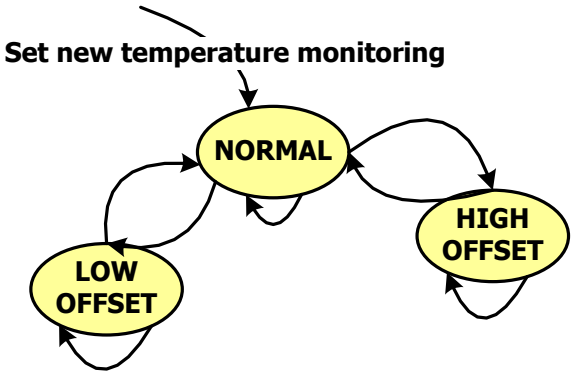

Figure 5-35. Finite state machine of high/low offset monitoring

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5.15 IRTX

5.15.1 Introduction

IRTX module provides the “Consumer IR” feature. According to Wikipedia, *“Consumer IR, consumer infrared, or CIR, refers to a wide variety of devices employing the infrared electromagnetic spectrum for wireless communications. Most commonly found in television remote controls, infrared ports are equally ubiquitous in consumer electronics, such as PDAs, laptops, and computers. The functionality of CIR is as broad as the consumer electronics that carry it. For instance, a television remote control can convey a "channel up" command to the television, while a computer might be able to surf the internet solely via CIR. The type, speed, bandwidth, and power of the transmitted information depends on the particular CIR protocol employed.”*

MediaTek’s IRTX provides three main stream CIR protocols: NEC, RC5 and RC6. It also supports Android IR API in which the OS version is above KitKat.

5.15.2 NEC Protocol

5.15.2.1 Introduction

The NEC protocol uses pulse distance encoding of the bits. Each pulse is a 560µs long 38kHz carrier burst (about 21 cycles). A logical "1" takes 2.25ms to transmit, while a logical "0" takes only half of that, i.e. 1.125ms, as shown in Figure 5-36. The recommended carrier duty-cycle is 1/4 or 1/3.

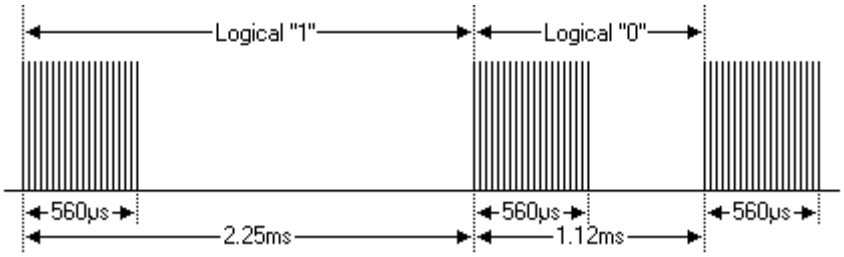

Figure 5-36. Logic representation for NEC protocol

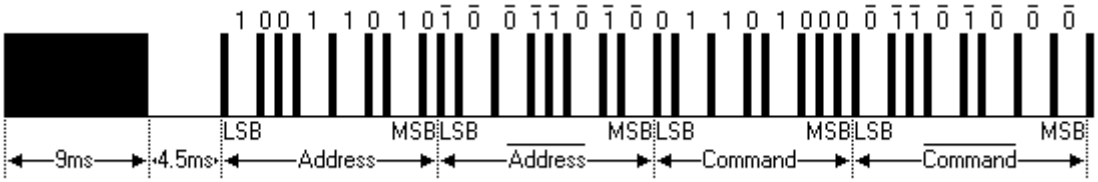

Figure 5-37. Pulse train in transmission of NEC protocol

The picture above shows the typical pulse train of the NEC protocol. With this protocol, the LSB is transmitted first. In this case Address $59 and Command $16 is transmitted. A message is started by a

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9ms AGC burst, which is used to set up the gain of the earlier IR receivers. This AGC burst is then followed by a 4.5ms space, which is then followed by the Address and Command. Address and Command are transmitted twice. In the second time, all bits are inverted and can be used for verification of the received message. The total transmission time is constant because every bit is repeated with its inverted length.

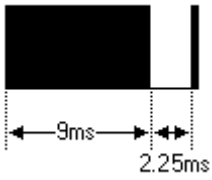

Figure 5-38. A message is started by a 9ms AGC burst

A command is transmitted only once even when the key on the remote control remains pressed. Every 110ms a repeat code is transmitted for as long as the key remains down. This repeated code is simply a 9ms AGC pulse followed by a 2.25ms space and a 560µs burst.

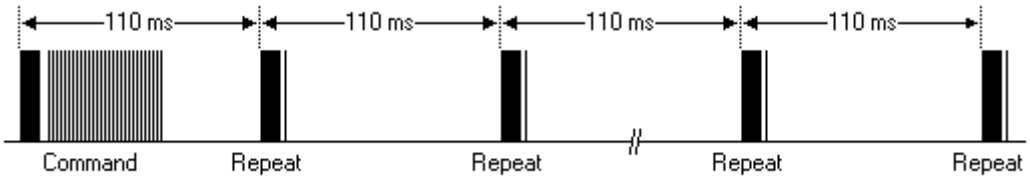

Figure 5-39. A repeat code is transmitted every 110ms

5.15.2.2 Features

- 8-bit address and 8-bit command length
- Address and command are transmitted twice for reliability.
- Pulse distance modulation
- 38kHz carrier frequency
- 1.125ms or 2.25ms bit time

5.15.3 Philips RC-5 Protocol

5.15.3.1 Introduction

The protocol uses bi-phase modulation (or so-called Manchester coding) of a 36kHz IR carrier frequency. All bits are of equal length to 1.778ms in this protocol, with half of the bit time filled with a burst of the 36kHz carrier and the other half being idle. A logical zero is represented by a burst in the first half of the bit time. A logical one is represented by a burst in the second half of the bit time. The

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pulse/pause ratio of the 36kHz carrier frequency is 1/3 or 1/4 to reduce power consumption.

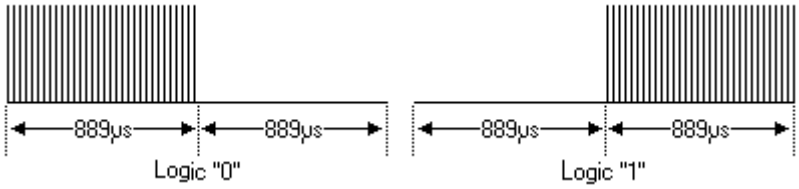

Figure 5-40. Coding method for RC5 protocol

5.15.3.2 Features

- 5-bit address and 6-bit command length (7 command bits for RC5X)
- Bi-phase coding (aka Manchester coding)
- 36kHz carrier frequency
- 1.778ms constant bit time (64 cycles of 36kHz)
- Manufacturer Philips

5.15.4 Philips RC-6 Protocol

5.15.4.1 Introduction

RC-6 is the successor of the RC-5 protocol. Like RC-5, the new RC-6 protocol is also defined by Philips. It is a very versatile and well defined protocol. Because of this versatility its original definition is many pages long. Here we only summarize the most important properties of this protocol. RC-6 signals are modulated on a 36kHz Infra Red carrier. The duty cycle of this carrier has to be between 25% and 50%.

Data are modulated using Manchester coding; this means that each bit (or symbol) has both a mark and space in the output signal. If the symbol is a "1", the first half of the bit time will be a mark and the second half a space. If the symbol is a "0", the first half of the bit time will be a space and the second half a mark.

The main timing unit is 1t, which is 16 times the carrier period (1/36k*16 = 444µs). With RC-6, total different symbols are defined:

- The leader pulse has a 6t mark time (2.666ms) and 2t space time (0.889ms). This leader pulse is normally used to set up the gain of the IR receiver unit.

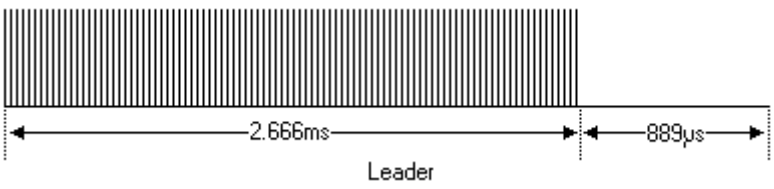

Figure 5-41. Lead pulse in RC6 protocol

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- Normal bits have 1t mark time (0.444ms) and 1t space time (0.444ms). "0" and "1" are encoded by the position of the mark and space in the bit time.

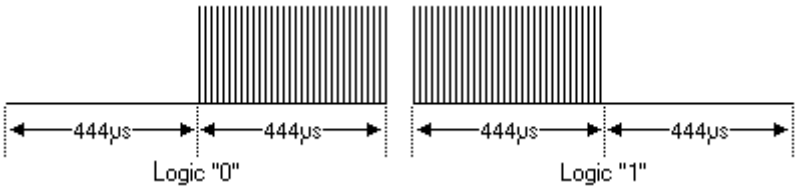

Figure 5-42. Coding method for RC6 protocol

- Trailer bits have 2t mark time (0.889ms) and 2t space time (0.889ms). "0" and "1" are encoded by the position of the mark and space in the bit time.

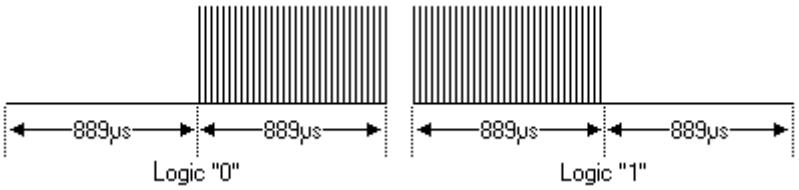

Figure 5-43. Trailer pulse in RC6 protocol

The leader and trailer symbols are only used in the header field of the messages.

5.15.4.2 Features

- Different modes of operation, depending on the intended use
- Dedicated Philips modes and OEM modes
- Variable command length, depending on the operation mode
- Bi-phase coding (aka Manchester coding)
- 35kHz carrier frequency
- Manufacturer Philips

5.15.5 Register Definition

See chapter 3.15 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

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5.16 Audio System

5.16.1 Introduction

The audio system provides the audio data exchange ability among AP, internal modem and external components. The interfaces are listed as the following:

- Master/Slave I2S input interface with SRC *1
- Master I2S output *2
- Master I2S input *1
- Slave PCM interface with SRC for internal MODEM *1
- Master/Slave PCM interface with SRC for internal/external MODEM *1
- Proprietary audio interface for MTK PMIC *1
- PCM/I2S merged interface for MTK connectivity IC *1

5.16.2 Features

- Audio playing
  - Supports 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, and 48kHz sampling rate output
  - Supports playing stereo data
- Audio recording
  - Supports 8, 16, 32, 48kHz sampling rate recording
  - Supports stereo recording
- Speech
  - Supports dual MIC
  - Supports 8/16kHz sampling rate recording
  - Supports side tone filter
  - Master/Slave PCM interface with SRC function
- I2S
  - Supports master/slave input mode
  - Supports master output mode
  - Supports 16/24-bit stereo data
  - Supports 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96, 176.4, and 192kHz sampling rate in master mode
  - Supports EIAJ/I2S format
- PCM/I2S merged interface
  - 4-pin interface for concurrently supporting I2S and PCM
  - PCM supports 8k/16k Hz sampling rate
  - I2S supports 32, 44.1, and 48 kHz sampling rate
- Hardware gain function with higher resolution to enhance the audio quality and flexibility of interconnection
- Flexible interconnection system to make data exchange between interfaces without intervention of CPU

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5.16.3 Block Diagram

The diagram and table below show the flexibility on the interconnection between audio interfaces.

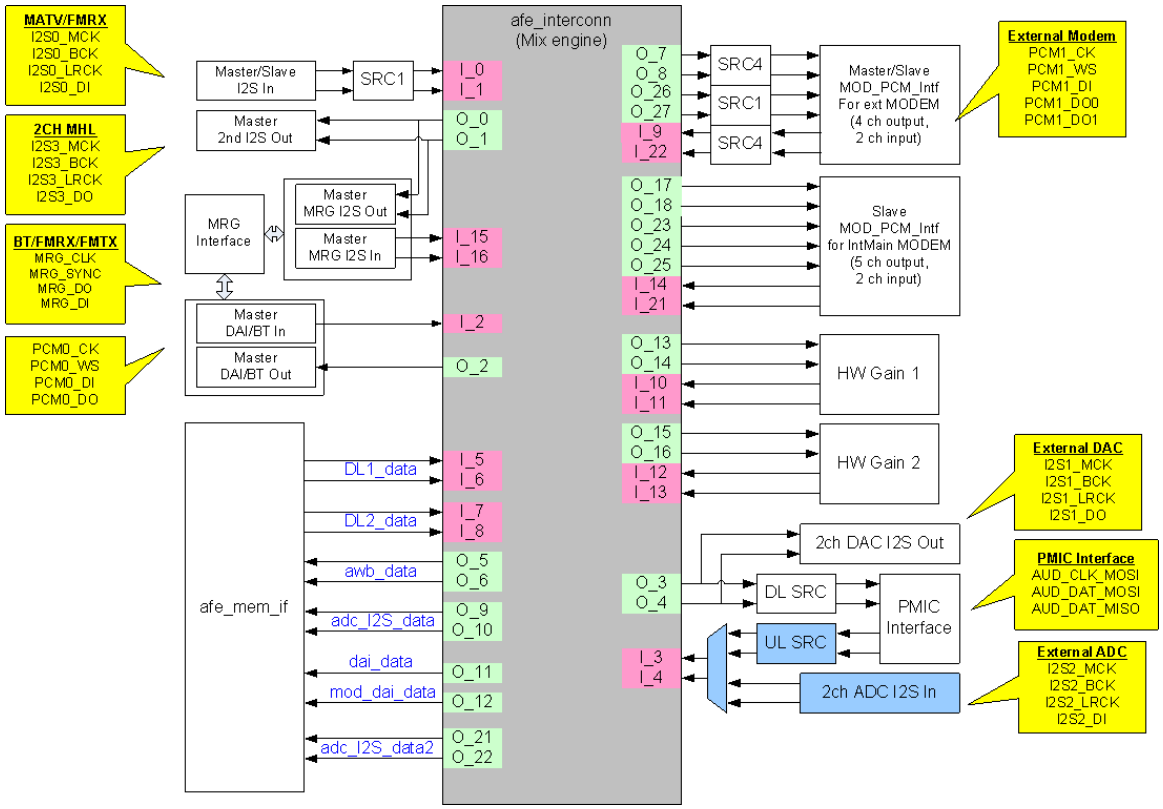

Figure 5-44. Block diagram of audio system

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Table 5-7. Interface of audio system

Input \ Output	O_00 I2S_2_LO	O_01 I2S_2_RO	O_02 DAI_O	O_03 I2S_LO	O_04 I2S_RO	O_05 MEM_AWB_LO	O_06 MEM_AWB_RO	O_07 MOD_DAI_LO	O_08 MOD_DAI_RO	O_09 MEM_ADC_LO	O_10 MEM_ADC_RO	O_11 MEM_DAI_O	O_12 MEM_MOD_DAI_1_LO	O_13 GAIN1_LO	O_14 GAIN1_RO	O_15 GAIN2_LO	O_16 GAIN2_RO	O_17 SPCM_LO	O_18 SPCM_RO	O_19 I2S_3_LO	O_20 I2S_3_RO	O_21 MEM_ADC2_LO	O_22 MEM_ADC2_RO	O_23 SPCM2_LO	O_24 SPCM2_RO	O_25 SPCM3_LO	O_26 MOD_DAI2_LO	O_27 MOD_DAI2_RO
I_00 I2S_I_L	RS	RS	RS	RS	RS	RS	x	S	S	S	S	x	x	S	S	RS	RS	S	RS	RS	RS	S	x	S	S	S	S	x
I_01 I2S_I_R	RS	RS	RS	RS	RS	x	RS	S	S	S	S	x	x	S	S	RS	RS	S	RS	RS	RS	S	x	S	S	S	S	x
I_02 DAI_I	S	S	S	S	S	S	x	S	S	S	S	x	x	S	S	S	S	S	S	x	x	x	x	x	x	x	x	x
I_03 ADC_I2S_I_L	S	S	RS	S	S	S	x	S	x	S	S	x	x	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S
I_04 ADC_I2S_I_R	S	S	RS	S	S	x	S	x	S	x	S	x	x	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S
I_05 MEM_DL1_LI	RS	RS	RS	RS	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	RS	RS	S	S	S	S	S	S	S
I_06 MEM_DL1_RI	RS	RS	RS	RS	S	x	S	x	S	x	S	x	x	S	S	S	S	S	S	RS	RS	S	S	S	S	S	S	S
I_07 MEM_DL2_LI	RS	RS	RS	RS	S	S	x	S	x	S	x	S	x	S	S	S	S	S	x	RS	RS	S	S	S	S	S	S	S
I_08 MEM_DL2_RI	RS	RS	RS	RS	S	x	S	x	S	x	S	x	x	S	S	S	S	S	x	RS	RS	S	S	S	S	S	S	S
I_09 MOD_DAI_I	S	S	S	S	S	S	x	S	x	S	x	S	x	S	S	S	S	S	S	S	S	x	x	x	x	x	x	x
I_10 GAIN1_LI	RS	x	RS	RS	x	S	x	S	x	S	x	S	x	S	S	S	S	S	S	S	S	x	x	x	x	x	x	x
I_11 GAIN1_RI	x	RS	RS	x	RS	x	S	x	S	S	S	S	x	x	x	x	x	x	S	x	x	S	S	S	S	S	S	S
I_12 GAIN2_LI	RS	x	RS	RS	x	S	x	S	x	S	x	S	x	x	x	x	x	S	x	S	x	S	S	S	S	S	S	S
I_13 GAIN2_RI	x	RS	RS	x	RS	x	S	x	S	S	S	S	x	x	x	x	x	x	S	x	x	S	S	S	S	S	S	S
I_14 SPCM_I	S	S	S	S	S	S	x	S	x	S	x	S	x	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S
I_15 MRG_I2S_LI	RS	RS	RS	RS	RS	RS	x	S	x	S	x	S	x	S	S	RS	S	S	S	S	S	S	S	S	S	S	S	S
I_16 MRG_I2S_RI	RS	RS	RS	RS	RS	x	RS	x	S	x	S	x	x	S	S	S	RS	S	S	S	S	S	S	S	S	S	S	S
I_17 ADC2_I2S_L	S	x	RS	S	x	S	x	S	x	S	x	S	x	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S
I_18 ADC2_I2S_R	x	S	RS	x	S	x	S	x	S	x	S	x	x	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S
I_19 MEM_DL1_2_L	RS	x	RS	RS	RS	S	x	S	x	S	x	S	x	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S
I_20 MEM_DL1_2_R	x	RS	RS	RS	RS	x	S	x	S	x	S	x	x	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S
I_21 SPCM2_I	S	S	S	S	S	x	S	x	S	x	S	x	x	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S
I_22 MOD_DAI2_I	S	S	S	S	S	x	S	x	S	x	S	x	S	S	S	S	S	S	S	x	x	x	x	S	S	S	x	x

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5.16.4 Register Definition

See chapter 3.16 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

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5.17 BTIF

5.17.1 Overview

Bluetooth Interface (BTIF) is designed in SOC (BT+GSM) in order to be instead of the UART interface between BT chip and baseband chip. As the UART design, BTIF is an APB slave and can transmit or receive data by MCU access or through DMA/VFIFO.

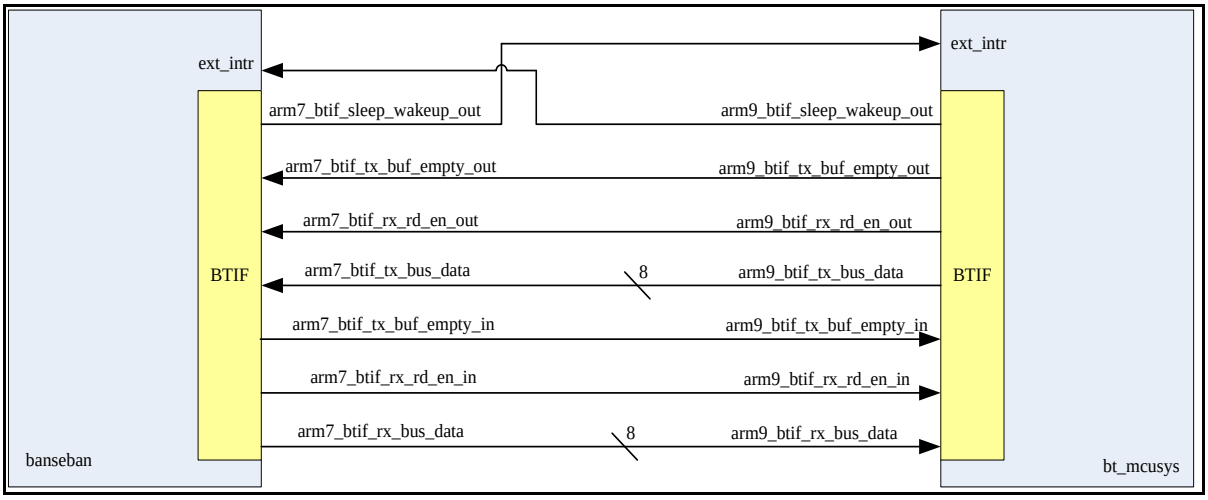

Figure 5-45. Interface connection between BT and baseband system

Detailed block diagram of BTIF is shown in Figure 5-46 and Table 5-8. The Control Register (CR) of BTIF can be set by MCU or DMA through APB interface. The CR of BTIF in btif_inntr_reg can setup FIFO enable, interrupt, wakeup event and so on. Btif_tx_fifo and btif_rx_fifo are used to temporarily store the transmitted and received data. The BTIF transmission is asynchronous handshake. Therefore, btif_rx_async is required to sync the received data.

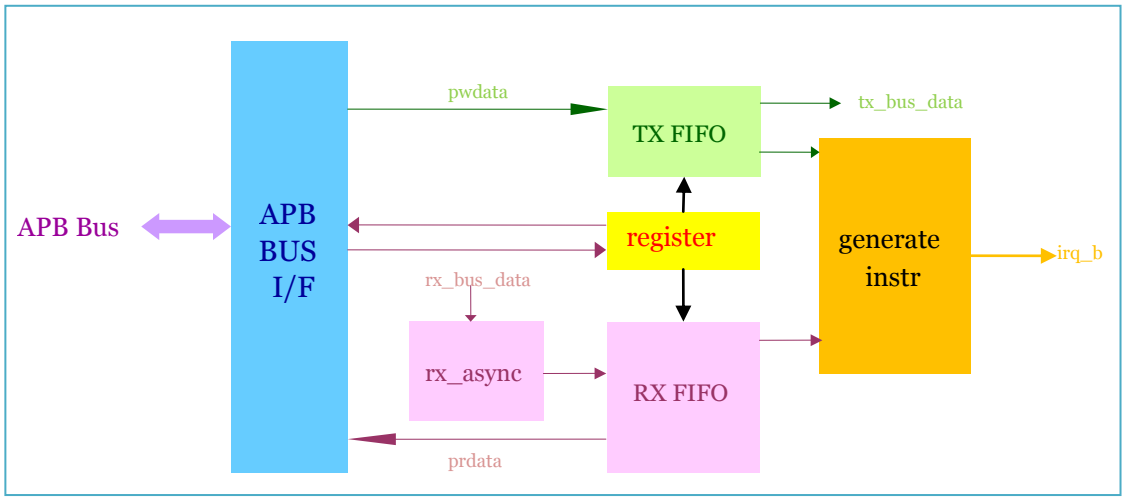

Figure 5-46. Block diagram of BTIF

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Table 5-8. BTIF: Design partition

Sub module name (hier1)	Description
btif_intr_reg	APB bus configures UART register and generates interrupt.
btif_rx_async	Synchronously receives control and data signal
btif_rx_fifo	Receives data from baseband
btif_tx_fifo	Transmits data to baseband

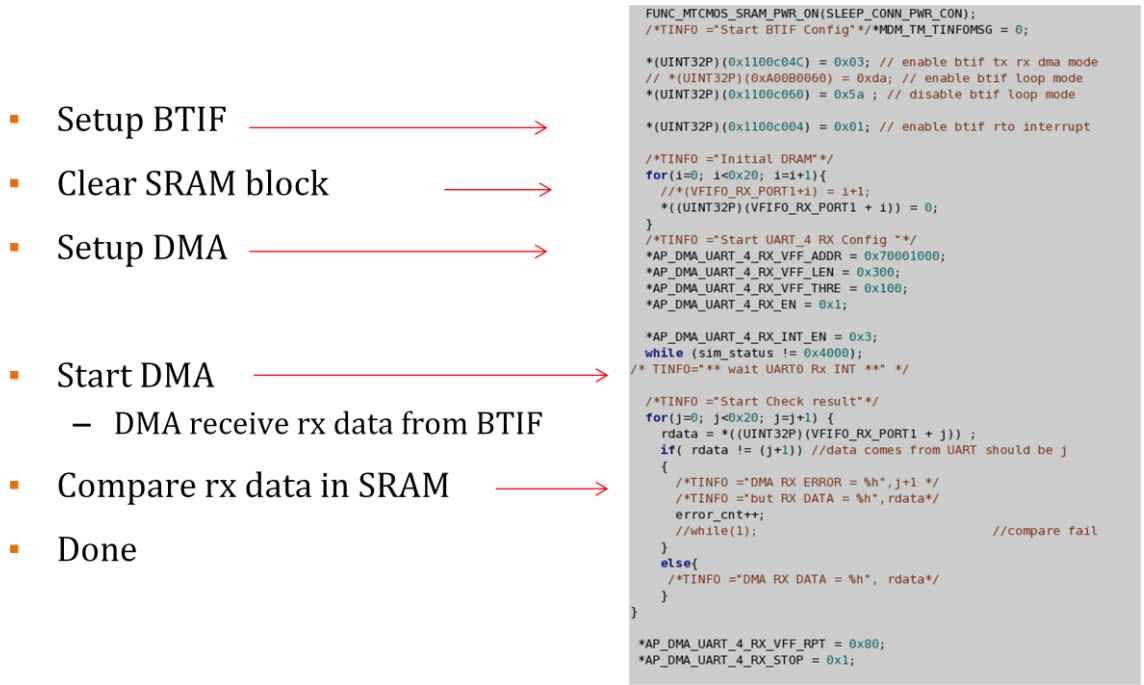
5.17.2 Theory of Operation

Table 5-9 lists the function of BTIF for test. There are four test items. The first is to test the transmitted data; the second received data and the third the interrupt functionality. Finally, the register is configured to verify the settings of BTIF.

Table 5-9. BTIF functions

Item	Main function	Description
1	Tx FIFO	Transmits data to baseband
2	Rx FIFO	Receives data from baseband
3	Interrupt	Generates BTIF interrupt
4	Register	APB bus configures BTIF register.

The software programming guide is listed below.



In simulating the whole chip, four patterns are used to verify BTIF, as shown in the following table.

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Table 5-10. Test patterns for whole chip simulation

Test list	Test name	Description
conn_mcu_btif.list	conn_btif	Tests DMA + BTIF transmitted and received data
conn_mcu_btif_toggle.list	conn_btif_toggle	Tests toggle coverage of interface
conn_mcu_btif_swrst.list	conn_btif_swrst	Tests interrupt
scpsys_wakeup_event.list	conn_btif_wake_ap	Tests wakeup signal to interrupt other subsys

5.17.3 Register Definition

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6 Multimedia

6.1 Display Controller

6.1.1 Introduction

The display controller contains multimedia data path v2.0 (MDP 2.0) and display pipeline (DISP). MDP 2.0 is the time sharing pipeline data flow controller to process resizing and rotation by memory access. The display pipeline outputs pixels to display interface with overlay, color enhancement, adaptive ambient light processing, color correction and gamma correction.

6.1.2 Features

- Multimedia Data Path v2.0. It has one read DMA, two resizers, one 2D-sharpness enhancement, one write DMA and one write rotator.
- Two display pipe lines. One of the pipelines has its own read DMA, overlay, color engine, adaptive ambient light processing, color correction, gamma correction and display interface controller as basic components. The other one only includes overlay, read DMA and display interface controller.
- Supports color enhancement engine
- Supports adaptive ambient light processing for backlight power saving and sunlight visibility improvement
- Supports color correction and gamma correction for accurate image reproduction
- Supports concurrent dual display output
- Display output interface: 1 DSI and 1 DPI. DPI interface can connect to external LVDS, HDMI, and MHL bridge chips to support these interfaces.

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6.1.3 Block Diagram

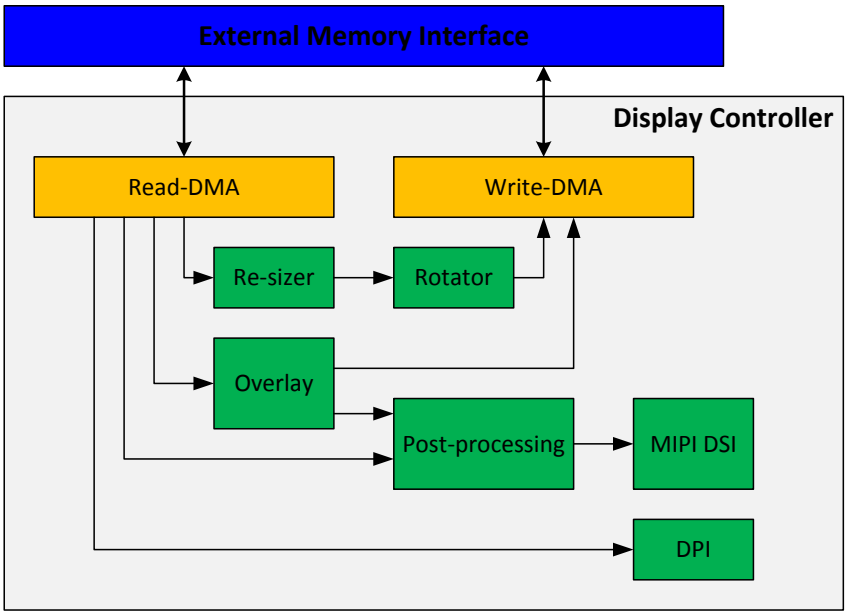

Figure 6-1. Display controller block diagram

6.1.4 Register Definition

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6.2 CAM

6.2.1 Introduction

Camera receives RAW and SOC sensor image data after processing of images and outputting YUV data to DRAM.

6.2.2 Features

The camera incorporates a feature-rich image signal processor to connect with a variety of image sensor components. This processor consists of timing generated unit (TG), lens/sensor compensation unit and image process unit.

- Interface
  - Main cam: MIPI 4 lane, 1.5Gbps/lane/parallel interface
  - Sub cam: MIPI 4 lane1.5Gbps/lane /parallel interface
- Raw dump frame rate is 16M@30fps
- Supports video snapshot, which enables user capture image while recording video
- Image processing
  - Bad pix compensation
  - Lens shading compensation
  - Demosaic
  - Color clipping
  - Gamma correction
  - Edge enhancement
  - Noise reduction with large kernel
  - Temporal noise reduction
  - Multi frame blending for lowlight condition
  - Preference color adaptation
- 3A statistics and correction
- Flicker detection
- Electronic image stabilization for video
- Video face beautifier
- Image face Beautifier
- Supports picture in picture/video in video
- High quality resizers

6.2.3 Register Definition

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6.3 SENINF_TOP (Sensor Interface)

6.3.1 Introduction

The SENINF_TOP module transfers sensor signals into image pixels and passes them to ISP.

6.3.2 Features

- MIPI interface
  - Two MIPI interfaces
  - Virtual channel/data type data interleaving
- Serial interface
  - One serial interface
- Parallel interface
  - One parallel interface
- Three sensor master clocks

6.3.3 Register Definition

See chapter 4.3 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

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6.4 FDVT

6.4.1 Introduction

6.4.1.1 Overview

Face Detection and Visual Tracking (FDVT) Engine is used to detect new coming faces and track the existing faces in an image. It has the capability of detecting the faces of Rotation-in-Plane (RIP) from -180 º to +180 º and Rotation-off-Plane (ROP) from -90º to +90º (see Figure 6-2).

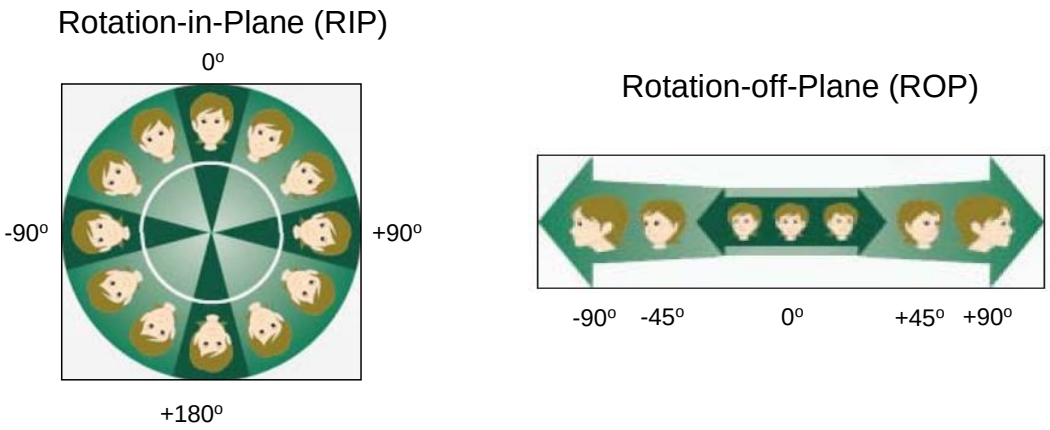

Figure 6-2. Definition of RIP and ROP

The input image of FDVT is the RGB565/YUV420/YUV422 data in the external memory, which is generated by ISP module. FDVT supports images of size up to 1022x1022 pixels. The FDVT outputs are the locations, sizes, estimated pose and confidence values of the detected faces, which are also stored in the external memory.

6.4.1.2 Theory of Operations

FDVT detects the faces in an image with the unit called Macro-window. The Macro-window scans the positions within the image. In each position, FDVT uses the predetermined features to determine if the Macro-window contains the face or not. In order to detect the large faces by using the Macro-window of the same size, FDVT rescales the original gray image into the smaller ones and does the scanning process in the re-scaled images. Figure 6-3 illustrates the concept of Macro-window detection.

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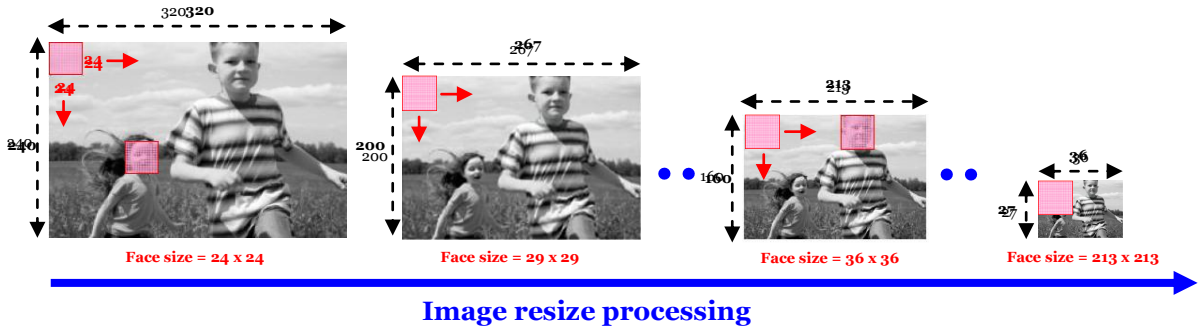

Figure 6-3. Example of face detection with 24x24 Macro-window

In the Macro-window of each position in the image, FDVT calculates the feature values and confidence values to determine if it contains the face. To increase the speed of calculating the values, FDVT uses the concept of integral image, which is generated by IIG module. If the face is detected in the Macro-window, FDVT will write the position, size, estimated pose and confidence value of the face to the external memory via DMA. Once all the re-scaled images are scanned completely, FDVT will send the interrupt signal to notify the firmware to read the face detection. Then, FDVT can prepare to do the detection in the next image. Figure 6-4 shows the FDVT operation flow mentioned above. Details on the operations are described in the next section.

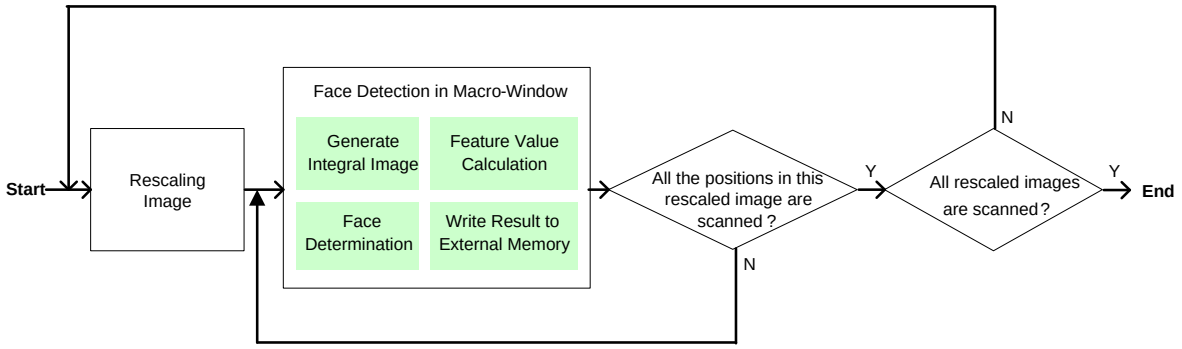

Figure 6-4. FDE operation flow

6.4.2 Software Control Flow and Register Settings

6.4.2.1 Software Control Introduction

Initially SW must initialize all registers (blue part). After that, not all the registers must be updated (only the red part needs to be updated frame by frame) (see Figure 6-5).

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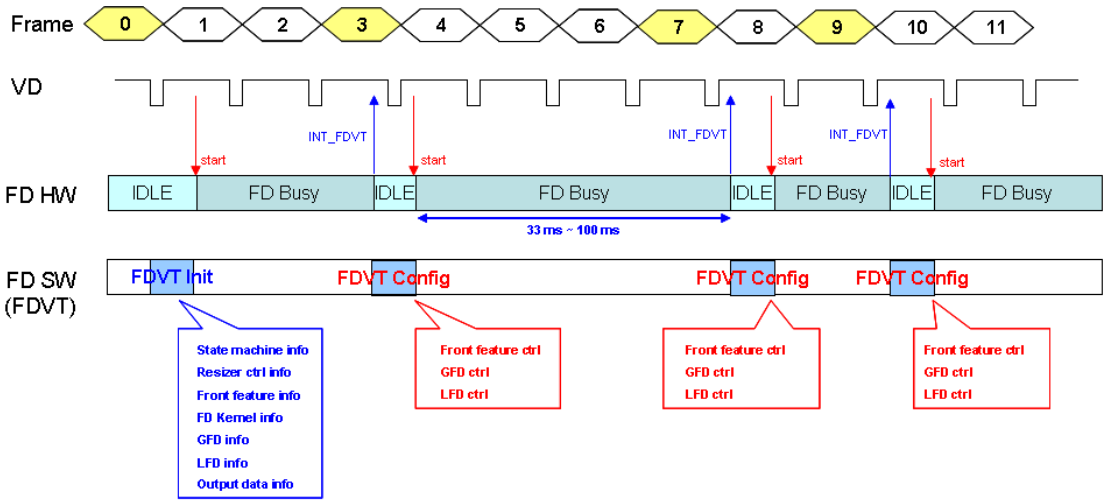

Figure 6-5. Register setting timing diagram

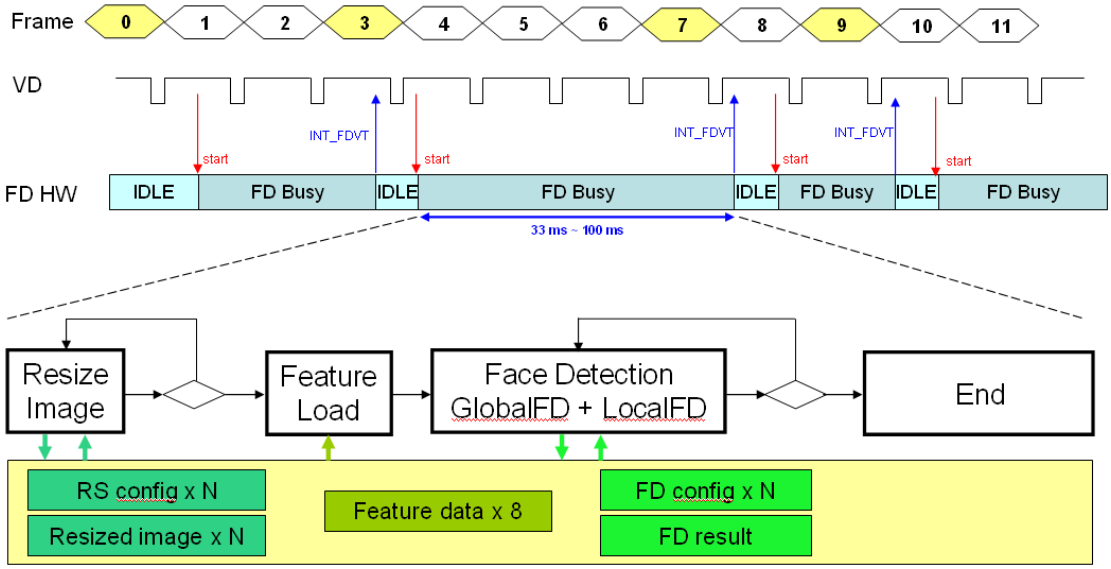

Figure 6-6. Hardware FDVT processing flow in one frame

First the resizer resizes the input image to several smaller images you need. RS_config (RS configuration) contains the resize information of each small image. If you have N small image, set up N RS_config. Hardware will read these configurations and store the corresponding smaller images to DRAM.

Next, HW loads all the front-end features from DRAM to SRAM. SW must set the front-end feature number of each data set (total 8 data sets).

The face detection part will start processing after the front-end feature load is finished. HW will load FD_config (FD configuration) to do GFD (Global Face Detection) and LFD (Local Face Detection) process. FD_config contains the face detection information of each small image. If you have N small

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image, set up N FD_config. Hardware will read these configurations to do further processing. If any face candidate is found, HW will store the face result (information) to DRAM.

6.4.3 Register Definition

See chapter 4.4 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

6.4.3.1 Parameter Settings in DRAM

RS_CONFIG (BIT 127 ~ 0)																
Bit	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112
Name	IGMA_EN	SRC_FORMAT			XMAG_YMAG											
Bit	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
Name		DES_IMG_HT												DES_IMG_WD		
Bit	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
Name	DES_IMG_WD									SRC_IMG_HT						
Bit	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
Name	SRC_IMG_HT					SRC_IMG_WD										
Bit	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Name	DES_BASE_ADR															
Bit	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Name	DES_BASE_ADR															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC_BASE_ADR															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC_BASE_ADR															

RS_CONFIG (BIT 255 ~ 128)																
Bit	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112
Name																
Bit	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
Name																
Bit	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
Name																
Bit	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
Name																
Bit	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Name																
Bit	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Name	SRC_IMG_STRIDE															
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															YOFFSET	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	YOFFSET							XOFFSET								

Note:

1. *Base address should be 16-byte aligned.*
2. *FD will not process the resized image width or height that is smaller than 24.*

SRC_BASE_ADR Rescaling source image source base address

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DES_BASE_ADR	Rescaling destination image destination base address (The size of destination buffer must be multiple of 16.)
SRC_IMG_WD	Rescaling source image width
SRC_IMG_HT	Rescaling source image height
DES_IMG_WD	Rescaling destination image width
DES_IMG_HT	Rescaling destination image height
XMAG_YMAG	Rescaling ratio (format: Q0.3.9)
SRC_FORMAT	Rescaling source image format **0** RGB **1** Y **2** YUYV **3** YVYU **4** VYUY **5** UYVY
IGMA_EN	Enables inverse gamma
XOFFSET	Beginning sub-pixel x position (less than 504)
YOFFSET	Beginning sub-pixel x position (less than 504)
SRC_IMG_STRIDE	Rescaling source image stride (Y must be multiple of 16; others must be multiple of 8.)

FD_CONFIG (BIT 127 ~ 0)

Bit	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112
Name	**IMG_STRIDE**															
Bit	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
Name										**SHIFT_V**						
Bit	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
Name	**SHIFT_H**							**IFACTOR**								
Bit	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
Name	**IFACTOR**	**SFACTOR**														
Bit	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Name											**ROP_ENABLE_FULL**	**ROP_ENABLE_SEMI**	**IMG_HT**			
Bit	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Name	**IMG_HT**						**IMG_WD**									
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**IMG_BASE_ADR**															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**IMG_BASE_ADR**															

Note: Base address should be 16-byte aligned.

IMG_BASE_ADR	Base address of the source (luma only) image
IMG_WD	Width of source image
IMG_HT	Height of source image
ROP_ENABLE_SEMI	Enables ROP50 and ROP-50 LFD detection **0** pose 12 ~ pose 35 will not be detected by LFD.

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1 pose 12 ~ pose 35 will be detected by LFD if LFD_POSE is set to detect this pose.

ROP_ENABLE_FULL Enables ROP90 and ROP-90 LFD detection

0 pose 36 ~ pose 59 will not be detected by LFD.

1 pose 36 ~ pose 59 will be detected by LFD if LFD_POSE is set to detect this pose.

SFACTOR Scaling factor relative to RGB image size. Format is 6.9 (>=1.0)

IFACTOR Inverse scaling factor relative to RGB image size. Format is 1.9 (<=1.0)

SHIFT_H Horizontal search range of active window. LFD searches from (LFDXX.x0-SHIFT_H) to (LFDXX.x0+SHIFT_H).The unit is one pixel of RGB image size.

SHIFT_V Vertical search range of active window. LFD searches from (LFDXX.y0-SHIFT_V) to (LFDXX.y0+SHIFT_V).The unit is one pixel of RGB image size.

IMG_STRIDE Stride of source image

FACE RESULT (BIT 127 ~ 0)																
Bit	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112
Name																
Bit	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
Name																
Bit	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
Name																
Bit	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
Name											DET_SIZE					ROP_DIR
Bit	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Name	ROP_DIR		RIP_DIR				FCV								Y1	
Bit	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Name	Y1								X1							
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	X1		Y0										X0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	X0						TYP	FACE_INDEX								

Note: The max. FACE RESULT number is 511.

FACE_INDEX Indicates face index number

TYP Indicates face type

0 Face is detected by GFD.

1 Face is detected by LFD.

X0, Y0, X1, Y1 Indicates face candidate position

FCV Indicates face confidence value of the face candidate

RIP_DIR Indicates face RIP (rotate in plane) direction

0 0°

1 30°

2 60°

...

11 -30°

Others Reserved

ROP_DIR Indicates face ROP (rotate out of plane) direction

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	0	0°
	1	50°
	2	-50°
	3	90°
	4	-90°
	Others	Reserved
DET_SIZE	Indicates face size index	

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6.5 DISPLAY PWM Generator

6.5.1 Introduction

The PWM generator provides PWM signals for the LED driver of mobile LCM.

6.5.2 Features

- Operating clock: 26MHz (default) or 104MHz
- Gradual PWM control

6.5.3 Register Definition

See chapter 4.5 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

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6.6 DPI (Digital Parallel Interface)

6.6.1 Introduction

The DPI controller provides data to the companion chip, such as HDMI, MHL, or other bridge chips.

6.6.2 Features

- Programmable 2D/3D, progressive/interlaced timing generator
- Programmable EAV, SAV embedded sync. Timing
- Fixed-coefficient color space transform
- Supports RGB 8-bit/YUV444 8-bit/YUV422 8-bit,10-bit,12-bit output data format
- Supports YC MUX (CCIR656-like) output format
- Support s dual edge output format
- Supports secure display
- 3-tap chroma LPF
- Internal pattern generator

6.6.3 Register Definition

See chapter 4.6 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

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6.7 Display Serial Interface

6.7.1 Introduction

The display serial interface (DSI) is based on MIPI Alliance Specification, supporting high-speed serial data transfer between host processor and peripheral devices such as display modules. DSI supports both video mode and command mode data transfer defined in MIPI spec, and it also provides bidirectional transimission with low-power mode to receive mesaages from the peripheral. DSI should work with MIPI_TX_Config module to obtain its engine clock to analog DPHY macro, and it should work with DMA engines in the previous stage of DISP path to read frame pixels from memory.

6.7.2 Features

The DSI engine has the following features for display serial interface:

- 1 clock lane and up to 4 data lanes
- Throughput up to 1G bps for 1 data lane
- Bidirectional data transmisstion in low-power mode in data lane 0
- Uni-directional data transmission in high-speed mode in data lane 0 ~ 3
- 128-enrty command queue for command transmission
- Supports 3 types of video modes: sync-event, sync-pulse, burst mode
- Pixel format of RGB565/RGB666/loosely RGB666/RGB888
- Supports non-continuous high-speed transmission in both clock/data lanes
- Supports command mode frame transmission free-run
- Supports peripheral TE and external TE signal detection
- Supports limited high-speed residual packet transmission during video mode blanking period
- Supports ultra-low power mode control
- Supports frame compression with UFOE module
- Supports low frame-rate (LFR) technique

6.7.3 Register Definition

See chapter 4.7 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

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6.8 JPEG Encoder

6.8.1 Introduction

The hardware JPEG encoder implements the baseline mode of Standard ISO/IEC 10918-1. After initialization by software, the hardware JPEG encoder can generate the entire compressed file. Figure 6-7 shows the procedure of the JPEG encoder. The YUV pixel data are retrieved from the memory and grouped into 8x8 blocks. YUV422 one plane and YUV420 two plane formats are supported. When encoding, the first thing to do is turning the pixel data into the frequency domain using FDCT. After the quantization is done, the quantized DCT coefficients are encoded by RLE and VLC. Then the bitstream of JPEG file is generated.

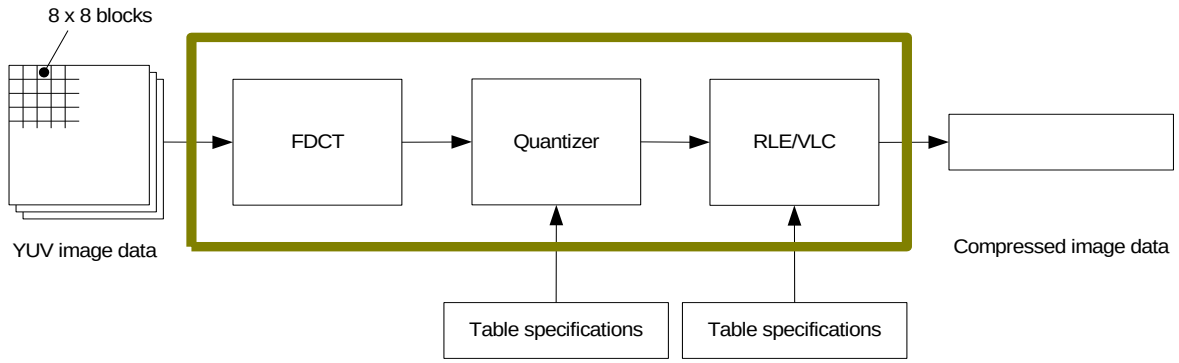

Figure 6-7. Procedure of JPEG encoder

6.8.2 Features

The JPEG encoder supports YUV 422 and 420 formats for color pictures. With software assistance and suitable destination memory address setting; JFIF/EXIF JPEG format can also be supported. For hardware reduction, it uses standard DC and AC Huffman tables for both luminance and chrominance components. To adjust the picture compression ratio and picture quality, there are 15 levels of quantization that can be programmed.

6.8.2.1 Software Reset Mechanism

To avoid problem occurred with wrong SMI protocol, the software should do reset based on the following procedure.

1. The EN bit in JPGENC_CTL should be set to 0.
2. The software polls the GMC_IDLE bit in JPGENC_DEBUG_INFO0.

Only when the GMC_IDLE bit is 1 can the RSTB bit in JPGENC_RST be set to 0 to do the reset scheme. Be sure to follow this procedure to do software reset.

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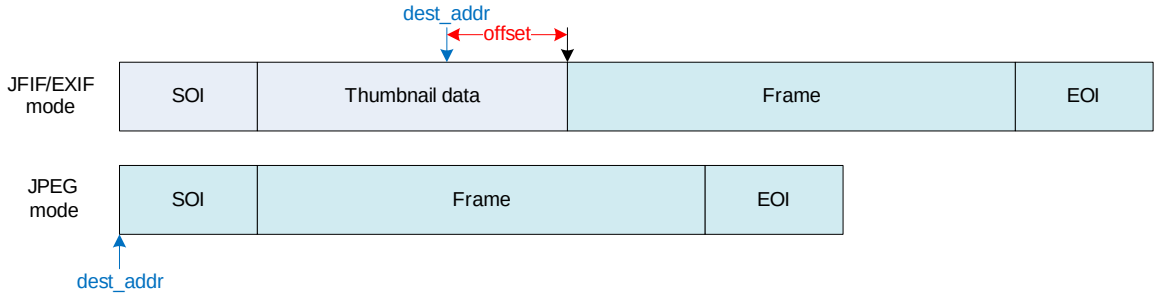
6.8.2.2 Byte Offset Address Setting

To align SMI bus bitwidth, the buffer address should be 16-bytes aligned. However, to reduce software bitstream copy and concatenate effort, software can program a byte offset setting (from 0~15 bytes) to offset the start position of bitstream written out by hardware. The illustration of this feature is as the following.



- Example: If SOI starts at 0x0000,
  - JFIF/EXIF mode: SOI+thumbnail data length = 50 bytes
    - dest_addr = 0x0030
      offset = 0x0002

6.8.3 DRAM Buffer Requirement

- Source frame buffer
  - YUV422:
    - One frame buffer
    - Buffer size
      - {[(width_y*2) + 127]/128}*128*[(height_y + 7)/8]*8
  - YUV420: Two frame buffers
    - Two frame buffers
    - Buffer size
      - Y: [(width_y + 127)/128]*128*[(height_y + 15)/16]*16
      - UV: [(width_y + 127)/128]*128*[(height_y + 7)/8]*8
- Bitstream buffer
  - One buffer
  - Buffer size (suggested)
    - YUV422: width_y* height_y*2
    - YUV420: width_y* height_y*1.5
    - Must be multiple of 128 bytes.

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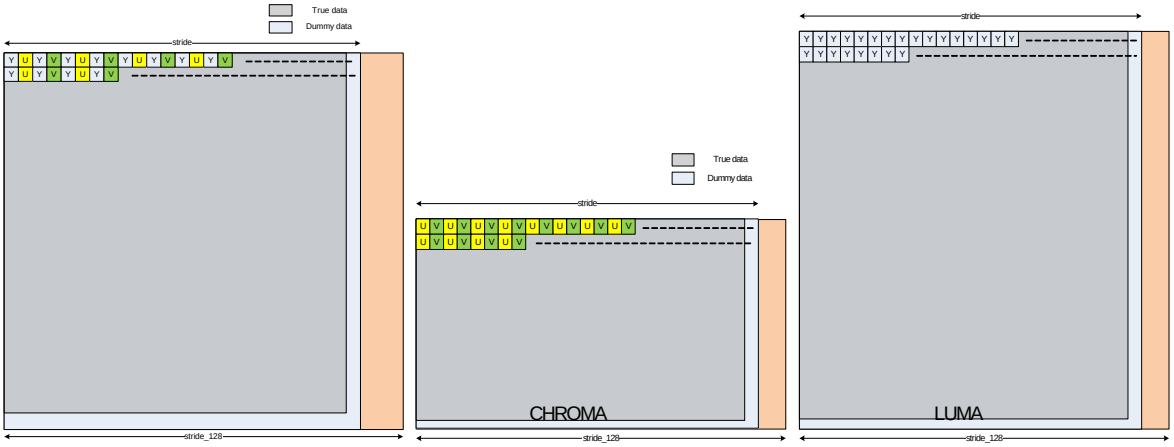

Figure 6-8. Memory footprint of source frame buffer

6.8.4 Register Definition

See chapter 4.8 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

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6.9 JPEG Decoder

6.9.1 Introduction

At present most images must be stored in JPEG format compressed files. To display such type of file and boost image processing performance, the hardware JPEG decoder is developed. The JPEG decoder is designed to decode baseline JPEG file with general YUV sampling combinations. Note that the progressive decoding is ***not*** supported in the hardware decoder).

To obtain the best speed performance, the JPEG decoder handles all portions of JPEG files except for the 17-byte SOF marker. The software only needs to program related control registers based on the SOF marker and wait for an interrupt coming from the hardware. Figure 6-9 is the basic JPEG file structure and starting address that JPEG decoder needs. The information of DQT and DHT table is included in the JPEG file which should be parsed by the JPEG decoder and stored in the memory.

Taking into consideration the limited size of memories, the hardware decoder also supports breakpoints insertion in huge JPEG files. Breakpoints insertion allows software to load partial JPEG file from the external flash into the internal memory if the JPEG file is too large to sit internally at a time.

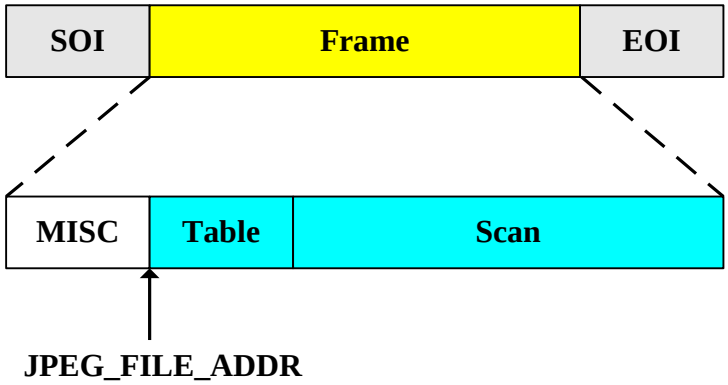

Figure 6-9. Basic structure of JPEG files

6.9.2 Features

The sleep controller receives commands from system software and controls the built-in power management unit to cut off the power supply of external clock source. The power of external clock source can be resumed by several events predefined by users. These events are issued by:

- Baseline JPEG decoding (no progressive decoding, no restart marker decoding, bypass to software solution)
- Sampling format limitation: See Figure 6-10.
- Hardware table parsing (SW handle SOF parsing)
- Supports file breakpoint

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- 1/2/4/8 block resize (some limitation due to format conversion, see section 6.9.2.3)
- Supports MCU rows pause/resume
- Error handling by bitstream overflow detection

The supported input sampling format of JPEG decoder is illustrated in Figure 6-10.

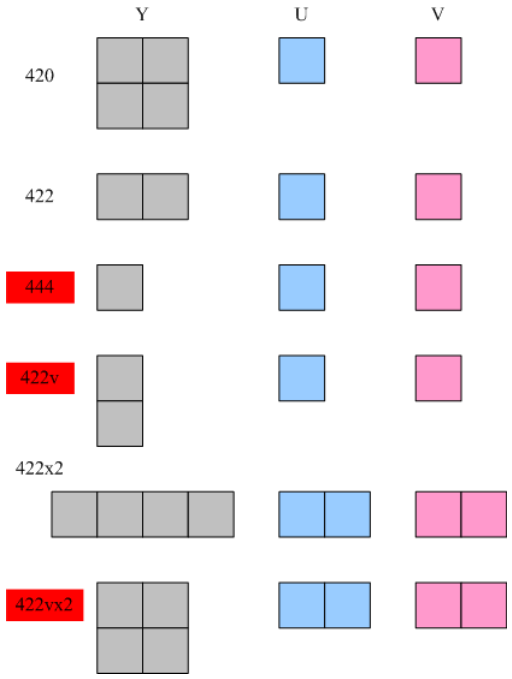

Figure 6-10. Supported sampling format of input JPEG file

For input sampling format that is not supported by the hardware, software solutions are adopted.

6.9.2.1 Software Reset Mechanism

To avoid unexpected memory access behavior, the soft reset scheme is also developed for JPEG decoder (same procedure with JPEG encoder). First, assert the soft reset bit in JPGDEC_RESET. Then hardware will issue a done interrupt when its state is not busy. Software de-asserts the soft reset bit and clears the interrupt status. Finally, assert the hard reset bit in JPGDEC_RESET to start the reset process.

To reset JPEG decoder and GDMA in the direct couple mode, perform soft reset mechanism to JPEG decoder and reset JPEG decoder first. Next, perform GDMA soft reset mechanism to reset GDMA.

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6.9.2.2 Operation Modes

6.9.2.2.1 Normal Mode (Full Frame Mode)

In normal mode, JPEG decoder outputs full frame to DRAM. ISP/MDP then takes over tor resize and process the image. For software usage, one set of frame buffer should be allocated to JPEG decoder, and set up the corresponding configuration and trigger hardware for decoding. JPEG decoder will return interrupt when full frame is decoded.

6.9.2.2.2 Pause/ Resume Mode

In pause/resume mode, JPEG decoder outputs multiple MCU rows to DRAM based on software configuration and pause. JPEG decoder returns interrupt when the assigned MCU rows are decoded. The next configuration and trigger resume JPEG decoder, and the following MCU rows are outputted correspondingly. For software usage, one set of MCU rows buffer should be allocated to JPEG decoder, when JPEG decoder finishes the assigned MCU rows and pause, software should do the next configuration and trigger hardware until full frame is decoded. JPEG decoder will return interrupt when full frame is decoded.

6.9.2.3 Block Resizing

To save memory usage for JPEG image with extreme large size, block level resizing is supported by JPEG decoder. Simple 1/2, 1/4, 1/8 block level resize using 2-tap bilinear filter is adopted.

Since sampling format conversion is required for JPEG decoder. Resize limitation exists for some source formats (e.g. for YUV444 input, only 1/4 resize can be performed).

		Config			
src format	dst format (3/1-plane)	Y_rsz	UV_h_rsz	UV_v_rsz	Limitation on real rsz
420	420	real_rsz	real_rsz	real_rsz	No
422	422	real_rsz	real_rsz	real_rsz	No
444	422	real_rsz	1+real_rsz	real_rsz	~ 1/4
422v	420	real_rsz	1+real_rsz	real_rsz	~ 1/4
422 x 2	422	real_rsz	real_rsz	real_rsz	No
422v x 2	420	real_rsz	1+real_rsz	real_rsz	~ 1/4

6.9.2.4 Error Handling Mechanism

Error handling is first performed in software header parsing stage. If the header is corrupted, software should not pass such file to hardware decoder. In hardware decoding stage, only part of error detection is supported (no error concealment capability). Several types of detection are supported, including invalid Huffman entry and block overflow. One flag will be raised when such error is

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detected and error interrupt will be issued. Hardware stops when 0xffd9 is encountered or the file size count is reached. If software is to stop JPEG decoder when error is detected, use the soft reset scheme.

6.9.3 DRAM Buffer Requirement

For JPEG decoder, two types of buffer should be allocated by software, bitstream buffer and decoded frame buffer.

The bitstream buffer is used to store the jpeg file bitstream. The start address should be 16-byte aligned, and the address position should be the first marker segment (e.g. DQT or DHT) after all APP markers are skipped. The break point address can be set based on the limited memory size. The related control register is JPEG_FILE_ADDR and JPEG_FILE_BRP. The allocated bitstream buffer size should be multiple of 128 bytes.

The decoded frame buffer is separate three-plane planar format; the supported color formats are YUV422, YUV420 and grayscale. Figure 6-11 is an example of the decoded frame buffer.

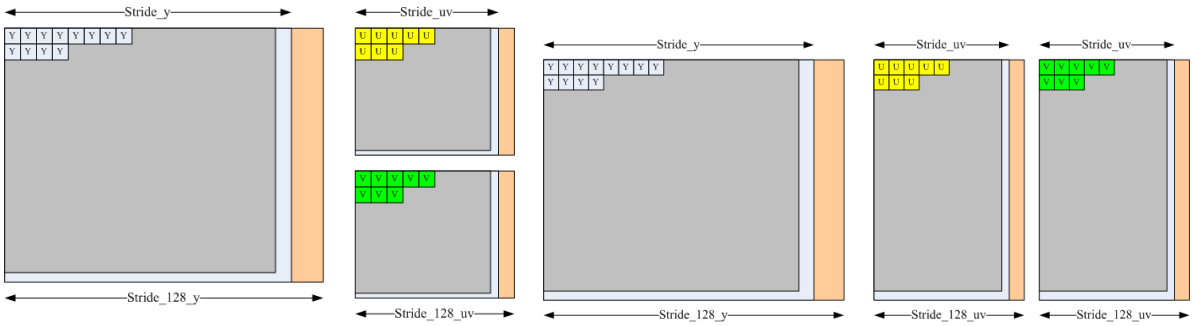

Figure 6-11. Memory footprint of source frame buffer

- Bitstream buffer
  - One buffer
  - Buffer size: Depends on available memory buffer
    - **Must be multiple of 128 bytes**
    - Loading as many as possible for better decoding performance is recommended.
    - Supports breakpoint feature
- Destination frame buffer
  - YUV422:
    - Three frame buffers
    - Buffer size
      - Y: [(width_y + 127)/128]*__128__*[(height_y + 7)/8]*8
      - U: [(width_u + 127)/128]*__128__*[(height_y + 7)/8]*8
      - V: [(width_v + 127)/128)*__128__*[(height_y + 7)/8]*8
- YUV420:
  - Three frame buffers
  - Buffer size

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- Y: [(width_y + 127)/128]*128*[(height_y + 15)/16)*16
- U: [(width_u + 127)/128)*128*[(height_y + 7)/8]*8
- V: [(width_v + 127)/128)*128*[(height_y + 7)/8]*8

6.9.4 Register Definition

See chapter 4.9 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

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6.10 Video Decoder

6.10.1 Introduction

MediaTek Video Decodor (VDEC) in MT6750 supports multi-standard video compression format, which greatly reduces the CPU loading and achieves high performance video decompression.

The video standard supported by VEDC includes:

- MPEG1/2
- H.264 CBP/MP/HP
- MPEG4 ASP
- DIVX3/DIVX4/DIVX5/DIVX6/DIVX HD/XVID
- Sorenson H.263, H.263
- De-Blocking Filter for MPEG2, H.263
- H.264 decoer Constraint Baseline Profile/Main/High Profile
- HEVC decoder main profile

VDEC support full-HD 30fps under the limitation that picture size > full-HD, (i.e. does not support picture width > 1920 or picture height > 1088).

6.10.2 Block Diagram

The architecture and core blocks of VDEC are shown in Figure 6-12, including the following parts: Entropy Decoder, IS/IQ/IT, MV Calculation, Intra Prediction, Motion Compensation and De-blocking Filter. The input to VDEC is a compressed video bitstream. After the decoding process, the reconstructed video will be sent to the display stage.

6.10.3 Interface

The interface of VDEC is shown in Figure 6-13. Related modules include SMI interface, APB interface and handshaking bus between VDEC and CDP. The output format supported by VDEC is:

- NV12_BLK (Video block mode), 420 format block mode, 2 plane (UV)
- NV12_BLK_FCM (video field compact mode), 420 format block mode, 2 plane (UV)

VDEC uses DRAM as bitstream input, working buffer, reference buffer and output, and DRAM access process is achieved by using SMI interface. Seven sets of SMI interfaces with 128 bits of read/write are used including MC/PP/PP_WRAP/AVC_MV/PRED_RD/PRED_WR/VLD. In addition, all ports are EMI ports, i.e. no SYSRAM is required.

Register settings are passed to VDEC by APB interface. There is one set of APB interfaces.

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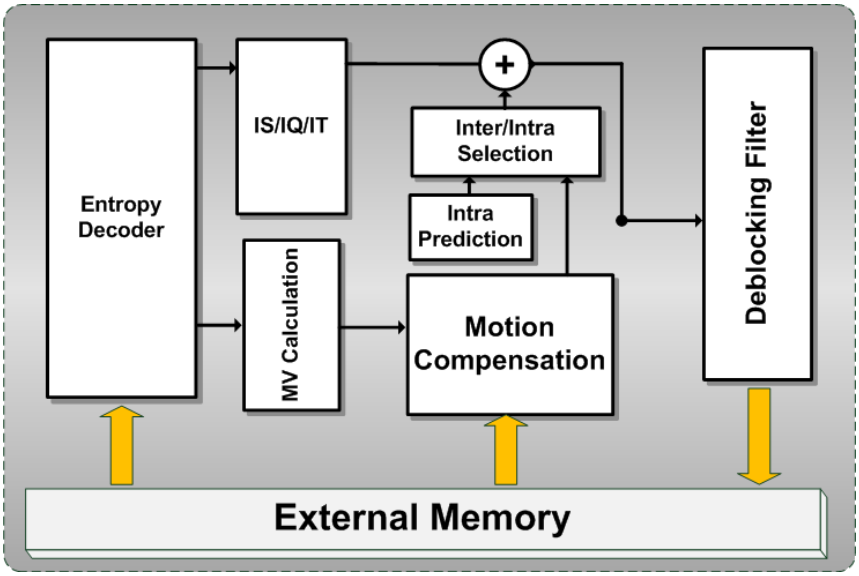

Figure 6-12. Block diagram of video decoder

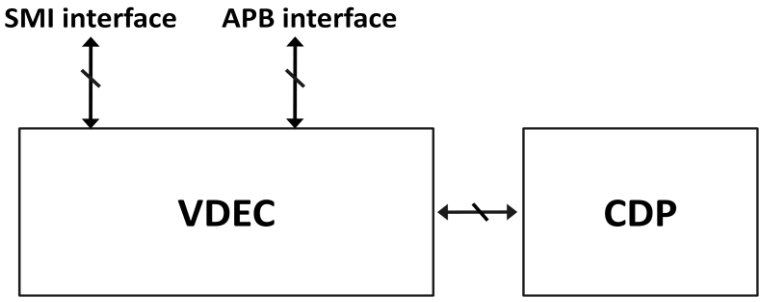

Figure 6-13 Interface of VDEC

6.10.4 Programming Guide

This section defines the recommended programming procedure for using VDEC to perform video decompression correctly. Moreover, this section also introduces common functions and settings, that is, these functions do not change from different video coding standards.

6.10.4.1 Base Settings

This section describes useful settings before programming VDEC, including clocks and base address of VDEC.

6.10.4.2 Clocks

Two clocks are required for VDEC:

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- smi_clk: 286MHz
- vdec_clk: 250MHz

For more details, see the CKGEN register map.

6.10.4.2.1 VDEC Register Base Address

Base address of each sub-module is described in Table 6-1.

Table 6-1. VDEC base address

CS	BASE (hex)	HW cs	Comment
VDEC_MISC	0x16020000	cs_vdec_dv	Legacy naming is DV_BASE.
VLD	0x16021000	cs_vdec_vld	
VLD_TOP	0x16021800	cs_vdec_vld	Partial bank of VLD_BASE, i.e. (VLD | 0x800)
MC	0x16022000	cs_vdec_mc	
AVC_VLD	0x16023000	cs_avc_vld	
AVC_MV	0x16024000	cs_avc_mv	
PP	0x16025000	cs_vdec_pp	
VDEC_GCON	0x16000000		VDEC global control registers
SMI_LARB1	0x16010000		SMI LARB1 control registers

6.10.4.3 VDEC Hardware Architecture

Figure 6-14 is the hardware architecture.

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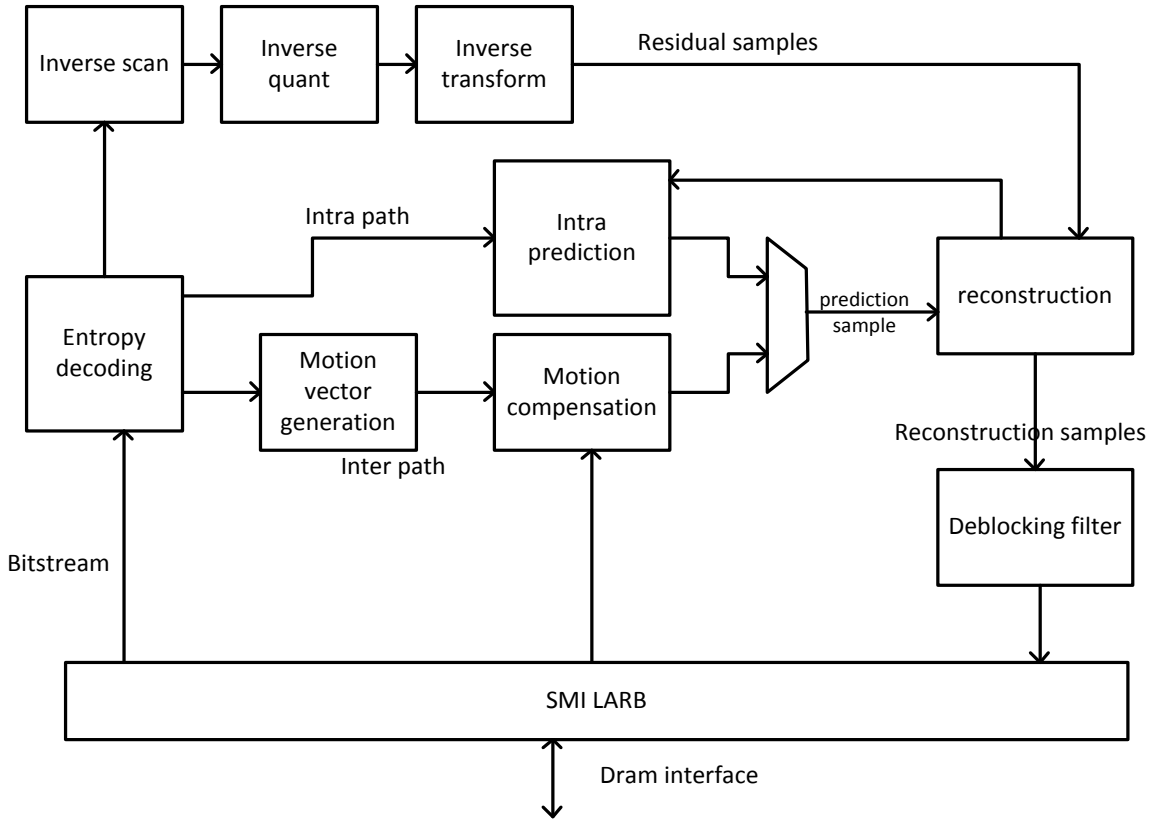

Figure 6-14. VDEC hardware architecture

6.10.4.4 Firmware Hardware Partition

Figure 6-15 is the typical decoding flow with FW/HW partition. SW takes charge frame level setting, including syntax decoded from frame header and proper DRAM buffer allocation, and triggers HW to decode the bitstream. An interrupt signal will be sent to CPU when HW finish decoding a frame and FW can reset HW and program setting for next frame if necessary. Details of FW decoding are described in section 6.10.4.5.

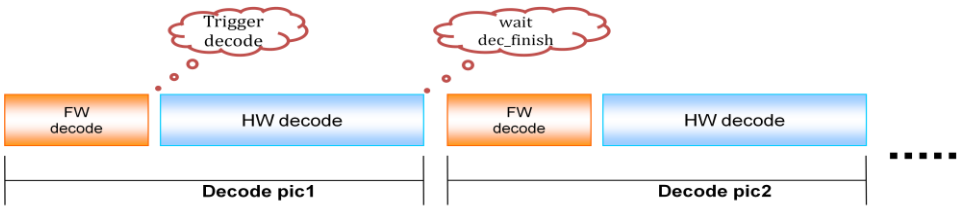

Figure 6-15. VDEC decoding flow

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6.10.4.5 FW Decoding Flow

This section describes our recommended step-by-step FW setup flow. Each step should be followed to ensure a correct decoding process.

1. Soft reset
   a. Issue reset vld_reg_66[0] = 1.
   b. Turn on VDEC related clocks.
   c. Release soft reset vld_reg_66[0] = 0.
2. Initialize Bitstream DMAs and Barrel-Shifters.
3. Decode frame layer syntax.
4. Maintain DPB buffer.
5. HW registers setting
   a. SQT setting
   b. MV setting
   c. MC setting
   d. De-blocking (PP) setting
   e. VLD setting
6. Trigger HW decoding.
7. Wait for decoding picture to finish via VDEC interrupt (HW auto turns off VDEC related clocks).

6.10.4.5.1 Software Reset and Power Control Flow

Figure 6-16 describes the software reset and power control flow. Details of each step will be described in the following sections.

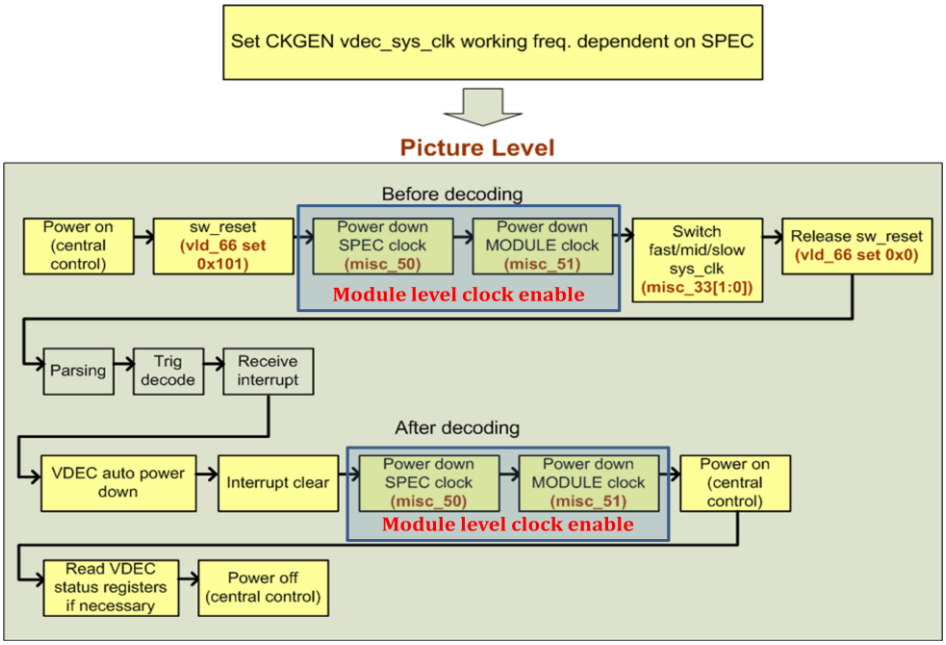

Figure 6-16. Software reset and power control

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- ✓ Power on (central control)
  - Set VDEC_GCON reg 0 bit[0] (vdec subsys clock enable) = 1.
  - Enable global clocks of VDEC (dram clock, vdec_sys clock, bus clock).
- ✓ VDEC auto power-down
  - Auto turn off dram clock, vdec_sys clock.
  - Auto set pdn_con_spec (vdec_misc_reg 50) = 32'hffffffff.
  - Auto set pdn_con_module (vdec_misc_reg 51) = 32'hffffffff.
- ✓ Interrupt clear
  - No interrupt clear from CPU
  - Use internal VDEC RISC clear int
    - VDEC_MISC reg 41
      - Bit [0] (risc_clr_int_mode) always set to 1.
      - Bit [4] (risc_int_clr): internal VDEC RISC clear int
- ✓ Power off (central control)
  - Set VDEC_GCON reg 0 bit[0] (vdec subsys clock enable) = 0

6.10.4.5.2 Turn off VDEC Auto Power Down

FW can turn off VDEC auto power-down by disabling the setting of "auto turn off dram clk, vdec sys clock" and disabling "Auto set pdn_con_spec = 32'hffffffff & Auto set pdn_con_module = 32'hffffffff".

Related register settings are:

- Disable "Auto turn off dram clock, vdec_sys clock"
  - Set VDEC_GCON reg 6 bit[0] = 1
- Disable "Auto set pdn_con_spec = 32'hffffffff & Auto set pdn_con_module = 32'hffffffff"
  - Set VDEC_MISC reg 59 bit[0] = 1

The decoding process will change after FW turns off VDEC auto power-down control. The difference is shown in Figure 6-17.

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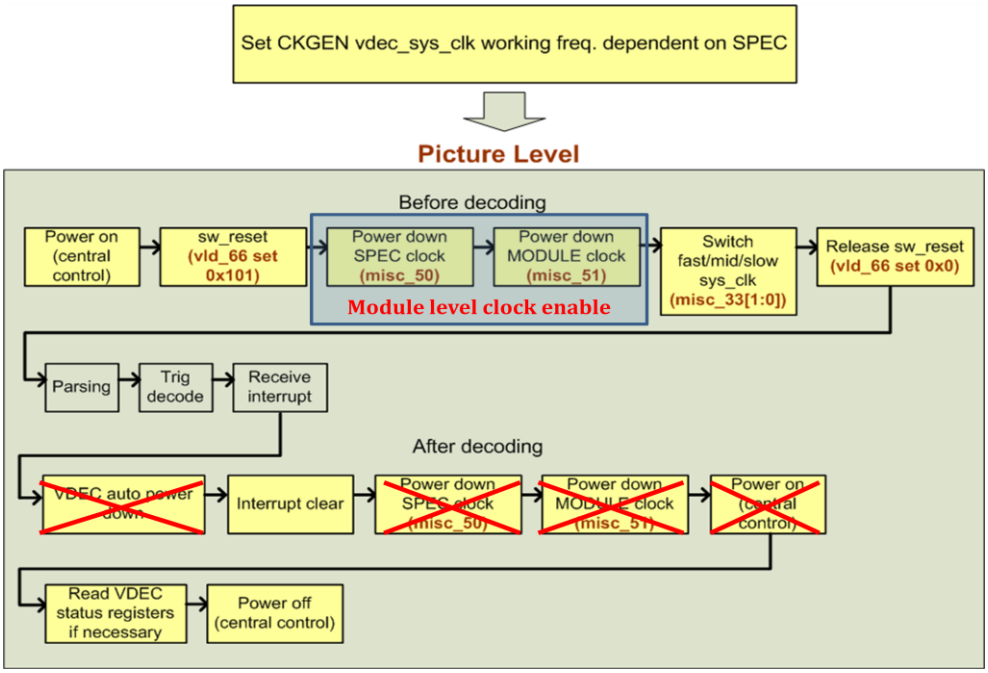

Figure 6-17. Software reset and power control (turn off VDEC auto power down)

6.10.4.5.3 Other Relative Registers about Power Control

FW can disable "Auto turn off dram clock, vdec_sys clock" when dec_error occurs by setting VDEC_GCON reg 6 bit[4] = 1.In addition, when dec_error occurs, there is **always no** "Auto set pdn_con_spec = 32'hffffffff & Auto set pdn_con_module = 32'hffffffff".

6.10.4.5.4 Clock and Power-down Setting

a. Enable global clocks of VDEC (DRAM clock, vdec_sys clock, bus clock)
   i. Set VDEC_GCON reg 0 bit[0] (vdec subsys clock enable) = 1.
b. Enable SRAMs of SMI/VDEC.
   i. ***SLEEP_IFR_PWR_CON = (**SLEEP_IFR_PWR_CON&0xffff00ff);
   ii. ***SLEEP_VDE_PWR_CON = (**SLEEP_IFR_PWR_CON&0xffff00ff);
c. Set clock gating for each standard and modules
   i. Software reset: set VLD reg 66 = 0x101
   ii. Set **pdn_con_spec** & **pdn_con_module** setting for different spec
      1. **pdn_con_spec (VDEC_MISC reg 50 (0xC8))**
         a) **pdn_con_module (VDEC_MISC reg 51 (0xCC))**
   iii. set **vdec_sys_clk_sel** for different spec :
      1. **vdec_sys_clk_sel (VDEC_MISC reg 33(0x84))**
   iv. release software reset: reset VLD reg 66 = 0x0

VDEC system clock frequent, as well as the module level power down control, depends on different specs.

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6.10.4.5.5 Interrupt Clear

In MT6750, there is no interrupt clear from CPU, i.e. interrupt clear should be achieved by FW setting up internal VDEC RISC. To perform interrupt clear, set up the following:

VDEC_MISC reg 41
- Bit [0] (risc_clr_int_mode) always set to 1
- Bit [4] (risc_int_clr): Internal VDEC RISC clear int

6.10.4.6 VDEC Break Function

This section describes the correct steps for FW to break VDEC before finishing decoding a picture.

1. Set up vdec_break.
   - Set VDEC_MISC reg 64 Bit [0] (vdec_break) = 1'b1.
2. Monitor status vdec_break_ok.
   - VDEC_MISC reg 65 Bit [0]: vdec_break_ok_0
   - VDEC_MISC reg 65 Bit [4]: vdec_break_ok_1
   - Monitor until both vdec_break_ok _0 = 1 && vdec_break_ok_1= 1.
3. Software reset
   - VLD reg 66 Bit [0]: vdec_sw_rst
   - Set vdec_sw_rst = 1, then reset vdec_sw_rst = 0
4. Turn off the clocks.
5. Finish.

6.10.5 Register Definition

See chapter 4.10 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

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6.11 H.264 Video Encoder

6.11.1 Introduction

This design is main stream H.264 video encoder. It is capable of encoding 1080P video at 30 frames per second (FPS) with promising superior video quality. This IP supports various encoding methods that satisfy basic requirements of easy software controllability. Furthermore, with advanced encoding technology, it brings astonishing high quality and low memory bandwidth requirements. It also considers the usage of portable devices and provides several power saving capabilities.

6.11.2 Features

The supported video codec and their capability are listed in the table below.

Table 6-2. Main features

H.264 encoder	Profile	High
	Level	4.1
	Speed	**1080p@30fps**

The video encoder takes DRAM as input, output and working buffer. It reads input frame buffers, executes video encoding and writes encoded bitstream to the output buffer. The driver software maintains all buffers and assigns proper values to the video encoder to allow the hardware to work correctly. Figure 6-18 shows the procedure of the video encoder. YUV420 two plane scan-line (NV12/NV21), YUV420 three plane scan-line (YV12/I420) or MTK block formats are supported.

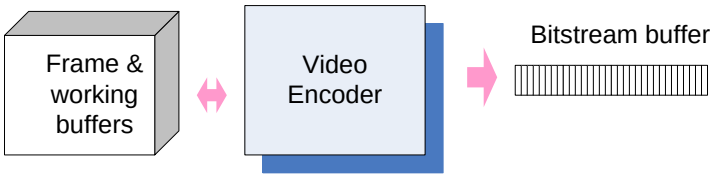

Figure 6-18. Procedure of video encoder

6.11.3 Block Diagram

Figure 6-19 is the brief IP architecture and local on-chip-bus architecture. The interface for controlling it is consisted of ARM APB bus and MediaTek proprietary SMI bus. It reports hardware event through interrupts or software polling. In addition, it adopts several SMI ports and one APB port. The video encoder is configured by software through the APB interface. As the register is configured, the sequencer will send the corresponding control signals to trigger sub-modules. DMA will acquire and store back the image data and bitstream from and to memory according to the configured address. ME will conduct motion estimation to decide motion vector for later encoding. MC will conduct motion compensation to give predicted pixel values. TQ will conduct transform and quantization operation

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and write reconstructed pixels to DB and quantized transformed coefficient to EC. DB will conduct de-blocking operation and allow the DMA to store back the processed frame as the next frame's reference frame. EC will conduct entropy encoding, and the coding can be variable length code, context based arithmetic code or context based variable length code. The encoded bitstream will be written to memory by DMA.

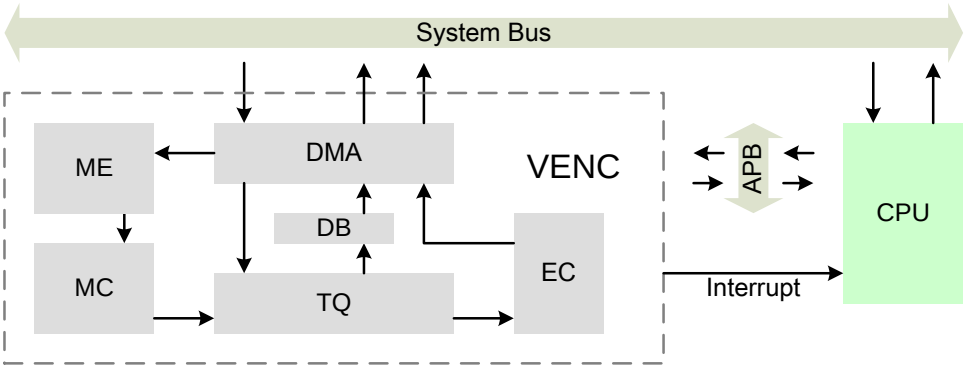

Figure 6-19. Block diagram of video encoder

6.11.4 Register Definition

See chapter 4.11 of *"MT6750 LTE-A Smartphone Application Processor Software Register Table"*.

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6.12 MFG

6.12.1 Introduction

MFG contains Mali-T860 MP2 GPU and clock/reset control logic. The Mali-T860 series of GPUs process extremely complicated graphics and perform general processing tasks assigned by the main application processor. This diagram shows the main components and interface of MFG.

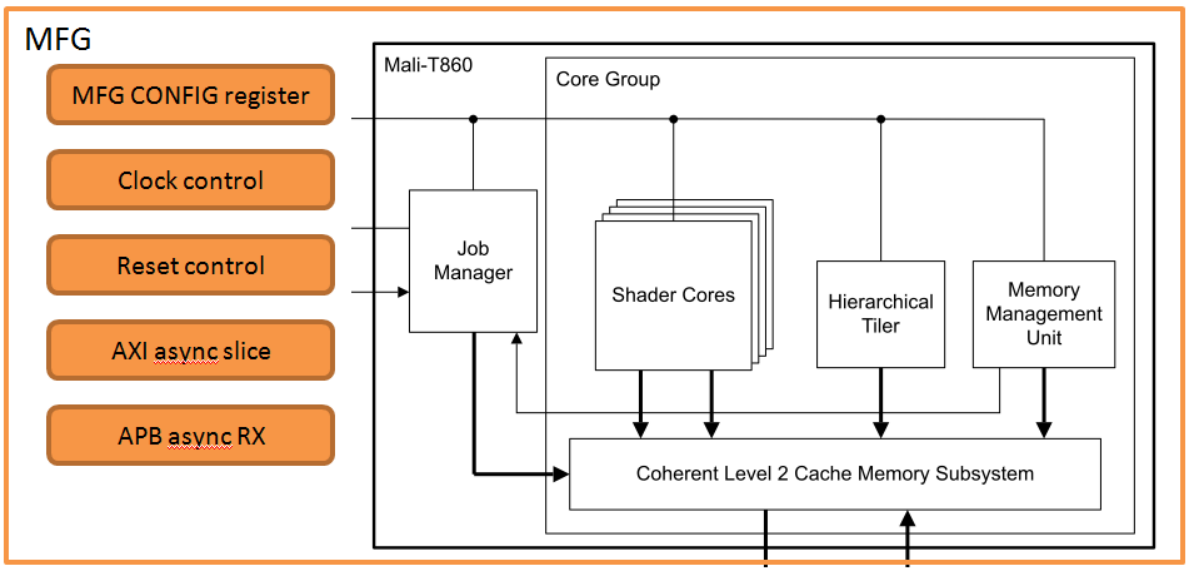

Figure 6-20. Block diagram and interface of MFG

6.12.2 Features

The Mali-T860 MP2 GPU includes the following features:

- A rich API feature set with high-performance support for both shader-based and fixed-function graphics APIs. These API graphics industry standards are:
  - *OpenGL ES 1.1 Specification* at *Khronos*
  - *OpenGL ES 2.0 Specification* at *Khronos*
  - *OpenGL ES 3.0 Specification* at *Khronos*
  - *OpenCL 1.0 Specification* at *Khronos*
  - *OpenCL 1.1 Specification* at *Khronos*
  - *OpenCL 1.2 Specification* at *Khronos*
- Anti-aliasing capabilities
- An effective core for *General Purpose computing on GPU* (GPGPU) applications
- High memory bandwidth and low power consumption for 3D graphics content.
- Image quality using double-precision FP64, and anti-aliasing.
- Frame buffer compression.
- Bus protocol
  - 128-bit AXI bus with up to read 64 outstanding and write 32 outstanding

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  - 32-bit APB bus
- Level-2 cache
  - 128KB
  - 4-way set associative
- Performance
  - Triangle rate 130M Tri/sec
  - Fill rate 1040M Pixels/sec
  - Shader rate 35 GFLOPS

6.12.3 Register Definition

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7 Analog Baseband

7.1 AP Mixedsys

7.1.1 Block Diagram

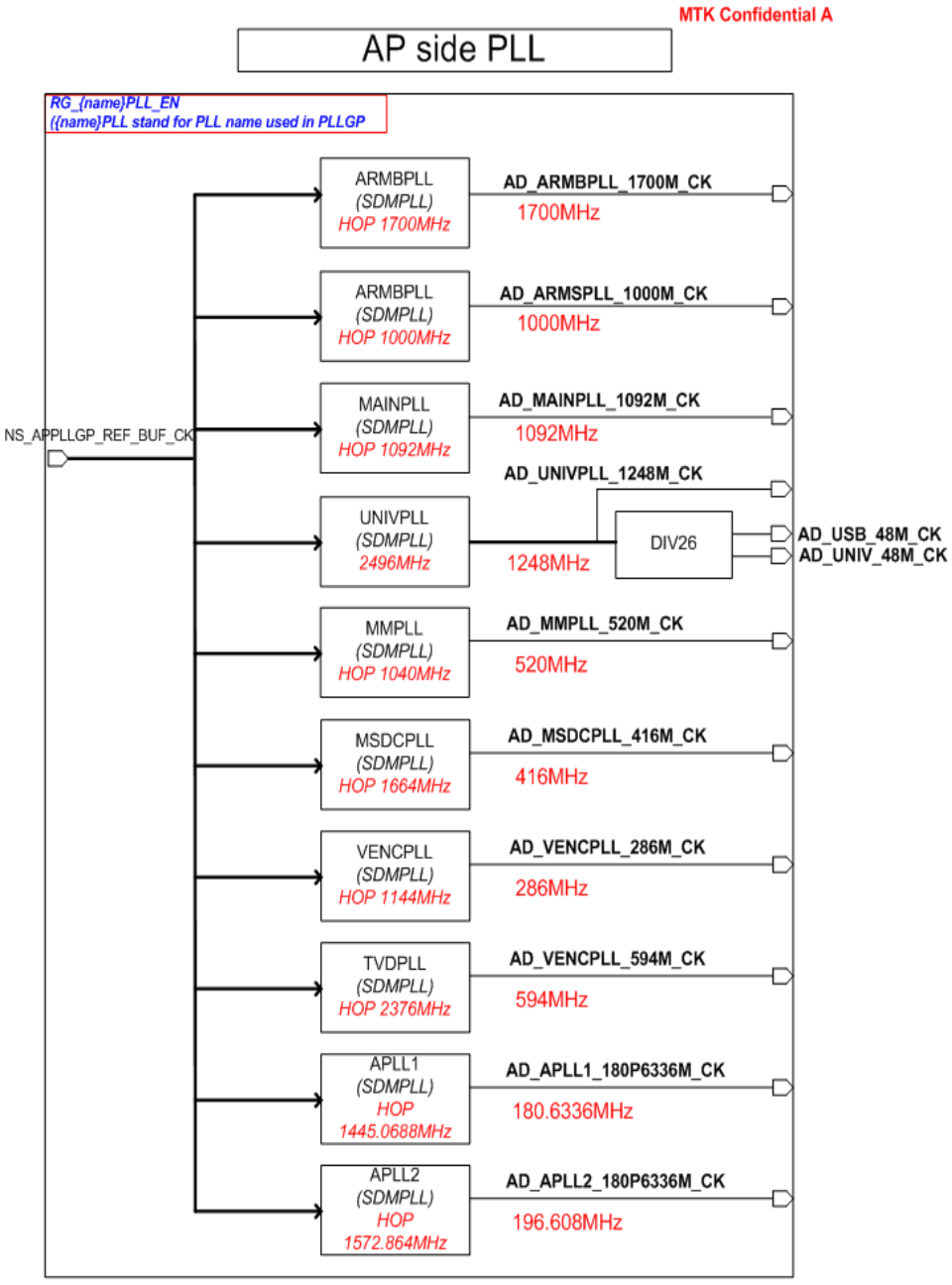

Figure 7-1. PLL block diagram

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7.1.2 Register Definition

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