# MT6809S

# P-Channel Enhancement Mode Field Effect Transistor

## **Product Summary**

- VDS = -60V
- I<sub>D</sub> = -80A (VGS= -10V)
- RDS(ON) 11 m Ω @VGS= -10V

#### Features

- Advanced Trench Process Technology.
- High Density Cell Design for Ultra Low On-Resistance.
- · Lead free product is acquired.
- RoHS Compliant.

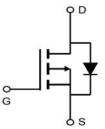
#### Applications

- Power Switching Application
- Hard switched and high frequency circuit
- UPS
- Load Switch



http://www.mtsemi.com

#### **Simplified Schematic**



#### MARKING DIAGRAM & PIN ASSIGNMENT



TO-252-2L

## Absolute Maximum Ratings (T<sub>A</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	Vds	-60	V
Gate-Source Voltage	Vgs	±20	V
Drain Current-Continuous	Ι <sub>D</sub>	-80	А
Drain Current-Continuous(T <sub>C</sub> =100°C)	I <sub>D</sub> (100℃)	-50	A
Pulsed Drain Current	I <sub>DM</sub>	-2180	A
Maximum Power Dissipation	PD	55	W
Derating factor		0.76	W/℃
Single pulse avalanche energy (Note 5)	E <sub>AS</sub>	222	mJ
Operating Junction and Storage Temperature Range	T <sub>J</sub> ,T <sub>STG</sub>	-55 To 150	°C

### **Thermal Characteristic**

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	R <sub>θJC</sub>	1.31	°C/W
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## Electrical Characteristics (Tc=25 $^{\circ}$ C unless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics	·	•	•			
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =-250µA	-60	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-60V,V <sub>GS</sub> =0V	-	-	-1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V,V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics (Note 3)	·	•	•			
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> ,I <sub>D</sub> =-250µA	-1.0	-2.6	-3.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-15A	-	11	22	mΩ
Forward Transconductance	<b>g</b> fs	V <sub>DS</sub> =-10V,I <sub>D</sub> =-20A	-	25	-	S
Dynamic Characteristics (Note4)	·	•	•			
Input Capacitance	C <sub>lss</sub>	(1 - 25)(1)(-0)(	-	7460	-	PF
Output Capacitance	C <sub>oss</sub>	$V_{DS}$ =-25V, $V_{GS}$ =0V,	-	819	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>	F=1.0MHz	-	635	-	PF
Switching Characteristics (Note 4)	·		•			•
Turn-on Delay Time	t <sub>d(on)</sub>		-	18	-	nS
Turn-on Rise Time	tr	V <sub>DD</sub> =-30V, R <sub>L</sub> =1.5Ω, V <sub>GS</sub> =-10V,R <sub>G</sub> =3Ω	-	19	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	45	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	49	-	nS
Total Gate Charge	Qg	- V <sub>DS</sub> =-30,I <sub>D</sub> =-20A, - V <sub>GS</sub> =-10V	-	79		nC
Gate-Source Charge	Q <sub>gs</sub>		-	19		nC
Gate-Drain Charge	Q <sub>gd</sub>		-	21		nC
Drain-Source Diode Characteristics	·	•	•			
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V,I <sub>S</sub> =-20A	-		-1.2	V
Diode Forward Current (Note 2)	Is		-	-	-80	A
Reverse Recovery Time	t <sub>rr</sub>	TJ = 25°C, IF =-20A	-	55		nS
Reverse Recovery Charge	Qrr	di/dt = -100A/µs(Note3)	-	65		nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

#### Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

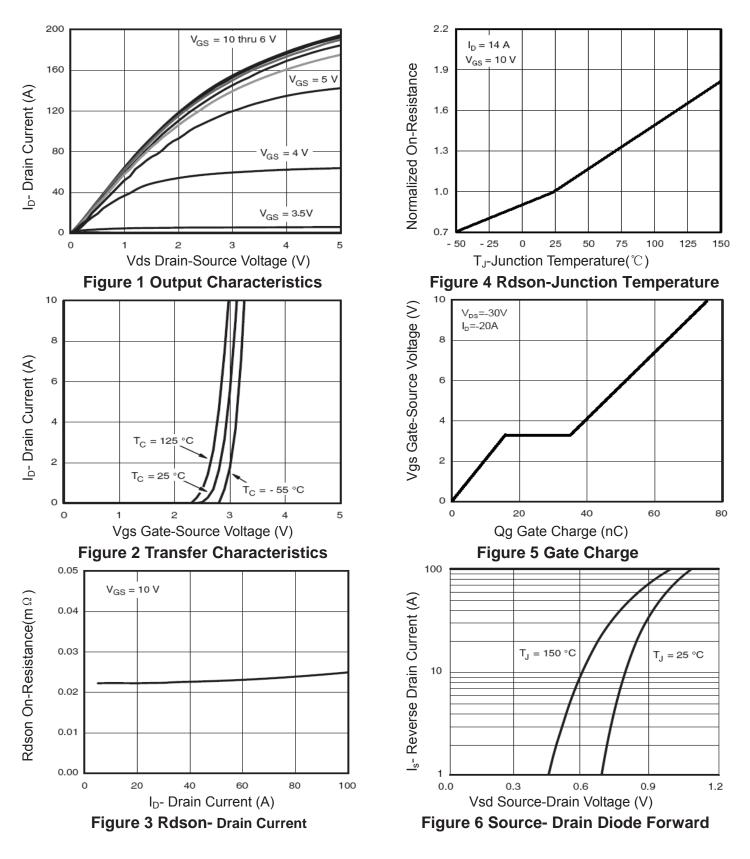
2. Surface Mounted on FR4 Board, t ≤ 10 sec.

**3.** Pulse Test: Pulse Width  $\leq$  300µs, Duty Cycle  $\leq$  2%.

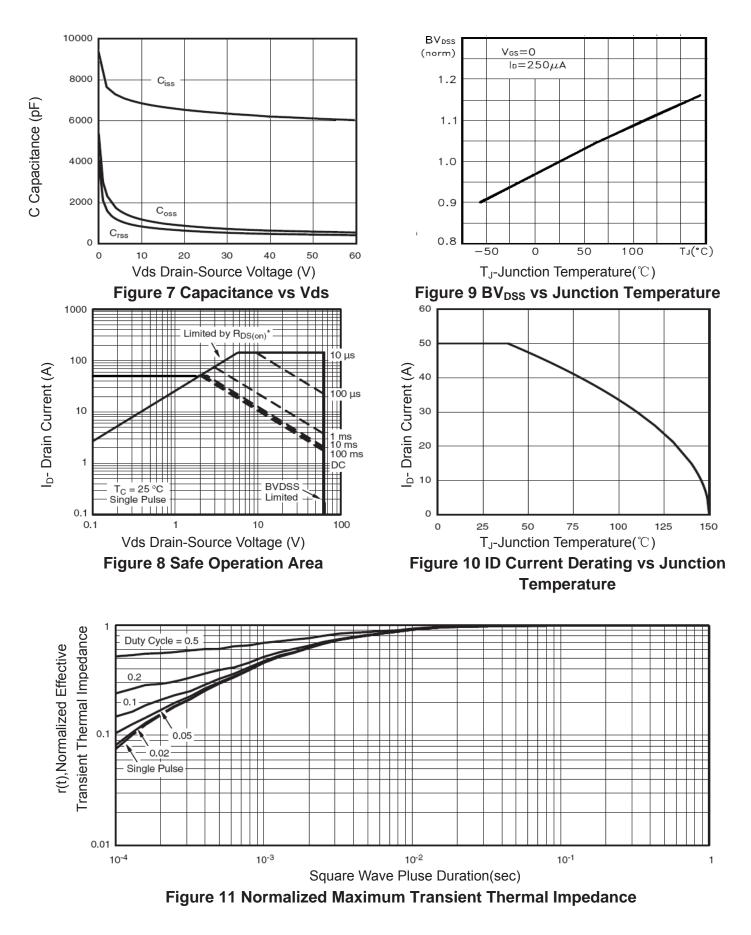
4. Guaranteed by design, not subject to production

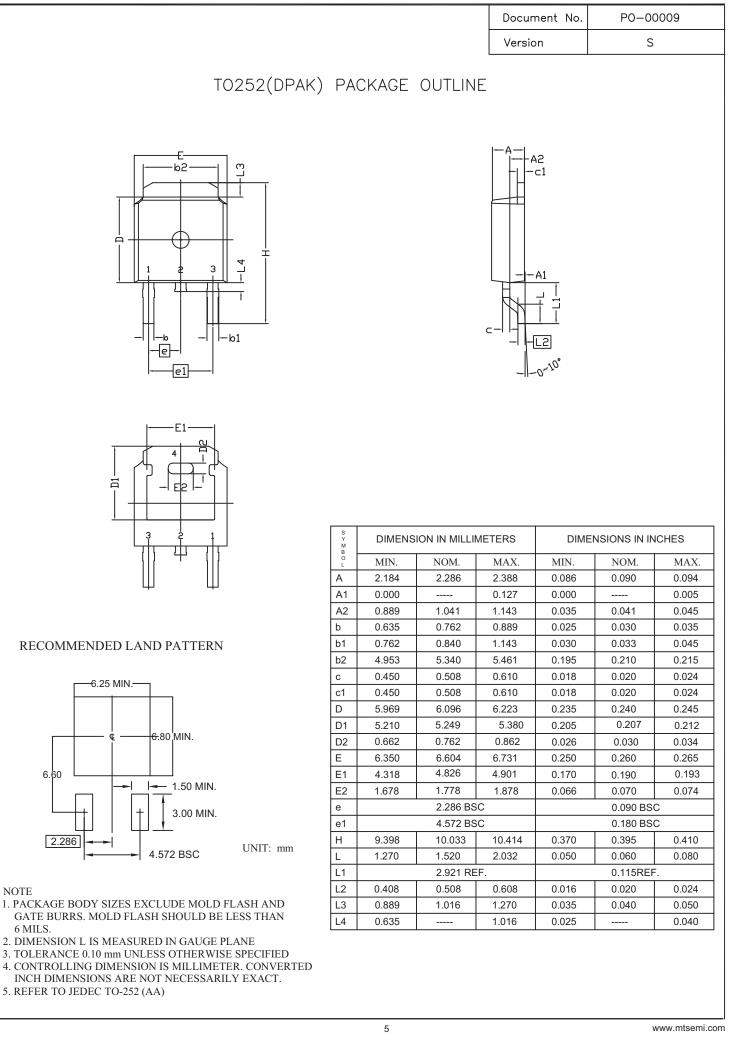
**5.** E<sub>AS</sub> condition: Tj=25  $^{\circ}$ C,V<sub>DD</sub>=-30V,V<sub>G</sub>=-10V,L=1mH,Rg=25 $\Omega$ ,I<sub>AS</sub>=38A

# **Characteristics Curve**



## **Characteristics Curve**





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