DESCRIPTION

The MT6823 is a 3W, filterless, ultra-low EMI noise, fully differential input, stereo class-D audio amplifier, which provides precise DC volume control from 24dB to -24dB with 30 steps. It is low noise, filter-free with PWM architecture, minimizing external component count, PCB area, system cost.

The chip features very low 0.1% THD+N, high 90dB SNR, and therefore offer high quality sound. MT6823 delivers up to 3W per channel into a 4Ω load with an efficiency up to 90%.

The MT6823 features a low-power consumption shutdown mode. Output short circuit and thermal overload protection prevent the device from damage during fault conditions

The high efficiency and a low shutdown current make the MT6823 an ideal choice for both battery-powered speakers and portable devices.

MT6823 integrates Maxic's unique EMI suppression technique, can work with FM tuner without extra Ferrite-bead components.

FEATURES

- 3W output at 10% THD with a 4Ω load and 5V power supply
- Fully differential inputs for both channel
- 30-steps DC volume control from -24dB to +24dB
- 2.5V~5V single supply operation
- Filterless and ultra-low EMI, can work with FM tuner without extra Ferrite-bead components
- Less than 0.1% THD+N
- Excellent Power up/down "Pop sound" suppression
- Low quiescent current and low-power shutdown current
- Few external components to save the space and cost
- Over current/Short circuit and over temperature protection
- Available in SOP16 package (Pb-free)

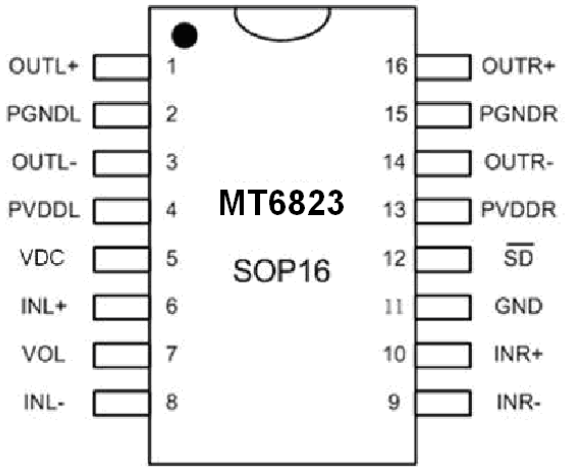
ORDERING INFORMATION

Part #	Package	Remarks
MT6823	SOP-16	Tape & Reel 2500pcs

APPLICATIONS

- Mobile phone
- Portable audio product
- Portable media player
- Personal navigation device
- Video game
- Cordless phone

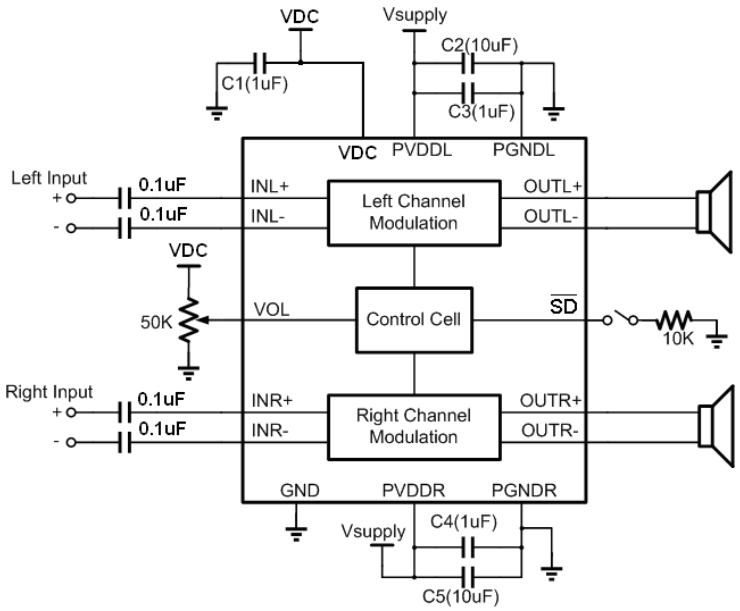
PIN CONFIGURATIONS



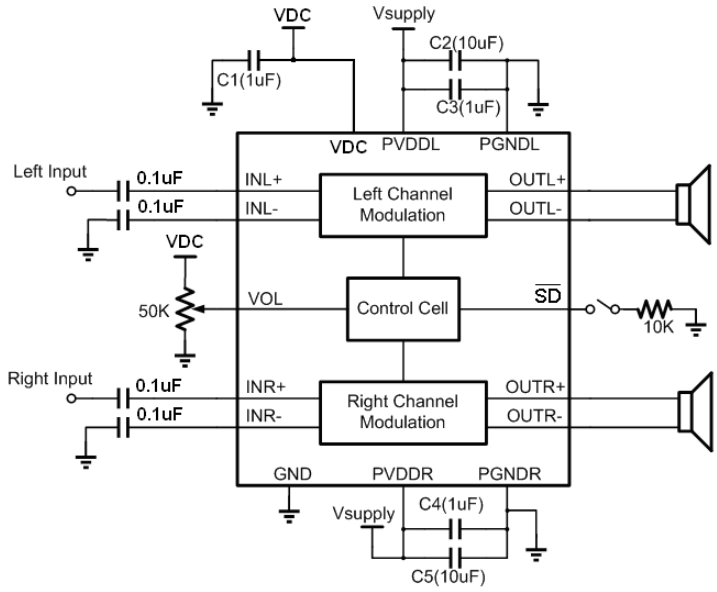
PIN DESCRIPTIONS

Pin#	Symbol	Function
1	OUTL+	Left channel positive output
2	PGNDL	Left channel ground
3	OUTL-	Left channel negative output
4	PVDDL	Left channel power supply
5	VDC	DC volume control reference voltage
6	INL+	Left channel non-inverting input
7	VOL	DC volume control for gain setting
8	INL-	Left channel inverting input
9	INR-	Right channel inverting input
10	INR+	Right channel non-inverting input
11	GND	Analog ground
12	$\overline{SD}$	Shutdown pin(active low)； Internal has a 300kohm resistor pull to VDD.
13	PVDDR	Right channel power supply
14	OUTR-	Right channel negative output
15	PGNDR	Right channel ground
16	OUTR+	Right channel positive output

TYPICAL APPLICATION CIRCUITS



MT6823: Differential Input Application Circuit



MT6823: Single-Ended Input Application Circuit

Note: C1~C5 are ceramic capacitor and should be put as close to MT6823 as possible!

ABSOLUTE MAXMUM RATINGS

VDD	Supply voltage	In active mode	–0.3 V to 5.5 V
		In $\overline{SD}$ mode	–0.3 V to 5.5 V
VI	Input voltage		–0.3 V to VDD + 0.3 V
	Continuous total power dissipation		See Dissipation Rating Table
TJ	Operating junction temperature		–40°C to 150°C
Tstg	Storage temperature		–65°C to 150°C
	Lead temperature from case for 10 seconds		260°C

THERMAL CHARACTERISTIC

Symbol	Description	Value	Units
θJA	Maximum Thermal Resistance	80	°C/W

RECOMMENTED OPERATING CONDITIONS

			MIN	MAX	UNIT
VDD	Supply voltage		2.5	5	V
VIH	High-level input voltage	$\overline{SD}$	1.3	VDD	V
VIL	Low-level input voltage	$\overline{SD}$	0	0.35	V
VIC	Common mode input voltage range	VDD = 2.5V - 5V	0.5	VDD–0.8	V
T_A	Operating free-air temperature		–40	85	°C

ELECTRICAL CHARACTERISTICS

TA = 25℃ (unless otherwise noted)

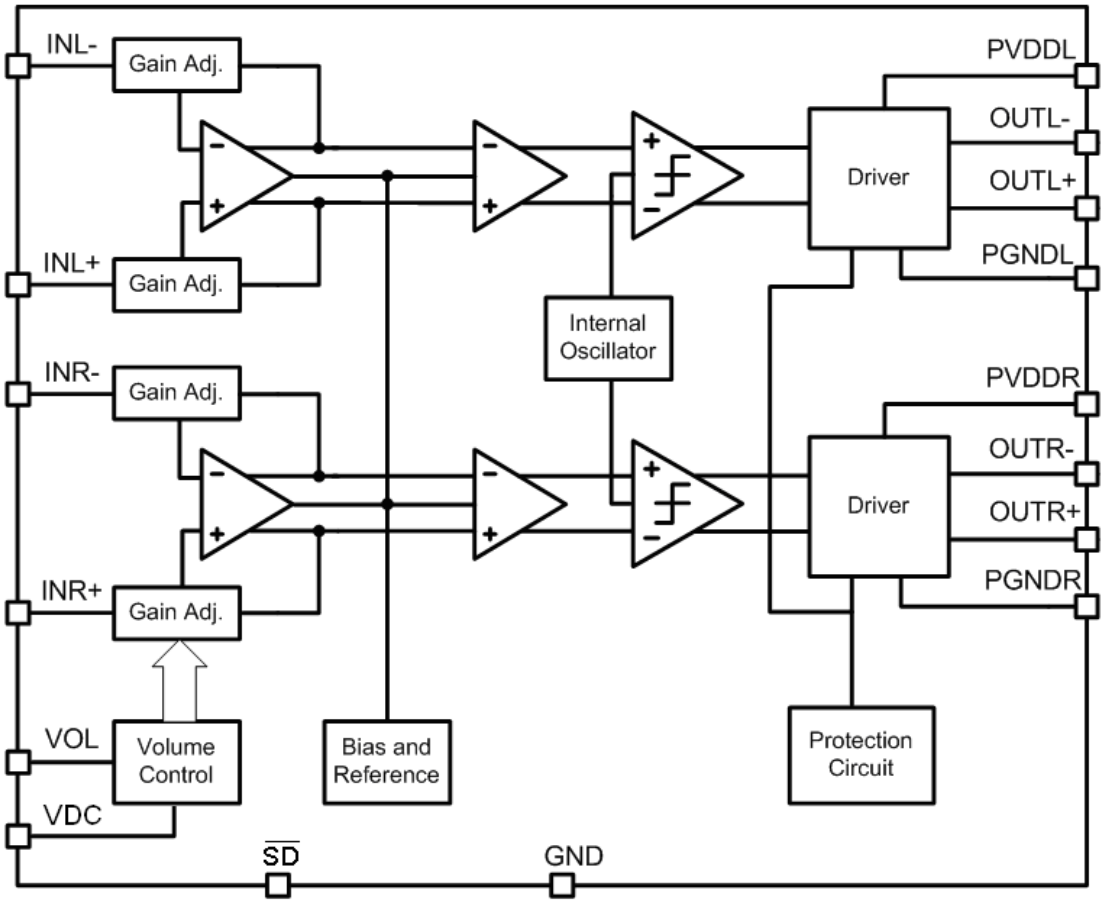
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
|VOS|	Output offset voltage	Inputs AC grounded, VDD = 2.5 V to 5 V		2	19	mV
|IIH|	High-level input current	VDD = 5.0 V, VI = 5.3 V			50	μA
|IIL|	Low-level input current	VDD = 5.0 V, VI = –0.3 V			5	μA
I(Q)	Quiescent current	VDD = 5.0 V, no load		10		mA
		VDD = 3.6 V, no load		6.5		
		VDD = 2.5 V, no load		5.3		
I(SD)	Shutdown current	V($\overline{SD}$)= 0.35 V, VDD = 3.6 V		10		μA
r_{DSON}(P)	Static drain-source on-state resistance	VDD = 2.5 V		715		mΩ
		VDD = 3.6 V		540		
		VDD = 5.0 V		490		
r_{DSON}(N)	Static drain-source on-state resistance	VDD = 2.5 V		720		mΩ
		VDD = 3.6 V		550		
		VDD = 5.0 V		510		
	Output impedance in SHUTDOWN mode	V($\overline{SD}$) = 0.35 V		>1		kΩ
f(sw)	Switching frequency	VDD = 2.5 V to 5 V		300		kHz
	Gain	See DC volume control table in page13				dB
R_{UP_SD}	Resistance from $\overline{SD}$ to VDD			300		kΩ

OPERATING CHARACTERISTICS

TA = 25℃ (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
PO	Output power (per channel)	THD + N = 10%, f = 1 kHz, RL = 4 Ω	VDD = 5 V		3.04		W
			VDD = 3.6 V		1.69		
			VDD = 2.5 V		0.73		
		THD + N = 1%, f = 1 kHz, RL = 4 Ω	VDD = 5 V		2.53		W
			VDD = 3.6 V		1.36		
			VDD = 2.5 V		0.59		
		THD + N = 10%, f = 1 kHz, RL = 8 Ω	VDD = 5 V		1.71		W
			VDD = 3.6 V		0.80		
			VDD = 2.5 V		0.37		
		THD + N = 1%, f = 1 kHz, RL = 8 Ω	VDD = 5 V		1.37		W
			VDD = 3.6 V		0.65		
			VDD = 2.5 V		0.30		
THD+N	Total harmonic distortion plus noise	VDD= 5V, PO=1W, RL=8Ω, f=1kHz			0.10%		
		VDD= 3.6V, PO=0.5 W, RL=8 Ω, f = 1kHz			0.12%		
		VDD=2.5V,PO=200mW, RL = 8 Ω, f = 1kHz			0.15%		
PSRR	Supply ripple rejection ratio	VDD = 3.6 V, Inputs ac-grounded with Ci=2μF	f=217Hz, V(ripple)=0.2Vpp		-65		dB
SNR	Signal-to-noise ratio	VDD = 5V, PO = 1W, RL = 8Ω			91		dB
Cs	Crosstalk	f = 1kHz			-76		dB
CMRR	Common mode rejection ratio	VDD = 3.6V, VIC = 1Vpp	f = 217Hz		–75		dB
	Start-up time from shutdown	VDD = 3.6V			80		ms

BLOCK DIAGRAM



TYPICAL OPERATING CHARACTERISTICS (TA=25°C)

THD+N vs. Output Power

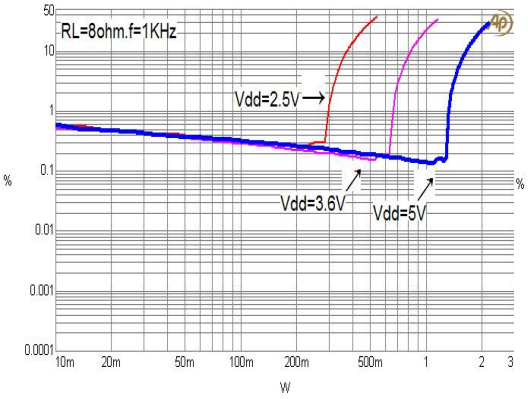


Fig. 1

THD+N vs. Output Power

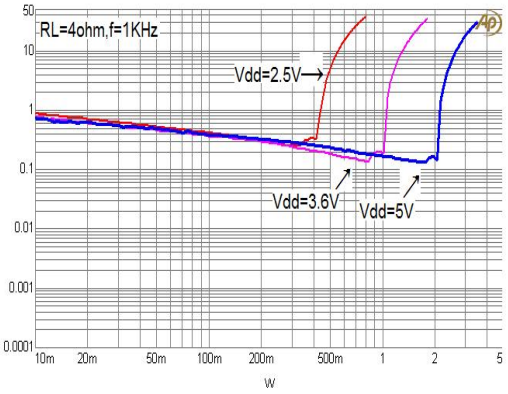


Fig. 2

THD+N vs. Frequency

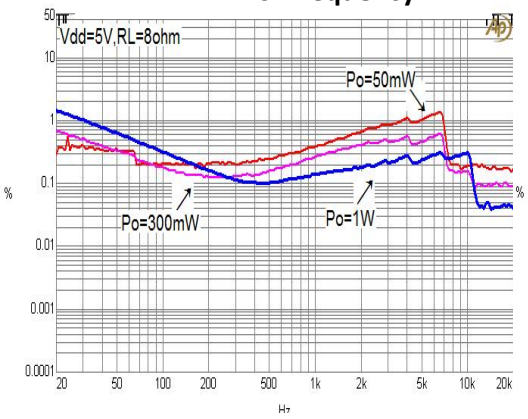


Fig. 3

THD+N vs. Frequency

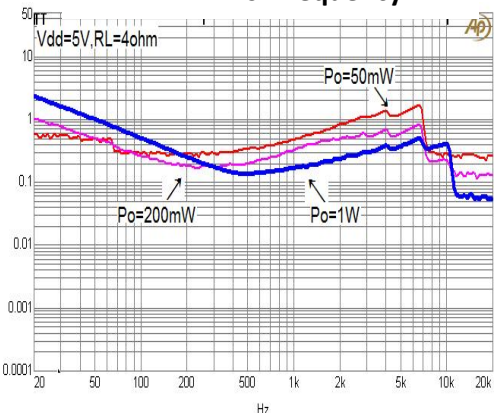


Fig. 4

THD+N vs. Frequency

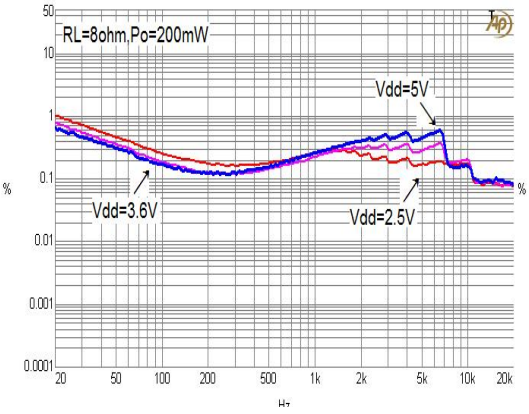


Fig. 5

THD+N vs. Frequency

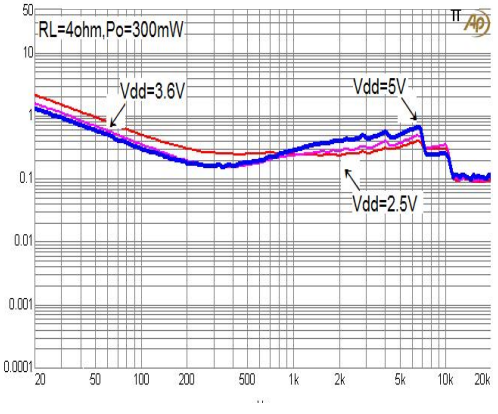


Fig. 6

Frequency Response

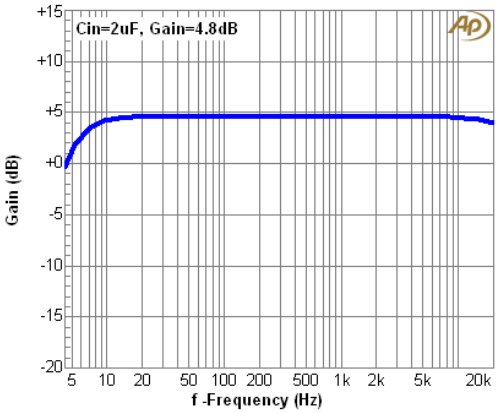


Fig. 7

Noise Floor

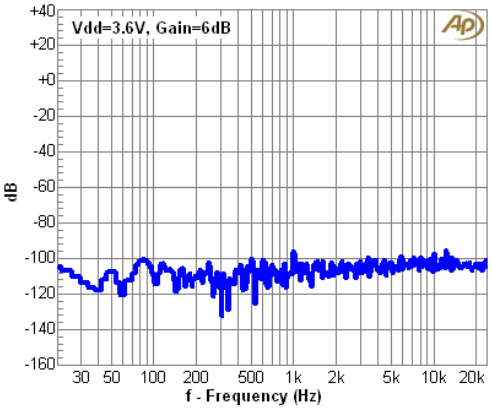


Fig. 8

PSRR vs. Frequency

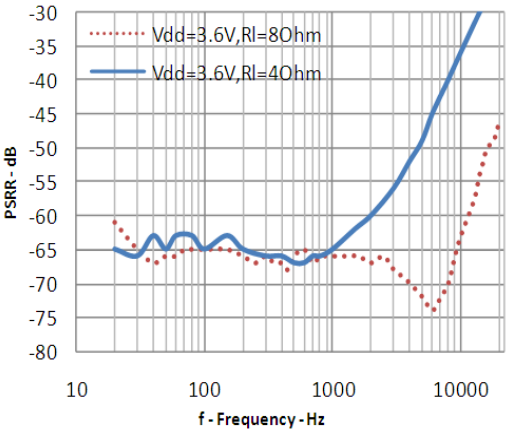


Fig. 9

CMRR vs. Frequency

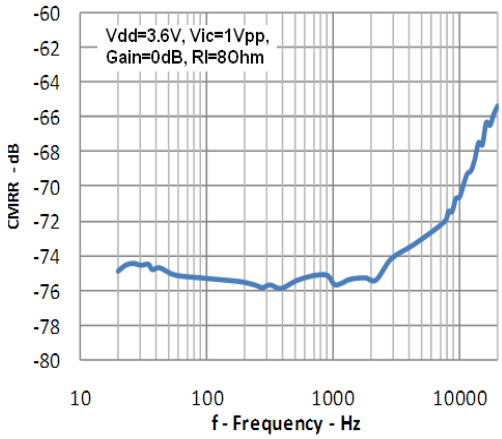


Fig. 10

Quiescent Current vs. Supply Voltage

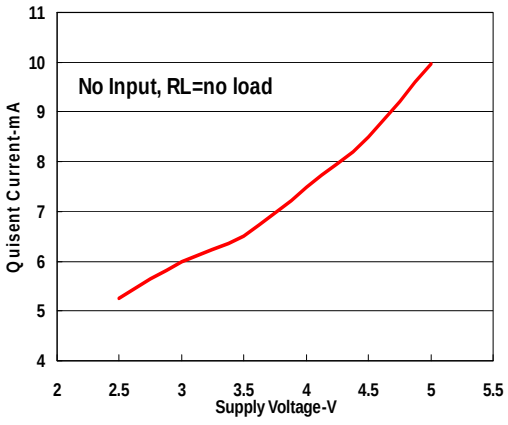


Fig. 11

Cross-talk vs. Frequency

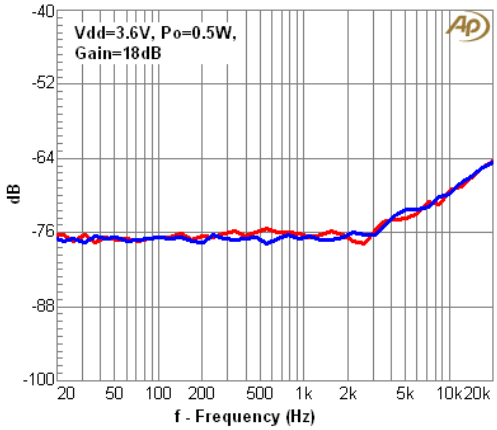


Fig. 12

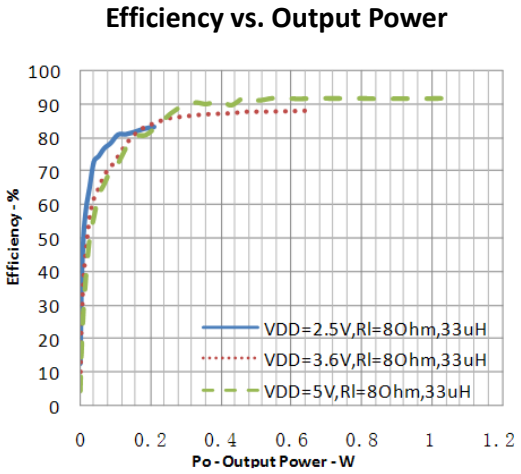


Fig. 13

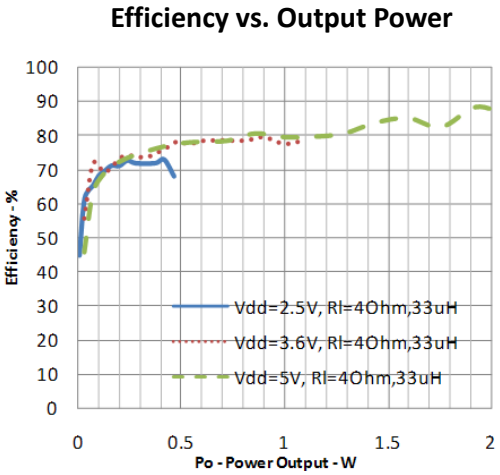


Fig. 14

APPLICATION INFORMATION

- **Inputs Setting**

MT6823: Fully differential input

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the MT6823 with a differential source, connect the positive lead of the audio source to the INL+/INR+ input through DC-cut capacitors (Ci) and the negative to the INL-/INR- input through DC-cut capacitors (Ci), as Fig.15 shows.

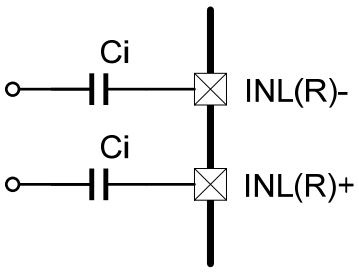


Fig.15. MT6823: Differential Input

If there is one channel unused, input pins of the unused channel side, should be connected to each other and connected to GND through a capacitor as Fig.16.

MT6823: Single-ended input

MT6823 is also can be used for single-end operation, see Fig.17, ac ground either input through a capacitor and apply the audio signal to the remaining input, and the unused input should be ac-grounded at the audio source instead of at the device input for best noise performance.

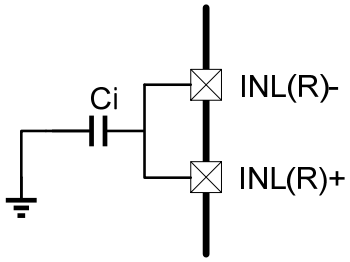


Fig.16. MT6823: Unused Channel Side

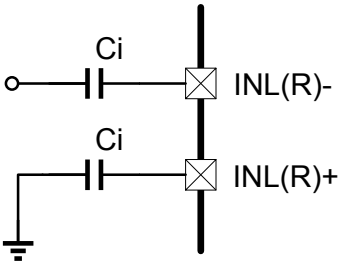


Fig.17. MT6823: Single-ended Input

- **Shut down Mode**

The MT6823 provides a shutdown mode for reduce supply current to the absolute minimum level during periods of non-use for battery-power conservation. The $\overline{SD}$ input pin should be held high during normal operation when the amplifier is in use. Pulling $\overline{SD}$ low causes the outputs to mute and the amplifier to enter a low-current state. $\overline{SD}$ pin internally has a 300 KΩ resistor pull up to VDD. So, this pin can be floating for normal operation.

- **DC volume control**

The MT6823 has an internal stereo volume control whose setting is a function of the DC voltage applied to the VOL input pin, which is reference to and should not exceed VDC (Pin5). The volume control consists of 30 steps that are individually selected by a variable DC voltage level on the VOL control pin. The range of the steps, controlled by the DC voltage, is from -24dB to 24dB.

Table 1 lists the voltage on the VOL pin and the corresponding gain. The volume control circuitry of the MT6823 is internally referenced to the VDC (Pin5) and GND. Any common-mode noise between the VOL terminal and these terminals will be sensed by the volume control circuitry. If the noise exceeds the step size voltage, the gain will change. In order to minimize this effect, care must be taken to ensure the signal driving the VOL terminal is always referenced to the VDC and GND of the MT6823, as Fig.18 shows.

There are three possible DC volume control circuitry:

(1) Using potentiometer, as shown in Fig.18a. The DC control signal is generated by the resistor divider from VDC. VDC directly connects the MT6823 Pin5.

(2) Using DAC (digital-to-analog converter), as shown in Fig.18b. The DC control signal is generated by a DAC, therefore, the MT6823's VDC must share the same power with the DAC.

(3) PWM control. The DC volume control signal is RC filtered from a PWM signal, which is generated from a MCU. The gain is decided by the PWM signal duty cycle. As mentioned above, the VDC must share the same power with MCU.

The ground connection between DC volume control circuits and MT6823 should be as short as possible and separate with the power ground.

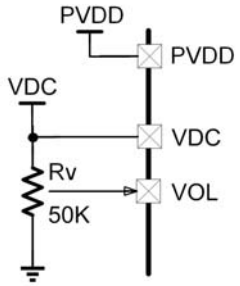


Fig.18a. Potentiometer DC volume control

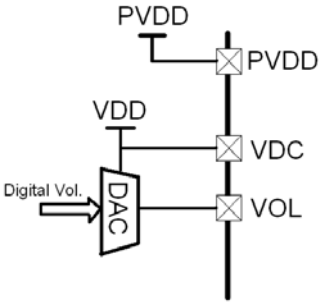


Fig.18b. DAC volume control

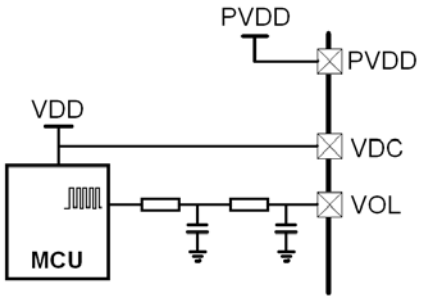


Fig.18c. PWM volume control

- **Power Supply Decoupling**

The MT6823 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) and PSRR is as low as possible. At this stage it is paramount that we acknowledge the need for separate power supplies and grounds. Noise currents in the output power stage need to be returned to output noise ground and nowhere else. Were these currents to circulate elsewhere, they may get into the power supply, the signal ground, etc, worse yet, they may form a loop and radiate noise. Any of these instances results in degraded amplifier performance. In the layout of the MT6823, the two channels amplifier should offer separate PVDD connections and PGND connections for each channel and signal currents for the inputs, reference, etc need to be returned to quite power supply VDD and GND.

As Fig.19 showing, optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent series resistance (ESR) ceramic capacitor, typically 1.0μF, placed as close as possible to the device VDD terminal works best. For filtering lower-frequency noise signals, a larger capacitor of 10μF (ceramic) or greater placed near the audio power amplifier is recommended, this capacitor serves as local storage capacitor for supplying current during large signal transients on the amplifier outputs.

- **Over Current Protection**

The MT6823 has output short circuit protection circuitry on the outputs that prevents damage to the device during output-to-output short, output-to-GND short, and output-to-VDD short. MT6823 enters the shutdown state and the outputs are disabled when detects output short. After 100ms, the chip re-enables output again. If the short-circuit condition is removed, the short-circuit flag is cleared and allows for normal operation. If the short-circuit condition is not removed, the protection circuitry actives again.

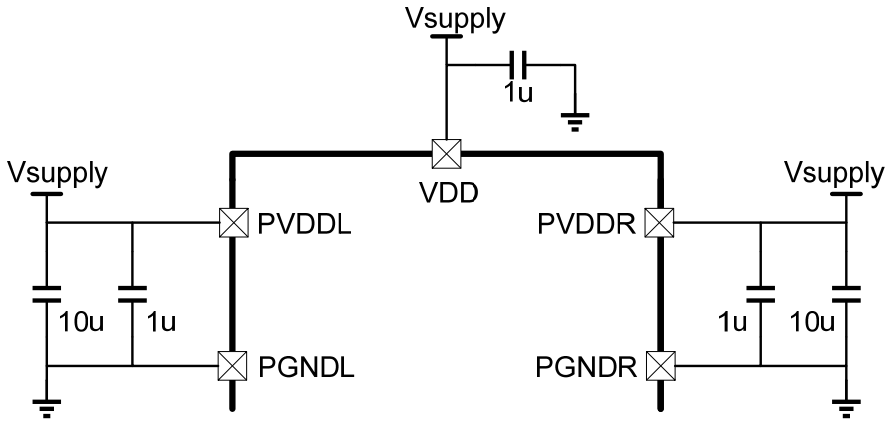


Fig.19. Power Supply Decoupling

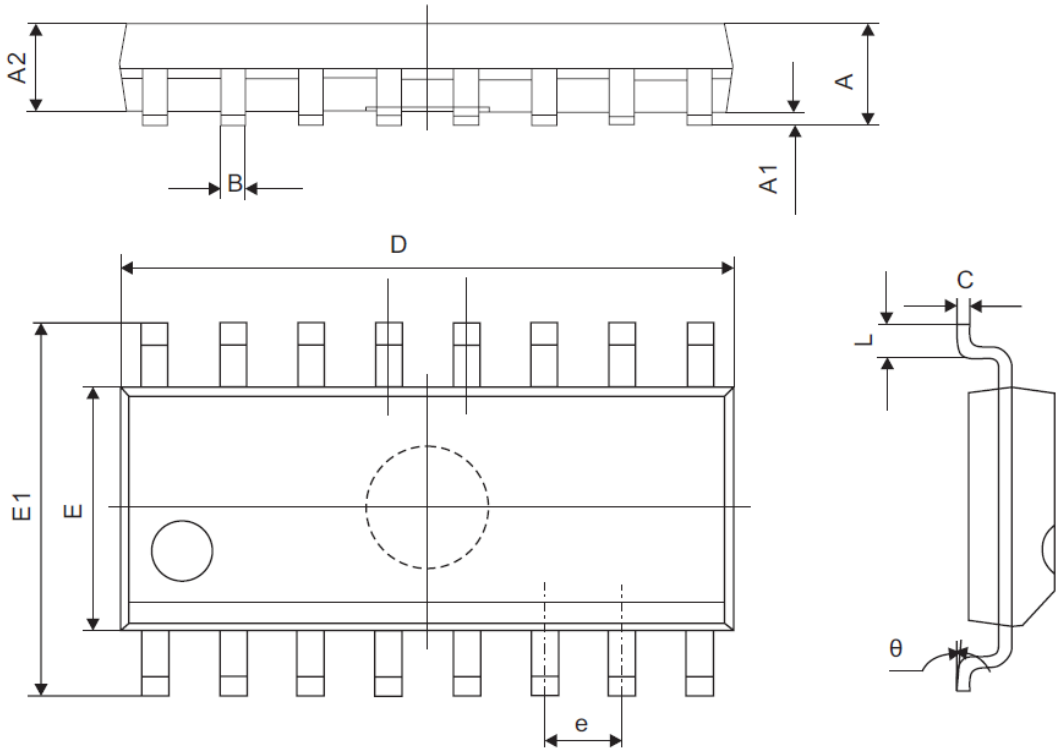
Table1. Gain Setting by DC Volume Control

Gain (dB)	Voltage (V) On VOL Pin		Gain (dB)	Voltage (V) On VOL Pin
+24	30*step~VDD		0	14*step~15*step
+22.5	29*step~30*step		-1.5	13*step~14*step
+21	28*step~29*step		-3	12*step~13*step
+19.5	27*step~28*step		-4.5	11*step~12*step
+18	26*step~27*step		-6	10*step~11*step
+16.5	25*step~26*step		-8	9*step~10*step
+15	24*step~25*step		-10	8*step~9*step
+13.5	23*step~24*step		-12	7*step~8*step
+12	22*step~23*step		-14	6*step~7*step
+10.5	21*step~22*step		-16	5*step~6*step
+9	20*step~21*step		-18	4*step~5*step
+7.5	19*step~20*step		-20	3*step~4*step
+6	18*step~19*step		-22	2*step~3*step
+4.5	17*step~18*step		-24	1*step~2*step
+3	16*step~17*step		Mute	0~1*step
+1.5	15*step~16*step			

Note: The value of 'step' is referenced to supply voltage VDD: step = VDD/37

PACKAGE DIMENSION

Package: SOP16



Symbol	Unit (mm)	
	Min	Max
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
B	0.330	0.510
C	0.190	0.250
D	9.800	10.000
E	3.800	4.000
E1	5.800	6.300
e	1.270(TYP)	
L	0.400	1.270
θ	0°	8°

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