DESCRIPTION

The MT6824 is a 3W, filterless, ultra-low EMI noise, fully differential input, stereo class-D audio amplifier, which provides digital volume control from 24dB to -24dB with 30 steps. It is low noise, filter-free with PWM architecture, minimizing external component count, PCB area, system cost.

The chip features very low 0.1% THD+N, high 90dB SNR, and therefore offer high quality sound. MT6824 delivers up to 3W per channel into a 4Ω load with an efficiency up to 90%.

The MT6824 features a low-power consumption shutdown mode. Output short circuit and thermal overload protection prevent the device from damage during fault conditions

The high efficiency and a low shutdown current make the MT6824 an ideal choice for both battery-powered speakers and portable devices.

MT6824 integrates Maxic's unique EMI suppression technique, can work with FM tuner without extra Ferrite-bead components.

FEATURES

- 3W output at 10% THD with a 4Ω load and 5V power supply
- Fully differential inputs for both channel
- 30-steps digital gain control from -24dB to +24dB
- Unique memory function of gain setting
- 2.5V~5V single supply operation
- Filterless and ultra-low EMI, can work with FM tuner without extra Ferrite-bead components
- Less than 0.1% THD+N
- Excellent Power up/down "Pop sound" suppression
- Low quiescent current and low-power shutdown current
- Over current/Short circuit and over temperature protection
- Available in TSSOP20 package (Pb-free)

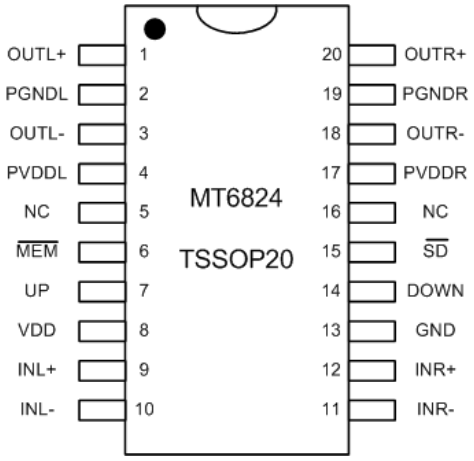
ORDERING INFORMATION

Part #	Package	Remarks
MT6824	TSSOP-20	Tube 50pcs/tube

APPLICATIONS

- Mobile phone
- Portable audio product
- Portable media player
- Personal navigation device
- Video game
- Cordless phone

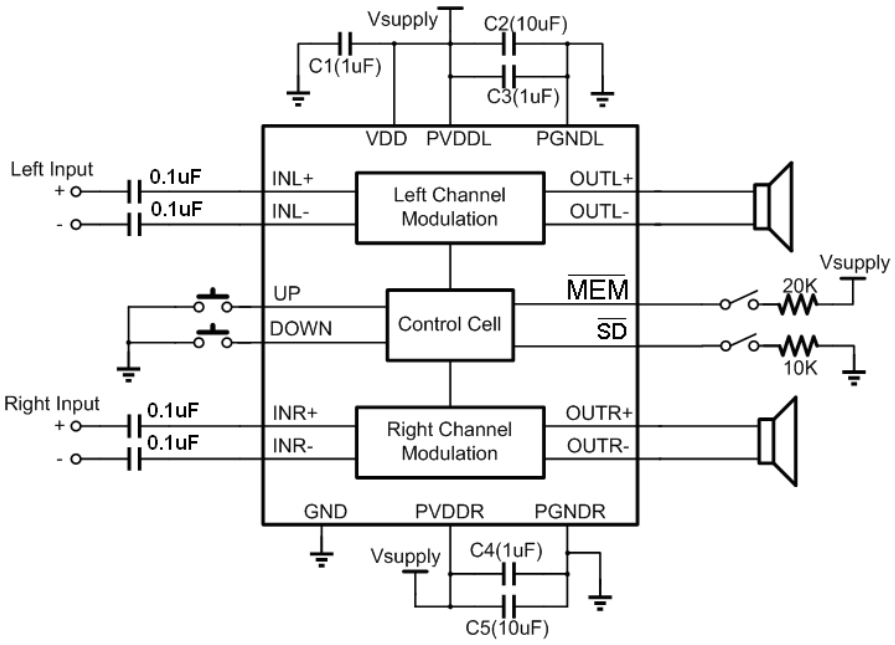
PIN CONFIGURATIONS



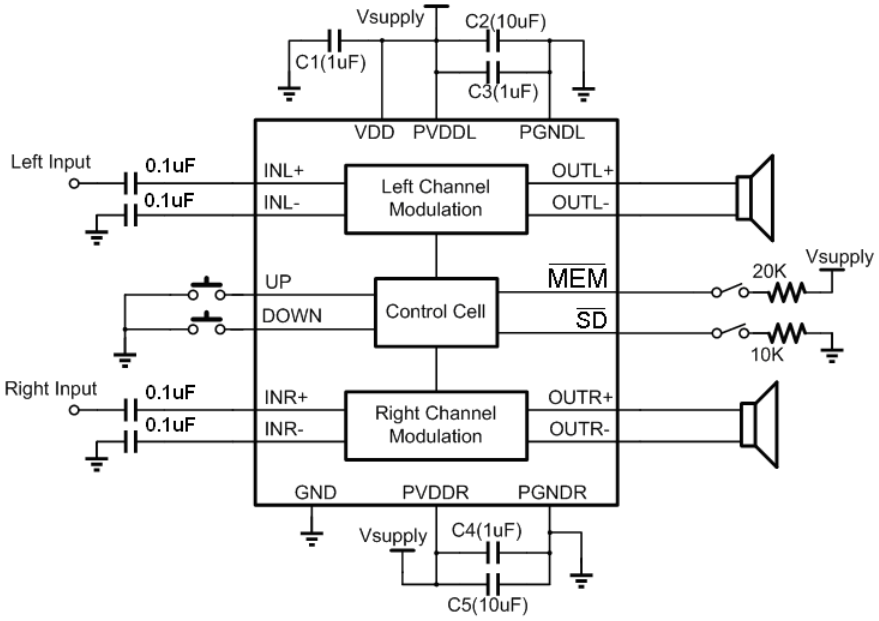
PIN DESCRIPTIONS

Pin#	Symbol	Function
1	OUTL+	Left channel positive output
2	PGNDL	Left channel ground
3	OUTL-	Left channel negative output
4	PVDDL	Left channel power supply
5	NC	No Connection
6	$\overline{\text{MEM}}$	Gain memory function select;
7	UP	Volume up control (active Low). Internal has 300Kohm resistor pull-up.
8	VDD	Analog power supply
9	INL+	Left channel noninverting input
10	INL-	Left channel inverting input
11	INR-	Right channel inverting input
12	INR+	Right channel noninverting input
13	GND	Analog ground
14	DOWN	Volume down control (active Low). Internal has 300Kohm resistor pull-up.
15	$\overline{\text{SD}}$	Shutdown pin(active low)； Internal has a 300kohm resistor pull to VDD.
16	NC	No Connection
17	PVDDR	Right channel power supply
18	OUTR-	Right channel negative output
19	PGNDR	Right channel ground
20	OUTR+	Right channel positive output

TYPICAL APPLICATION CIRCUITS



MT6824: Differential Input Application Circuit



MT6824: Single-Ended Input Application Circuit

Note: C1~C5 are ceramic capacitor and should be put as close to MT6824 as possible!

ABSOLUTE MAXMUM RATINGS

VDD	Supply voltage	In active mode	–0.3 V to 5.5 V
		In $\overline{SD}$ mode	–0.3 V to 5.5 V
VI	Input voltage		–0.3 V to VDD + 0.3 V
	Continuous total power dissipation		See Dissipation Rating Table
TJ	Operating junction temperature		–40°C to 150°C
Tstg	Storage temperature		–65°C to 150°C
	Lead temperature from case for 10 seconds		260°C

THERMAL CHARACTERISTIC

Symbol	Description	Value	Units
θJA	Maximum Thermal Resistance	80	°C/W

RECOMMENTED OPERATING CONDITIONS

			MIN	MAX	UNIT
VDD	Supply voltage		2.5	5	V
VIH	High-level input voltage	$\overline{SD}$	1.3	VDD	V
VIL	Low-level input voltage	$\overline{SD}$	0	0.35	V
VIC	Common mode input voltage range	VDD = 2.5V - 5V	0.5	VDD–0.8	V
T_A	Operating free-air temperature		–40	85	°C

ELECTRICAL CHARACTERISTICS

TA = 25℃ (unless otherwise noted)

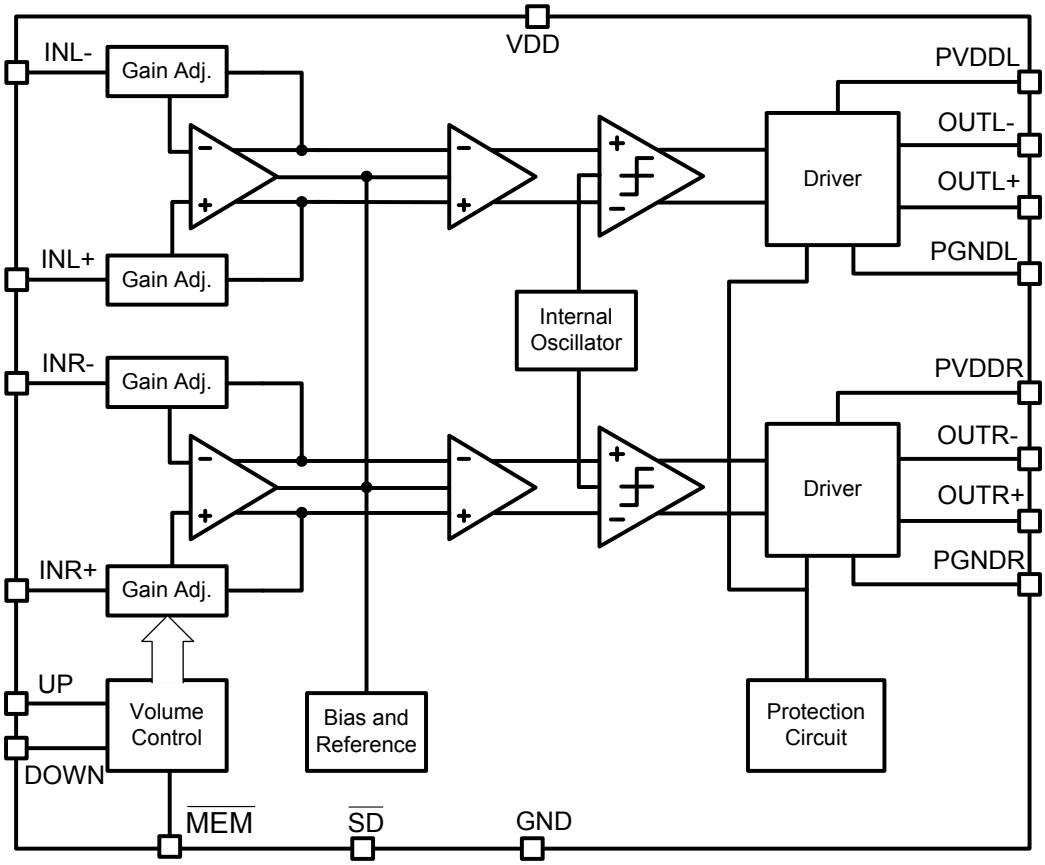
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
|VOS|	Output offset voltage	Inputs AC grounded, VDD = 2.5 V to 5 V		2	19	mV
|IIH|	High-level input current	VDD = 5.0 V, VI = 5.3 V			50	μA
|IIL|	Low-level input current	VDD = 5.0 V, VI = –0.3 V			5	μA
I(Q)	Quiescent current	VDD = 5.0 V, no load		10		mA
		VDD = 3.6 V, no load		6.5		
		VDD = 2.5 V, no load		5.3		
I(SD)	Shutdown current	V($\overline{SD}$)= 0.35 V, VDD = 3.6 V		10		μA
r_{DSON}(P)	Static drain-source on-state resistance	VDD = 2.5 V		715		mΩ
		VDD = 3.6 V		540		
		VDD = 5.0 V		490		
r_{DSON}(N)	Static drain-source on-state resistance	VDD = 2.5 V		720		mΩ
		VDD = 3.6 V		550		
		VDD = 5.0 V		510		
	Output impedance in SHUTDOWN mode	V($\overline{SD}$) = 0.35 V		>1		kΩ
f(sw)	Switching frequency	VDD = 2.5 V to 5 V		300		kHz
	Gain	See Digital volume control table in page12				dB
R_{UP_SD}	Resistance from $\overline{SD}$ to VDD			300		kΩ

OPERATING CHARACTERISTICS

TA = 25℃ (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power (per channel)	THD + N = 10%, f = 1 kHz, RL = 4 Ω	VDD = 5 V		3.04		W
			VDD = 3.6 V		1.69		
			VDD = 2.5 V		0.73		
		THD + N = 1%, f = 1 kHz, RL = 4 Ω	VDD = 5 V		2.53		W
			VDD = 3.6 V		1.36		
			VDD = 2.5 V		0.59		
		THD + N = 10%, f = 1 kHz, RL = 8 Ω	VDD = 5 V		1.71		W
			VDD = 3.6 V		0.80		
			VDD = 2.5 V		0.37		
		THD + N = 1%, f = 1 kHz, RL = 8 Ω	VDD = 5 V		1.37		W
			VDD = 3.6 V		0.65		
			VDD = 2.5 V		0.30		
THD+N	Total harmonic distortion plus noise	VDD= 5V, PO=1W, RL=8Ω, f=1kHz			0.10%		
		VDD= 3.6V, PO=0.5 W, RL=8 Ω, f = 1kHz			0.12%		
		VDD=2.5V,PO=200mW, RL = 8 Ω, f = 1kHz			0.15%		
PSRR	Supply ripple rejection ratio	VDD = 3.6 V, Inputs ac-grounded with Ci=2μF	f=217Hz, V(ripple)=0.2Vpp		-65		dB
SNR	Signal-to-noise ratio	VDD = 5V, PO = 1W, RL = 8Ω			91		dB
Cs	Crosstalk	f = 1kHz			-76		dB
CMRR	Common mode rejection ratio	VDD = 3.6V, VIC = 1Vpp	f = 217Hz		–75		dB
	Start-up time from shutdown	VDD = 3.6V			12		ms

BLOCK DIAGRAM



TYPICAL OPERATING CHARACTERISTICS (TA=25°C)

THD+N vs. Output Power

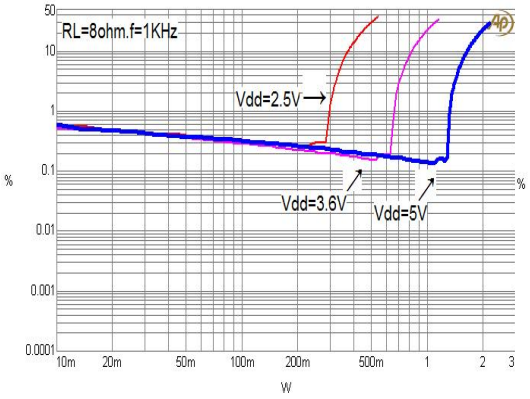


Fig.1

THD+N vs. Output Power

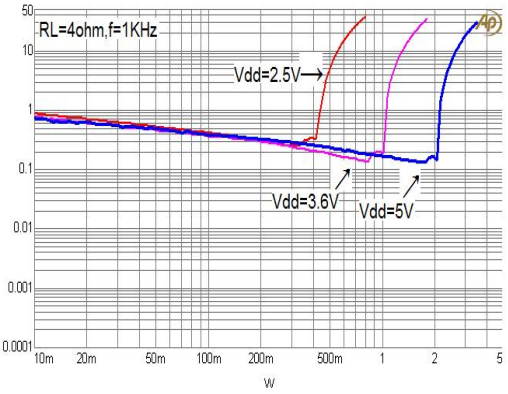


Fig.2

THD+N vs. Frequency

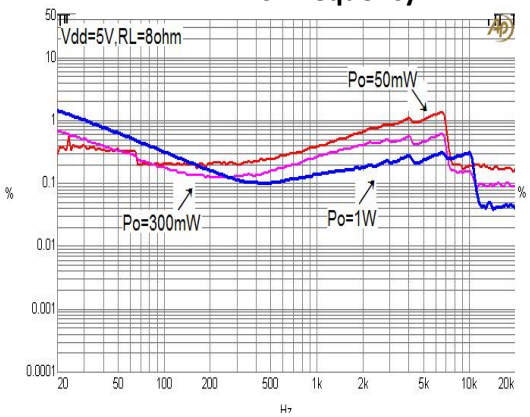


Fig.3

THD+N vs. Frequency

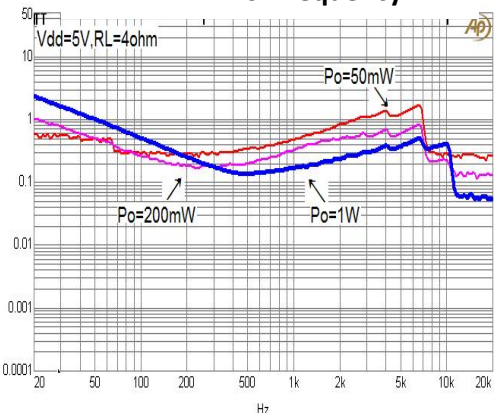


Fig.4

THD+N vs. Frequency

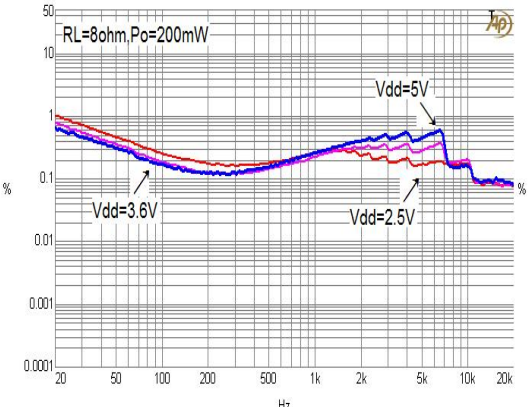


Fig.5

THD+N vs. Frequency

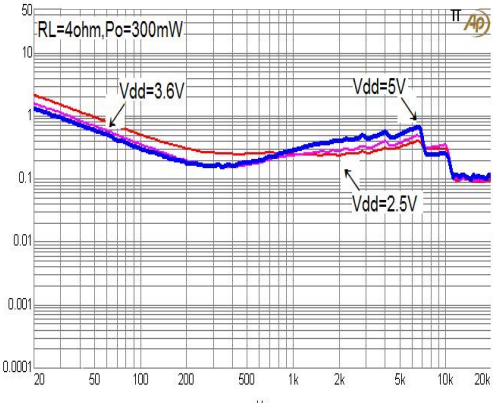


Fig.6

Frequency Response

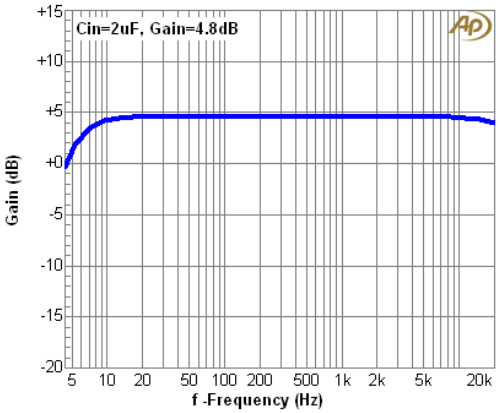


Fig.7

Noise Floor

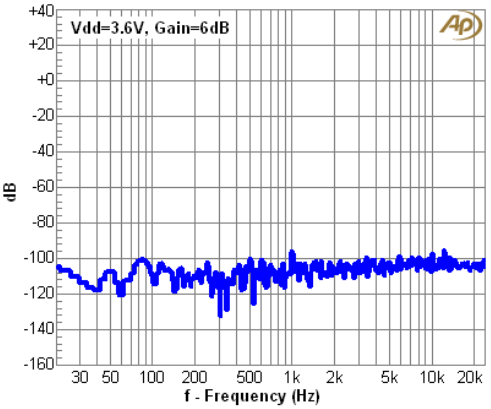


Fig.8

PSRR vs. Frequency

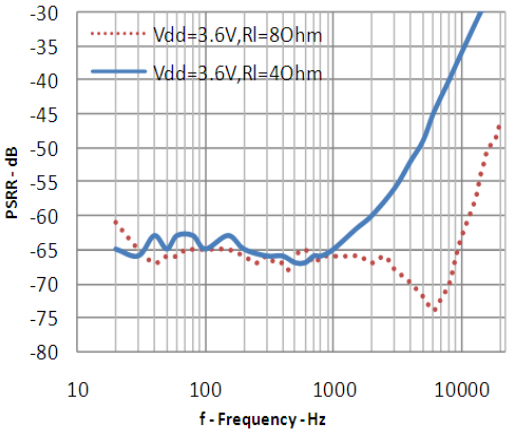


Fig.9

CMRR vs. Frequency

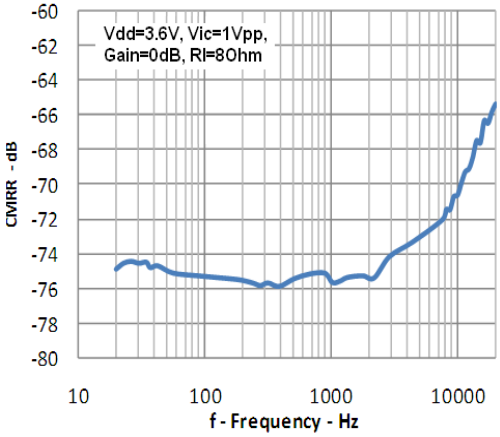


Fig.10

Quiescent Current vs. Supply Voltage

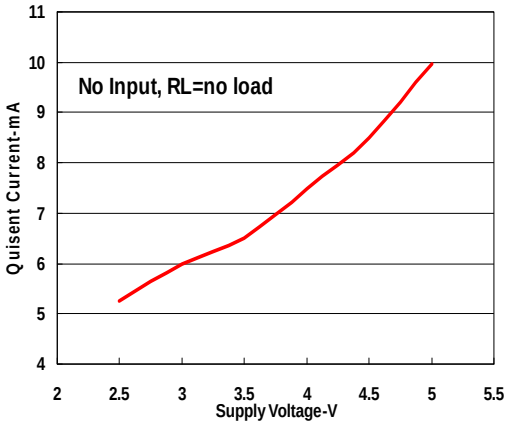


Fig.11

Cross-talk vs. Frequency

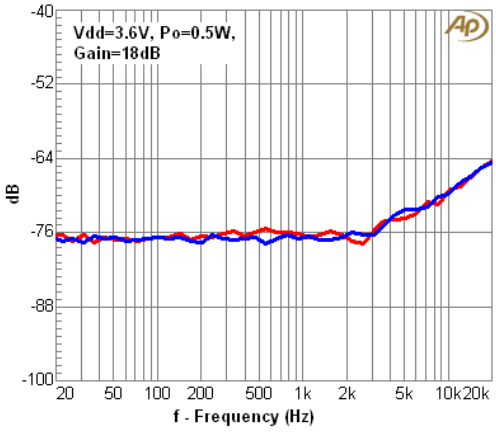


Fig.12

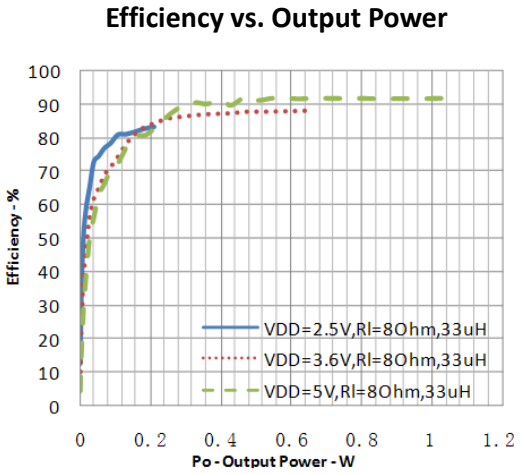


Fig.13

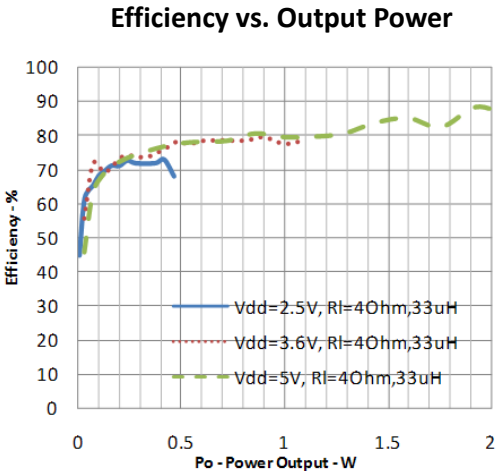


Fig.14

APPLICATION INFORMATION

- Inputs Setting

MT6824: Fully differential input

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the MT6824 with a differential source, connect the positive lead of the audio source to the INL+/INR+ input through DC-cut capacitors (Ci) and the negative to the INL-/INR- input through DC-cut capacitors (Ci), as Fig.15 shows.

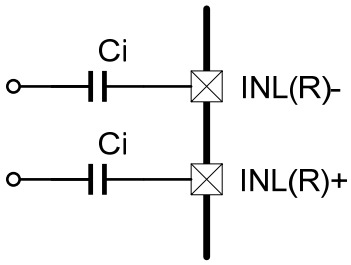


Fig.15. MT6824: Differential Input

If there is one channel unused, input pins of the unused channel, should be connected to each other and connected to GND through a capacitor as Fig.16.

MT6824: Single-ended input

MT6824 is also can be used for single-end operation, see Fig.17, ac ground either input through a capacitor and apply the audio signal to the remaining input, and the unused input should be ac-grounded at the audio source instead of at the device input for best noise performance.

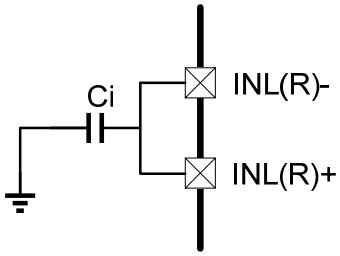


Fig.16. MT6824: Unused Channel

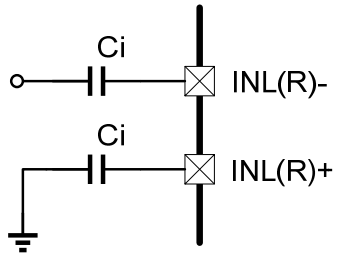


Fig.17. MT6824: Single-ended Input

- Shut down Mode

The MT6824 provides a shutdown mode for reduce supply current to the absolute minimum level during periods of non-use for battery-power conservation. The $\overline{SD}$ input pin should be held high during normal operation when the amplifier is in use. Pulling $\overline{SD}$ low causes the outputs to mute and the amplifier to enter a low-current state. $\overline{SD}$ pin internally has a 300 KΩ resistor pull up to VDD. So, this pin can be floating for normal operation.

- Digital Gain control

The MT6824 features a digital volume control which consists of the UP, DOWN and $\overline{MEM}$ pins. Volume changes are effected by toggling either the UP or DOWN pins with a logic low. After a period of 90ms with either the UP or DOWN pins held low, the volume will change to the next specified step. The delay allows the user to pull the UP or DOWN terminal low once for one volume change, or hold down to ramp several volume changes. The delay is optimally configured for push button volume control.

If either the UP or DOWN pin remains low after the first volume transition the volume will change again, but this time after 460ms. And then the followed transition occurs at 173ms for each volume transition. This is intended to provide the user with a volume control that pauses briefly after initial application, and then slowly increases the rate of volume change as it is continuously applied. This cycle is shown in the timing diagram shown in Fig.18.

There are 30 discrete gain settings ranging from +24dB maximum to -24dB minimum. The $\overline{MEM}$ pin provides two selectable functions of gain setting. If there is a logic low on this pin, the memory function is enabled, the last gain setting will be memorized when the chip is shut down, so the MT6824 will revert back to its previous gain setting when it is waked up next time. And if there is a logic high on the $\overline{MEM}$ pin, the memory function is disabled and the MT6824 will revert back to system default gain setting (6dB) next restart. Volume levels for each step vary and are specified in Gain Setting table.

If both the UP and DN pins are held high, no volume change will occur. Trigger points for the UP and DOWN pins are at 70% of VDD minimum for a logic high, and 20% of VDD maximum for a logic low. It is recommended, however, to toggle UP and DOWN between VDD and GND for best performance.

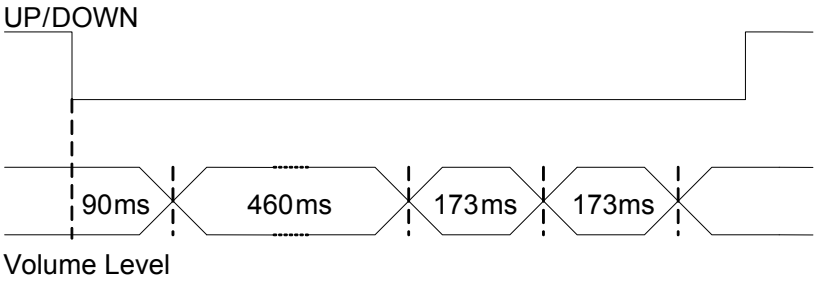


Fig.18. Timing Diagram

Table1. Gain Setting by Digital Volume Control

Gain (dB)	Step		Gain (dB)	Step
+24	30		0	14
+22.5	29		-1.5	13
+21	28		-3	12
+19.5	27		-4.5	11
+18	26		-6	10
+16.5	25		-8	9
+15	24		-10	8
+13.5	23		-12	7
+12	22		-14	6
+10.5	21		-16	5
+9	20		-18	4
+7.5	19		-20	3
+6	18		-22	2
+4.5	17		-24	1
+3	16		Mute	0
+1.5	15			

- Power Supply Decoupling

The MT6824 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) and PSRR is as low as possible. At this stage it is paramount that we acknowledge the need for separate power supplies and grounds. Noise currents in the output power stage need to be returned to output noise ground and nowhere else. Were these currents to circulate elsewhere, they may get into the power supply, the signal ground, etc, worse yet, they may form a loop and radiate noise. Any of these instances results in degraded amplifier performance. In the layout of the MT6824, the two channels amplifier should offer separate PVDD connections and PGND connections for each channel and signal currents for the inputs, reference, etc need to be returned to quite power supply VDD and GND.

As Fig.19 showing, optimum decoupling is

achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent series resistance (ESR) ceramic capacitor, typically 1.0μF, placed as close as possible to the device VDD terminal works best. For filtering lower-frequency noise signals, a larger capacitor of 10μF (ceramic) or greater placed near the audio power amplifier is recommended, this capacitor serves as local storage capacitor for supplying current during large signal transients on the amplifier outputs.

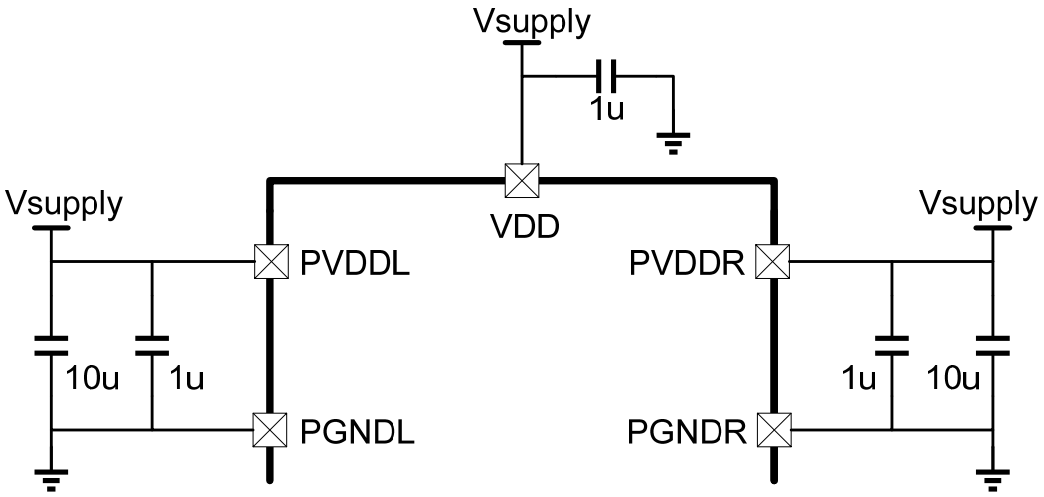


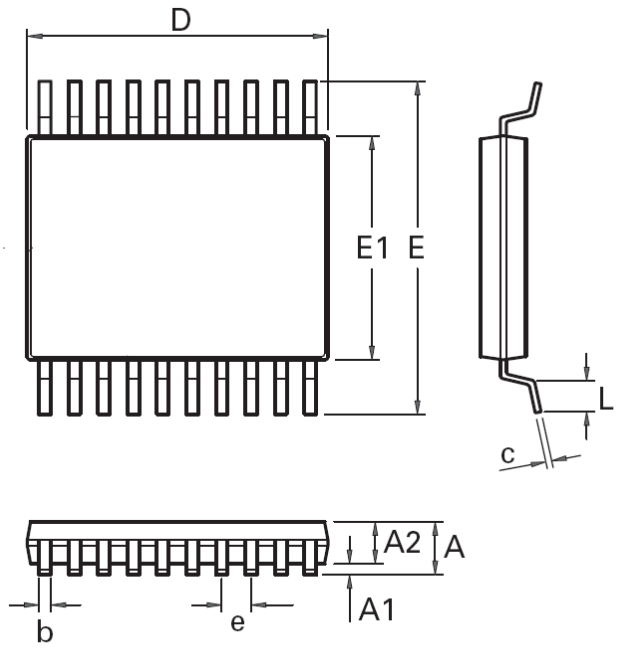
Fig.19. Power Supply Decoupling

- Over Current Protection

The MT6824 has output short circuit protection circuitry on the outputs that prevents damage to the device during output-to-output short, output-to-GND short, and output-to-VDD short. MT6824 enters the shutdown state and the outputs are disabled when detects output short. After 100ms, the chip will re-enable output again. The short circuit flag will be cleared and allows for normal operation if the short circuit condition is removed. If the short circuit condition is not removed, the protection circuitry actives again.

PACKAGE DIMENSION

Package: TSSOP20



Symbol	Unit (mm)		
	Min	Nor	Max
A	-	-	1.2
A1	0.05	-	0.15
A2	0.90	1.00	1.05
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
L	0.45	-	0.75
e	0.65 BSC		
b	0.20	-	0.30
c	0.13	-	0.19

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