Ralink
A MEDIATEK COMPANY

MT7610EN DATASHEET

802.11a/b/g/n/ac Wi-Fi Client Single Chip

Document Revision History

Revision	Date	Author	Description
0.01	2012/07/30	Ben Lin	Preliminary release
0.10	2012/10/23	Ben Lin	1. Correct LDO_V15A definition 2. Change the package outline: Thickness=0.8mm 3. Correct typos
0.11	2013/01/03	Jamie Huang	Change word format
0.12	2013/01/16	Jamie Huang	Change part number to MT7610EN
0.13	2013/02/06	Jamie Huang	Update thermal characteristics.
0.14	2013/02/20	Jamie Huang	Update power-on-reset timing diagram.

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1 System Overview

1.1 General Descriptions

The MT7610EN is a highly integrated Wi-Fi single chip which supports 433Mbps PHY rate. It is compliant with IEEE 802.11ac draft specification, offering feature-rich wireless connectivity and reliable throughput from an extended distance.

Optimized RF architecture and baseband algorithms provide superb performance and low power consumption. MT7610EN integrates PA/LNA such that the number of the external components is reduced to minimum. Intelligent MAC design deploys a high efficient DMA engine and hardware data processing accelerators which offloads the host processor.

The MT7610EN is designed to support standard based features in the areas of security, quality of service and international regulations, giving end users the greatest performance any time and in any circumstance.

1.2 Features

- IEEE 802.11 a/b/g/n and 802.11ac draft compliant
- Embedded high-performance 32-bit RISC microprocessor
- Highly integrated RF with 55nm CMOS technology
- Dual band 1T1R mode with support of 433Mbps PHY rate
- Support STBC, transmit Beamforming
- Greenfield, mixed mode, legacy modes support
- Frame aggregation
- External LNA and PA support
- Integrate high efficiency switching regulator
- Best-in-class power consumption performance
- Compact 8mm x 8mm QFN68L package
- IEEE 802.11d and 802.11h compliant
- Security support for WFA WPA/WPA2 personal, WPS2.0, WAPI
- Supports 802.11w protected managed frames
- QoS support of WFA WMM, WMM PS
- TCP checksum offload
- 802.11 to 802.3 header translation offload
- Supports Wi-Fi Direct
- Fully compliance with PCIe base specification v2.0 with OBFF, LTR ECN support.
- Per packet transmit power control
- Antenna diversity
- Auto-calibration

- 9 programmable general purpose Input / Output
- 2 configurable LED pins

1.3 Applications

- AP router
- xDSL modem

1.4 Block Diagram

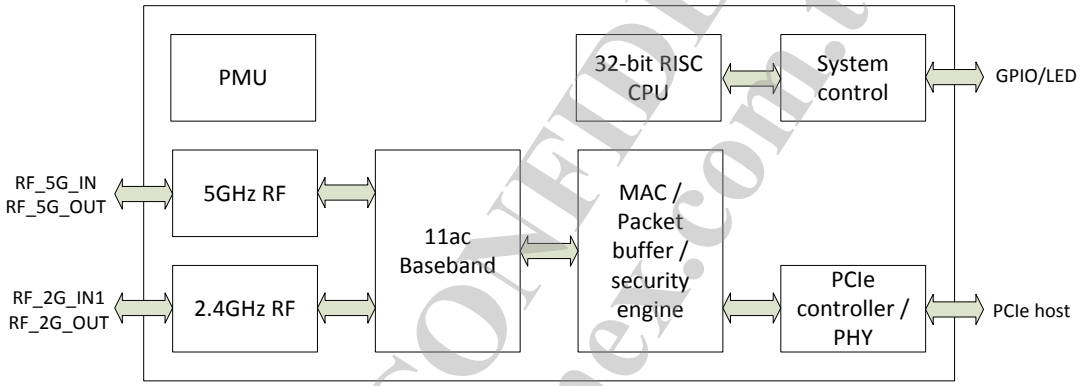


Figure 1 MT7610EN block diagram

2 Product Descriptions

2.1 Pin Layout

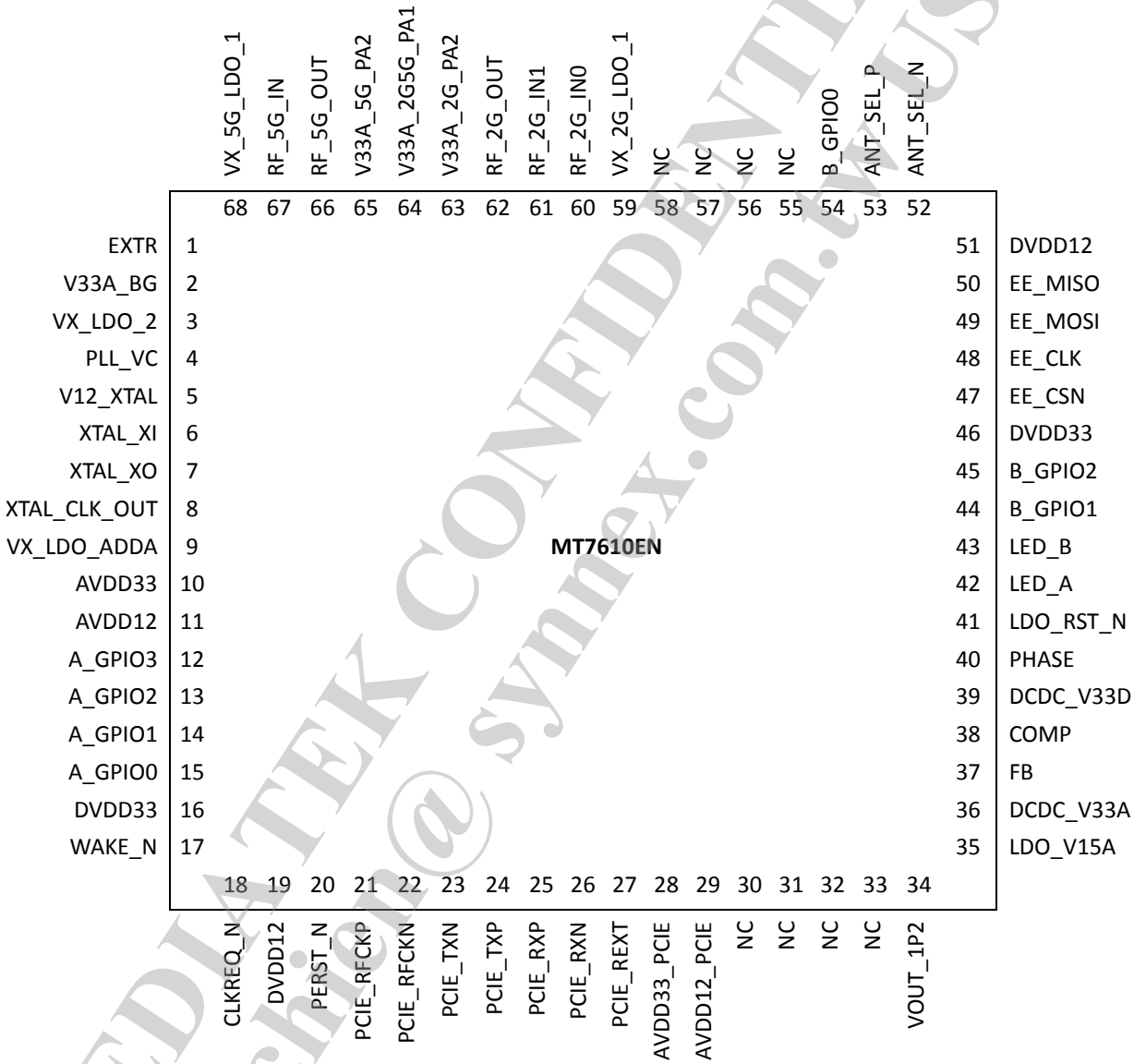


Figure 2 Top view of MT7610EN QFN pin-out.

2.2 PIN Description

QFN68	Pin Name	Pin description	Default PU/PD	I/O	Supply domain

Reset and clocks					
41	LDO_RST_N	External system reset active low	N/A	Input	DVDD33
5	V12_XTAL	XTAL 1.2v bypass	N/A	Analog	
6	XTAL_XI	Crystal input or external clock input	N/A	Input	
7	XTAL_XO	Crystal output	N/A	Input	
PCIe interface					
17	WAKE_N	Request system to wake from the sleep/suspend state	PU	Output	DVDD33
18	CLKREQ_N	Reference clock request signal	PU	Output	DVDD33
20	PERST_N	PCIe functional reset	PU	Input	DVDD33
21	PCIE_RFCKP	PCIe differential reference clock	N/A	Input	AVDD33_PCIE
22	PCIE_RFCKN	PCIe differential reference clock	N/A	Input	AVDD33_PCIE
23	PCIE_TXN	PCIe differential transmit pair	N/A	Output	AVDD33_PCIE
24	PCIE_TXP	PCIe differential transmit pair	N/A	Output	AVDD33_PCIE
25	PCIE_RXP	PCIe differential transmit pair	N/A	Input	AVDD33_PCIE
26	PCIE_RXN	PCIe differential transmit pair	N/A	Input	AVDD33_PCIE
27	PCIE_REXT	PCIe resister reference	N/A	Analog	
EEPROM/flash interface					
50	EE_MISO	External memory data input / Antenna select	PD	Input	DVDD33
49	EE_MOSI	External memory data output / Antenna select	PD	Output	DVDD33
48	EE_CLK	External clock	PD	Output	DVDD33
47	EE_CSN	External chip select	PD	Output	DVDD33
Programmable I/O					
15	A_GPIO0	Programmable input/output	N/A	In/out	DVDD33
14	A_GPIO1	Programmable input/output	N/A	In/out	DVDD33
13	A_GPIO2	Programmable input/output	N/A	In/out	DVDD33
12	A_GPIO3	Programmable input/output	N/A	In/out	DVDD33
54	B_GPIO0	Programmable input/output	PU	In/out	DVDD33
44	B_GPIO1	Programmable input/output	PU	In/out	DVDD33
45	B_GPIO2	Programmable input/output	PU	In/out	DVDD33
LED					
42	LED_A	Programmable open-drain LED controller	PU	Output	DVDD33
43	LED_B	Programmable open-drain LED controller	PU	Output	DVDD33
Antenna select					
53	ANT_SEL_P	Diversity antenna pin	PD	Output	DVDD33
52	ANT_SEL_N	Diversity antenna pin	PU	Output	DVDD33
WIFI radio interface					

1	EXTR	RF BG reference	N/A	Analog	
67	RF_5G_IN	RF a-band input port	N/A	Input	
66	RF_5G_OUT	RF a-band output port	N/A	Output	
62	RF_2G_OUT	RF g-band output port	N/A	Output	
61	RF_2G_IN1	RF g-band input port 1	N/A	Input	
60	RF_2G_IN0	RF g-band input port 0	N/A	Input	
8	XTAL_CLK_OUT	XTAL buffered clock output	N/A	Output	
PMU/SMPS					
34	VOUT_1P2	LDO 1.2V output	N/A	Output	
35	LDO_V15A	Digital LDO 1.5V input	N/A	Input	
36	DCDC_V33A	SMPS 3.3V power supply	N/A	Input	
39	DCDC_V33D	SMPS 3.3V power supply	N/A	Input	
37	FB	SMPS control	N/A	Analog	
38	COMP	SMPS control	N/A	Analog	
40	PHASE	SMPS control	N/A	Analog	
Miscellaneous					
4	PLL_VC	PLL V-tune control	N/A	Analog	
30, 31, 32, 33, 55, 56, 57, 58	NC	Reserved	N/A		
Power supplies					
10	AVDD33	Analog 3.3v power supply	N/A	Power	
16, 46	DVDD33	Digital 3.3v I/O power supply	N/A	Power	
19, 51	DVDD12	Digital 1.2v core power supply	N/A	Power	
11	AVDD12	Analog 1.2v power supply	N/A	Power	
28	AVDD33_PCIE	PCIe 3.3V power supply	N/A	Power	
29	AVDD12_PCIE	PCIe 1.2V power supply	N/A	Power	
2	V33A_BG	RF 3.3v power supply	N/A	Power	
63	V33A_2G_PA2	RF 3.3v power supply	N/A	Power	
64	V33A_2G5G_PA1	RF 3.3v power supply	N/A	Power	
65	V33A_5G_PA2	RF 3.3v power supply	N/A	Power	
3	VX_LDO_2	RF 1.5v power supply	N/A	Power	
9	VX_LDO_ADDA	RF 1.5v power supply	N/A	Power	
59	VX_2G_LDO_1	RF 1.5v power supply	N/A	Power	
68	VX_5G_LDO_1	RF 1.5v power supply	N/A	Power	
E-PAD	VSS	Ground	N/A	Ground	

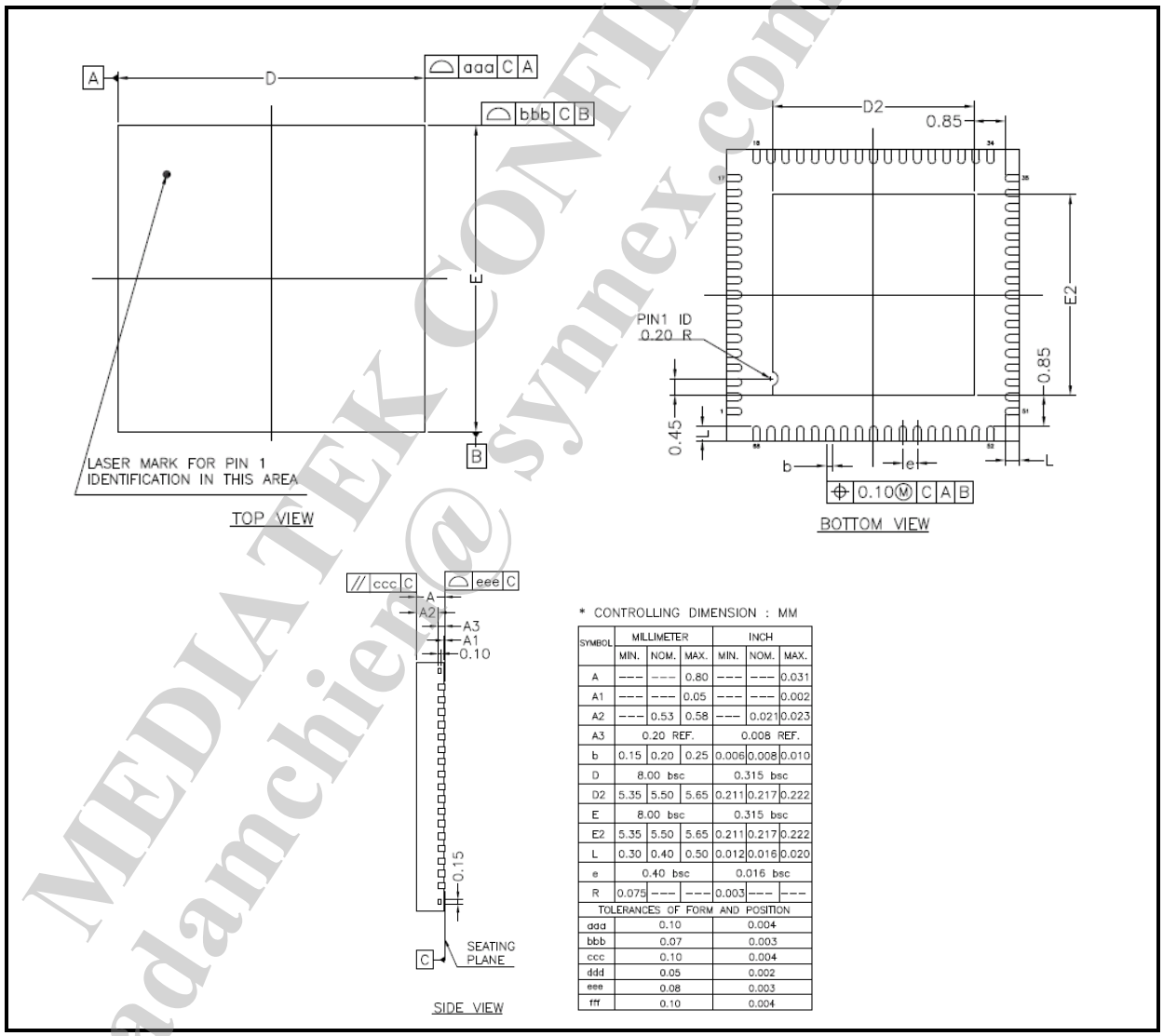
Table 1 Pin descriptions

2.3 Strapping option

QFN68	Pin Name	Pin description	Default PU/PD
49	EE_MOSI	CHIP_MODE[2]: Pull down	PD
48	EE_CLK	XTAL_20_SEL XTAL is 20MHz: Pull up XTAL is 40MHz: Pull down	PD
47	EE_CSN	EXT_EE_SEL: Pull down	PD
53	ANT_SEL_P	CHIP_MODE[1]: Pull down	PD
52	ANT_SEL_N	CHIP_MODE[0]: Pull up	PU

Table 2 Strapping option

2.4 Package information



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.80	---	---	0.031
A1	---	---	0.05	---	---	0.002
A2	---	0.53	0.58	---	0.021	0.023
A3	0.20 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	8.00 bsc			0.315 bsc		
D2	5.35	5.50	5.65	0.211	0.217	0.222
E	8.00 bsc			0.315 bsc		
E2	5.35	5.50	5.65	0.211	0.217	0.222
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.40 bsc			0.016 bsc		
R	0.075	---	---	0.003	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

Figure 3 Package outline drawing

2.5 Ordering Information

Part number	Package	Operational temperature range
MT7610EN/A-L	8x8x0.8 mm 68-QFN	-10~70°C

Table 3 Ordering information

2.6 TOP Marking Information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MT7610EN : Part number
DDDD     : Date code
####     : Internal control code
BBBBBBB  : Lot number
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Figure 4 Top marking

3 Electrical characteristics

3.1 Absolute maximum rating

Symbol	Parameters	Maximum rating	Unit
VDD33	3.3V Supply Voltage	-0.3 to 3.6	V
VDD12	1.2V Supply Voltage	-0.3 to 1.5	V
VDD15	1.5V Supply Voltage	-0.3 to 1.8	V
T_{STG}	Storage Temperature	-40 to +125	°C
VESD	ESD protection (HBM)	2000	V

Table 4 Absolute maximum ratings

3.2 Recommended operating range

Symbol	Rating	MIN	TYP	MAX	Unit
VDD33	3.3V Supply Voltage	2.97	3.3	3.63	V
VDD12	1.2V Supply Voltage	1.14	1.2	1.26	V
VDD15	1.5V Supply Voltage	1.425	1.5	1.575	V
$T_{AMBIENT}$	Ambient Temperature	-10	-	70	°C

Table 5 Recommended operating range

3.3 DC characteristics

Symbol	Parameter	Conditions	MIN	MAX	Unit
V_{IL}	Input Low Voltage	LVTTL	-0.28	0.6	V
V_{IH}	Input High Voltage		2.0	3.63	V
V_{T-}	Schmitt Trigger Negative Going Threshold Voltage	LVTTL	0.68	1.36	V
V_{T+}	Schmitt Trigger Positive Going Threshold Voltage		1.36	1.7	V
V_{OL}	Output Low Voltage	$\|I_{OL}\|$ = 1.6~14 mA	-0.28	0.4	V
V_{OH}	Output High Voltage	$\|I_{OH}\|$ = 1.6~14 mA	2.4	VDD33+0.33	V
R_{PU}	Input Pull-Up Resistance	PU=high, PD=low	40	190	KΩ
R_{PD}	Input Pull-Down Resistance	PU=low, PD=high	40	190	KΩ

Table 6 DC description

3.4 Thermal characteristics

Symbol	Description	Performance	
		TYP	Unit
T_J	Maximum Junction Temperature (Plastic Package)	125	°C
Θ_{JA}	Junction to ambient temperature thermal resistance[1]	35.29	°C/W
Θ_{JC}	Junction to case temperature thermal resistance	7.76	°C/W
Ψ_{Jt}	Junction to the package thermal resistance[2]	5.48	°C/W

Note:

[1] Half mini-card, 4-layer PCB
[2] 8mm x 8mm QFN68L package

Table 7 Thermal information

3.5 Power-on-reset timing

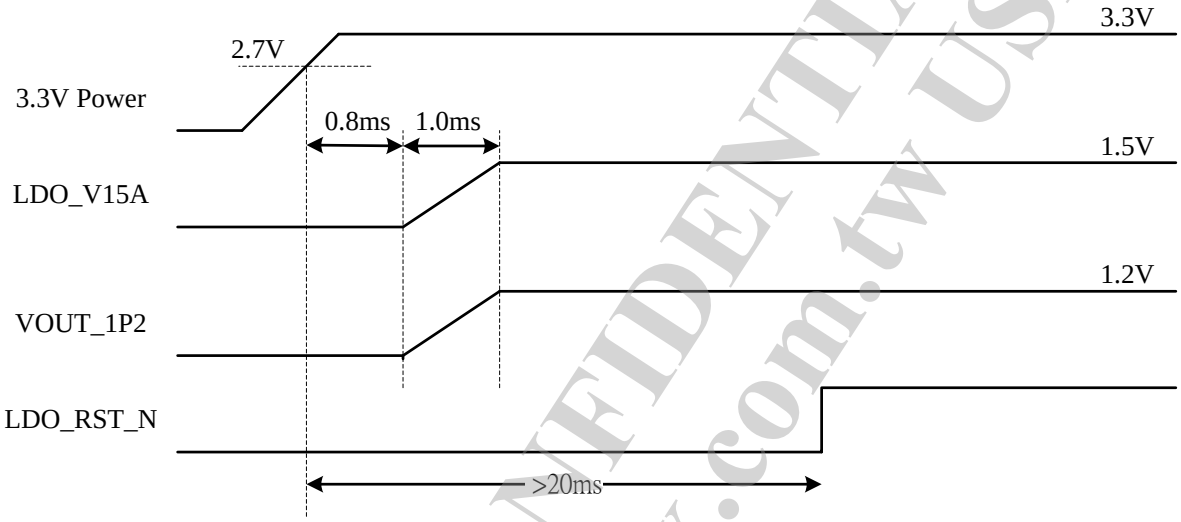

Figure 5 POR timing

ESD CAUTION

MT7610E is ESD (electrostatic discharge) sensitive device and may be damaged with ESD or spike voltage. Although MT7610E is with built-in ESD protection circuitry, please handle with care to avoid the permanent malfunction or the performance degradation.