Mosway Technologies Ltd.

MT8006A/B

High and Low Side Driver

General Description

The MT8006 is a high voltage, high speed power MOSFET and IGBT driver based on P_SUB P_EPI process. The floating channel driver can be used to drive two N-channel power MOSFET or IGBT independently which operates up to 300 V. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross -conduction. Propagation delays are matched to simplify use in high frequency applications. It has two versions MT8006A & MT8006B.

Features

- Fully operational to +300 V
- 3.3 V logic compatible
- dV/dt Immunity ±50 V/nsec
- Floating channel designed for bootstrap operation
- Gate drive supply range from 12 V to 20 V
- Output Source / Sink Current Capability 450mA / 900mA (at Vcc = 15V)
- Independent Logic Inputs to Accommodate All Topologies
- -5V negative Vs ability
- Matched propagation delay for both channels

Applications

- Small and medium- power motor driver
- Power MOSFET or IGBT driver
- Half−Bridge Power Converters
- Full-Bridge Power Converters
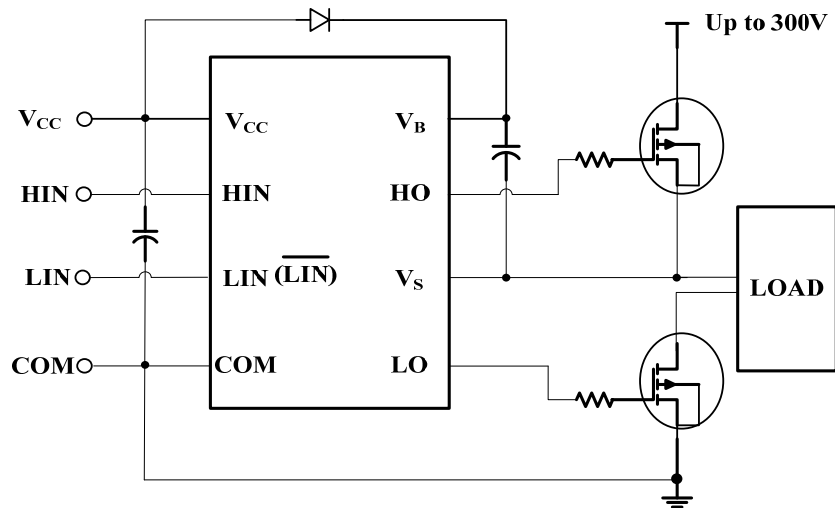- Any Complementary Drive Converters

Packages/Order information
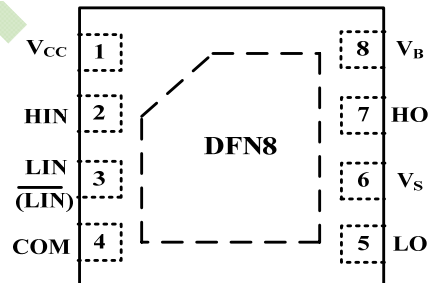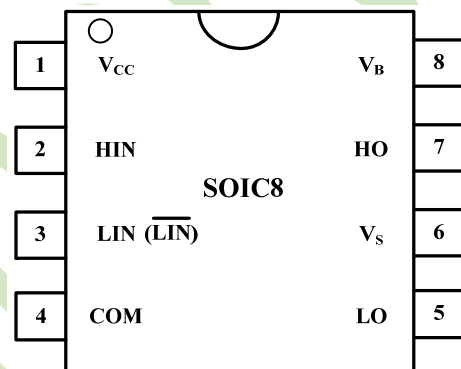
(LIN: A version $\overline{\text{LIN}}$: B version)

Part number	Order Code	Package
MT8006A	MT8006ASEC-R1	SOIC8
	MT8006ADEC-R1	DFN8
MT8006B	MT8006BSEC-R1	SOIC8
	MT8006BDEC-R1	DFN8

Typical Application Circuit

Pin Description

PIN NO.	PIN NAME	PIN FUNCTION
1	V_{CC}	Low side and main power supply
2	HIN	Logic input for high side gate driver output (HO)
3	LIN($\overline{LIN}$)	Logic input for low side gate driver output (LO)
4	COM	Ground
5	LO	Low side gate drive output A version: in phase with LIN B version: out of phase with LIN
6	V_S	High side floating supply return or bootstrap return
7	HO	High side gate drive output, in phase with HIN
8	V_B	High side floating supply

Functional Block Diagram
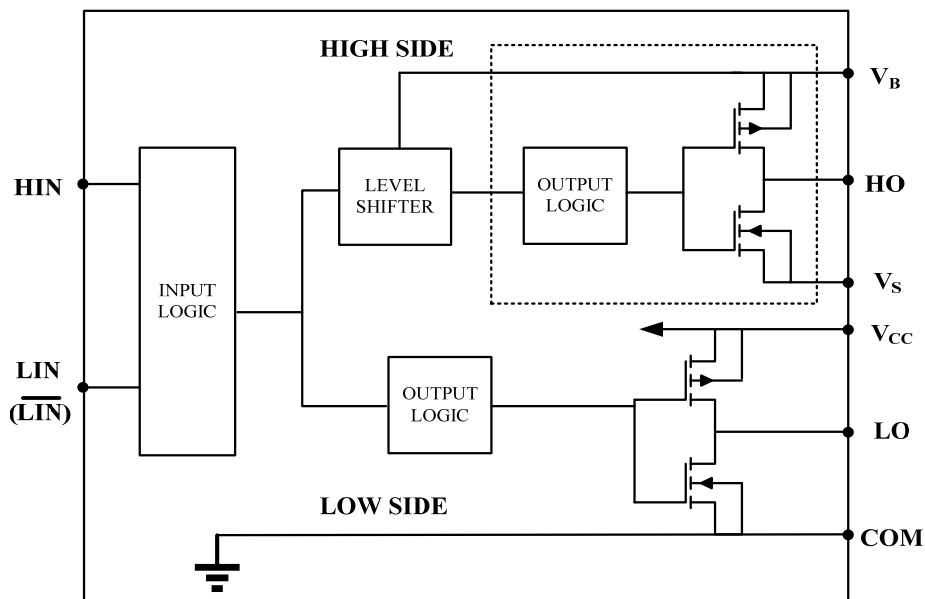
Absolute Maximum Ratings [Note1]

Symbol	Definition		MIN.	MAX.	Units
V_B	High side floating supply		-0.3	300	V
V_S	High side floating supply return		$V_B - 22$	$V_B + 0.3$	
V_{HO}	High side gate drive output		$V_S -0.3$	$V_B + 0.3$	
V_{CC}	Low side and main power supply		-0.3	22	
V_{LO}	Low side gate drive output		-0.3	$V_{CC} + 0.3$	
V_{IN}	Logic input of HIN & LIN		-0.3	$V_{CC} + 0.3$	
ESD	HBM Model		2.5		kV
	Machine Model		200		V
P_D	Package Power Dissipation @ TA $\leq$25°C	8 Lead SOIC	--	0.625	W
Rth_{JA}	Thermal Resistance Junction to Ambient	8 Lead SOIC	--	200	°C /W
T_J	Junction Temperature		--	150	°C
T_S	Storage Temperature		-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)		--	300	

Note 1: Exceeding these ratings may damage the device.

Recommended Operating Conditions

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	$V_S +12$	$V_S +20$	V
V_S	High side floating supply return	-	300	
V_{HO}	High side gate drive output voltage	V_S	V_B	
V_{CC}	Low side supply	12	20	
V_{LO}	Low side gate drive output voltage	0	V_{CC}	
V_{IN}	Logic input voltage(HIN & LIN)	0	V_{CC}	
T_A	Ambient temperature	-40	125	℃

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Definition	TYP.	MAX.	Units
t_{onH}	High side turn-on propagation delay	170	240	ns
t_{offH}	High side turn-off propagation delay	170	240	
t_{onL}	Low side turn-on propagation delay	170	240	
t_{offL}	Low side turn-off propagation delay	170	240	
MT	Delay matching	—	50	
t_r	Turn-on rise time	50	90	
t_f	Turn-off fall time	30	80	

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

| Symbol	Definition	MIN.	TYP.	MAX.	Units
V_{IH}	Logic "1"(HIN & LIN) input voltage	2.5	-	-	V
V_{IL}	Logic "0" (HIN & LIN) input voltage	-	-	0.8	
V_{OH}	High level output voltage, V_{BIAS} - V_O	-	-	0.3	
V_{OL}	Low level output voltage, V_O	-	-	0.3	
I_{QCC}	Quiescent V_{CC} supply current	-	160	220	μA
I_{QBS}	Quiescent V_B supply current	-	80	150	
V_{CCU+}	V_{CC} supply UVLO threshold	-	10.2	-	V
V_{CCU-}		-	9.4	-	
V_{BSU+}	V_{BS} supply UVLO threshold	-	9.9	-	
V_{BSU-}		-	9.5	-	
I_{LK}	Leakage current from V_S(600V) to GND		-	50	μA
I_{IN+}	Logic "1" input bias current	-	6	10	
I_{IN-}	Logic "0" input bias current	-	1	2	
I_{O+}	Output high short circuit pulsed current		450		mA
I_{O-}	Output low short circuit pulsed current		900		

Logic Function

A version

B version
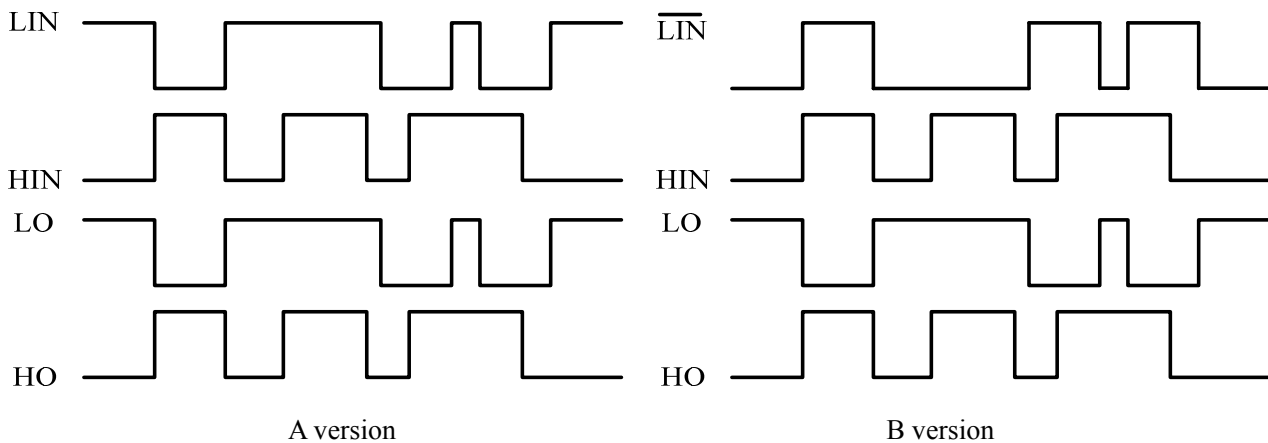
Timing Spec
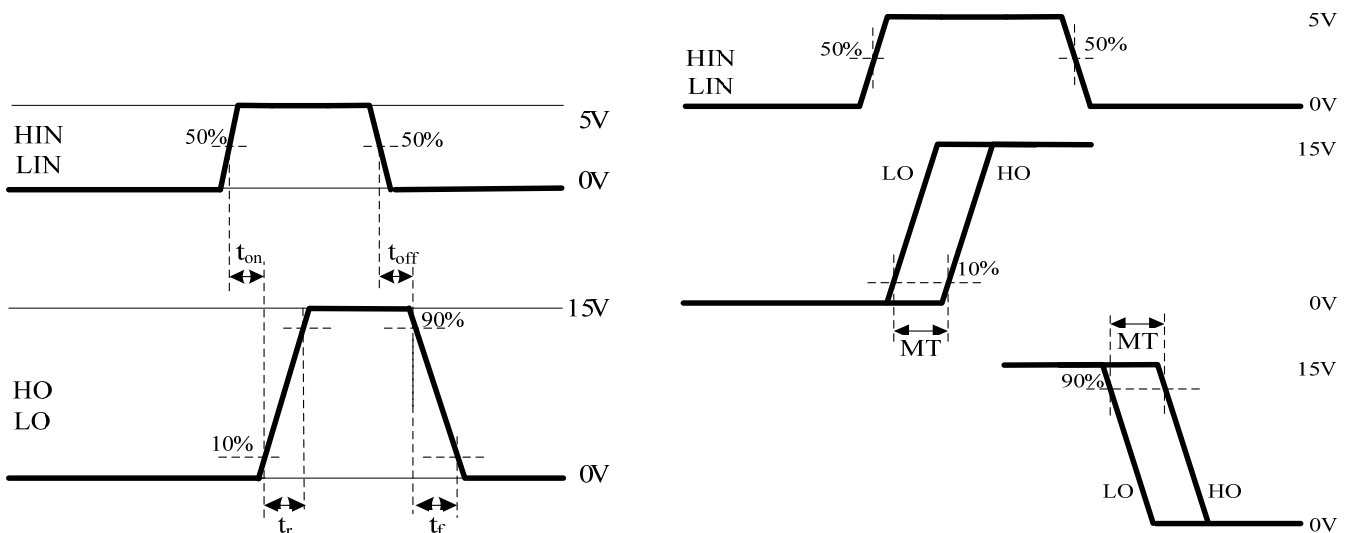
Package Information

SOIC8 Package Dimensions

Size Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	-	-	1.75	D	4.70	4.90	5.10
A1	0.10	-	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e	1.27BSC		
b	0.39	-	0.48	h	0.25	-	0.50
b1	0.38	0.41	0.43	L	0.50	-	0.80
c	0.21	-	0.26	L1	1.05BSC		
c1	0.19	0.20	0.21	θ	0	-	8°

Package Outlines
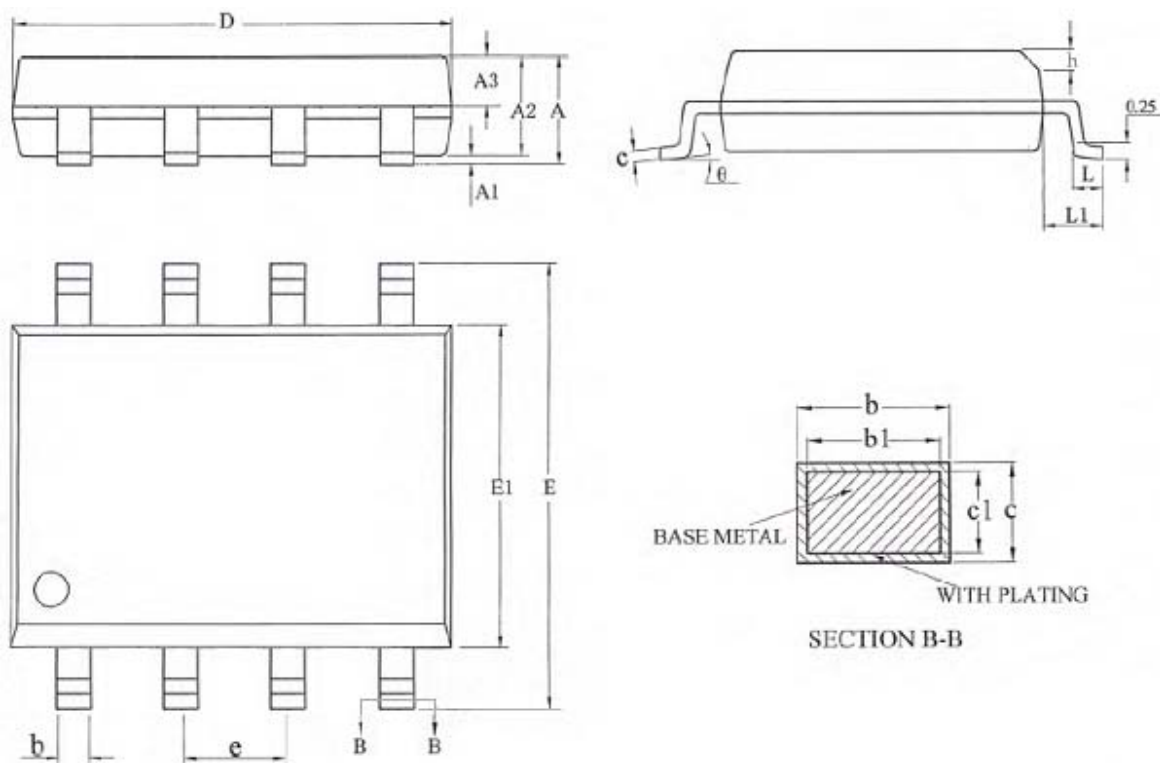
SOIC8 Package Mark Information
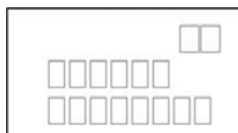
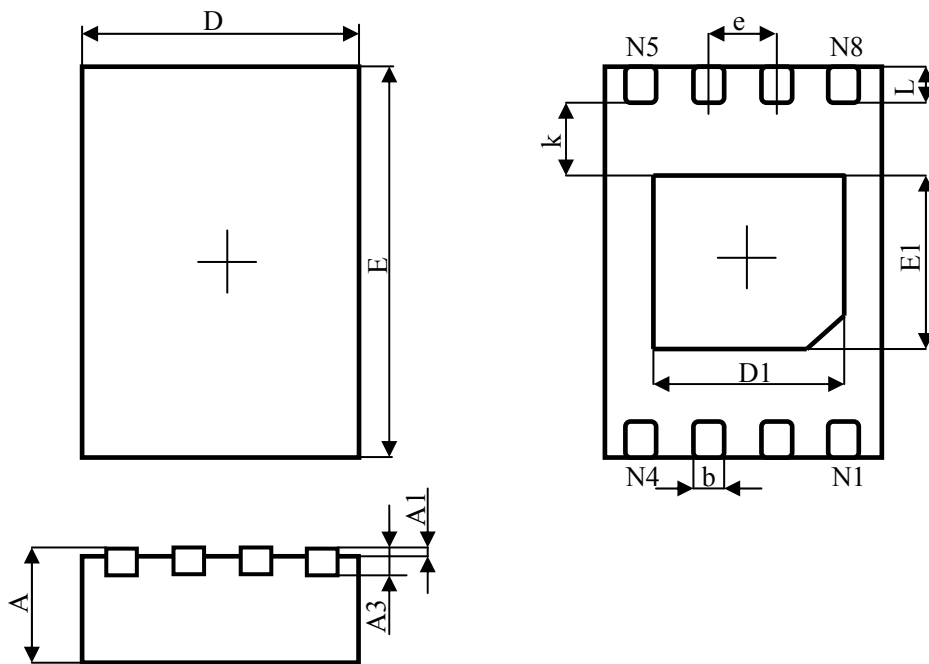| TOP Mark |
|---|
| Logo |
| MT8006M[Note1] |
| YWWXXXXX[Note2] |

Note1：M：A or B;

Note2：Y：Year code，WW：Week codes，XXXXX：Package codes

DFN8 Package Dimensions

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.

A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	1.924	2.076	0.076	0.082
E	2.924	3.076	0.115	0.121
D1	1.400	1.600	0.055	0.063
E1	1.400	1.600	0.055	0.063
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.224	0.376	0.009	0.015

Package Outlines

DFN8 Package Mark Information
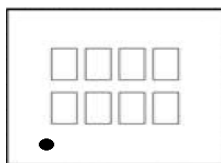
TOP Mark
8006
AYWX[Note]
Pin 1 indicator point

Note：A：Internal code，Y：Year code，W：Week codes， X：Package codes

Important Notice

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