Audio Multiplexer with Headphone Driver & PGA Output

Datasheet

Product Specification

Legal Notice

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1 General Description

1.1 Overview

The MediaTek MT8292 introduces the advantages of an input multiplexer, the headphone driver and the PGA outputs. The MT8292 performs 8:1 stereo input multiplexer. The analog input pins can either independently support GPIO function or provide extra GPIO pins to use.

Each of the stereo PGA outputs as well as a headphone driver can reach 2Vrms in a 9V or 12V supply environment. On the other hand, through the two wire control, the MT8292 can control the digital function of the host IC (ie., the MT538x for example). Together with an external audio ADC and an audio DAC, the MT8292 can reach high voltage and gain output.

1.2 Key Features

- 56-pin QFN package
- Allows 2Vrms input swing from analog input and supports 2Vrms PGA output
- MUTE and PGA function
- Headphone driver output
- Stereo PGA gain control from 15dB to -36dB for each output
- Headphone PGA gain from 21dB to -36dB for output
- Two Wire control
- General purpose I/O function
- +8.2V to +13.2V analog power supply
- +3.0V to +3.6V digital power supply

- Eight channels of analog output (three L/R line outputs and a headphone output)
- 8-channel analog multiplexer input 96dB SNR and dynamic range
- Analog inputs also share general purpose I/O function

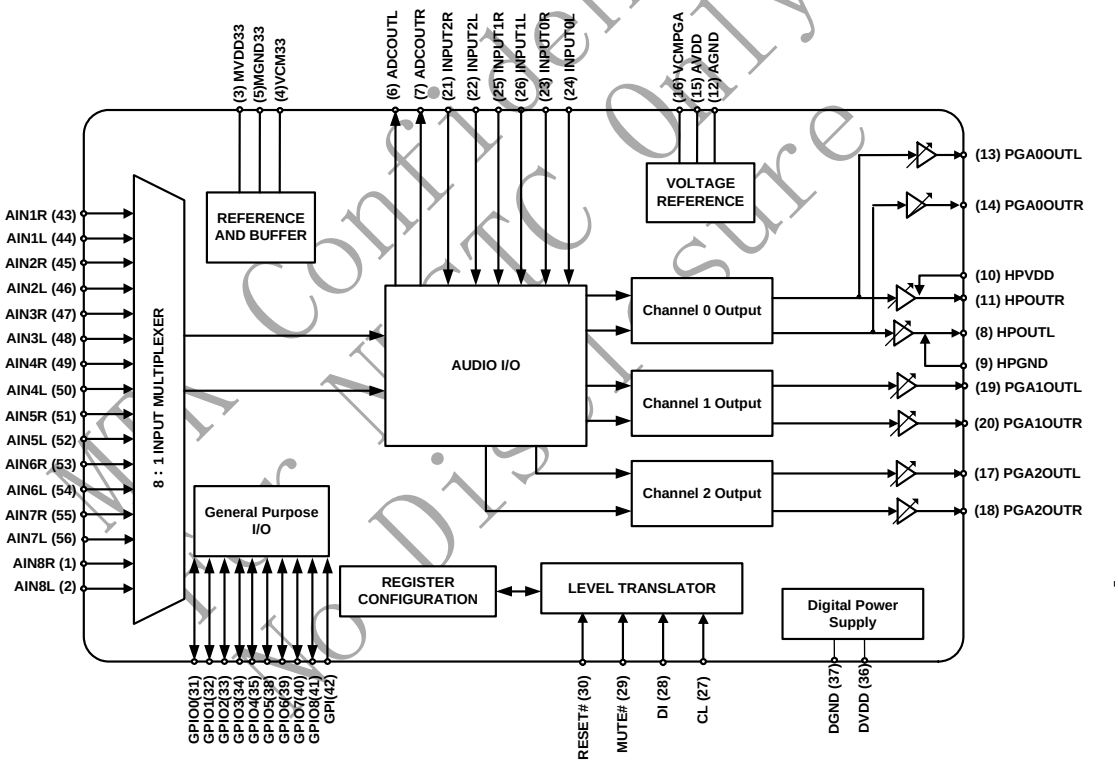


Figure 1: Application Block Diagram

2 Pin Allocation and Description

2.1 Pinout Diagram

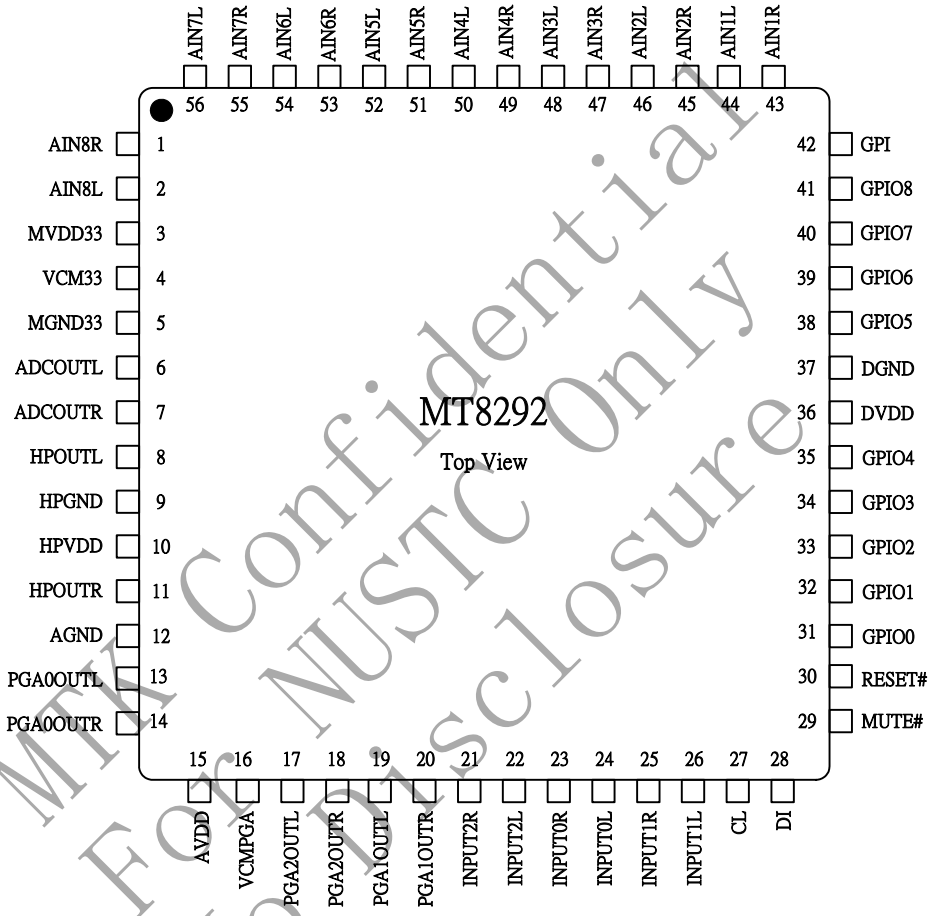


Figure 2: 56-Pin QFN Package Pinout

*AIN1R (pin 43) to AIN8L (pin2) support GPIO function

*In reset mode, GPIO0 (pin 31) activates high level and supports hardware trapped function to control PGA output mute or un-mute.

2.2 Pin Description

No	PIN NAME	TYPE	FUNCTION
1	AIN8R	Analog Input	Channel 8 right input
2	AIN8L	Analog Input	Channel 8 left input
3	MVDD33	Supply	Multiplexer positive supply 3.3 voltage
4	VCM33	Analog Output	Multiplexer midrail divider decoupling pin
5	MGND33	Supply	Multiplexer negative supply
6	ADCOUTL	Analog Output	Analog multiplexer left output
7	ADCOUTR	Analog Output	Analog multiplexer right output
8	HPOUTL	Analog Output	Headphone right channel output
9	HPGND	Supply	Headphone ground supply pin
10	HPVDD	Supply	Headphone power supply pin
11	HPOUTR	Analog Output	Headphone right channel output
12	AGND	Supply	Analog negative supply
13	PGA0OUTL	Analog Input	PGA channel 0 left output
14	PGA0OUTR	Analog Input	PGA channel 0 right output
15	AVDD	Supply	Analog positive supply 12 voltage or 9 voltage
16	VCMPGA	Analog Output	PGA midrail divider decoupling pin
17	PGA2OUTL	Analog Input	PGA channel 2 left output
18	PGA2OUTR	Analog Input	PGA channel 2 right output
19	PGA1OUTL	Analog Input	PGA channel 1 left output
20	PGA1OUTR	Analog Input	PGA channel 1 right output
21	INPUT2R	Analog Input	Channel 2 right input to PGA gain module
22	INPUT2L	Analog Input	Channel 2 left input to PGA gain module
23	INPUT0R	Analog Input	Channel 0 right input to PGA gain module
24	INPUT0L	Analog Input	Channel 0 left input to PGA gain module
25	INPUT1R	Analog Input	Channel 1 right input to PGA gain module
26	INPUT1L	Analog Input	Channel 1 left input to PGA gain module
27	CL	Digital Input	Control clock pin in serial mode

28	DI	Digital Input	Control data pin in serial mode
29	MUTE#	Digital Input	Hardware mute function when this pin is driven low
30	RESET#	Digital Input	The device enters a low power mode when this pin is driven low
31	GPIO0	Digital Input	General Purpose I/O 0 and also shares hardware trapped function
32	GPIO1	Digital Input	General Purpose I/O 1
33	GPIO2	Digital Input	General Purpose I/O 2
34	GPIO3	Digital Input	General Purpose I/O 3
35	GPIO4	Digital Input	General Purpose I/O 4
36	DVDD	Digital Input	Digital positive supply 3.3 voltage
37	DGND	Supply	Digital negative supply
38	GPIO5	Digital Input	General Purpose I/O 5
39	GPIO6	Digital Input	General Purpose I/O 6
40	GPIO7	Digital Input	General Purpose I/O 7
41	GPIO8	Digital Input	General Purpose I/O 8
42	GPI	Digital Input	Only General Purpose Input and support internal digital scan mode
43	AIN1R	Analog Input	Channel 1 right input (default)
44	AIN1L	Analog Input	Channel 1 left input (default)
45	AIN2R	Analog Input	Channel 2 right input
46	AIN2L	Analog Input	Channel 2 left input
47	AIN3R	Analog Input	Channel 3 right input
48	AIN3L	Analog Input	Channel 3 left input
49	AIN4R	Analog Input	Channel 4 right input
50	AIN4L	Analog Input	Channel 4 left input
51	AIN5R	Analog Input	Channel 5 right input
52	AIN5L	Analog Input	Channel 5 left input
53	AIN6R	Analog Input	Channel 6 right input
54	AIN6L	Analog Input	Channel 6 left input
55	AIN7R	Analog Input	Channel 7 right input
56	AIN7L	Analog Input	Channel 7 left input

3 Specifications

3.1.1 Absolute Maximum Ratings

CONDITION	MIN	MAX
Analog supply voltage	-0.3V	+14.8V
Digital supply voltage	-0.3V	+3.6V
Analog inputs voltage	AGND -0.3V	AVDD +0.3V
Storage temperature, Tstg	-40°C	$+150^\circ$C
Junction temperature, Tj	-40°C	$+125^\circ$C
Operating temperature, Tp	-10°C	$+70^\circ$C

3.1.2 Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Analog supply range	AVDD, HPVDD	8.2	-	13.2	V
Digital supply range	DVDD	3.0	3.3	3.6	V
Ground	HPGND, AGND, DGND, MGND33	-	0	-	V
|DGNG – AGND|	-	-	-	0.3	V

3.1.3 Electrical Characteristics

AVDD=9V or 12V, DVDD=3.3V, ADCGND/DACGND=0V, Ta=$+25^\circ$C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels						
Input LOW level	VIL	-	-	-	0.8	V
Input HIGH level	VIH	-	2.0	-	-	V
Output LOW	VOL	-	-	-	0.4	V
Output HIGH	VOH	-	2.4	-	-	V
Analog Output Reference Levels						
0dBFs full scale output voltage	-	At every outputs	1.9	2.0	2.1	Vrms
SNR	-	A-weighted	-	96	-	dB

THD+N	-	1kHz 0dB analog input	-	-86	-	dB
Dynamic range	-	1kHz, THD+N @-60dBFs	-	96	-	dB
Output channel separation	-	1kHz, 0dBFs	-	90	-	dB
Programmable gain range (analog)	-	1kHz, Input	-36	-	15	dB
Power down current	IAVDD	AVDD=9V or 12V	-	0.1	-	mA
	IDVDD	DVDD=3.3V	-	0.1	-	mA
Power supply rejection ratio	PSRR	1kHz 100mVpp	-	50	-	dB
Headphone Buffer						
Gain range (analog)	-	1kHz, Input	-36	-	21	dB
THD+N	-	1kHz, RL=32ohms @Po=10mWrms	-	-87	-	dB
		1kHz, RL=32ohms @Po=20mWrms	-	-80	-	dB
Power supply rejection ratio	PSRR	20Hz to 20kHz without supply decoupling	-	-50	-	dB
SNR	-	A-weighted	-	96	-	dB
Analog Input Performance						
Input signal level (0dB)	-	-	-	2	-	Vrms
SNR	-	A-weighted	-	96	-	dB
Dynamic range	-	1kHz, THD+N @-60dBFs	-	100	-	dB
THD+N	-	1kHz, 0dBFs	-	-86	-	dB
		1kHz, -3dBFs	-	-86	-	dB
Input channel separation	-	1kHz, Input	-	90	-	dB
Power supply rejection ratio	PSRR	1kHz 100mVpp	-	54	-	dB
		20Hz to 20kHz 100mVpp	-	50	-	dB
Supply Current						
Analog supply current	-	AVDD=9V or 12V	-	12	-	mA
		HPVDD=9V or 12V	-	10	-	mA
Digital supply current	-	DVDD=3.3V	-	10	-	mA

3.2 Control Interface Timing: 2-Wire Port

PARAMETER	SYMBOL	MIN	MAX	UNIT
CL Clock Frequency	-	-	512	KHz
Start Condition Hold time	t_{st}	2.1	-	us
Clock Low Time	t_{lw}	1.2	-	us
Clock High Time	t_{hg}	1.2	-	us
Rise Time for DI, CL	t_{rs}	-	0.75	us
Fall Time for DI, CL	t_{ft}	-	375	ns
Data Setup Time	t_{su}	250	-	ns
Data Hold Time	t_{hd}	-	500	ns
Stop Time for Stop Condition	t_{sp}	2.1	-	us

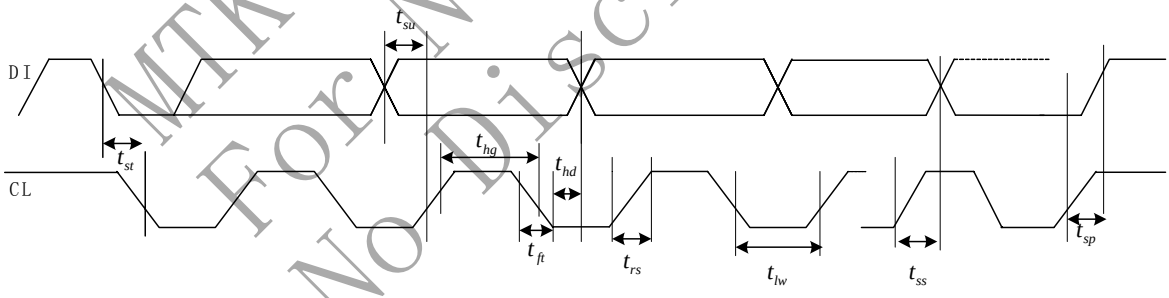


Figure 3: Control Port Timing

4 Digital Interface

4.1 Two - Wire Control Bus

The MT8292 can be controlled by two-wire bus which can read/write the internal register to control the MT8292. Each byte put on SDA line must be 8 bits long. After the start condition, if the MT8292 receives the device address which matches 0x38h, then the MT8292 responds by pulling SDI low (ACK).

After the MT8292 acknowledges the correct device ID address, the controller can send the register address byte. The MT8292 also acknowledges the register address by the same way as describing above. If the read/write bit is '0', indicating a write cycle, the MT8292 waits for a data phase (8 bits) and writes the input data to the pointed register. If it is a read cycle, the MT8292 outputs the data from the pointed address.

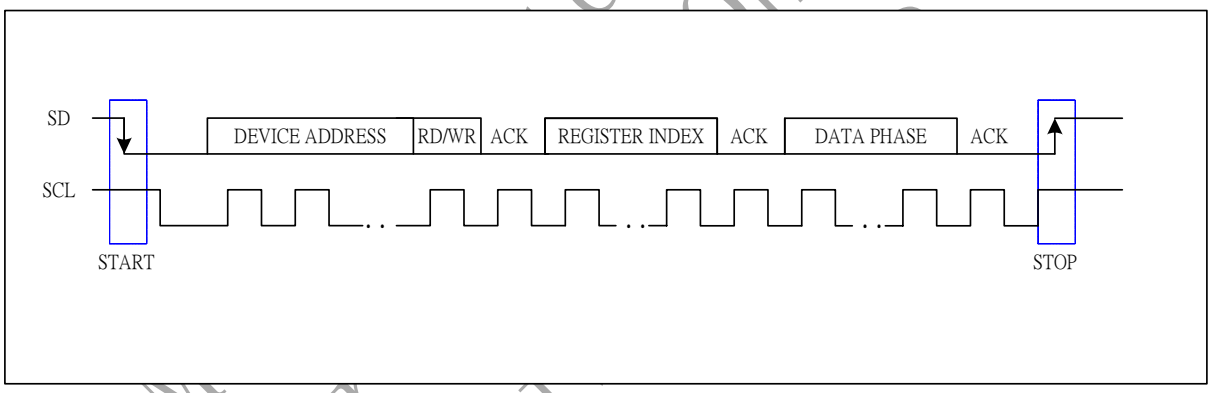


Figure 4: Two-Wire Interface

5 System Description

5.1 Internal Power on Reset Circuit

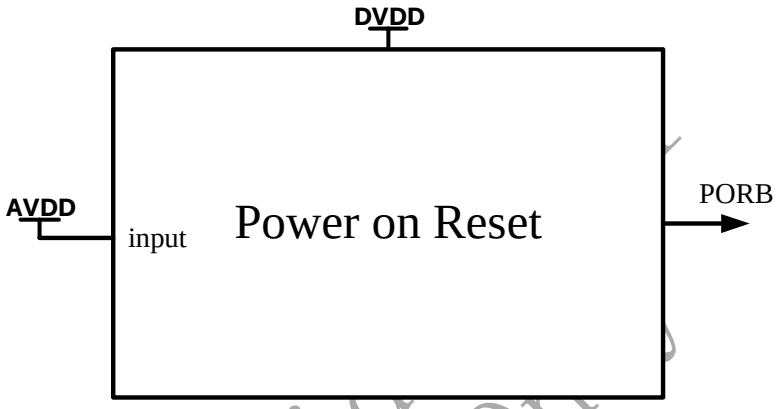


Figure 5: Power On Reset Block

Internal power on reset circuit is shown in Figure 5, which is used to reset the digital logic state into the initial state after AVDD and DVDD are power up.

When the chip is on power up, internal power on reset circuit needs DVDD to operate. PORB is low when AVDD is below the threshold voltage, and PORB is set high after AVDD is over the threshold voltage and internal time delay passed.

When the chip is on power down, PORB is pulled to low after AVDD is lower than the threshold voltage and internal time delay passed. If DVDD is removed, the PORB follows the DVDD voltage.

Figure6 shows the power on and power down sequences when DVDD leads AVDD.

Figure 6: Power On/Off Timing 1

Figure 7 shows the power on and power down sequences when AVDD leads DVDD.

Figure 7: Power On/Off Timing 2

6 Description

6.1 Analog PGA Output

6.1.1 PROGRAMMABLE GAIN AMPLIFIER (PGA)

PGA circuit provides the analog gain tuning output. The tuning range of the PGA gain is from -36 dB to +15 dB controlled by the registers, PGA0LG, PGA0RG, PGA1LG and PGA1RG, PGA2LG and PGA2RG. The default gain of PGA circuit is 0 dB and the detailed value is described in the following register map.

Name	Register address	Bit	Default	Description
PGA0LG	08H	5:0	13H	PGA0 L channel gain
PGA0RG	09H	5:0	13H	PGA0 R channel gain
PGA1LG	0AH	5:0	13H	PGA1 L channel gain
PGA1RG	0BH	5:0	13H	PGA1 R channel gain
PGA2LG	0CH	5:0	13H	PGA2 L channel gain
PGA2RG	0DH	5:0	13H	PGA2 R channel gain

6.1.2 HEADPHONE

Headphone circuit provides the output driven capability for 32 Ohm or 16 Ohm load. It also provides the analog gain tuning and the tuning range from 21 dB to -36 dB controlled by the registers, HPLA and HPRA. The default gain of headphone circuit is 0 dB and the detailed value is described in the following register map.

Name	Register address	Bit	Default	Description
HPLA	00H	5:0	13H	Headphone L channel gain
HPRA	01H	5:0	13H	Headphone R channel gain

6.2 PGA Gain Control

6.2.1 OUTPUT PGA GAIN CONTROL

It provides an output PGA to control the output volume.

Name	Register address	Bit	Default	Description
PGA0LG	0x08	5:0	0x13	Left channel PGA0 gain, see Table 1
PGA0RG	0x09	5:0	0x13	Right channel PGA0 gain, see Table 1
PGA1LG	0x0A	5:0	0x13	Left channel PGA1 gain, see Table 1
PGA1RG	0x0B	5:0	0x13	Right channel PGA1 gain, see Table 1
PGA2LG	0x0C	5:0	0x13	Left channel PGA2 gain, see Table 1
PGA2RG	0x0D	5:0	0x13	Right channel PGA2 gain, see Table 1

DAO0L/0R/1L/1R/2L/2R	Attenuation
0x00	-36 dB
0x01	-32 dB
0x02	-28 dB
0x03	-24 dB
0x04	-22 dB
0x05	-20 dB
0x06	-18 dB
0x07	-16 dB
0x08	-14 dB
0x09	-12 dB
0x0A	-10 dB
0x0B	-8 dB
0x0C	-7 dB (in -1 dB steps)
:	:
0x12	-1 dB
0x13 (default)	0 dB
:	:
0x1f	12 dB
:	:
0x22	15 dB

Table 1: DAC PGA Gain Mapping

6.2.2 HEADPHONE OUTPUT PGA GAIN CONTROL

There are analog output PGA controls for the headphone output.

Name	Register address	Bit	Default	Description
HP_GAINL	0x00	5:0	0x13	Headphone left channel PGA gain, see Table 2
HP_GAINR	0x01	5:0	0x13	Headphone right channel PGA gain, see Table 2
HP_GAINM	0x02	5:0	0x13	Headphone PGA gain control for both channel, see Table 2
HPLG_UPD	0x03	0	0x0	Update the PGA gain 0: store HP_GAINL and not change the output PGA gain 1: store HP_GAINL and update the output volume
HPRG_UPD	0x03	1	0x0	Update the PGA gain 0: store HP_GAINR and not change the output PGA gain 1: store HP_GAINR and update the output volume
HPMG_UPD	0x03	2	0x0	Update the PGA gain 0: store HP_GAINM and not change the output PGA gain 1: store HP_GAINM and update the output volume

HP_GAINL/R/M[4:0]	PGA gain
0x00	-36 dB
0x01	-32 dB
0x02	-28 dB
0x03	-24 dB
0x04	-22 dB
0x05	-20 dB
0x06	-18 dB
0x07	-16 dB
0x08	-14 dB
0x09	-12 dB
0x0A	-10 dB
0x0B	-8 dB
0x0C	-7 dB (in -1 dB step)
:	:

0x13	0 dB (default)
:	:
0x27	20 dB
0x28	21 dB

Table 1: Headphone PGA Gain Mapping

If the updated bit is 0, the PGA gain is written to the intermediate latch and not applied to the output PGA. If the updated bit is 1, the value stored in the intermediate latch is applied to the output PGA.

6.2.3 PGA MUTE CONTROL

The output PGA provides the mute control register.

Name	Register address	Bit	Default	Description
HPMUTEL	0x0F	0	0x1	Headphone left channel PGA mute enable 0: normal operation 1: PGA mute
HPMUTER		1	0x1	Headphone right channel PGA mute enable 0: normal operation 1: PGA mute
PGA0LMUTE		2	0x1	Left channel PGA0 mute enable 0: normal operation 1: PGA mute
PGA0RMUTE		3	0x1	Right channel PGA0 mute enable 0: normal operation 1: PGA mute
PGA1LMUTE		4	0x1	Left channel PGA1 mute enable 0: normal operation 1: PGA mute
PGA1RMUTE		5	0x1	Right channel PGA1 mute enable 0: normal operation 1: PGA mute
PGA2LMUTE		6	0x1	Left channel PGA2 mute enable 0: normal operation 1: PGA mute
PGA2RMUTE		7	0x1	Right channel PGA2 mute enable 0: normal operation 1: PGA mute

6.3 GPIO CONTROL

GPIO (General Purpose Input/Output) can be controlled by GPIO function enable bit, GPIO pad direction bit and driving strength bit:

Name	Register address	Bit	Default	Description
DGPIO[0]	0x27	0	0x0	GPIO 0 function enable bit 0: disable 1: enable
DGPIO[1]		1	0x0	GPIO 1 function enable bit 0: disable 1: enable
DGPIO[2]		2	0x0	GPIO 2 function enable bit 0: disable 1: enable
DGPIO[3]		3	0x0	GPIO 3 function enable bit 0: disable 1: enable
DGPIO[4]		4	0x0	GPIO 4 function enable bit 0: disable 1: enable
DGPIO[5]		5	0x0	GPIO 5 function enable bit 0: disable 1: enable
DGPIO[6]		6	0x0	GPIO 6 function enable bit 0: disable 1: enable
DGPIO[7]		7	0x0	GPIO 7 function enable bit 0: disable 1: enable
DGPIO[8]	0x28	0	0x0	GPIO 8 function enable bit 0: disable 1: enable
DGPIO[9]		1	0x0	GPIO 9 function enable bit 0: disable 1: enable

Name	Register address	Bit	Default	Description

DGPIO_PADCTL0[0]	0x29	0	0x0	GPIO 0 output enable bit 0: input 1: output
DGPIO_PADCTL0 [1]		1	0x1	GPIO 0 current driving strength bit 0 0: weak 1: strong
DGPIO_PADCTL0 [2]		2	0x1	GPIO 0 current driving strength bit 1 0: weak 1: strong
DGPIO_PADCTL0 [4]		4	0x0	GPIO 1 output enable bit 0: input 1: output
DGPIO_PADCTL0 [5]		5	0x1	GPIO 1 current driving strength bit 0 0: weak 1: strong
DGPIO_PADCTL0 [6]		6	0x1	GPIO 1 current driving strength bit 1 0: weak 1: strong

Name	Register address	Bit	Default	Description
DGPIO_PADCTL1[0]	0x2A	0	0x0	GPIO 2 output enable bit 0: input 1: output
DGPIO_PADCTL1 [1]		1	0x1	GPIO 2 current driving strength bit 0 0: weak 1: strong
DGPIO_PADCTL1 [2]		2	0x1	GPIO 2 current driving strength bit 1 0: weak 1: strong
DGPIO_PADCTL1 [4]		4	0x0	GPIO 3 output enable bit 0: input 1: output
DGPIO_PADCTL1 [5]		5	0x1	GPIO 3 current driving strength bit 0 0: weak 1: strong

DGPIO_PADCTL1 [6]		6	0x1	GPIO 3 current driving strength bit 1 0: weak 1: strong

Name	Register address	Bit	Default	Description
DGPIO_PADCTL2[0]	0x2B	0	0x0	GPIO 4 output enable bit 0: input 1: output
DGPIO_PADCTL2 [1]		1	0x1	GPIO 4 current driving strength bit 0 0: weak 1: strong
DGPIO_PADCTL2 [2]		2	0x1	GPIO 4 current driving strength bit 1 0: weak 1: strong
DGPIO_PADCTL2 [4]		4	0x0	GPIO 5 output enable bit 0: input 1: output
DGPIO_PADCTL2 [5]		5	0x1	GPIO 5 current driving strength bit 0 0: weak 1: strong
DGPIO_PADCTL2 [6]		6	0x1	GPIO 5 current driving strength bit 1 0: weak 1: strong

Name	Register address	Bit	Default	Description
DGPIO_PADCTL3[0]	0x2C	0	0x0	GPIO 6 output enable bit 0: input 1: output
DGPIO_PADCTL3 [1]		1	0x1	GPIO 6 current driving strength bit 0 0: weak 1: strong

DGPIO_PADCTL3 [2]		2	0x1	GPIO 6 current driving strength bit 1 0: weak 1: strong
DGPIO_PADCTL3 [4]		4	0x0	GPIO 7 output enable bit 0: input 1: output
DGPIO_PADCTL3 [5]		5	0x1	GPIO 7 current driving strength bit 0 0: weak 1: strong
DGPIO_PADCTL3 [6]		6	0x1	GPIO 7 current driving strength bit 1 0: weak 1: strong

Name	Register address	Bit	Default	Description
DGPIO_PADCTL4[0]	0x2D	0	0x0	GPIO 8 output enable bit 0: input 1: output
DGPIO_PADCTL4 [1]		1	0x1	GPIO 8 current driving strength bit 0 0: weak 1: strong
DGPIO_PADCTL4 [2]		2	0x1	GPIO 8 current driving strength bit 1 0: weak 1: strong
DGPIO_PADCTL4 [4]		4	0x0	GPIO 9 output enable bit 0: input 1: output
DGPIO_PADCTL4 [5]		5	0x1	GPIO 9 current driving strength bit 0 0: weak 1: strong
DGPIO_PADCTL4 [6]		6	0x1	GPIO 9 current driving strength bit 1 0: weak 1: strong

Name	Register address	Bit	Default	Description
DGPOUT[0]	0x2E	0	0x0	GPIO 0 output bit setting 0: set to 0 1: set to 1
DGPOUT[1]		1	0x0	GPIO 1 output bit setting 0: set to 0 1: set to 1
DGPOUT[2]		2	0x0	GPIO 2 output bit setting 0: set to 0 1: set to 1
DGPOUT[3]		3	0x0	GPIO 3 output bit setting 0: set to 0 1: set to 1
DGPOUT[4]		4	0x0	GPIO 4 output bit setting 0: set to 0 1: set to 1
DGPOUT[5]		5	0x0	GPIO 5 output bit setting 0: set to 0 1: set to 1
DGPOUT[6]		6	0x0	GPIO 6 output bit setting 0: set to 0 1: set to 1
DGPOUT[7]		7	0x0	GPIO 7 output bit setting 0: set to 0 1: set to 1
DGPOUT[8]	0x2F	0	0x0	GPIO 8 output bit setting 0: set to 0 1: set to 1
DGPOUT[9]		1	0x0	GPIO 9 output bit setting 0: set to 0 1: set to 1

6.5 POWER DOWN CONTROL

Once the left or the right channel or PGA output is powered down, all devices are turned off. The theoretical power consumption is therefore zero.

Name	Register address	Bit	Default	Description

AINPD	0x13	0	0x0	Analog input power down 0: power on 1: power down
PGA0PD[2:0]		1	0x0	PGA 0 power down 0: power on 1: power down
PGA1PD[2:0]		2	0x0	PGA 1 power down 0: power on 1: power down
PGA2PD[2:0]		3	0x0	PGA 2 power down 0: power on 1: power down
HPPD		4	0x0	Headphone PGA power down 0: power on 1: power down
PDRES		5	0x0	Analog RES power down 0: power on 1: power down

6.6 MULTIPLEXER GPIO CONTROL

While AMX[7:0] is set low, AIN1L/1R ~ AIN8L/8R is disconnected from multiplexer and connected to 1.65V. While GPIO function is used, ENGPIO[7:0] should be set high to disconnect PIN from 1.65V.

Name	Register address	Bit	Default	Description
ENPGIO	0X1A	0	0x0	Disconnect AIN1L and AIN1R to 1.65V when AMX[0] is low. 0: Connect to 1.65V 1: Disconnect
		1	0x0	Disconnect AIN2L and AIN2R to 1.65V when AMX[1] is low. 0: Connect to 1.65V 1: Disconnect
		2	0x0	Disconnect AIN3L and AIN3R to 1.65V when AMX[2] is low. 0: Connect to 1.65V 1: Disconnect

		3	0x0	Disconnect AIN4L and AIN4R to 1.65V when AMX[3] is low. 0: Connect to 1.65V 1: Disconnect
		4	0x0	Disconnect AIN5L and AIN5R to 1.65V when AMX[4] is low. 0: Connect to 1.65V 1: Disconnect
		5	0x0	Disconnect AIN6L and AIN6R to 1.65V when AMX[5] is low. 0: Connect to 1.65V 1: Disconnect
		6	0x0	Disconnect AIN7L and AIN7R to 1.65V when AMX[6] is low. 0: Connect to 1.65V 1: Disconnect
		7	0x0	Disconnect AIN8L and AIN8R to 1.65V when AMX[7] is low. 0: Connect to 1.65V 1: Disconnect

Analog Pin Pair [AIN1L/1R/2L/2R/…./8L/8R] also can be configured as normal GPIO (General Purpose Input/Output) and can be controlled by GPIO function enable bit, GPIO pad direction bit and driving strength bit: after setting up ENGPIO[7:0] (1Ah) to a specific value(please see the register map 1Ah for details)

Name	Register address	Bit	Default	Description
AGPIO_IES[0]	0x1B	0	0x0	GPIO pair 0 [AIN1L/1R]]function enable bit 0: disable (As analog pin pair) 1: enable (As GPIO)
AGPIO_IES[1]		1	0x0	GPIO pair 1 [AIN2L/2R]]function enable bit 0: disable (As analog pin pair) 1: enable (As GPIO)
AGPIO_IES[2]		2	0x0	GPIO pair 2 [AIN3L/3R]]function enable bit 0: disable (As analog pin pair) 1: enable (As GPIO)
AGPIO_IES[3]		3	0x0	GPIO pair 3 [AIN4L/4R]]function enable bit 0: disable (As analog pin pair) 1: enable (As GPIO)

AGPIO_IES[4]		4	0x0	GPIO pair 4 [AIN5L/5R]]function enable bit 0: disable (As analog pin pair) 1: enable (As GPIO)
AGPIO_IES[5]		5	0x0	GPIO pair 5 [AIN6L/6R]]function enable bit 0: disable (As analog pin pair) 1: enable (As GPIO)
AGPIO_IES[6]		6	0x0	GPIO pair 6 [AIN7L/7R]]function enable bit 0: disable (As analog pin pair) 1: enable (As GPIO)
AGPIO_IES[7]		7	0x0	GPIO pair 7 [AIN8L/8R]]function enable bit 0: disable (As analog pin pair) 1: enable (As GPIO)

Name	Register address	Bit	Default	Description
AGPIO_PD[0]	0x1C	0	0x0	GPIO pair 0 [AIN1L/1R]]function pull down when GPIO as GPI 0: no pull down 1: pull down
AGPIO_PD[1]		1	0x0	GPIO pair 1 [AIN2L/2R]]function pull down when GPIO as GPI 0: no pull down 1: pull down
AGPIO_PD[2]		2	0x0	GPIO pair 2 [AIN3L/3R]]function pull down when GPIO as GPI 0: pull down 1: no pull down
AGPIO_PD[3]		3	0x0	GPIO pair 3 [AIN4L/4R]]function pull down when GPIO as GPI 0: no pull down 1: pull down
AGPIO_PD[4]		4	0x0	GPIO pair 4 [AIN5L/5R]]function pull down when GPIO as GPI 0: pull down 1: no pull down
AGPIO_PD[5]		5	0x0	GPIO pair 5 [AIN6L/6R]]function pull down when GPIO as GPI 0: no pull down 1: pull down

AGPIO_PD[6]		6	0x0	GPIO pair 6 [AIN7L/7R]]function pull down when GPIO as GPI 0: no pull down 1: pull down
AGPIO_PD[7]		7	0x0	GPIO pair 7 [AIN8L/8R]]function pull down when GPIO as GPI 0: no pull down 1: pull down

Name	Register address	Bit	Default	Description
AGPIO_E[0]	0x1D	0	0x0	GPIO 0 [AIN1L] function direction bit 0: input 1: output
AGPIO_E[1]		1	0x0	GPIO 1 [AIN1R] function direction bit 0: input 1: output
AGPIO_E[2]		2	0x0	GPIO 2 [AIN2L] function direction bit 0: input 1: output
AGPIO_E[3]		3	0x0	GPIO 3 [AIN2R] function direction bit 0: input 1: output
AGPIO_E[4]		4	0x0	GPIO 4 [AIN3L] function direction bit 0: input 1: output
AGPIO_E[5]		5	0x0	GPIO 5 [AIN3R] function direction bit 0: input 1: output
AGPIO_E[6]		6	0x0	GPIO 6 [AIN4L] function direction bit 0: input 1: output
AGPIO_E[7]		7	0x0	GPIO 7 [AIN4R] function direction bit 0: input 1: output

Name	Register address	Bit	Default	Description
AGPIO_E[8]	0x1E	0	0x0	GPIO 8 [AIN5L] function direction bit 0: input 1: output
AGPIO_E[9]		1	0x0	GPIO 9 [AIN5R] function direction bit 0: input 1: output
AGPIO_E[10]		2	0x0	GPIO 10 [AIN6L] function direction bit 0: input 1: output
AGPIO_E[11]		3	0x0	GPIO 11 [AIN6R] function direction bit 0: input 1: output
AGPIO_E[12]		4	0x0	GPIO 12 [AIN7L] function direction bit 0: input 1: output
AGPIO_E[13]		5	0x0	GPIO 13 [AIN7R] function direction bit 0: input 1: output
AGPIO_E[14]		6	0x0	GPIO 14 [AIN8L] function direction bit 0: input 1: output
AGPIO_E[15]		7	0x0	GPIO 15 [AIN8R] function direction bit 0: input 1: output

Name	Register address	Bit	Default	Description
AGPIO_E2[0]	0x1F	0	0x1	GPIO 0 [AIN1L] function driving strength bit 0 0: weak 1: strong
AGPIO_E2[1]		1	0x1	GPIO 1 [AIN1R] function driving strength bit 0 0: weak 1: strong

AGPIO_E2[2]		2	0x1	GPIO 2 [AIN2L] function driving strength bit 0 0: weak 1: strong
AGPIO_E2[3]		3	0x1	GPIO 3 [AIN2R] function driving strength bit 0 0: weak 1: strong
AGPIO_E2[4]		4	0x1	GPIO 4 [AIN3L] function driving strength bit 0 0: weak 1: strong
AGPIO_E2[5]		5	0x1	GPIO 5 [AIN3R] function driving strength bit 0 0: weak 1: strong
AGPIO_E2[6]		6	0x1	GPIO 6 [AIN4L] function driving strength bit 0 0: weak 1: strong
AGPIO_E2[7]		7	0x1	GPIO 7 [AIN4R] function driving strength bit 0 0: weak 1: strong

Name	Register address	Bit	Default	Description
AGPIO_E2[8]	0x20	0	0x1	GPIO 8 [AIN5L] function driving strength bit 0 0: weak 1: strong
AGPIO_E2[9]		1	0x1	GPIO 9 [AIN5R] function driving strength bit 0 0: weak 1: strong
AGPIO_E2[10]		2	0x1	GPIO 10 [AIN6L] function driving strength bit 0 0: weak 1: strong
AGPIO_E2[11]		3	0x1	GPIO 11 [AIN6R] function driving strength bit 0 0: weak 1: strong
AGPIO_E2[12]		4	0x1	GPIO 12 [AIN7L] function driving strength bit 0 0: weak 1: strong

AGPIO_E2[13]		5	0x1	GPIO 13 [AIN7R] function driving strength bit 0 0: weak 1: strong
AGPIO_E2[14]		6	0x1	GPIO 14 [AIN8L] function driving strength bit 0 0: weak 1: strong
AGPIO_E2[15]		7	0x1	GPIO 15 [AIN8R] function driving strength bit 0 0: weak 1: strong

Name	Register address	Bit	Default	Description
AGPIO_E4[0]	0x21	0	0x1	GPIO 0 [AIN1L]] function driving strength bit 1 0: weak 1: strong
AGPIO_E4[1]		1	0x1	GPIO 1 [AIN1R]] function driving strength bit 1 0: weak 1: strong
AGPIO_E4[2]		2	0x1	GPIO 2 [AIN2L]] function driving strength bit 1 0: weak 1: strong
AGPIO_E4[3]		3	0x1	GPIO 3 [AIN2R]] function driving strength bit 1 0: weak 1: strong
AGPIO_E4[4]		4	0x1	GPIO 4 [AIN3L]] function driving strength bit 1 0: weak 1: strong
AGPIO_E4[5]		5	0x1	GPIO 5 [AIN3R]] function driving strength bit 1 0: weak 1: strong
AGPIO_E4[6]		6	0x1	GPIO 6 [AIN4L]] function driving strength bit 1 0: weak 1: strong
AGPIO_E4[7]		7	0x1	GPIO 7 [AIN4R]] function driving strength bit 1 0: weak 1: strong

Name	Register address	Bit	Default	Description
AGPIO_E4[8]	0x22	0	0x1	GPIO 8 [AIN5L]] function driving strength bit 1 0: weak 1: strong
AGPIO_E4[9]		1	0x1	GPIO 9 [AIN5R]] function driving strength bit 1 0: weak 1: strong
AGPIO_E4[10]		2	0x1	GPIO 10 [AIN6L]] function driving strength bit 1 0: weak 1: strong
AGPIO_E4[11]		3	0x1	GPIO 11 [AIN6R]] function driving strength bit 1 0: weak 1: strong
AGPIO_E4[12]		4	0x1	GPIO 12 [AIN7L]] function driving strength bit 1 0: weak 1: strong
DGPIO_E4[13]		5	0x1	GPIO 13 [AIN7R]] function driving strength bit1 0: weak 1: strong
DGPIO_E4[14]		6	0x1	GPIO 14 [AIN8L]] function driving strength bit 1 0: weak 1: strong
DGPIO_E4[15]		7	0x1	GPIO 15 [AIN8R]] function driving strength bit 1 0: weak 1: strong

Name	Register address	Bit	Default	Description
AGPIO[0]	0x23	0	0x0	Analog Pad as AIN1L function enable bit 0: disable 1: enable

AGPIO[1]		1	0x0	Analog Pad as AIN1R function enable bit 0: disable 1: enable
AGPIO[2]		2	0x0	Analog Pad as AIN2L function enable bit 0: disable 1: enable
AGPIO[3]		3	0x0	Analog Pad as AIN2R function enable bit 0: disable 1: enable
AGPIO[4]		4	0x0	Analog Pad as AIN3L function enable bit 0: disable 1: enable
AGPIO[5]		5	0x0	Analog Pad as AIN3R function enable bit 0: disable 1: enable
AGPIO[6]		6	0x0	Analog Pad as AIN4L function enable bit 0: disable 1: enable
AGPIO[7]		7	0x0	Analog Pad as AIN4R function enable bit 0: disable 1: enable

Name	Register address	Bit	Default	Description
AGPIO[8]	0x24	0	0x0	Analog Pad as AIN5L function enable bit 0: disable 1: enable
AGPIO[9]		1	0x0	Analog Pad as AIN5R function enable bit 0: disable 1: enable
AGPIO[10]		2	0x0	Analog Pad as AIN6L function enable bit 0: disable 1: enable

AGPIO[11]		3	0x0	Analog Pad as AIN6R function enable bit 0: disable 1: enable
AGPIO[12]		4	0x0	Analog Pad as AIN7L function enable bit 0: disable 1: enable
AGPIO[13]		5	0x0	Analog Pad as AIN7R function enable bit 0: disable 1: enable
AGPIO[14]		6	0x0	Analog Pad as AIN8L function enable bit 0: disable 1: enable
AGPIO[15]		7	0x0	Analog Pad as AIN8R function enable bit 0: disable 1: enable

Name	Register address	Bit	Default	Description
AGPOUT[0]	0x25	0	0x0	Analog Pad as AIN1L output bit setting 0: set to 0 1: set to 1
AGPOUT[1]		1	0x0	Analog Pad as AIN1R output bit setting 0: set to 0 1: set to 1
AGPOUT[2]		2	0x0	Analog Pad as AIN2L output bit setting 0: set to 0 1: set to 1
AGPOUT[3]		3	0x0	Analog Pad as AIN2R output bit setting 0: set to 0 1: set to 1
AGPOUT[4]		4	0x0	Analog Pad as AIN3L output bit setting 0: set to 0 1: set to 1

AGPOUT[5]		5	0x0	Analog Pad as AIN3R output bit setting 0: set to 0 1: set to 1
AGPOUT[6]		6	0x0	Analog Pad as AIN4L output bit setting 0: set to 0 1: set to 1
AGPOUT[7]		7	0x0	Analog Pad as AIN4R output bit setting 0: set to 0 1: set to 1

Name	Register address	Bit	Default	Description
AGPOUT[8]	0x26	0	0x0	Analog Pad as AIN5L output bit setting 0: set to 0 1: set to 1
AGPOUT[9]		1	0x0	Analog Pad as AIN5R output bit setting 0: set to 0 1: set to 1
AGPOUT[10]		2	0x0	Analog Pad as AIN6L output bit setting 0: set to 0 1: set to 1
AGPOUT[11]		3	0x0	Analog Pad as AIN6R output bit setting 0: set to 0 1: set to 1
AGPOUT[12]		4	0x0	Analog Pad as AIN7L output bit setting 0: set to 0 1: set to 1
AGPOUT[13]		5	0x0	Analog Pad as AIN7R output bit setting 0: set to 0 1: set to 1
AGPOUT[14]		6	0x0	Analog Pad as AIN8L output bit setting 0: set to 0 1: set to 1

AGPOUT[15]		7	0x0	Analog Pad as AIN8R output bit setting 0: set to 0 1: set to 1

7 Register Map

Register	Default	7	6	5	4	3	2	1	0
00h	13			HP_GAINL[5:0]					
01h	13			HP_GAINR[5:0]					
02h	13			HP_GAINM[5:0]					
03h	00						HPMG_UPD	HPRG_UPD	HPLG_UPD
08h	13			PGA0LG [5:0]					
09h	13			PGA0RG [5:0]					
0Ah	13			PGA1LG [5:0]					
0Bh	13			PGA1RG [5:0]					
0Ch	13			PGA2LG [5:0]					
0Dh	13			PGA2RG [5:0]					
0Fh	FF	PGA2RMUTE	PGA2LMUTE	PGA1RMUTE	PGA1LMUTE	PGAORMUTE	PGAOLMUTE	HPMUTER	HPMUTEL
10h	03							MUTERA	MUTELA
11h	00	AMX[7:0]							
13h	00			PDRES	HPPD	PGAPD[2:0]			AINPD
15h	10				RAMPMUTE_EN				
1Ah	00	ENGPIO[7:0]							
1Bh	00	AGPIO_IES[7:0]							
1Ch	00	AGPIO_PD[7:0]							
1Dh	00	AGPIO_E[7:0]							
1Eh	00	AGPIO_E[15:8]							
1Fh	FF	AGPIO_E2[7:0]							
20h	FF	AGPIO_E2[15:8]							
21h	FF	AGPIO_E4[7:0]							
22h	FF	AGPIO_E4[15:8]							
23h	00	AGPIO[7:0]							
24h	00	AGPIO[15:8]							
25h	00	AGPOUT[7:0]							
26h	00	AGPOUT[15:8]							
27h	00	DGPIO[7:0]							
28h	00								DGPIO8
29h	66	DGPIO_PADCTL1[7:0]							
2Ah	66	DGPIO_PADCTL2[7:0]							
2Bh	66	DGPIO_PADCTL3[7:0]							
2Ch	66	DGPIO_PADCTL4[7:0]							
2Dh	06	DGPIO_PADCTL5[7:0]							
2Eh	00	DGPOUT[7:0]							
2Fh	00								DGPOUT8
36h	XX	DGPIN[7:0]							
37h	XX							DGPIN[9:8]	

+00h Headphone Analog Attenuation Left

Bit	7	6	5	4	3	2	1	0
Name			**HP_GAINL[5:0]**					
Type			R/W					
Reset			0	1	0	0	1	1

HP_GAINL Attenuation data for headphone left.

00H -36dB
01H -32dB
02H -28dB
03H -24dB
04H -22dB
05H -20dB
06H -18dB
07H -16dB
08H -14dB
09H -12dB
0AH -10dB
0BH -8dB
0CH -7dB
0DH -6dB
………
13H 0dB
14H 1dB
15H 2dB
………
28H 21dB

+01h Headphone Analogue attenuation Right

Bit	7	6	5	4	3	2	1	0
Name			**HP_GAINR[5:0]**					
Type			R/W					
Reset			0	1	0	0	1	1

HP_GAINR Attenuation data for headphone right.

00H **-**36dB
01H **-**32dB
02H **-**28dB

03H -24dB
04H **-**22dB
05H **-**20dB
06H -18dB
07H -16dB
08H -14dB
09H -12dB
0AH -10dB
0BH -8dB
0CH -7dB
0DH -6dB
………..
13H 0dB
14H 1dB
15H 2dB
………..
28H 21dB

+02h Headphone Analog Attenuation Master

Bit	7	6	5	4	3	2	1	0
Name			**HP_GAINM[4:0]**					
Type			R/W					
Reset			0	1	0	0	1	1

HP_GAINM Attenuation data for headphone master.

00H **-**36dB
01H **-**32dB
02H **-**28dB
03H -24dB
04H **-**22dB
05H **-**20dB
06H -18dB
07H -16dB
08H -14dB
09H -12dB
0AH -10dB
0BH -8dB
0CH -7dB
0DH -6dB
………..

13H 0dB
14H 1dB
15H 2dB
………..
28H 21dB

+03h Headphone Analog attenuation Update

Bit	7	6	5	4	3	2	1	0
Name						**HPMG_UPD**	**HPRG_UPD**	**HPLG_UPD**
Type						R/W	R/W	R/W
Reset						0	0	0

HPLG_UPD Headphone attenuation update
0 don't care
1 update
HPRG_UPD Headphone attenuation update
0 don't care
1 update
HPMG_UPD Headphone attenuation update
0 don't care
1 update

+08h L-channel PGA0 Gain Setting

Bit	7	6	5	4	3	2	1	0
Name			**PGA0LG[5:0]**					
Type			R/W					
Reset			0	1	0	0	1	1

PGA0LG[5:0] L-channel PGA0 Gain Setting
00H **-**36dB
01H **-**32dB
02H **-**28dB
03H **-**24dB
04H **-**22dB
05H **-**20dB
06H **-**18dB
07H **-**16dB
08H **-**14dB

09H -12dB
0AH -10dB
0BH -8dB
0CH -7dB
0DH -6dB
………
13H 0dB
14H 1dB
15H 2dB
………
22H 15dB

+09h R-channel PGA0 Gain Setting

Bit	7	6	5	4	3	2	1	0
Name			**PGA0RG[5:0]**					
Type			R/W					
Reset			0	1	0	0	1	1

DAO0RG[5:0] R-channel PGA0 Gain Setting

00H -36dB
01H -32dB
02H -28dB
03H -24dB
04H -22dB
05H -20dB
06H -18dB
07H -16dB
08H -14dB
09H -12dB
0AH -10dB
0BH -8dB
0CH -7dB
0DH -6dB
………
13H 0dB
14H 1dB
15H 2dB
………
22H 15dB

+0Ah L-channel PGA1 Gain Setting

Bit	7	6	5	4	3	2	1	0
Name			**PGA1LG[5:0]**					
Type			R/W					
Reset			0	1	0	0	1	1

PGA1LG[5:0] L-channel PGA1 Gain Setting

00H -36dB
01H -32dB
02H -28dB
03H -24dB
04H -22dB
05H -20dB
06H -18dB
07H -16dB
08H -14dB
09H -12dB
0AH -10dB
0BH -8dB
0CH -7dB
0DH -6dB
………
13H 0dB
14H 1dB
15H 2dB
………
22H 15dB

+0Bh R-channel PGA1 Gain Setting

Bit	7	6	5	4	3	2	1	0
Name			**PGA1RG[5:0]**					
Type			R/W					
Reset			0	1	0	0	1	1

PGA1RG[5:0] R-channel PGA1 Gain Setting

00H -36dB

01H -32dB
02H -28dB
03H -24dB
04H -22dB
05H -20dB
06H -18dB
07H -16dB
08H -14dB
09H -12dB
0AH -10dB
0BH -8dB
0CH -7dB
0DH -6dB
………..
13H 0dB
14H 1dB
15H 2dB
………..
22H 15dB

+0Ch L-channel PGA2 Gain Setting

Bit	7	6	5	4	3	2	1	0
Name			**PGA2LG[5:0]**					
Type			R/W					
Reset			0	1	0	0	1	1

PGA2LG[5:0] L-channel PGA2 Gain Setting

00H -36dB
01H -32dB
02H -28dB
03H -24dB
04H -22dB
05H -20dB
06H -18dB
07H -16dB
08H -14dB
09H -12dB
0AH -10dB
0BH -8dB

0CH -7dB
0DH -6dB
………..
13H 0dB
14H 1dB
15H 2dB
………..
22H 15dB

+0Dh R-channel PGA2 Gain Setting

Bit	7	6	5	4	3	2	1	0
Name			**PGA2RG[5:0]**					
Type			R/W					
Reset			0	1	0	0	1	1

PGA2RG[5:0] R-channel PGA2 Gain Setting

00H **-**36dB
01H **-**32dB
02H **-**28dB
03H -24dB
04H **-**22dB
05H **-**20dB
06H -18dB
07H -16dB
08H -14dB
09H -12dB
0AH -10dB
0BH -8dB
0CH -7dB
0DH -6dB
………..
13H 0dB
14H 1dB
15H 2dB
………..
22H 15dB

+0Fh Channel Output PGA/Headphone Amplifier Mute Control

Bit	7	6	5	4	3	2	1	0
Name	**PGA2RMUTE**	**PGA2LMUTE**	**PGA1RMUTE**	**PGA1LMUTE**	**PGA0RMUTE**	**PGA0LMUTE**	**HPMUTER**	**HPMUTEL**
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

PGA2RMUTE R-channel output PGA2 mute
- **0** Disable Mute
- **1** Mute R-channel Output PGA2

PGA2LMUTE L-channel output PGA2 mute
- **0** Disable Mute
- **1** Mute L-channel Output PGA2

PGA1RMUTE R-channel output PGA1 mute
- **0** Disable Mute
- **1** Mute R-channel Output PGA1

PGA1LMUTE L-channel output PGA1 mute
- **0** Disable Mute
- **1** Mute L-channel Output PGA1

PGA0RMUTE R-channel output PGA0 mute
- **0** Disable Mute
- **1** Mute R-channel Output PGA0

PGA0LMUTE L-channel output PGA0 mute
- **0** Disable Mute
- **1** Mute L-channel Output PGA0

HPMUTER Headphone Amplifier R-channel mute
- **0** Disable Mute
- **1** Mute Headphone R-channel Output PGA

HPMUTEL Headphone Amplifier L-channel mute
- **0** Disable Mute
- **1** Mute Headphone L-channel Output PGA

+10h Analog MUX Input Control

Bit	7	6	5	4	3	2	1	0
Name							**MUTERA**	**MUTELA**
Type							R/W	R/W
Reset							0	0

MUTERA right channel mute
1 mute, no input to PGA
MUTELA left channel mute
1 mute, no input to PGA

+11h Input MUX Selection

Bit	7	6	5	4	3	2	1	0
Name	**AMX[7:0]**							
Type	R/W							
Reset	0	0	0	0	0	0	0	1

AMX[7:0] Input mux selection
1000000 select AIN8
0100000 select AIN6
……
0000001 select AIN1

+13h POWER DOWN REGISTER

Bit	7	6	5	4	3	2	1	0
Name			PDRES	HPPD	PGAPD[2:0]			AINPD
Type			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

AINPD Analog input power down
0 power on
1 power down

PGAOPD[0] PGA 0 power down
0 power on
1 power down

PGAOPD[1] PGA 1power down

0 power on
1 power down

PGAOPD[2] PGA 2 power down
0 power on
1 power down

HPPD Headphone PGA power down
0 power on
1 power down

PDRES Analog RES power down
0 power on
1 power down

+15h MUTE Control Register

Bit	7	6	5	4	3	2	1	0
Name				**RAMPMUTE_EN**				
Type				R/W				
Reset				1				

RAMPMUTE_EN Chanel 0, channel 1, channel 2 and Headphone PGA RAMPUTE control
0 disable
1 enable

+1Ah Disconnect MUX input

Bit	7	6	5	4	3	2	1	0
Name	**ENGPIO[7:0]**							
Type				R/W				
Reset	0	0	0	0	0	0	0	0

ENGPIO Disconnect MUX input (AMX[7:0] must also be 0)

+1Bh Analog Pin Pair convert to GPIO Function

Bit	7	6	5	4	3	2	1	0
Name	**AGPIO_IES[7:0]**							
Type				R/W				
Reset	0	0	0	0	0	0	0	0

AGPIO_IES[0] Convert analog pin as digital GPIO PAIR [AIN1L/AIN1R] function
0 analog pin usage
1 digital GPIO usage

AGPIO_IES[1] Convert analog pin as digital GPIO PAIR [AIN2L/AIN2R] function
0 analog pin usage
1 digital GPIO usage

AGPIO_IES[2] Convert analog pin as digital GPIO PAIR [AIN3L/AIN3R] function
0 analog pin usage
1 digital GPIO usage

AGPIO_IES[3] Convert analog pin as digital GPIO PAIR [AIN4L/AIN4R] function
0 analog pin usage
1 digital GPIO usage

AGPIO_IES[4] Convert analog pin as digital GPIO PAIR [AIN5L/AIN5R] function
0 analog pin usage
1 digital GPIO usage

AGPIO_IES[5] Convert analog pin as digital GPIO PAIR [AIN6L/AIN6R] function
0 analog pin usage
1 digital GPIO usage

AGPIO_IES[6] Convert analog pin as digital GPIO PAIR [AIN7L/AIN7R] function
0 analog pin usage
1 digital GPIO usage

AGPIO_IES[7] Convert analog pin as digital GPIO PAIR [AIN8L/AIN8R] function
0 analog pin usage
1 digital GPIO usage

+1Ch Analog PIN Pair convert to GPIO Function pull down bit

Bit	7	6	5	4	3	2	1	0
Name	**AGPIO_PD[7:0]**							
Type				R/W				
Reset	0	0	0	0	0	0	0	0

AGPIO_PD[0] **A**nalog pin pair [AIN1L/AIN1R] becomes GPIO function, you can use this bit to decide pull down when GPIO used as GPI

0 don't pull down

1 pull down

AGPIO_PD[1] **A**nalog pin pair [AIN2L/AIN2R] becomes GPIO function, you can use this bit to decide pull down when GPIO used as GPI

0 don't pull down

1 pull down

AGPIO_PD[2] **A**nalog pin pair [AIN3L/AIN3R] becomes GPIO function, you can use this bit to decide pull down when GPIO used as GPI

0 don't pull down

1 pull down

AGPIO_PD[3] **A**nalog pin pair [AIN4L/AIN4R] becomes GPIO function, you can use this bit to decide pull down when GPIO used as GPI

0 don't pull down

1 pull down

AGPIO_PD[4] **A**nalog pin pair [AIN5L/AIN5R] becomes GPIO function, you can use this bit to decide pull down when GPIO used as GPI

0 don't pull down

1 pull down

AGPIO_PD[5] **A**nalog pin pair [AIN6L/AIN6R] becomes GPIO function, you can use this bit to decide pull down when GPIO used as GPI

0 don't pull down

1 pull down

AGPIO_PD[6] **A**nalog pin pair [AIN7L/AIN7R] becomes GPIO function, you can use this bit to decide pull down when GPIO used as GPI

0 don't pull down

1 pull down

AGPIO_PD[7] **A**nalog pin pair [AIN8L/AIN8R] becomes GPIO function, you can use this bit to decide pull down when GPIO used as GPI

0 don't pull down

1 pull down

+1Dh Analog PIN Pair convert to GPIO Function Direction Bit

Bit	7	6	5	4	3	2	1	0
Name	**AGPIO_E[7:0]**							
Type				R/W				
Reset	0	0	0	0	0	0	0	0

AGPIO_E[0] **A**nalog pin [AIN1L] becomes GPIO function, you can use this bit to decide GPIO direction.

0 as input

1 as output

AGPIO_E[1] **A**nalog pin [AIN1R] becomes GPIO function, you can use this bit to decide GPIO direction.

0 as input

1 as output

AGPIO_E[2] **A**nalog pin [AIN2L] becomes GPIO function, you can use this bit to decide GPIO direction.

0 as input

1 as output

AGPIO_E[3] **A**nalog pin [AIN2R] becomes GPIO function, you can use this bit to decide GPIO direction.

0 as input

1 as output

AGPIO_E[4] **A**nalog pin [AIN3L] becomes GPIO function, you can use this bit to decide GPIO direction.

0 as input

1 as output

AGPIO_E[5] **A**nalog pin [AIN3R] becomes GPIO function, you can use this bit to decide GPIO direction.

0 as input

1 as output

AGPIO_E[6] **A**nalog pin [AIN4L] becomes GPIO function, you can use this bit to decide GPIO direction.

0 as input

1 as output

AGPIO_E[7] **A**nalog pin [AIN4R] becomes GPIO function, you can use this bit to decide GPIO direction.

0 as input

1 as output

+1Eh Analog PIN Pair convert to GPIO Function Direction Bit

Bit	7	6	5	4	3	2	1	0
Name	**AGPIO_E[15:8]**							
Type				R/W				
Reset	0	0	0	0	0	0	0	0

AGPIO_E[8] **A**nalog pin [AIN5L] becomes GPIO function, you can use this bit to decide GPIO direction.

0 as input

1 as output

AGPIO_E[9] **A**nalog pin [AIN5R] becomes GPIO function, you can use this bit to decide GPIO direction.

0 as input

1 as output

AGPIO_E[10] **A**nalog pin [AIN6L] becomes GPIO function, you can use this bit to decide GPIO direction.

0 as input

1 as output

AGPIO_E[11] **A**nalog pin [AIN6R] becomes GPIO function, you can use this bit to decide GPIO direction.

0 as input

1 as output

AGPIO_E[12] **A**nalog pin [AIN7L] becomes GPIO function, you can use this bit to decide GPIO direction.

0 as input

1 as output

AGPIO_E[13] **A**nalog pin [AIN7R] becomes GPIO function, you can use this bit to decide GPIO direction.

0 as input

1 as output

AGPIO_E[14] **A**nalog pin [AIN8L] becomes GPIO function, you can use this bit to decide GPIO direction.

0 as input

1 as output

AGPIO_E[15] **A**nalog pin [AIN8R] becomes GPIO function, you can use this bit to decide GPIO direction.

0 as input

1 as output

+1Fh Analog PIN Pair convert to GPIO Function Driving Strength Bit 0

Bit	7	6	5	4	3	2	1	0
Name	AGPIO_E2[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

AGPIO_E2[0] **A**nalog pin [AIN1L] becomes GPIO function, you can use this bit to decide GPIO driving strength.

0 weak

1 strong

AGPIO_E2[1] **A**nalog pin [AIN1R] becomes GPIO function, you can use this bit to decide GPIO driving strength..

0 weak

1 strong

AGPIO_E2[2] **A**nalog pin [AIN2L] becomes GPIO function, you can use this bit to decide GPIO driving strength

0 weak

1 strong

AGPIO_E2[3] **A**nalog pin [AIN2R] becomes GPIO function, you can use this bit to decide GPIO driving strength.

0 weak

1 strong

AGPIO_E2[4] **A**nalog pin [AIN3L] becomes GPIO function, you can use this bit to decide GPIO driving strength

0 weak

1 strong

AGPIO_E2[5] **A**nalog pin [AIN3R] becomes GPIO function, you can use this bit to decide GPIO driving strength.

0 weak

1 strong

AGPIO_E2[6] **A**nalog pin [AIN4L] becomes GPIO function, you can use this bit to decide GPIO driving strength

0 weak

1 strong

AGPIO_E2[7] **A**nalog pin [AIN4R] becomes GPIO function, you can use this bit to decide GPIO driving strength.

0 weak

1 strong

+20h Analog PIN Pair convert to GPIO Function Driving Strength Bit 0

Bit	7	6	5	4	3	2	1	0
Name	AGPIO_E2[15:8]							
Type				R/W				
Reset	1	1	1	1	1	1	1	1

AGPIO_E2[8] **A**nalog pin [AIN5L] becomes GPIO function, you can use this bit to decide GPIO driving strength.

0 weak

1 strong

AGPIO_E2[9] **A**nalog pin [AIN5R] becomes GPIO function, you can use this bit to decide GPIO driving strength..

0 weak

1 strong

AGPIO_E2[10] **A**nalog pin [AIN6L] becomes GPIO function, you can use this bit to decide GPIO driving strength

0 weak

1 strong

AGPIO_E2[11] **A**nalog pin [AIN6R] becomes GPIO function, you can use this bit to decide GPIO driving strength.

0 weak

1 strong

AGPIO_E2[12] **A**nalog pin [AIN7L] becomes GPIO function, you can use this bit to decide GPIO driving strength

0 weak

1 strong

AGPIO_E2[13] **A**nalog pin [AIN7R] becomes GPIO function, you can use this bit to decide GPIO driving strength.

0 weak

1 strong

AGPIO_E2[14] **A**nalog pin [AIN8L] becomes GPIO function, you can use this bit to decide GPIO driving strength

0 weak

1 strong

AGPIO_E2[15] **A**nalog pin [AIN8R] becomes GPIO function, you can use this bit to decide GPIO driving strength.

0 weak

1 strong

+21h Analog PIN Pair convert to GPIO Function Driving Strength Bit 1

Bit	7	6	5	4	3	2	1	0
Name	**AGPIO_E4[7:0]**							
Type				R/W				
Reset	1	1	1	1	1	1	1	1

AGPIO_E4[0] **A**nalog pin [AIN1L] becomes GPIO function, you can use this bit to decide GPIO driving strength.

0 weak

1 strong

AGPIO_E4[1] **A**nalog pin [AIN1R] becomes GPIO function, you can use this bit to decide GPIO driving strength..

0 weak

1 strong

AGPIO_E4[2] **A**nalog pin [AIN2L] becomes GPIO function, you can use this bit to decide GPIO driving strength

0 weak

1 strong

AGPIO_E4[3] **A**nalog pin [AIN2R] becomes GPIO function, you can use this bit to decide GPIO driving strength.

0 weak

1 strong

AGPIO_E4[4] **A**nalog pin [AIN3L] becomes GPIO function, you can use this bit to decide GPIO driving strength

0 weak

1 strong

AGPIO_E4[5] **A**nalog pin [AIN3R] becomes GPIO function, you can use this bit to decide GPIO driving strength.

0 weak

1 strong

AGPIO_E4[6] **A**nalog pin [AIN4L] becomes GPIO function, you can use this bit to decide GPIO driving strength

0 weak

1 strong

AGPIO_E4[7] **A**nalog pin [AIN4R] becomes GPIO function, you can use this bit to decide GPIO driving strength.

0 weak

1 strong

+22h Analog PIN Pair convert to GPIO Function Driving Strength Bit 1

Bit	7	6	5	4	3	2	1	0
Name	**AGPIO_E4[15:8]**							
Type				R/W				
Reset	1	1	1	1	1	1	1	1

AGPIO_E4[8] **A**nalog pin [AIN5L] becomes GPIO function, you can use this bit to decide GPIO driving strength.

0 weak
1 strong

AGPIO_E4[9] **A**nalog pin [AIN5R] becomes GPIO function, you can use this bit to decide GPIO driving strength..
0 weak
1 strong

AGPIO_E4[10] **A**nalog pin [AIN6L] becomes GPIO function, you can use this bit to decide GPIO driving strength
0 weak
1 strong

AGPIO_E4[11] **A**nalog pin [AIN6R] becomes GPIO function, you can use this bit to decide GPIO driving strength.
0 weak
1 strong

AGPIO_E4[12] **A**nalog pin [AIN7L] becomes GPIO function, you can use this bit to decide GPIO driving strength
0 weak
1 strong

AGPIO_E4[13] **A**nalog pin [AIN7R] becomes GPIO function, you can use this bit to decide GPIO driving strength.
0 weak
1 strong

AGPIO_E4[14] **A**nalog pin [AIN8L] becomes GPIO function, you can use this bit to decide GPIO driving strength
0 weak
1 strong

AGPIO_E4[15] **A**nalog pin [AIN8R] becomes GPIO function, you can use this bit to decide GPIO driving strength.

0 weak

1 strong

+23h Analog PAD as GPIO Function Enable 0

Bit	7	6	5	4	3	2	1	0
Name	AGPIO[7:0]							
Type				R/W				
Reset	0	0	0	0	0	0	0	0

AGPIO[7:0] ANALOG PAD AS GPIO FUNCTION ENABLE BIT

0 disable

1 enable, output configured by AGPOUT[7:0] if AGPIO_E[7:0] = 8'hff (as output mode)

+24h Analog PAD as GPIO Function Enable 1

Bit	7	6	5	4	3	2	1	0
Name	AGPIO[15:8]							
Type								
Reset							0	0

ADGPIO[15:8] ANALOG PAD AS GPIO FUNCTION ENABLE BIT

0 disable

1 enable, output configured by AGPOUT[15:8] if AGPIO_E[15:8] = 8'hff (as output mode)

+25h Analog PAD as GPIO Output Control 0

Bit	7	6	5	4	3	2	1	0
Name	AGPOUT[7:0]							
Type				R/W				
Reset	0	0	0	0	0	0	0	0

DGPOUT[7:0] ANALOG PAD AS GPIO OUTPUT CONTROL BIT

+26h Analog PAD as GPIO Output Control 1

Bit	7	6	5	4	3	2	1	0
Name	**AGPOUT[15:8]**							
Type							R/W	R/W
Reset							0	0

AGPOUT[15:8] **ANALOG PAD AS GPIO OUTPUT CONTROL BIT**

+27h GPIO Function Enable

Bit	7	6	5	4	3	2	1	0
Name	**DGPIO[7:0]**							
Type				R/W				
Reset	0	0	0	0	0	0	0	0

DGPIO[7:0] **GPIO FUNCTION ENABLE BIT**

0 disable
1 enable

+28h GPIO Function Enable 1

Bit	7	6	5	4	3	2	1	0
Name								**DGPIO8**
Type								R/W
Reset								0

DGPIO8 **GPIO FUNCTION ENABLE BIT**

0 disable
1 enable

+29h GPIO PAD Control 0

Bit	7	6	5	4	3	2	1	0
Name		**P1_E4**	**P1_E2**	**P1_E**		**P0_E4**	**P0_E2**	**P0_E**
Type		R/W	R/W	R/W		R/W	R/W	R/W

Reset		1	1	0		1	1	0

P0_E GPIO 0 DIRECTION BIT
0 input
1 output
P0_E2 GPIO 0 DRIVING STENGTH BIT1
0 weak
1 strong
P0_E4 GPIO 0 DRIVING STENGTH BIT2
0 weak
1 strong
P1_E GPIO 1 DIRECTION BIT
0 input
1 output
P1_E2 GPIO 1 DRIVING STENGTH BIT1
0 weak
1 strong
P1_E4 GPIO 1 DRIVING STENGTH BIT2
0 weak
1 strong

+2Ah GPIO PAD Control 1

Bit	7	6	5	4	3	2	1	0
Name		**P3_E4**	**P3_E2**	**P3_E**		**P2_E4**	**P2_E2**	**P2_E**
Type		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	1	0		1	1	0

P2_E GPIO 2 DIRECTION BIT
0 input
1 output
P2_E2 GPIO 2 DRIVING STENGTH BIT1
0 weak
1 strong
P2_E4 GPIO 2 DRIVING STENGTH BIT2
0 weak
1 strong
P3_E GPIO 3 DIRECTION BIT
0 input
1 output
P3_E2 GPIO 3 DRIVING STENGTH BIT1
0 weak
1 strong
P3_E4 GPIO 3 DRIVING STENGTH BIT2
0 weak
1 strong

+2Bh GPIO PAD Control 2

Bit	7	6	5	4	3	2	1	0
Name		**P5_E4**	**P5_E2**	**P5_E**		**P4_E4**	**P4_E2**	**P4_E**
Type		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	1	0		1	1	0

P4_E GPIO 4 DIRECTION BIT
0 input
1 output
P4_E2 GPIO 4 DRIVING STENGTH BIT1
0 weak
1 strong
P4_E4 GPIO 4 DRIVING STENGTH BIT2

0 weak
1 strong

P5_E GPIO 5 DIRECTION BIT
0 input
1 output

P5_E2 GPIO 5 DRIVING STENGTH BIT1
0 weak
1 strong

P5_E4 GPIO 5 DRIVING STENGTH BIT2
0 weak
1 strong

+2Ch GPIO PAD Control 3

Bit	7	6	5	4	3	2	1	0
Name		**P7_E4**	**P7_E2**	**P7_E**		**P6_E4**	**P6_E2**	**P6_E**
Type		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	1	0		1	1	0

P6_E GPIO 6 DIRECTION BIT
0 input
1 output

P6_E2 GPIO 6 DRIVING STENGTH BIT1
0 weak
1 strong

P6_E4 GPIO 6 DRIVING STENGTH BIT2
0 weak
1 strong

P7_E GPIO 7 DIRECTION BIT
0 input
1 output

P7_E2 GPIO 7 DRIVING STENGTH BIT1
0 weak
1 strong

P7_E4 GPIO 7 DRIVING STENGTH BIT2
0 weak
1 strong

+2Dh GPIO PAD Control 4

Bit	7	6	5	4	3	2	1	0
Name						**P8_E4**	**P8_E2**	**P8_E**
Type						R/W	R/W	R/W
Reset						1	1	0

P8_E GPIO 8 DIRECTION BIT

0 input

1 output

P8_E2 GPIO 8 DRIVING STENGTH BIT1

0 weak

1 strong

P8_E4 GPIO 8 DRIVING STENGTH BIT2

0 weak

1 strong

+2Eh GPIO Output Control 0

Bit	7	6	5	4	3	2	1	0
Name	**DGPOUT[7:0]**							
Type				R/W				
Reset	0	0	0	0	0	0	0	0

DGPOUT[7:0] GPIO OUTPUT CONTROL BIT

+2Fh GPIO Output Control 1

Bit	7	6	5	4	3	2	1	0
Name								**DGPOUT8**
Type								R/W
Reset								0

DGPOUT8 GPIO OUTPUT CONTROL BIT

+36h GPIO Input Control 0

Bit	7	6	5	4	3	2	1	0
Name	**DGPIN [7:0]**							
Type	R							

Reset	0	0	0	0	0	0	0	0

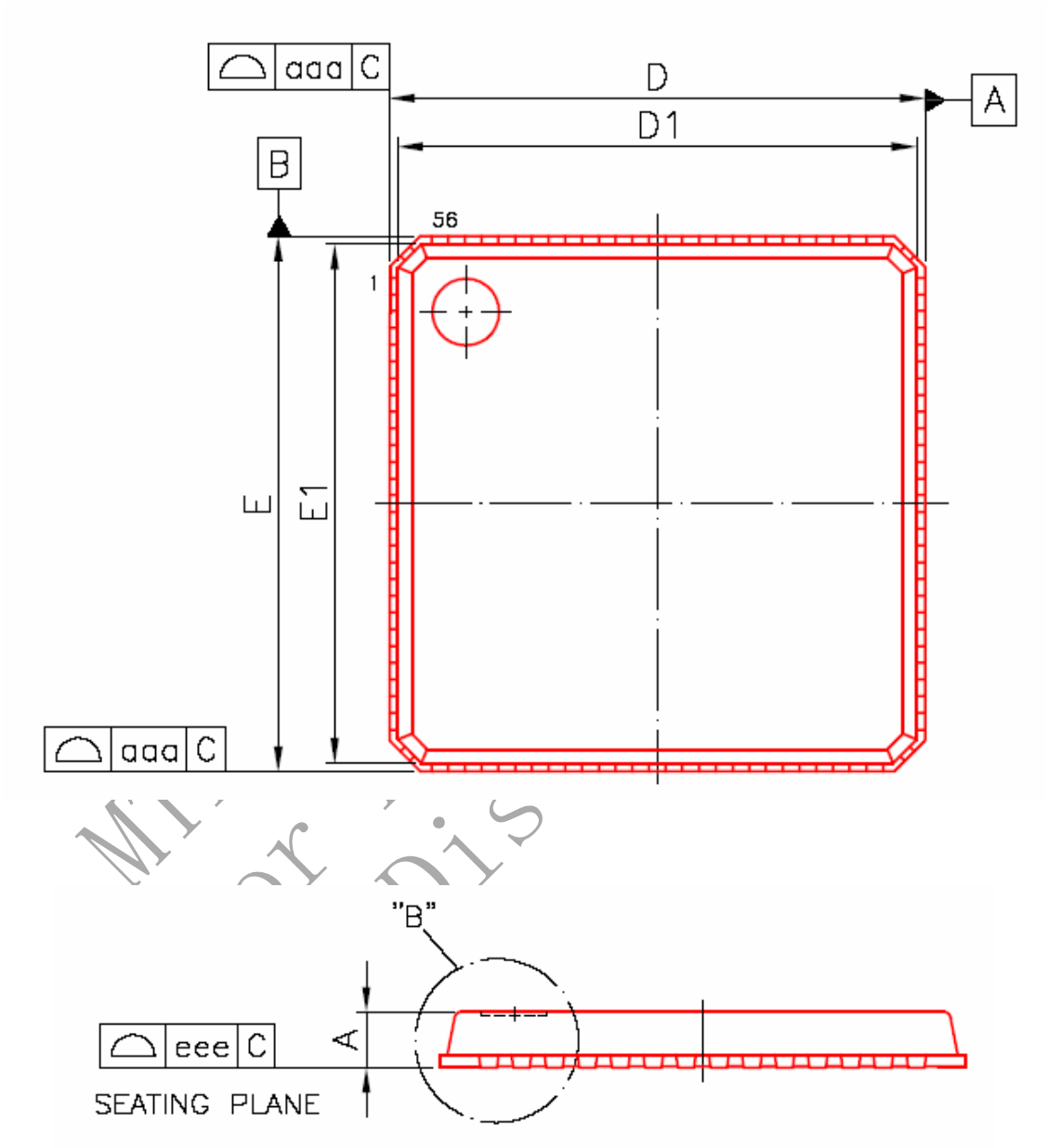
DGPIN[7:0] GPIO INPUT CONTROL BIT

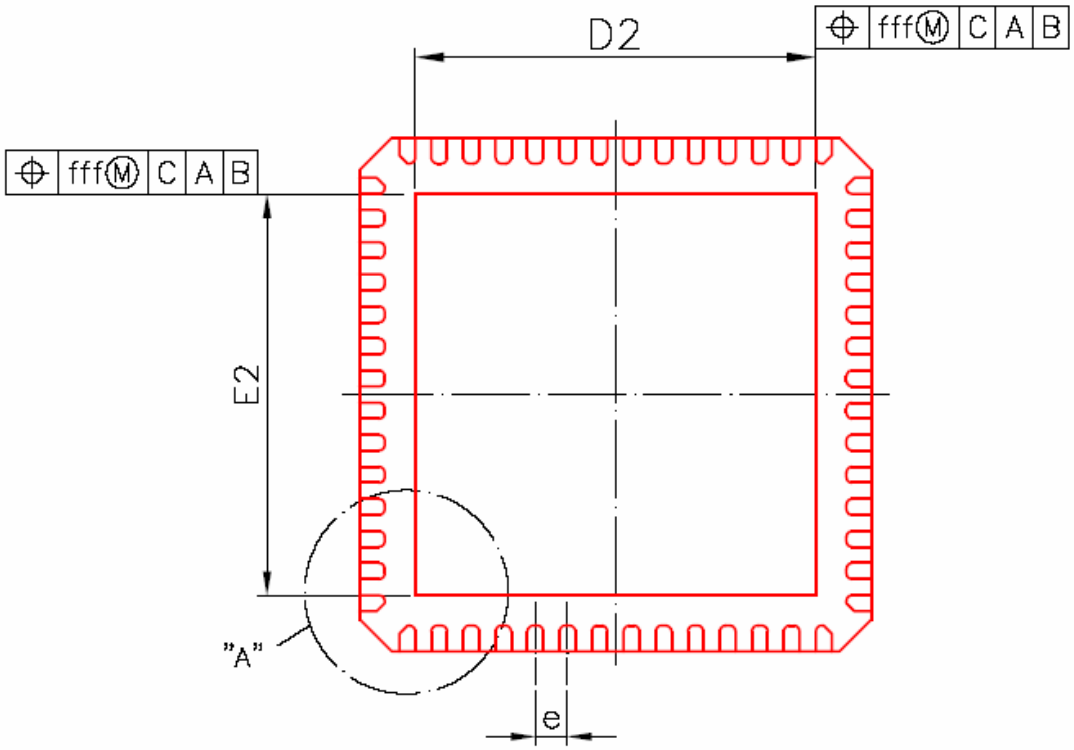
+37h GPIO Input Control 1

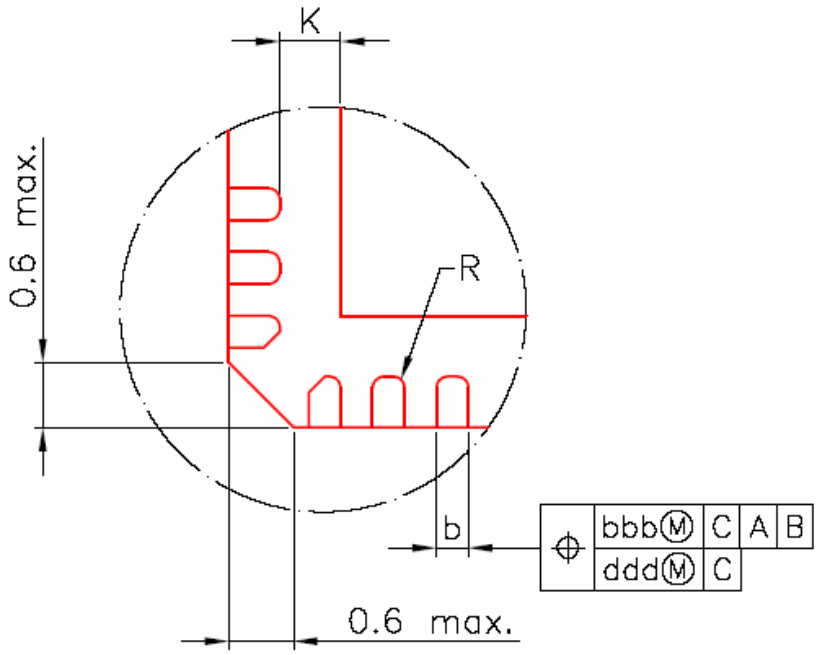
Bit	7	6	5	4	3	2	1	0
Name							**DGPIN[9:8]**	
Type	R							
Reset							0	0

DGPIN[9:8] GPIO INPUT CONTROL BIT

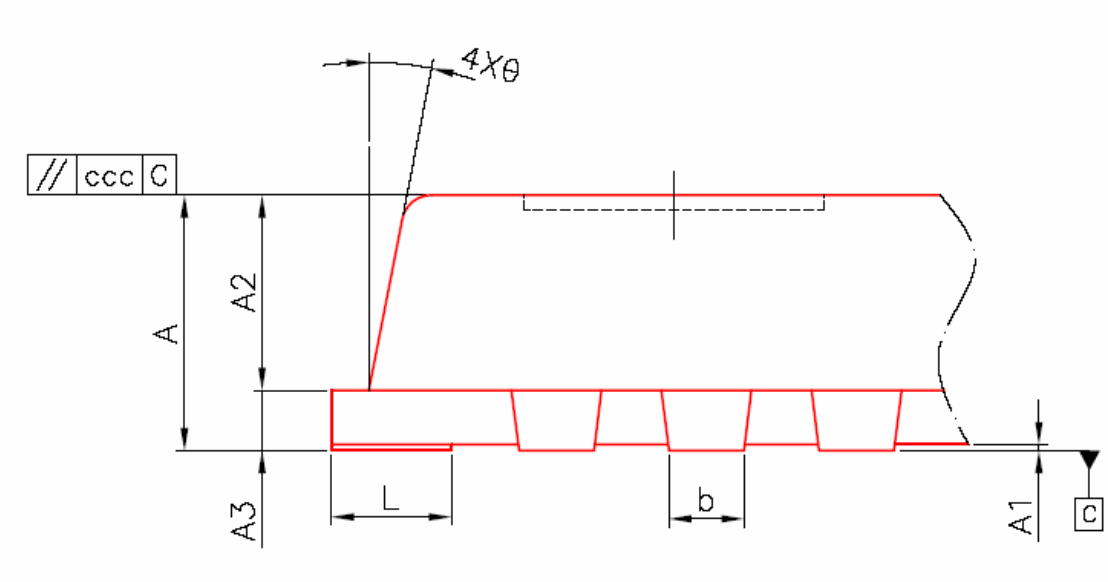
8 Package Mechanical Data (56-pin QFN)







DETAIL: A



DETAIL: B

Exposed Pad Size						
L/F	D2/E2(mm)			D2/E2(inch)		
	MIN	NOM	MAX	MIN	NOM	MAX
1	4.22	4.37	4.52	0.166	0.172	0.178
2	5.90	6.05	6.20	0.232	0.238	0.244

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	1.00	--	--	0.063
A1	0.00	0.02	0.05	0.002	--	0.006
A2	0.60	0.65	0.80	0.053	0.055	0.057
A2	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	8.00 BSC			0.315 BSC		
D1/E1	7.75 BSC			0.305 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	--	14°	0°	--	14°
R	0.09	--	--	0.004	--	--
K	0.20	--	--	0.008	--	--

aaa	**--**	**--**	**0.15**	**--**	**--**	**0.006**
bbb	**--**	**--**	**0.10**	**--**	**--**	**0.004**
ccc	**--**	**--**	**0.10**	**--**	**--**	**0.004**
ddd	**--**	**--**	**0.05**	**--**	**--**	**0.002**
eee	**--**	**--**	**0.08**	**--**	**--**	**0.003**
fff	**--**	**--**	**0.10**	**--**	**--**	**0.004**

NOTE:

1. CONTROLLING DIMENSION: MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.