Features

- Internal control latches and address decoder
- Short set-up and hold times
- Wide operating voltage: 4.5V to 13.2V
- 12Vpp analog signal capability
- R_{ON} 65Ω max. @ V_{DD}=12V, 25°C
- $\Delta R_{ON} \leq 10Ω$ @ V_{DD}=12V, 25°C
- Full CMOS switch for low distortion
- Minimum feedthrough and crosstalk
- Separate analog and digital reference supplies
- Low power consumption ISO-CMOS technology

Applications

- Key systems
- PBX systems
- Mobile radio
- Test equipment/instrumentation
- Analog/digital multiplexers
- Audio/Video switching

Ordering Information

MT8806AC	24 Pin Ceramic DIP
MT8806AE	24 Pin Plastic DIP
MT8806AP	28 Pin PLCC

-40° to 85°C

Description

The Mitel MT8806 is fabricated in MITEL's ISO-CMOS technology providing low power dissipation and high reliability. The device contains a 8 x 4 array of crosspoint switches along with a 5 to 32 line decoder and latch circuits. Any one of the 32 switches can be addressed by selecting the appropriate five address bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input. V_{SS} is the ground reference of the digital inputs. The range of the analog signal is from V_{DD} to V_{EE}. Chip Select (CS) allows the crosspoint array to be cascaded for matrix expansion.
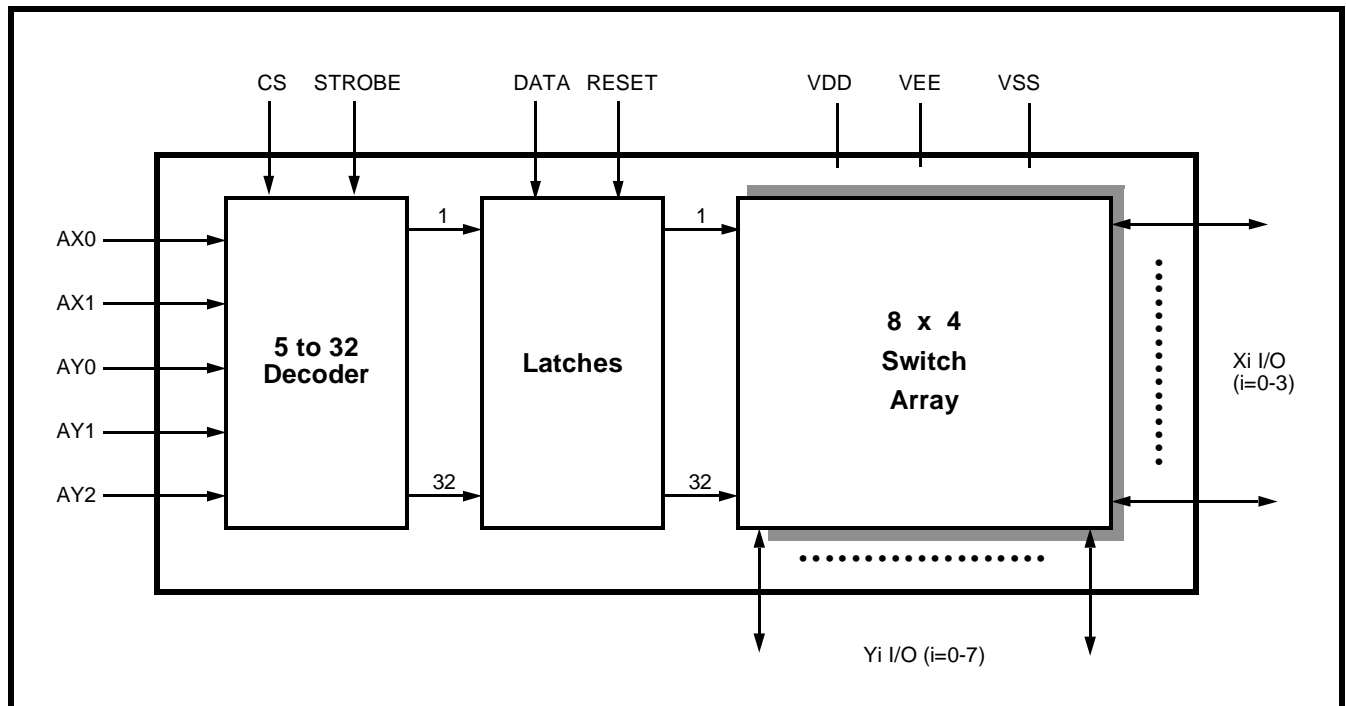

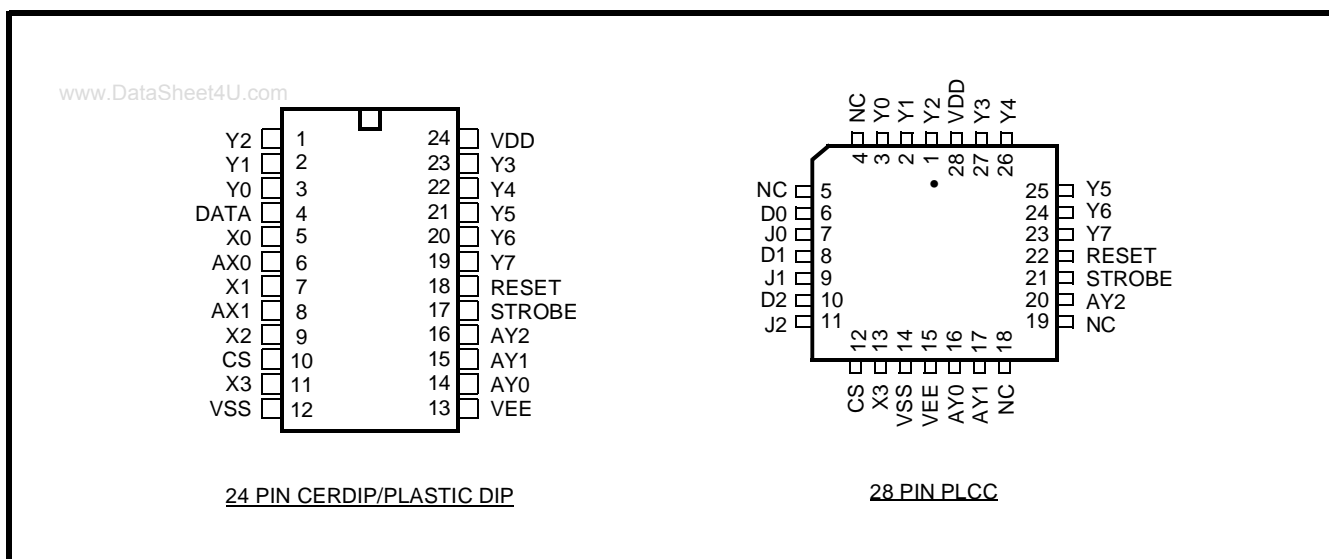**Figure 1 - Functional Block Diagram**

Figure 2 - Pin Connections

Pin Description

Pin #*	Name	Description
1-3	Y2-Y0	**Y2-Y0 Analog (Inputs/Outputs):** these are connected to the Y2-Y0 columns of the switch array.
4	DATA	**DATA (Input):** a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High.
5	X0	**X0 Analog (Input/Output):** this is connected to the X0 row of the switch array.
6	AX0	**X0 Address Line (Input).**
7	X1	**X1 Analog (Input/Output):** this is connected to the X1 row of the switch array.
8	AX1	**X1 Address Line (Input).**
9	X2	**X2 Analog (Input/Output):** this is connected to the X2 row of the switch array.
10	CS	**Chip Select (Input):** this is used to select the device. Active High.
11	X3	**X3 Analog (Input/Output):** this is connected to the X3 row of the switch array.
12	V_{SS}	**Digital Ground Reference.**
13	V_{EE}	**Negative Power Supply.**
14-16	AY0-AY2	**Y0 -Y2 Address Lines (Inputs).**
17	STROBE	**STROBE (Input):** enables function selected by address and data. Address must be stable before STROBE goes high and DATA must be stable on the falling edge of the STROBE. Active High.
18	RESET	**Master RESET (Input):** this is used to turn off all switches regardless of the condition of CS. Active High.
19-23	Y7-Y3	**Y7-Y3 Analog (Inputs/Outputs):** these are connected to the Y7-Y3 columns of the switch array.
24	VDD	**Positive Power Supply.**

* Plastic DIP and CERDIP only

Functional Description

The MT8806 is an analog switch matrix with an array size of 8 x 4. The switch array is arranged such that there are 8 columns by 4 rows. The columns are referred to as the Y inputs/outputs and the rows are the X inputs/outputs. The crosspoint analog switch array will interconnect any X I/O with any Y I/O when turned on and provide a high degree of isolation when turned off. The control memory consists of a 32 bit write only RAM in which the bits are selected by the address inputs (AY0-AY2, AX0 & AX1). Data is presented to the memory on the DATA input. Data is asynchronously written into memory whenever both the CS (Chip Select) and the STROBE inputs are high and is latched on the falling edge of STROBE. A logical "1" written into a memory cell turns the corresponding crosspoint switch on and a logical "0" turns the crosspoint off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y inputs/ outputs can be interconnected by establishing appropriate patterns in the control memory. A logical "1" on the RESET input will asynchronously return all memory locations to logical "0" turning off all crosspoint switches regardless of whether CS is high or low. Two voltage reference pins (V_{SS} and V_{EE}) are provided for the MT8806 to enable switching of negative analog signals. The range for digital signals is from V_{DD} to V_{SS} while the range for analog signals is from V_{DD} to V_{EE}. V_{SS} and V_{EE} pins can be tied together if a single voltage reference is needed.

Address Decode

The five address inputs along with the STROBE and CS (Chip Select) inputs are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, RESET must be low and CS must go high while the address and data are set up. Then the STROBE input is set high and then low causing the data to be latched. The data can be changed while STROBE is high, however, the corresponding switch will turn on and off in accordance with the DATA input. DATA must be stable on the falling edge of STROBE in order for correct data to be written to the latch.

MT8806 ISO-CMOS

Absolute Maximum Ratings*- Voltages are with respect to V$_{EE}$ unless otherwise stated.

	Parameter		Symbol	Min	Max	Units
1	Supply Voltage		V$_{DD}$	-0.3	15.0	V
			V$_{SS}$	-0.3	V$_{DD}$+0.3	V
2	Analog Input Voltage		V$_{INA}$	-0.3	V$_{DD}$+0.3	V
3	Digital Input Voltage		V$_{IN}$	V$_{SS}$-0.3	V$_{DD}$+0.3	V
4	Current on any I/O Pin		I		±15	mA
5	Storage Temperature		T$_S$	-65	+150	°C
6	Package Power Dissipation	PLASTIC DIP	P$_D$		0.6	W
		CERDIP	P$_D$		1.0	W

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to V$_{EE}$ unless otherwise stated.

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Operating Temperature	T$_O$	-40	25	85	°C	
2	Supply Voltage	V$_{DD}$	4.5		13.2	V	
		V$_{SS}$	V$_{EE}$		V$_{DD}$-4.5	V	
3	Analog Input Voltage	V$_{INA}$	V$_{EE}$		V$_{DD}$	V	
4	Digital Input Voltage	V$_{IN}$	V$_{SS}$		V$_{DD}$	V	

DC Electrical Characteristics†- Voltages are with respect to V$_{EE}$=V$_{SS}$=0V, V$_{DD}$=12V unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Quiescent Supply Current	I$_{DD}$		1	100	µA	All digital inputs at V$_{IN}$=V$_{SS}$ or V$_{DD}$
				0.4	1.5	mA	All digital inputs at V$_{IN}$=2.4 + V$_{SS}$; V$_{SS}$ =7.0V
				5	15	mA	All digital inputs at V$_{IN}$=3.4V
2	Off-state Leakage Current (See G.9 in Appendix)	I$_{OFF}$		±1	±500	nA	IV$_{Xi}$ - V$_{Yj}$I = V$_{DD}$ - V$_{EE}$ See Appendix, Fig. A.1
3	Input Logic "0" level	V$_{IL}$			0.8+V$_{SS}$	V	V$_{SS}$ =7.5V; V$_{EE}$=0V
4	Input Logic "1" level	V$_{IH}$	2.0+V$_{SS}$			V	V$_{SS}$ =6.5V; V$_{EE}$=0V
5	Input Logic "1" level	V$_{IH}$	3.3			V	
6	Input Leakage (digital pins)	I$_{LEAK}$		0.1	10	µA	All digital inputs at V$_{IN}$ = V$_{SS}$ or V$_{DD}$

† DC Electrical Characteristics are over recommended temperature range.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

DC Electrical Characteristics- Switch Resistance - V$_{DC}$ is the external DC offset applied at the analog I/O pins.

	Characteristics	Sym	25°C Typ	25°C Max	70°C Typ	70°C Max	85°C Typ	85°C Max	Units	Test Conditions
1	On-state Resistance V$_{DD}$=12V, V$_{DD}$=10V, V$_{DD}$= 5V (See G.1, G.2, G.3 in Appendix)	R$_{ON}$	45 55 120	65 75 185		75 85 215		80 90 225	Ω Ω Ω	V$_{SS}$=V$_{EE}$=0V,V$_{DC}$=V$_{DD}$/2, IV$_{Xi}$-V$_{Yj}$I = 0.4V See Appendix, Fig. A.2
2	Difference in on-state resistance between two switches (See G.4 in Appendix)	ΔR$_{ON}$	5	10		10		10	Ω	V$_{DD}$=12V, V$_{SS}$=V$_{EE}$=0, V$_{DC}$=V$_{DD}$/2, IV$_{Xi}$-V$_{Yj}$I = 0.4V See Appendix, Fig. A.2

AC Electrical Characteristics[†] - Crosspoint Performance - Voltages are with respect to V_{DD}=5V, V_{SS}=0V, V_{EE}=-7V, unless otherwise stated.

	Characteristics	Sym	Min	Typ[‡]	Max	Units	Test Conditions
1	Switch I/O Capacitance	C_S		20		pF	f=1 MHz
2	Feedthrough Capacitance	C_F		0.2		pF	f=1 MHz
3	Frequency Response Channel "ON" $20LOG(V_{OUT}/V_{Xi})$=-3dB	F_{3dB}		45		MHz	Switch is "ON"; V_{INA} = 2Vpp sinewave; R_L = 1kΩ See Appendix, Fig. A.3
4	Total Harmonic Distortion (See G.5, G.6 in Appendix)	THD		0.01		%	Switch is "ON"; V_{INA} = 2Vpp sinewave f= 1kHz; R_L=1kΩ
5	Feedthrough Channel "OFF" Feed.=$20LOG (V_{OUT}/V_{Xi})$ (See G.8 in Appendix)	FDT		-95		dB	All Switches "OFF"; V_{INA}= 2Vpp sinewave; f= 1kHz; R_L = 1kΩ. See Appendix, Fig. A.4
6	Crosstalk between any two channels for switches Xi-Yi and Xj-Yj. Xtalk=$20LOG (V_{Yj}/V_{Xi})$. (See G.7 in Appendix).	X_{talk}		-45		dB	V_{INA}=2Vpp sinewave f= 10MHz; R_L = 75Ω.
				-90		dB	V_{INA}=2Vpp sinewave f= 10kHz; R_L = 600Ω.
				-85		dB	V_{INA}=2Vpp sinewave f= 10kHz; R_L = 1kΩ.
				-80		dB	V_{INA}=2Vpp sinewave f= 1kHz; R_L = 10kΩ. Refer to Appendix, Fig. A.5 for test circuit.
7	Propagation delay through switch	t_{PS}			30	ns	R_L=1kΩ; C_L=50pF

† Timing is over recommended temperature range. See Fig. 3 for control and I/O timing details.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
Crosstalk measurements are for Plastic DIPS only, crosstalk values for PLCC packages are approximately 5dB better.

AC Electrical Characteristics[†] - Control and I/O Timings - Voltages are with respect to V_{DD}=5V, V_{SS}=0V, V_{EE}=-7V, unless otherwise stated.

	Characteristics	Sym	Min	Typ[‡]	Max	Units	Test Conditions
1	Control Input crosstalk to switch (for CS, DATA, STROBE, Address)	CX_{talk}		30		mVpp	V_{IN}=3V squarewave; R_{IN}=1kΩ, R_L=10kΩ. See Appendix, Fig. A.6
2	Digital Input Capacitance	C_{DI}		10		pF	f=1MHz
3	Switching Frequency	F_O			20	MHz	
4	Setup Time DATA to STROBE	t_{DS}	10			ns	R_L= 1kΩ, C_L=50pF ①
5	Hold Time DATA to STROBE	t_{DH}	10			ns	R_L= 1kΩ, C_L=50pF ①
6	Setup Time Address to STROBE	t_{AS}	10			ns	R_L= 1kΩ, C_L=50pF ①
7	Hold Time Address to STROBE	t_{AH}	10			ns	R_L= 1kΩ, C_L=50pF ①
8	Setup Time CS to STROBE	t_{CSS}	10			ns	R_L= 1kΩ, C_L=50pF ①
9	Hold Time CS to STROBE	t_{CSH}	10			ns	R_L= 1kΩ, C_L=50pF ①
10	STROBE Pulse Width	t_{SPW}	20			ns	R_L= 1kΩ, C_L=50pF ①
11	RESET Pulse Width	t_{RPW}	40			ns	R_L= 1kΩ, C_L=50pF ①
12	STROBE to Switch Status Delay	t_S		40	100	ns	R_L= 1kΩ, C_L=50pF ①
13	DATA to Switch Status Delay	t_D		50	100	ns	R_L= 1kΩ, C_L=50pF ①
14	RESET to Switch Status Delay	t_R		35	100	ns	R_L= 1kΩ, C_L=50pF ①

† Timing is over recommended temperature range. See Fig. 3 for control and I/O timing details.
Digital Input rise time (tr) and fall time (tf) = 5ns.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
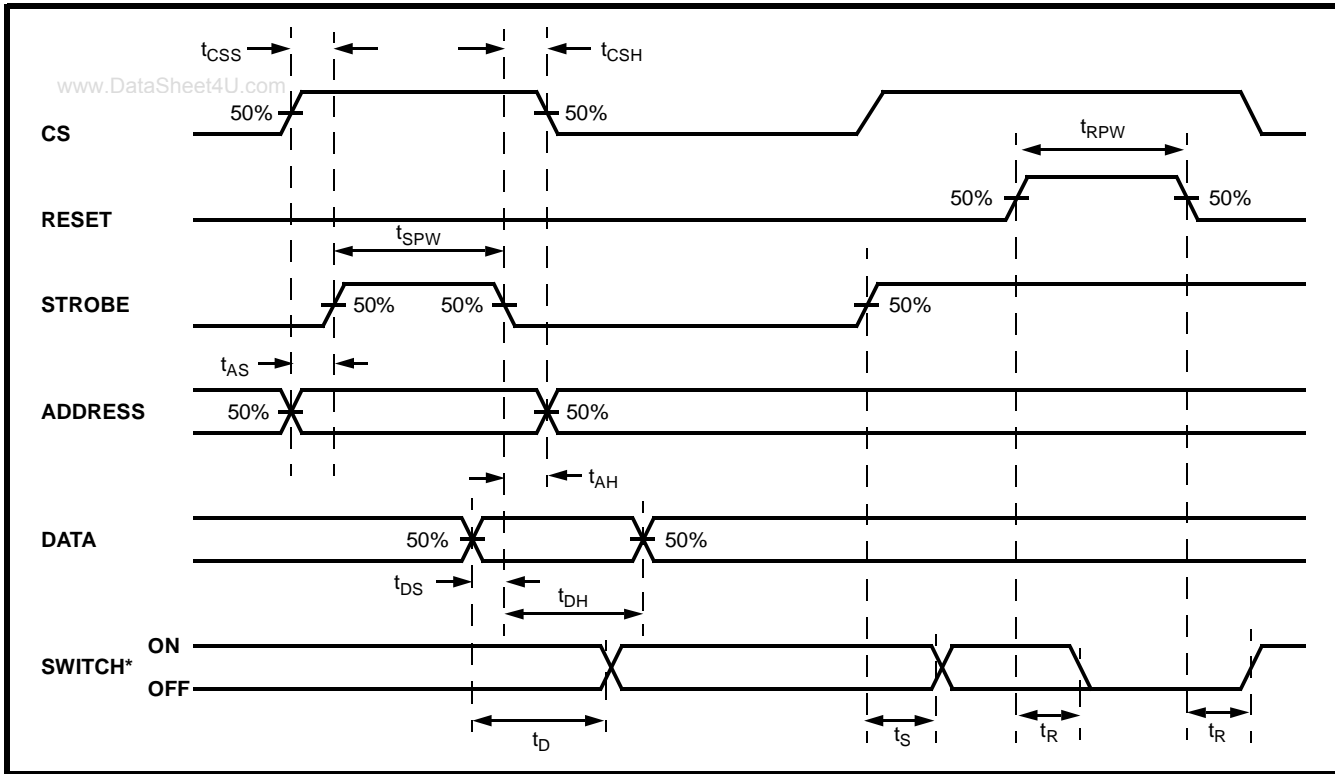① Refer to Appendix, Fig. A.7 for test circuit.

Figure 3 - Control Memory Timing Diagram

t_CSS t_CSH CS 50% 50% t_RPW

RESET 50% 50%

t_SPW STROBE 50% 50% 50%

t_AS ADDRESS 50% 50%

t_AH DATA 50% 50%

t_DS t_DH

SWITCH* ON OFF

t_D t_S t_R t_R

* See Appendix, Fig. A.7 for switching waveform

AX0	AX1	AY0	AY1	AY2	Connection
0	0	0	0	0	X0-Y0
0	0	1	0	0	X0-Y1
0	0	0	1	0	X0-Y2
0	0	1	1	0	X0-Y3
0	0	0	0	1	X0-Y4
0	0	1	0	1	X0-Y5
0	0	0	1	1	X0-Y6
0	0	1	1	1	X0-Y7
1 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	0 ↓ 1	X1-Y0 ↓ ↓ X1-Y7
0 ↓ 0	1 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	X2-Y0 ↓ ↓ X2-Y7
1 ↓ 1	1 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	X3-Y0 ↓ ↓ X3-Y7

Table 1. Address Decode Truth Table