 MITEL®

ISO²-CMOS MT8880/MT8880-1/MT8880-2
Integrated DTMF Transceiver
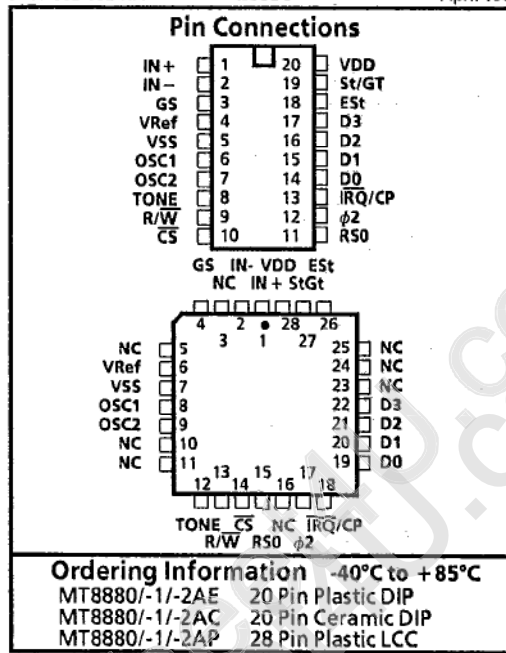
T-75-27-11

Features
- Complete DTMF transmitter/receiver
- Central office quality
- Low power consumption
- Microprocessor port
- Adjustable guard time
- Automatic tone burst mode
- Call progress mode

Applications
- Credit card systems
- Paging systems
- Repeater systems/mobile radio
- Interconnect dialers
- Personal computers

Description

The MT8880 is a monolithic DTMF transceiver with call progress filter. It is fabricated in Mitel's ISO²-CMOS technology which provides low power dissipation and high reliability. The DTMF receiver is based upon the industry standard MT8870 monolithic DTMF receiver; the transmitter utilizes a switched capacitor D/A converter for low distortion, high accuracy DTMF signalling. Internal counters provide a burst mode such that tone bursts can be transmitted with precise timing. A call progress filter can be selected allowing a microprocessor to analyze call progress tones. A standard microprocessor bus is provided and is directly compatible with 6800 series microprocessors. The

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Pin Connections

IN+	1	20	VDD
IN−	2	19	St/GT
GS	3	18	ESt
VRef	4	17	D3
VSS	5	16	D2
OSC1	6	15	D1
OSC2	7	14	D0
TONE	8	13	IRQ/CP
R/W	9	12	φ2
CS	10	11	RS0

GS   IN− VDD ESt
NC   IN+ StGt

NC 5, VRef 6, VSS 7, OSC1 8, OSC2 9, NC 10, NC 11
25 NC, 24 NC, 23 NC, 22 D3, 21 D2, 20 D1, 19 D0

TONE CS NC IRQ/CP
R/W RS0 φ2

Ordering Information   −40°C to +85°C
MT8880/-1/-2AE   20 Pin Plastic DIP
MT8880/-1/-2AC   20 Pin Ceramic DIP
MT8880/-1/-2AP   28 Pin Plastic LCC

MT8880-1 is functionally identical to the MT8880 except for the performance of the receiver section which is enhanced to accept lower signal levels and specifies signal level rejection. The MT8880-2 is electrically identical to the MT8880 but does not offer the call progress function.
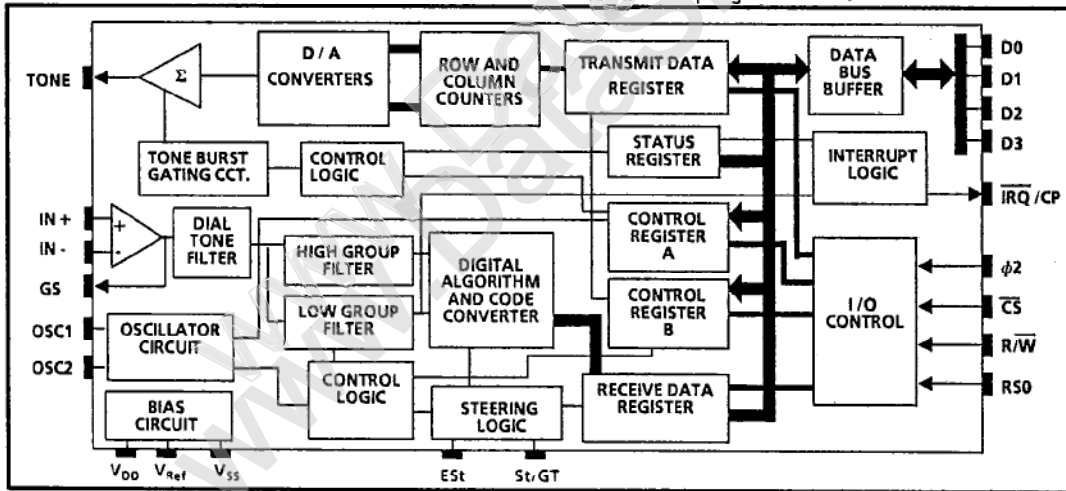

Figure 1- Functional Block Diagram

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Power supply voltage V_{DD}-V_{SS}	V_{DD}		6	V
2	Voltage on any pin	V_I	$V_{SS}-0.3$	$V_{DD}+0.3$	V
3	Current at any pin (Except V_{DD} and V_{SS})			10	mA
4	Storage temperature	T_{ST}	-65	$+150$	°C
5	Package power dissipation	P_D		1000	mW

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Positive power supply	V_{DD}	4.75	5.00	5.25	V	
2	Operating temperature	T_O	-40		$+85$	°C	
3	$\Phi 2$ clock frequency	f_C	0.001		1.0	MHz	
4	Crystal clock frequency	f_{CLK}	3.575965	3.579545	3.583124	MHz	

‡ Typical figures are at 25 °C and for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics† - $f_C = 3.579545$ MHz, $\phi2 = 1$ MHz, $V_{SS} = 0$ V.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	S U P	Operating supply voltage	V_{DD}	4.75	5.0	5.25	V	
2		Operating supply current	I_{DD}			10	mA	
3		Power consumption	P_C			52.5	mW	
4	I N P U T S	High level input voltage (OSC1)	V_{IHO}	3.5			V	
5		Low level input voltage (OSC1)	V_{ILO}			1.5	V	
6		Steering threshold voltage	V_{TSt}	2.2	2.3	2.5	V	$V_{DD}=5$ V
7	O U T P U T S	Low level output voltage (OSC2)	V_{OLO}			0.1	V	No load
8		High level output voltage (OSC2)	V_{OHO}	4.9			V	No load
9		Output leakage current (IRQ)	I_{OZ}		1	10	µA	$V_{OH}=2.4$ V
10		V_{Ref} output voltage	V_{Ref}	2.4	2.5	2.7	V	No load
11		V_{Ref} output resistance	R_{OR}			1	kΩ	
12	D A T A	Low level input voltage	V_{IL}			0.8	V	
13		High level input voltage	V_{IH}	2.0			V	
14		Source current	I_{OH}	-1.4	-6.6		mA	$V_{OH}=2.4$V
15	B U S	Sink current	I_{OL}	2.0	4.0		mA	$V_{OL}=0.4$V
16		Input leakage current	I_{IZ}			10	µA	$V_{IN}=0.4$ to 2.4 V
17	ESt and StGt	Source current	I_{OH}	-0.02	-0.9		mA	$V_{OH}=4.6$V
18		Sink current	I_{OL}	1.0	2.7		mA	$V_{OL}=0.4$V
19	$\overline{IRQ}/$ CP	Sink current	I_{OL}	4	16		mA	$V_{OL}=0.4$V

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25 °C, $V_{DD} = 5$V and for design aid only: not guaranteed and not subject to production testing.

Electrical Characteristics

Gain Setting Amplifier - Voltages are with respect to ground (V_{SS}) unless otherwise stated, V_{SS} = 0 V, V_{DD}=5V, T_O=25°C.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input leakage current	I_{IN}		±100		nA	$V_{SS} \leq V_{IN} \leq V_{DD}$
2	Input resistance	R_{IN}		10		MΩ	
3	Input offset voltage	V_{OS}		25		mV	
4	Power supply rejection	PSRR		60		dB	1 kHz
5	Common mode rejection	CMRR		60		dB	-3.0 V ≤ V_{IN} ≤ 3.0 V
6	DC open loop voltage gain	A_{VOL}		65		dB	
7	Unity gain bandwidth	BW		1.5		MHz	
8	Output voltage swing	V_O		4.5		V_{pp}	$R_L \geq$ 100 kΩ to V_{SS}
9	Allowable capacitive load (GS)	C_L		100		pF	
10	Allowable resistive load (GS)	R_L		50		kΩ	
11	Common mode range	V_{CM}		3.0		V_{pp}	No Load

‡ Typical figures are at 25°C and for design aid only: not guaranteed and not subject to production testing.

MT8880-1 AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ	Max	Units	Notes*
1	R X	Valid input signal levels (each tone of composite signal)		-31			dBm	1,2,3,5,6,9
				21.8			mV_{RMS}	1,2,3,5,6,9
						+1	dBm	1,2,3,5,6,9
						869	mV_{RMS}	1,2,3,5,6,9
2		Input Signal Level Reject		-37			dBm	1,2,3,5,6,9
				10.9			mV_{RMS}	1,2,3,5,6,9

† V_{DD}=5 V, V_{SS}=0 , T_A=25°C, Φ2=1MHz and f_c=3.579545 MHz using test circuit shown in Figure 15.

MT8880/8880-2 AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
1	R X	Valid Input signal levels (each tone of composite signal)		-29			dBm	1,2,3,5,6,9
				27.5			mV_{RMS}	1,2,3,5,6,9
						+1	dBm	1,2,3,5,6,9
						869	mV_{RMS}	1,2,3,5,6,9

† V_{DD}=5 V, V_{SS}=0 , T_A=25°C, Φ2=1MHz and f_c=3.579545 MHz using test circuit shown in Figure 15.

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.
V_{SS} = 0 V, Φ2 = 1 MHz f_c = 3.579545 MHz.

		Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
1		Positive twist accept				6	dB	2,3,6,9
2		Negative twist accept				6	dB	2,3,6,9
3	R X	Freq. deviation accept		±1.5% ± 2Hz				2,3,5,9
4		Freq. deviation reject		±3.5%				2,3,5
5		Third tone tolerance			-16		dB	2,3,4,5,9,10
6		Noise tolerance			-12		dB	2,3,4,5,7,9,10
7		Dial tone tolerance			22		dB	2,3,4,5,8,9,11

†Characteristics are over recommended operating conditions unless otherwise stated
‡ Typical figures are at 25°C, V_{DD} = 5V, and for design aid only: not guaranteed and not subject to production testing
*See "Notes" following AC Electrical Characteristics Tables

AC Electrical Characteristics'- Call Progress - Voltages are with respect to ground (V$_{SS}$) unless otherwise stated

V$_{SS}$ = 0 V, $\Phi2$ = 1 MHz f$_C$ = 3.579545 MHz

	Characteristics	Sym	Min	Typ^t	Max	Units	Notes*
1	Lower freq. (ACCEPT)	f$_{LA}$		320		Hz	@ −25 dBm
2	Upper freq. (ACCEPT)	f$_{HA}$		510		Hz	@ −25 dBm
3	Lower freq. (REJECT)	f$_{LR}$		290		Hz -	@ −25 dBm
4	Upper freq. (REJECT)	f$_{HR}$		540		Hz	@ −25 dBm

†Characteristics are over recommended operating conditions unless otherwise stated
‡ Typical figures are at 25°C, V$_{DD}$ = 5V, and for design aid only: not guaranteed and not subject to production testing
*See "Notes" AC Electrical Characteristics Tables

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AC Electrical Characteristics ' - Voltages are with respect to ground (V$_{SS}$) unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Conditions
1	R X	Tone present detect time	t$_{DP}$	3	11	14	ms	Note 12
2		Tone absent detect time	t$_{DA}$	0.5	4	8.5	ms	Note 12
3		Tone duration accept	t$_{REC}$			40	ms	User adjustable#
4		Tone duration reject	t$_{\overline{REC}}$	20			ms	User adjustable#
5		Interdigit pause accept	t$_{ID}$			40	ms	User adjustable#
6		Interdigit pause reject	t$_{DO}$	20			ms	User adjustable#
7		Delay St to b3	t$_{PStb3}$		13		μs	
8		Delay St to RX$_0$-RX$_3$	t$_{PStRX}$		8		μs	
9	T X	Tone burst duration	t$_{BST}$	50		52	ms	DTMF mode
10		Tone pause duration	t$_{PS}$	50		52	ms	DTMF mode
11		Tone burst duration (extended)	t$_{BSTE}$	100		104	ms	Call Progress mode
12		Tone pause duration (extended)	t$_{PSE}$	100		104	ms	Call Progress mode
13	TONE OUT	High group output level	V$_{HOUT}$	-6.1		-2.1	dBm	R$_L$ = 10kΩ
14		Low group output level	V$_{LOUT}$	-8.1		-4.1	dBm	R$_L$ = 10kΩ
15		Pre-emphasis	dB$_P$		2	3	dB	R$_L$ = 10kΩ
16		Output distortion (Single Tone)	THD		-25		dB	25 kHz Bandwidth R$_L$ = 10 kΩ
17		Frequency deviation	f$_D$		±0.7	±1.5	%	f$_C$ = 3.579545 MHz
18		Output load resistance	R$_{LT}$	10		50	kΩ	
19	MPU INTERFACE	$\Phi2$ cycle period	t$_{CYC}$	1		1000	μs	
20		$\Phi2$ high pulse width	t$_{CH}$	450			ns	
21		$\Phi2$ low pulse width	t$_{CL}$	430			ns	
22		$\Phi2$ rise and fall time	t$_R$, t$_F$			25	ns	
23		Address, R/$\overline{W}$ hold time	t$_{AH}$,t$_{RWH}$	26			ns	
24		Address, R/$\overline{W}$ setup time (before $\Phi2$)	t$_{AS}$,t$_{RWS}$	23			ns	
25		Data hold time (read)	t$_{DHR}$	22			ns	*
26		$\Phi2$ to valid data delay (read)	t$_{DDR}$			290	ns	200 pF load
27		Data setup time (write)	t$_{DSW}$	45			ns	
28		Data hold time (write)	t$_{DHW}$	10			ns	
29		Input Capacitance (data bus)	C$_{IN}$		5		pF	
30		Output Capacitance ($\overline{IRQ}$/CP)	C$_{OUT}$		5		pF	

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AC Electrical Characteristics¹ (Cont'd)-Voltages are with respect to ground (V$_{SS}$) unless otherwise stated

		Characteristics	Sym	Min	Typ$^+$	Max	Units	Notes*
31	D T M F	Crystal/clock frequency	f$_C$	3.5759	3.5795	3.5831	MHz	
32		Clock input rise time	t$_{LHCL}$			110	ns	Ext. clock
33		Clock input duty cycle	t$_{HLCL}$			110	ns	Ext. clock
34	C L	Clock input duty cycle	DC$_{CL}$	40	50	60	%	Ext. clock
35	K	Capacitive load (OSC2)	C$_{LO}$			30	pF	

¹Timing is over recommended temperature & power supply voltages. f$_C$=3.579545 MHz
$^+$ Typical figures are at 25°C and for design aid only: not guaranteed and not subject to production testing.
* The data bus output buffers are no longer sourcing or sinking current by t$_{DHR}$.
$^\#$ See Figure 7 regarding guard time adjustment.

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NOTES: 1) dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2) Digit sequence consists of all 16 DTMF tones.
3) Tone duration = 40 ms. Tone pause = 40 ms.
4) Nominal DTMF frequencies are used.
5) Both tones in the composite signal have an equal amplitude.
6) The tone pair is deviated by ± 1.5 % ± 2 Hz.
7) Bandwidth limited (3 kHz) Gaussian noise.
8) The precise dial tone frequencies are 350 and 440 Hz (± 2 %).
9) For an error rate of less than 1 in 10,000.
10) Referenced to the lowest amplitude tone in the DTMF signal.
11) Referenced to the minimum valid accept level.
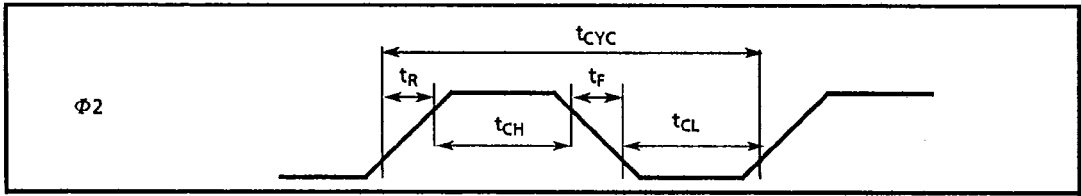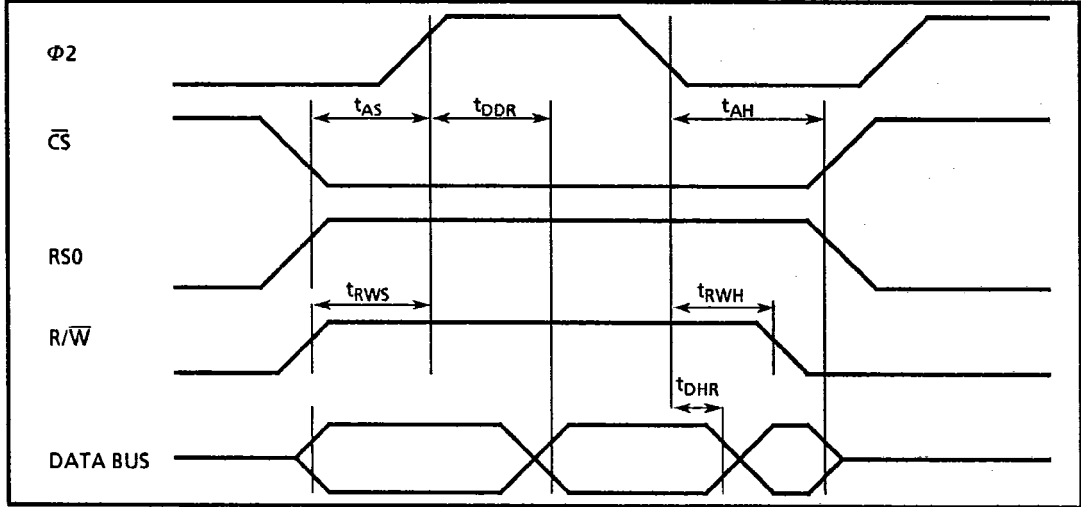12) For guard time calculation purposes.
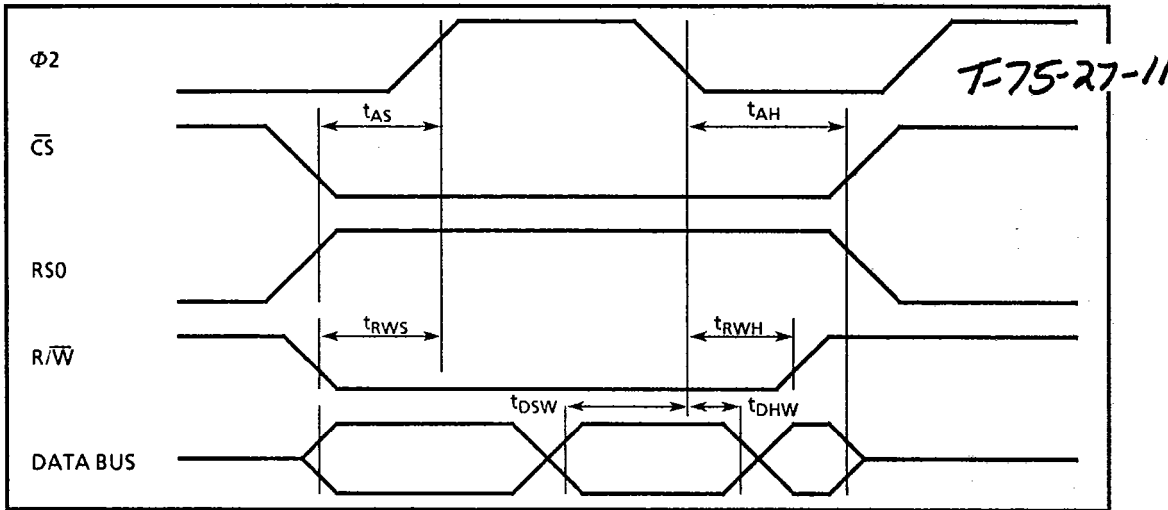

Figure 2 - Φ2 Pulse

Figure 3 - MPU Read Cycle

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Figure 4 - MPU Write Cycle

Pin Description

Pin #	Name	Description
1	IN+	Non-inverting op-amp input.
2	IN−	Inverting op-amp input.
3	GS	Gain Select. Gives access to output of front end differential amplifier for connection of feedback resistor.
4	V_{Ref}	Reference Voltage output, nominally $V_{DD}/2$ is used to bias inputs at mid-rail (see Fig. 15).
5	V_{SS}	Negative power supply input.
6	OSC1	DTMF clock/oscillator input.
7	OSC2	Clock output. A 3.579545 MHz crystal connected between OSC1 and OSC2 completes the internal oscillator circuit. Leave open circuit when OSC1 is clock input.
8	TONE	Dual Tone Multi-Frequency output.
9	R/$\overline{W}$	Read/Write input. Controls the direction of data transfer to and from the MPU and the transceiver registers. TTL compatible.
10	$\overline{CS}$	Chip select, TTL input ($\overline{CS}$=0 to select the chip).
11	RS0	Register Select input. See register decode table. TTL compatible.
12	Φ2	System Clock input. TTL compatible.
13	$\overline{IRQ}$/CP	Interrupt Request to MPU (open drain output). Also, when call progress (CP) mode has been selected and interrupt enabled the $\overline{IRQ}$/CP pin will output a rectangular wave signal representative of the input signal applied at the input op-amp. The input signal must be within the bandwidth limits of the call progress filter. See Figure 10.
14-17	D0-D3	Microprocessor data bus (TTL compatible). High impedance when $\overline{CS}$ = 1.
18	ESt	Early Steering output. Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
19	St/GT	Steering Input/Guard Time output (bidirectional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
20	V_{DD}	Positive power supply input.

Functional Description

The MT8880 Integrated DTMF Transceiver architecture consists of a high performance DTMF receiver with internal gain setting amplifier and a DTMF generator which employs a burst counter such that precise tone bursts and pauses can be synthesized. A call progress mode can be selected such that frequencies within the specified passband can be detected. A standard microprocessor interface allows access to an internal status register, two control registers and two data registers.

Input Configuration

The input arrangement of the MT8880 provides a differential-input operational amplifier as well as a bias source (V_{Ref}) which is used to bias the inputs at $V_{DD}/2$. Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. In a single-ended configuration, the input pins are connected as shown in Figure 5.

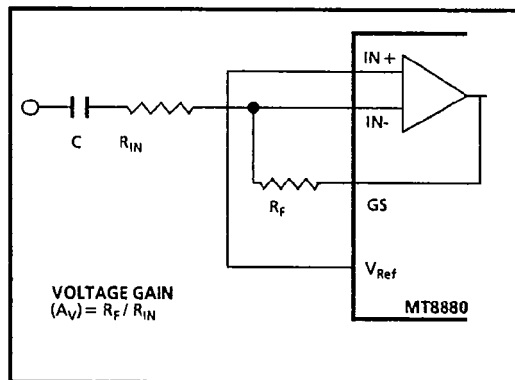Figure 6 shows the necessary connections for a differential input configuration.

VOLTAGE GAIN
(A_V) = R_F / R_{IN} MT8880

Figure 5 - Single-Ended Input Configuration

Receiver Section

Separation of the low and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high group frequencies (see Fig. 9). The low group filter also incorporates notches at 350 Hz and 440 Hz for exceptional dial tone rejection. Each filter output is followed by a single order switched capacitor filter section which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to

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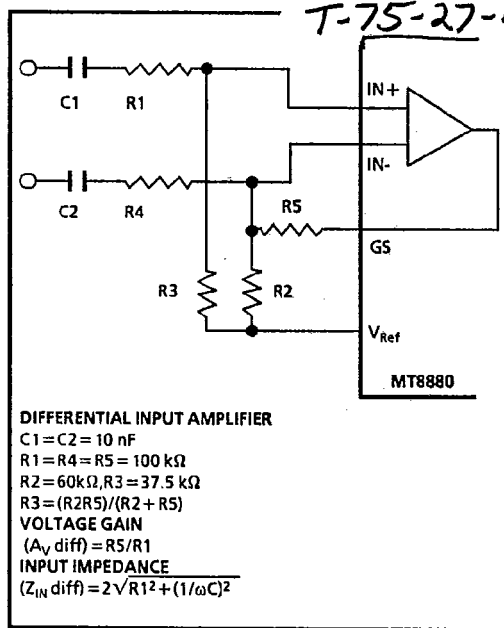
DIFFERENTIAL INPUT AMPLIFIER
C1=C2= 10 nF
R1=R4=R5= 100 kΩ
R2=60kΩ,R3 =37.5 kΩ
R3 = (R2R5)/(R2+ R5)
VOLTAGE GAIN
(A_V diff) = R5/R1
INPUT IMPEDANCE
(Z_{IN} diff) = $2\sqrt{R1^2+(1/\omega C)^2}$

Figure 6 - Differential Input Configuration

prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state.

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes v_c (see Figure 7) to rise as the capacitor discharges. Provided that the signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), v_c reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Figure 9) into the Receive Data Register. At this point the GT output is activated and drives v_c to V_{DD}. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag goes high, signalling that a received tone pair has been registered. The status of the delayed steering flag can be monitored by checking the appropriate bit in the status register. If Interrupt mode has been selected, the $\overline{IRQ}$/CP pin will pull low when the delayed steering flag is active.

The contents of the output latch are updated on an active delayed steering transition. This data is presented to the four bit bidirectional data bus when the Receive Data Register is read. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop out) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.
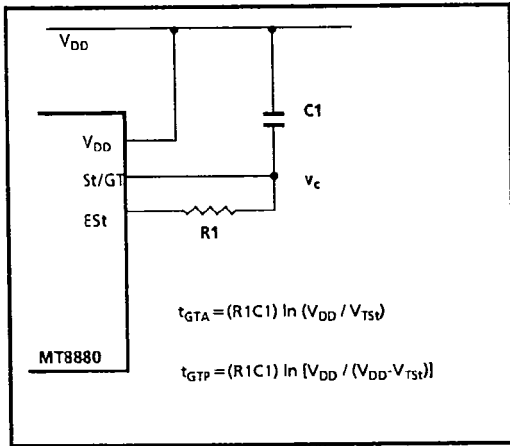
Guard Time Adjustment $T\text{-}75\text{-}27\text{-}11$

The simple steering circuit shown in Figure 7 is adequate for most applications. Component values are chosen according to the formula:

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{ID} = t_{DA} + t_{GTA}$$

The value of t_{DP} is a device parameter (see AC Electrical Characterstics) and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C1 of 0.1 μF is recommended for most applications, leaving R1 to be selected by the designer. Different steering arrangements may be used to select independently the guard times for tone present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity.

$$t_{GTP} = (R_P C1)\ \ln [V_{DD} / (V_{DD} \cdot V_{TSt})]$$
$$t_{GTA} = (R1 C1)\ \ln (V_{DD} / V_{TSt})$$
$$R_P = (R1 R2) / (R1 + R2)$$

a) decreasing tGTP; (tGTP < tGTA)

$$t_{GTP} = (R1 C1)\ \ln [V_{DD} / (V_{DD} \cdot V_{TSt})]$$
$$t_{GTA} = (R_P C1)\ \ln (V_{DD} / V_{TSt})$$
$$R_P = (R1 R2) / (R1 + R2)$$

b) decreasing tGTA; (tGTP > tGTA)

Figure 8 - Guard Time Adjustment

$$t_{GTA} = (R1 C1)\ \ln (V_{DD} / V_{TSt})$$
$$t_{GTP} = (R1 C1)\ \ln [V_{DD} / (V_{DD} \cdot V_{TSt})]$$

Figure 7. Basic Steering Circuit
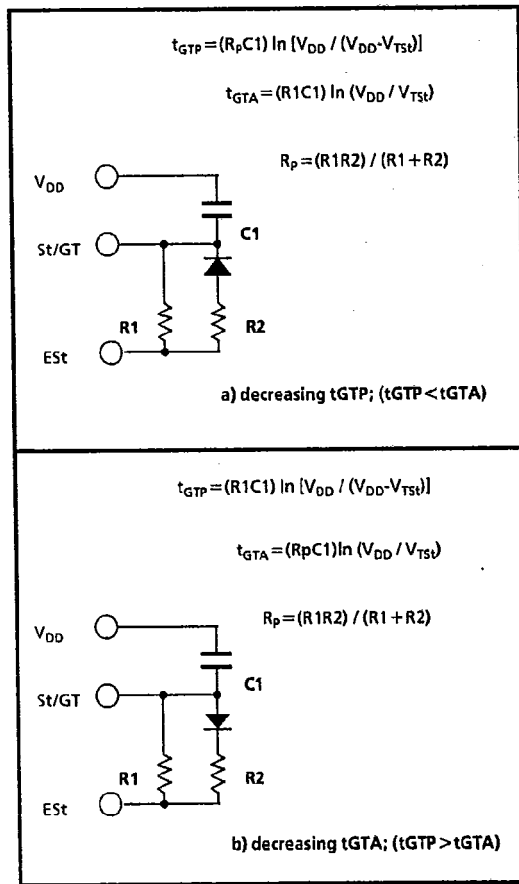
Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal; condition long enough to be registered. Alternatively, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figure 8. The receiver timing is shown in Figure 11 with a description of the events in Figure 13.

Call Progress Filter

A call progress mode, using the MT8880/MT8880-1, can be selected allowing the detection of various tones which identify the progress of a telephone call on the network. The MT8880-2 does not offer the call progress function. The call progress tone input and DTMF input are common, however, call progress tones can only be detected when CP mode has been selected. DTMF signals cannot be detected if CP mode has been selected (see Table 5). Figure 10 indicates the useful detect bandwidth of the call progress filter. Frequencies presented to the input which are within the 'accept' bandwidth limits of the filter are hard-limited by a high gain comparator with the $\overline{IRQ}$/CP pin serving as the output. The squarewave output obtained from the schmitt trigger can be analysed by a microprocessor or counter arrangement to determine the nature of the call progress tone being detected. Frequencies which are in the 'reject' area will not be detected and consequently the $\overline{IRQ}$/CP pin will remain low.

DTMF Generator

The DTMF transmitter employed in the MT8880 is capable of generating all sixteen standard DTMF tone pairs with low distortion and high accuracy. All frequencies are derived from an external 3.579545 MHz crystal. The sinusoidal waveforms for the individual tones are digitally synthesized using row and column programmable dividers and switched capacitor D/A converters. The row and column tones are mixed and filtered providing a DTMF signal with low total harmonic distortion and high accuracy. To specify a DTMF signal data conforming to the encoding format shown in Figure 9 must be written to the transmit data register. Note that this is the same as the receiver output code. The individual tones which are generated (f_{LOW} and f_{HIGH}) are referred to as Low Group and High Group tones. As seen from the table, the low group frequencies are 697, 770, 852 and 941 Hz. The high group frequencies are 1209, 1336, 1477 and 1633 Hz. Typically the high group to low group

F_{LOW}	F_{HIGH}	DIGIT	D_3	D_2	D_1	D_0
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	1477	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	1477	6	0	1	1	0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	1477	9	1	0	0	1
941	1336	0	1	0	1	0
941	1209	*	1	0	1	1
941	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0

0 = LOGIC LOW, 1 = LOGIC HIGH

Figure 9 - Functional Encode/Decode Table
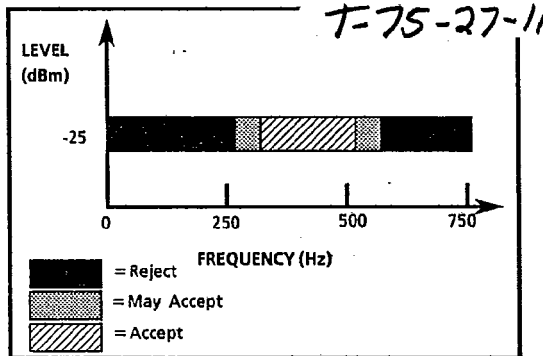

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Figure 10- Call Progress Response

amplitude ratio (twist) is 2 dB to compensate for high group attenuation on long loops.

The period of each tone consists of 32 equal time segments. The period of a tone is controlled by varying the length of these time segments. During write operations to the Transmit Data Register the 4 bit data on the bus is latched and converted to 2 of 8 coding for use by the programmable divider circuitry. This code is used to specify a time segment length which will ultimately determine the
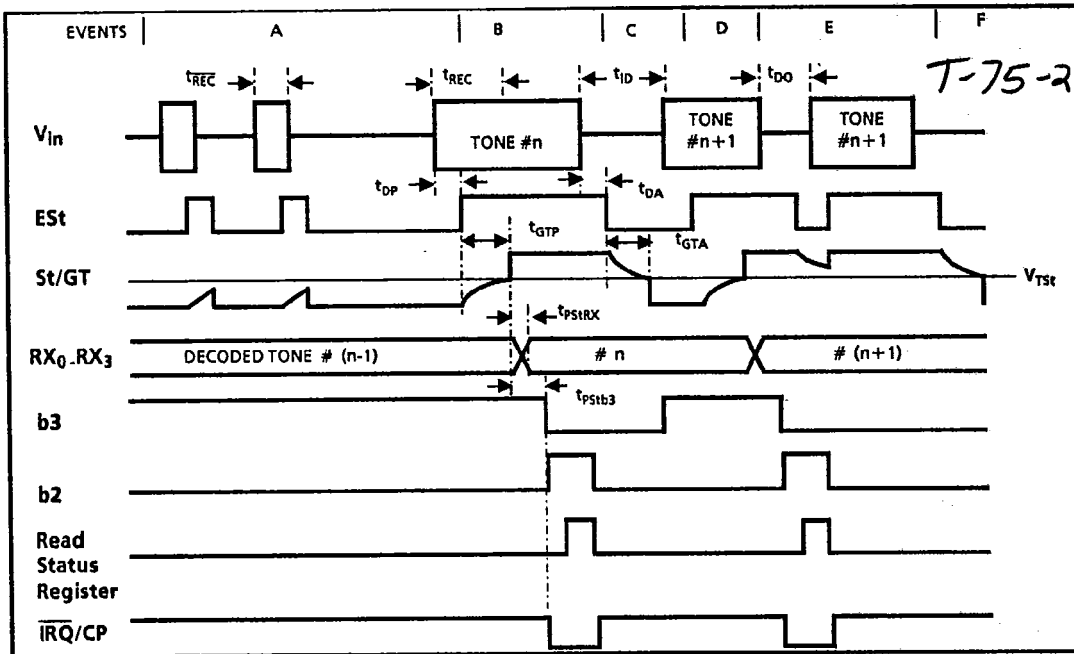
3-73

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Figure 11- Receiver Timing Diagram

frequency of the tone. When the divider reaches the appropriate count as determined by the input code, a reset pulse is issued and the counter starts again. The number of time segments is fixed at 32, however, by varying the segment length as described above the frequency can also be varied. The divider output clocks another counter which addresses the sinewave lookup ROM.

The lookup table contains codes which are used by the switched capacitor D/A converter to obtain discrete and highly accurate DC voltage levels. Two identical circuits are employed to produce row and column tones which are then mixed using a low noise summing amplifier. The oscillator described needs no "start-up" time as in other DTMF generators since the crystal oscillator is running continuously thus providing a high degree of tone burst accuracy. A bandwidth limiting filter is incorporated and serves to attenuate distortion products above 8 kHz. It can be seen from Figure 12 that the distortion products are very low in amplitude.
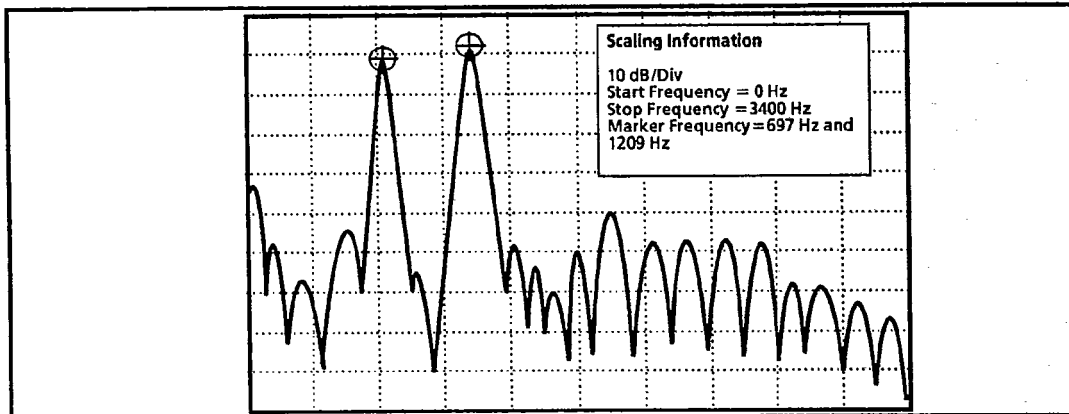

Scaling Information

10 dB/Div
Start Frequency = 0 Hz
Stop Frequency = 3400 Hz
Marker Frequency = 697 Hz and 1209 Hz

Figure 12 - Spectrum Plot

Burst Mode

In certain telephony applications it is required that DTMF signals being generated are of a specific duration determined either by the particular application or by any one of the exchange transmitter specifications currently existing. Standard DTMF signal timing can be accomplished by making use of the Burst Mode. The transmitter is capable of issuing symmetric bursts/pauses of predetermined duration. This burst/pause duration is 51 ms±1 ms which is a standard interval for autodialer and central office applications. After the burst/pause has been issued, the appropriate bit is set in the Status Register indicating that the transmitter is ready for more data. The timing described above is available when DTMF mode has been selected. However, when CP mode (Call Progress mode) is selected, a secondary burst/pause time is available such that this interval is extended to 102 ms ±2 ms. The extended interval is useful when precise tone bursts of longer than 51 ms duration and 51 ms pause are desired. Note that when CP mode and Burst mode have been selected, DTMF tones may be transmitted only and *not* received. In certain applications where a non-standard burst/pause time is desirable, a software timing loop or external timer can be used to provide the timing pulses when the burst mode is disabled by enabling and disabling the transmitter.

Single Tone Generation T-75-27-11

A single tone mode is available whereby individual tones from the low group or high group can be generated. This mode can be used for DTMF test equipment applications, acknowledgement tone generation and distortion measurements. Refer to Control Register B description for details.

Distortion Calculations

The MT8880 is capable of producing precise tone bursts with minimal error in frequency (see Table 1). The internal summing amplifier is followed by a first-order lowpass switched capacitor filter to minimize harmonic components and intermodulation products. The total harmonic distortion for a *single tone* can be calculated using Equation 1 which is the ratio of the total power of all the extraneous frequencies to the power of the fundamental frequency expressed as a percentage. The Fourier components of the tone output correspond to $V_{2f}....V_{nf}$ as measured on the output waveform. The total harmonic distortion for a *dual tone* can be calculated using Equation 2. V_L and V_H

EXPLANATION OF EVENTS

A)	TONE BURSTS DETECTED, TONE DURATION INVALID, RX DATA REGISTER NOT UPDATED.
B)	TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN RX DATA REGISTER.
C)	END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, INFORMATION IN RX DATA REGISTER RETAINED UNTIL NEXT VALID TONE PAIR.
D)	TONE #n+1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN RX DATA REGISTER.
E)	ACCEPTABLE DROPOUT OF TONE #n+1, TONE ABSENT DURATION INVALID, DATA REMAINS UNCHANGED.
F)	END OF TONE #n+1 DETECTED, TONE ABSENT DURATION VALID, INFORMATION IN RX DATA REGISTER RETAINED UNTIL NEXT VALID TONE PAIR.

EXPLANATION OF SYMBOLS

V_{in}	DTMF COMPOSITE INPUT SIGNAL.
ESt	EARLY STEERING OUTPUT. INDICATES DETECTION OF VALID TONE FREQUENCIES.
St/GT	STEERING INPUT/GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT.
RX_0-RX_3	4-BIT DECODED DATA IN RECEIVE DATA REGISTER
b3	DELAYED STEERING. INDICATES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME THUS CONSTITUTING A VALID SIGNAL. ACTIVE LOW FOR THE DURATION OF A VALID DTMF SIGNAL.
b2	INDICATES THAT VALID DATA IS IN THE RECEIVE DATA REGISTER. THE BIT IS CLEARED AFTER THE STATUS REGISTER IS READ.
$\overline{IRQ}$/CP	INTERRUPT IS ACTIVE INDICATING THAT NEW DATA IS IN THE RX DATA REGISTER. THE INTERRUPT IS CLEARED AFTER THE STATUS REGISTER IS READ.
$t_{\overline{REC}}$	MAXIMUM DTMF SIGNAL DURATION NOT DETECTED AS VALID.
t_{REC}	MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION.
t_{ID}	MINIMUM TIME BETWEEN VALID SEQUENTIAL DTMF SIGNALS.
t_{DO}	MAXIMUM ALLOWABLE DROPOUT DURING VALID DTMF SIGNAL.
t_{DP}	TIME TO DETECT VALID FREQUENCIES PRESENT.
t_{DA}	TIME TO DETECT VALID FREQUENCIES ABSENT.
t_{GTP}	GUARD TIME, TONE PRESENT.
t_{GTA}	GUARD TIME, TONE ABSENT

Figure 13 - Description of Timing Events

$$THD(\%) = 100 \frac{\left(\sqrt{V^2_{2f} + V^2_{3f} + V^2_{4f} + ...V^2_{nf}}\right)}{V_{fundamental}}$$

Equation 1. THD (%) For a Single Tone

$$THD(\%) = 100 \frac{\left(\sqrt{\begin{array}{c} V^2_{2L} + V^2_{3L} + ...V^2_{nL} + V^2_{2H} + \\ V^2_{3H} + ..V^2_{nH} + V^2_{IMD} \end{array}}\right)}{\sqrt{V^2_L + V^2_H}}$$

Equation 2. THD (%) For a Dual Tone

ACTIVE INPUT	OUTPUT FREQUENCY (Hz)		% ERROR
	SPECIFIED	ACTUAL	
L1	697	699.1	+0.30
L2	770	766.2	-0.49
L3	852	847.4	-0.54
L4	941	948.0	+0.74
H1	1209	1215.9	+0.57
H2	1336	1331.7	-0.32
H3	1477	1471.9	-0.35
H4	1633	1645.0	+0.73

Table 1 . Actual Frequencies Versus Standard Requirements

correspond to the low group amplitude and high group amplitude, respectively and V^2_{IMD} is the sum of all the intermodulation components. The internal switched-capacitor filter following the D/A converter keeps distortion products down to a very low level as shown in Figure 12.

DTMF Clock Circuit

The internal clock circuit is completed with the addition of a standard television colour burst crystal having a resonant frequency of 3.579545 MHz. A number of MT8880 devices can be connected as shown in Figure 14 such that only one crystal is required. Alternatively, the OSC1 inputs on all

devices can be driven from a TTL buffer (capacitive coupling) with the OSC2 outputs left unconnected.
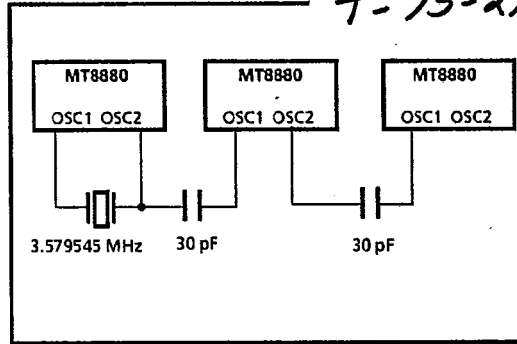
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Figure 14 - Common Crystal Connection

Microprocessor Interface

The MT8880 employs a microprocessor interface which allows precise control of transmitter and receiver functions. There are five internal registers associated with the microprocessor interface which can be subdivided into three categories, ie; data transfer, transceiver control and transceiver status. There are two registers associated with data transfer operations. The Receive Data Register contains the output code of the last valid DTMF tone pair to be decoded and is a read only register. The data entered in the Transmit Data Register will determine which tone pair is to be generated (see Figure 9 for coding details). Data can only be written to the transmit register. Transceiver control is accomplished with two Control Registers (CRA and CRB) which occupy the same address space. A write operation to CRB can be executed by setting the appropriate bit in CRA. The following write operation to the same address will then be directed to CRB and subsequent write cycles will then be directed back to CRA. A software reset must be included at the beginning of all programs to initialize the control registers after power up or power reset (see Figure 18). Refer to Tables 3, 4, 5 and 6 for details concerning the Control Registers. The IRQ/CP pin can be programmed such that it will provide an interrupt request signal upon validation of DTMF signals or when the transmitter is ready for more data (Burst mode only). The IRQ/CP pin is configured as an open drain output device and as such requires a pull-up resistor (see Figure 15).

RS0	R/W̄	FUNCTION
0	0	Write to Transmit Data Register
0	1	Read from Receive Data Register
1	0	Write to Control Register
1	1	Read from Status Register

Table 2 - Internal Register Functions

b3	b2	b1	b0
RSEL	IRQ	CP/DTMF̄	TOUT

Table 3- CRA Bit Positions

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b3	b2	b1	b0
C/R̄	S/D̄	TEST	BURST

Table 4- CRB Bit Positions

3

BIT	NAME	FUNCTION	DESCRIPTION
b0	TOUT	TONE OUTPUT	A logic '1' enables the tone output. This function can be implemented in either the burst mode or non-burst mode.
b1		MODE CONTROL	In DTMF mode (logic '0') the device is capable of generating and receiving Dual Tone Multi-Frequency signals. When the CP (Call Progress) mode is selected (logic '1') a 6th order bandpass filter is enabled to allow call progress tones to be detected. Call progress tones which are within the specified bandwidth will be presented at the IRQ̄/CP pin in rectangular wave format if the IRQ bit has been enabled (b2 = 1). Also, when the CP mode and BURST mode have both been selected, the transmitter will issue DTMF signals with a burst and pause of 102 ms (typ) duration. This signal duration is twice that obtained from the DTMF transmitter if DTMF mode had been selected. Note that DTMF signals cannot be decoded when the CP mode of operation has been selected.
b2	IRQ	INTERRUPT ENABLE	A logic '1' enables the INTERRUPT mode. When this mode is active and the DTMF mode has been selected (b1 = 0) the IRQ̄/CP pin will pull to a logic '0' condition when either 1) a valid DTMF signal has been received and has been present for the guard time duration or 2) the transmitter is ready for more data (BURST mode only).
b3	RSEL	REGISTER SELECT	A logic '1' selects Control Register B on the next Write cycle to the Control Register address. Subsequent Write cycles to the Control Register are directed back to Control Register A.

Table 5 - Control Register A Description

BIT	NAME	FUNCTION	DESCRIPTION
b0	BURST	BURST MODE	A logic '0' enables the burst mode. When this mode is selected, data corresponding to the desired DTMF tone pair can be written to the Transmit Register resulting in a tone burst of a specific duration (see AC Characteristics). Subsequently, a pause of the same duration is induced. Immediately following the pause, the Status Register is updated indicating that the Transmit Register is ready for further instructions and an interrupt will be generated if the interrupt mode has been enabled. Additionally, if call progress (CP) mode has been enabled, the burst and pause duration is increased by a factor of two. When the burst mode is not selected (logic '1') tone bursts of any desired duration may be generated.
b1	TEST	TEST MODE	By enabling the tet mode (logic '1'), the $\overline{IRQ}$/CP pin will present the delayed steering (inverted) signal from the DTMF receiver. Refer to Figure 11 (b3 waveform) for details concerning the output waveform. DTMF mode must be selected (CRA b1 = 0) before test mode can be implemented.
b2	S/$\overline{D}$	SINGLE /DUAL TONE GENERATION	A logic '0' will allow Dual Tone Multi-Frequency signals to be produced. If single tone generation is enabled (logic '1'), either row or column tones (low group or high group) can be generated depending on the state of b3 in Control Register B.
b3	C/$\overline{R}$	COLUMN/ROW TONES	When used in conjunction with b2 (above) the transmitter can be made to generate single row or single column frequencies. A logic '0' will select row frequencies and a logic '1' will select column frequencies.

Table 6 - Control Register B Description

BIT	NAME	STATUS FLAG SET	STATUS FLAG CLEARED
b0	IRQ	Interrupt has occurred. Bit one (b1) and or bit two (b2) is set.	Interrupt is inactive. Cleared after Status Register is read.
b1	TRANSMIT DATA REGISTER EMPTY (BURST MODE ONLY)	Pause duration has terminated and transmitter is ready for new data.	Cleared after Status Register is read or when in non-burst mode.
b2	RECEIVE DATA REGISTER FULL	Valid data is in the Receive Data Register.	Cleared after Status Register is read.
b3	DELAYED STEERING	Set upon the valid detection of the absence of a DTMF signal.	Cleared upon the detection of a valid DTMF signal.

Table 7 - Status Register Description

Notes:
R1, R2 = 100 kΩ 1%
R3 = 374k Ω 1 %
R4 = 3 kΩ 10 %
R$_L$ = 10 k Ω (min)
C1 = 100 nF 5 %
C2 = 100 nF 5 %
C3 = 100 nF 10 % *
C4 = 10 nF 10 %
X-tal = 3.579545 MHz

* Microprocessor based systems can inject undesirable noise into the supply rails. The performance of the MT8880 can be optimized by keeping noise on the supply rails to a minimum. The decoupling capacitor (C3) should be connected close to the device and ground loops should be avoided.

Figure 15 - Application Circuit (Single-Ended Input)
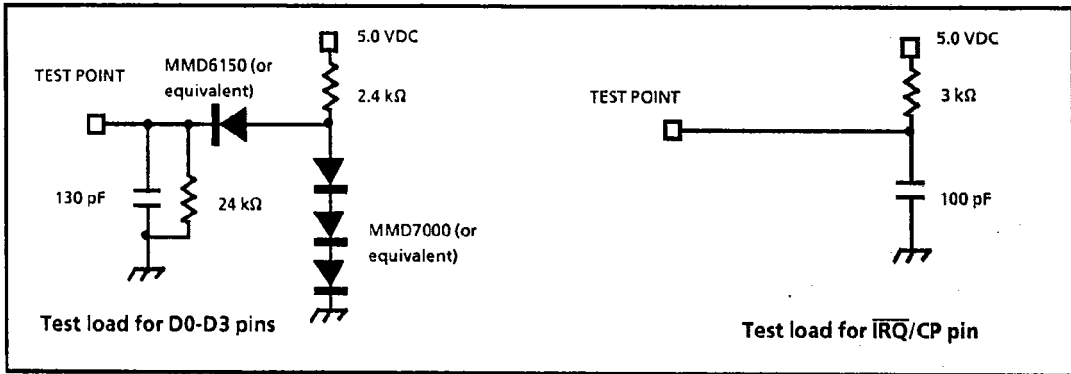
Figure 16- Test Circuits

Figure 17- MT8880 to 6802 Interface

EXAMPLE 1: A software reset must be included at the beginning of all programs to initialize the control registers after power up:

Description	Control			Data			
	$\overline{CS}$	RS0	R/$\overline{W}$	b3	b2	b1	b0
1) Write to Control Register	0	1	0	0	0	0	0
2) Write to Control Register	0	1	0	0	0	0	0
3) Write to Control Register	0	1	0	1	0	0	0
4) Write to Control Register	0	1	0	0	0	0	0

EXAMPLE 2: Transmit DTMF tones of 50 ms burst/50 ms pause and Receive DTMF Tones

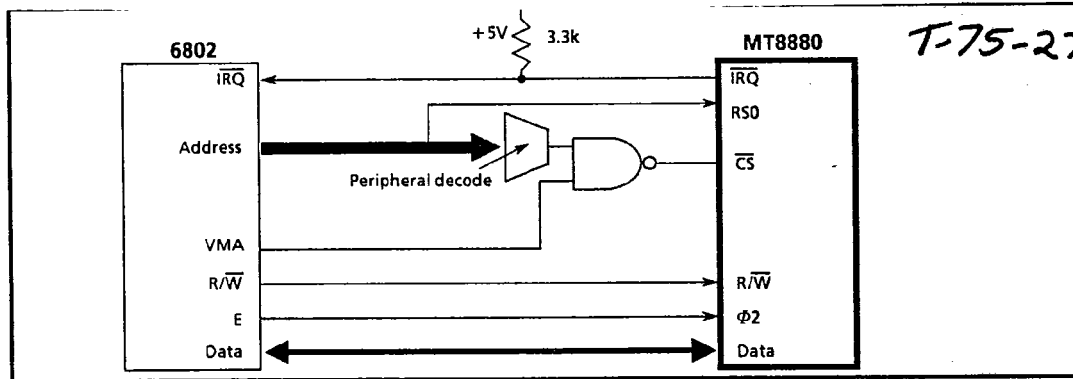| Description	$\overline{CS}$	RS0	R/$\overline{W}$	b3	b2	b1	b0
1) Write to Control Register A (tone out, DTMF, $\overline{IRQ}$, Select Control Register B)	0	1	0	1	1	0	1
2) Write to Control Register B (burst mode)	0	1	0	0	0	0	0
3) Write to Transmit Data Register (send a digit 7)	0	0	0	0	1	1	1
----------------------------*wait for an interrupt or poll Status Register*-------------------------------							
4) Read the Status Register	0	1	1	X	X	X	X
-if bit 1 is set, the Tx is ready for the next tone, in which case ... Write to Transmit Register (send a digit 5)	0	0	0	0	1	0	1
-if bit 2 is set, a DTMF tone has been received, in which case .... Read the Receive Data Register	0	0	1	X	X	X	X
-if both bits are set ... Read the Receive Data Register	0	0	1	X	X	X	X
Write to Transmit Data Register	0	0	0	0	1	0	1

NOTE: IN THE TX BURST MODE, STATUS REGISTER BIT 1 WILL NOT BE SET UNTIL 100 ms (±2 ms) AFTER THE DATA IS WRITTEN TO THE TX DATA REGISTER. IN EXTENDED BURST MODE THIS TIME WILL BE DOUBLED TO 200 ms (± 4 ms).

Figure 18 - Application Hints

Package Outlines

35E D ■ 6249370 0005778 6 ■ MITC

T-90-20

DIM	18-Pin SOIC		20-Pin SOIC	
	Min	Max	Min	Max
A	0.093 (2.35)	0.104 (2.65)	0.093 (2.35)	0.104 (2.65)
A_1	0.004 (0.10)	0.012 (0.30)	0.004 (0.10)	0.012 (0.30)
B	0.014 (0.351)	0.019 (0.488)	0.014 (0.351)	0.019 (0.488)
C	0.009 (0.231)	0.013 (0.318)	0.009 (0.231)	0.013 (0.318)
D	0.447 (11.35)	0.469 (11.90)	0.496 (12.60)	0.518 (13.00)
E	0.291 (7.40)	0.305 (7.75)	0.291 (7.40)	0.305 (7.75)
e	0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)	
F	0.044 (1.125)	0.064 (1.625)	0.044 (1.125)	0.064 (1.625)
G	0.040 (1.016)	0.050 (1.270)	0.040 (1.016)	0.050 (1.270)
H	0.394 (10.00)	0.419 (10.65)	0.394 (10.00)	0.419 (10.65)
K	0.035 (0.889)	0.045 (1.143)	0.035 (0.889)	0.045 (1.143)
L	0.016 (0.40)	0.050 (1.27)	0.016 (0.40)	0.050 (1.27)
O_1	-	0.005 (0.13)	-	0.005 (0.13)
O_2	-	0.005 (0.13)	-	0.005 (0.13)

NOTE: ( ) millimeters

NOTES:
1) A & B Maximum dimensions include allowable mold flash.
2) O_1 & O_2 are SYMMETRY dimensions.

Lead SOIC Package (S Suffix)

Package Outlines

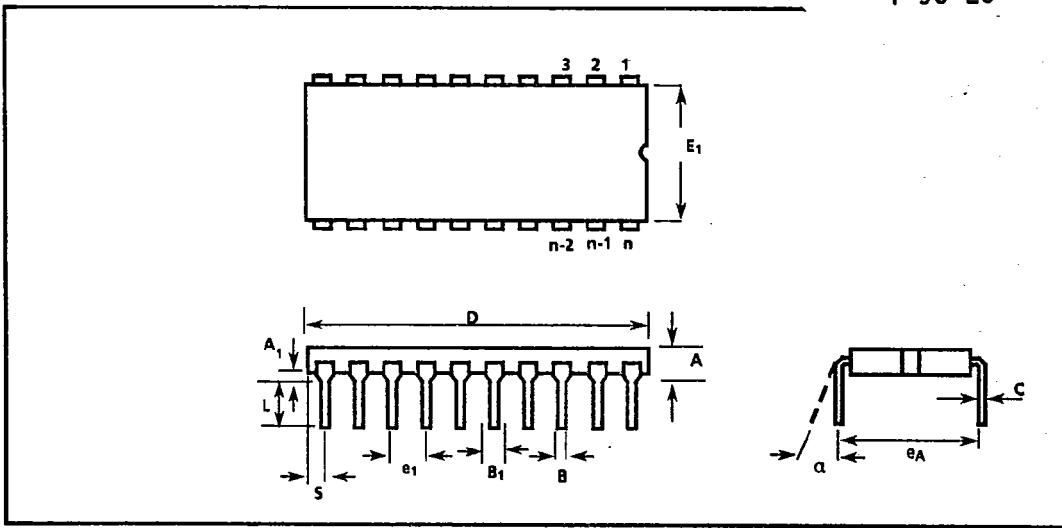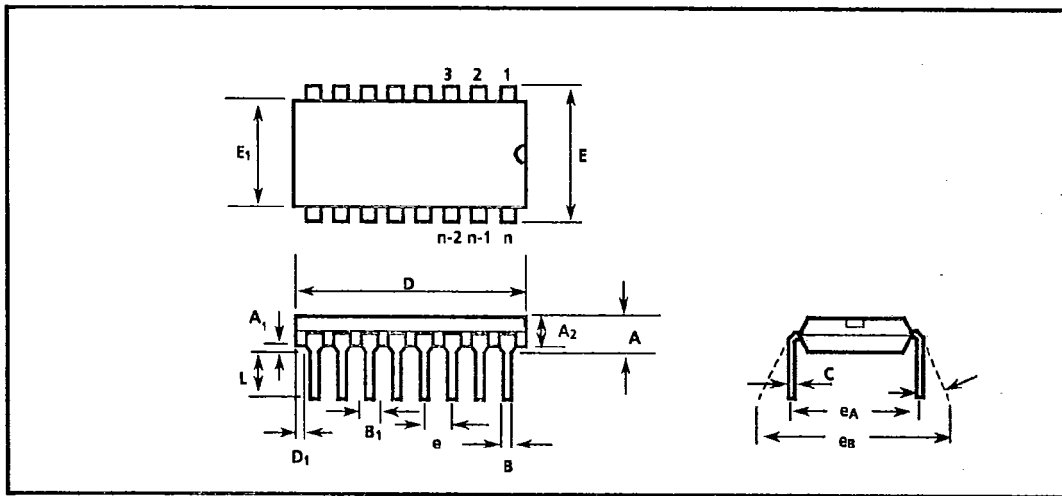Ceramic Dual-In-Line Packages (CDIP) - C Suffix

Plastic Dual-In-Line Packages (PDIP) - E Suffix

DIM	8-Pin Plastic Min	Max	Ceramic Min	Max	16-Pin Plastic Min	Max	Ceramic Min	Max	18-Pin Plastic Min	Max	Ceramic Min	Max	20-Pin Plastic Min	Max	Ceramic Min	Max
A		0.210 (5.33)	0.105 (2.67)	0.200 (5.08)		0.210 (5.33)	0.105 (2.67)	0.200 (5.08)		0.210 (5.33)	0.105 (2.67)	0.200 (5.08)		0.210 (5.33)	0.105 (2.67)	0.200 (5.08)
A_1			0.025 (0.64)	0.055 (1.39)			0.025 (0.64)	0.055 (1.39)			0.025 (0.64)	0.055 (1.39)			0.025 (0.64)	0.055 (1.39)
A_2	0.115 (2.93)	0.195 (4.95)			0.115 (2.93)	0.195 (4.95)			0.115 (2.93)	0.195 (4.95)			0.115 (2.93)	0.195 (4.95)		
B	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.021 (0.533)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.021 (0.533)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.021 (0.533)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.021 (0.533)
B_1	0.045 (1.15)	0.070 (1.77)	0.035 (0.89)	0.060 (1.52)	0.045 (1.15)	0.070 (1.77)	0.035 (0.89)	0.060 (1.52)	0.045 (1.15)	0.070 (1.77)	0.035 (0.89)	0.060 (1.52)	0.045 (1.15)	0.070 (1.77)	0.035 (0.89)	0.060 (1.52)
C	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)
D	0.348 (8.84)	0.430 (10.92)	0.380 (9.7)	0.550 (13.9)	0.745 (18.93)	0.840 (21.33)		0.784 (19.9)	0.845 (21.47)	0.925 (23.49)	0.880 (22.36)	0.930 (23.62)	0.925 (23.49)	1.060 (26.9)		0.996 (25.3)
D_1	0.005 (0.13)				0.005 (0.13)				0.005 (0.13)				0.005 (0.13)			
E	0.290 (7.37)	0.330 (8.38)			0.290 (7.37)	0.330 (8.38)			0.290 (7.37)	0.330 (8.38)			0.290 (7.37)	0.330 (8.38)		
E_1	0.240 (6.10)	0.280 (7.11)	0.280 (7.12)	0.310 (7.87)	0.240 (6.10)	0.280 (7.11)	0.280 (7.12)	0.310 (7.87)	0.240 (6.10)	0.280 (7.11)	0.280 (7.12)	0.310 (7.87)	0.240 (6.10)	0.280 (7.11)	0.280 (7.12)	0.310 (7.87)
e	0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)			
e_1			0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)	
e_A	0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (2.54 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)	
e_B		0.430 (10.92)				0.430 (10.92)				0.430 (10.92)				0.430 (10.92)		
L	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)
S				0.120 (3.04)				0.120 (3.04)				0.120 (3.04)				0.120 (3.04)
α			0°	15°			0°	15°			0°	15°			0°	15°

NOTE: ( ) Millimeters

Package Outlines

T-90-20

DIM	22-Pin Plastic Min	Max	22-Pin Ceramic Min	Max	24-Pin Plastic Min	Max	24-Pin Ceramic Min	Max	28-Pin Plastic Min	Max	28-Pin Ceramic Min	Max	40-Pin Plastic Min	Max	40-Pin Ceramic Min	Max
A		0.210 (5.33)	0.090 (2.29)	0.225 (5.71)		0.250 (6.35)	0.085 (2.2)	0.190 (4.8)		0.250 (6.35)	0.085 (2.2)	0.190 (4.8)		0.250 (6.35)	0.085 (2.2)	0.190 (4.8)
A_1			0.025 (0.64)	0.055 (1.39)			0.020 (0.51)	0.070 (1.77)			0.020 (0.51)	0.070 (1.77)			0.020 (0.51)	0.070 (1.77)
A_2	0.125 (3.18)	0.195 (4.95)			0.125 (3.18)	0.195 (4.95)			0.125 (3.18)	0.195 (4.95)			0.125 (3.18)	0.195 (4.95)		
B	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.023 (0.584)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.023 (0.584)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.023 (0.584)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.023 (0.584)
B_1	0.045 (1.15)	0.070 (1.77)	0.028 (0.71)	0.060 (1.52)	0.030 (0.77)	0.070 (1.77)	0.028 (0.71)	0.060 (1.52)	0.030 (0.77)	0.070 (1.77)	0.028 (0.71)	0.060 (1.52)	0.030 (0.77)	0.070 (1.77)	0.028 (0.71)	0.060 (1.52)
C	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)
D	1.050 (26.67)	1.120 (28.44)	1.040 (26.42)	1.260 (32.0)	1.150 (29.3)	1.290 (32.7)	1.180 (29.88)	1.291 (32.80)	1.380 (35.1)	1.565 (39.7)	1.380 (35.06)	1.520 (38.61)	1.980 (50.3)	2.095 (53.2)	1.980 (50.30)	2.110 (53.60)
D_1	0.005 (0.13)				0.005 (0.13)				0.005 (0.13)				0.005 (0.13)			
E	0.390 (9.91)	0.430 (10.92)			0.600 (15.24)	0.670 (17.02)			0.600 (15.24)	0.670 (17.02)			0.600 (15.24)	0.670 (17.02)		
E_1	0.330 (8.39)	0.380 (9.65)	0.350 (8.89)	0.410 (10.41)	0.485 (12.32)	0.580 (14.73)	0.516 (13.11)	0.610 (15.49)	0.485 (12.32)	0.580 (14.73)	0.480 (12.19)	0.610 (15.49)	0.485 (12.32)	0.580 (14.73)	0.480 (12.19)	0.618 (15.70)
e	0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)			
e_1			0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)	
e_A	0.400 BSC (10.16 BSC)		0.400 BSC (10.16 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)	
e_B		0.500 (12.70)				0.700 (17.78)				0.700 (17.78)				0.700 (17.78)		
L	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.200 (5.08)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.200 (5.08)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.200 (5.08)	0.125 (3.18)	0.175 (4.44)
S				0.120 (3.04)				0.100 (2.54)				0.800 (2.05)				0.800 (2.05)
α			0°	15°			0°	15°			0°	15°			0°	15°

NOTE: ( ) Millimeters

Plastic J-Lead Chip Carrier (P-Suffix)
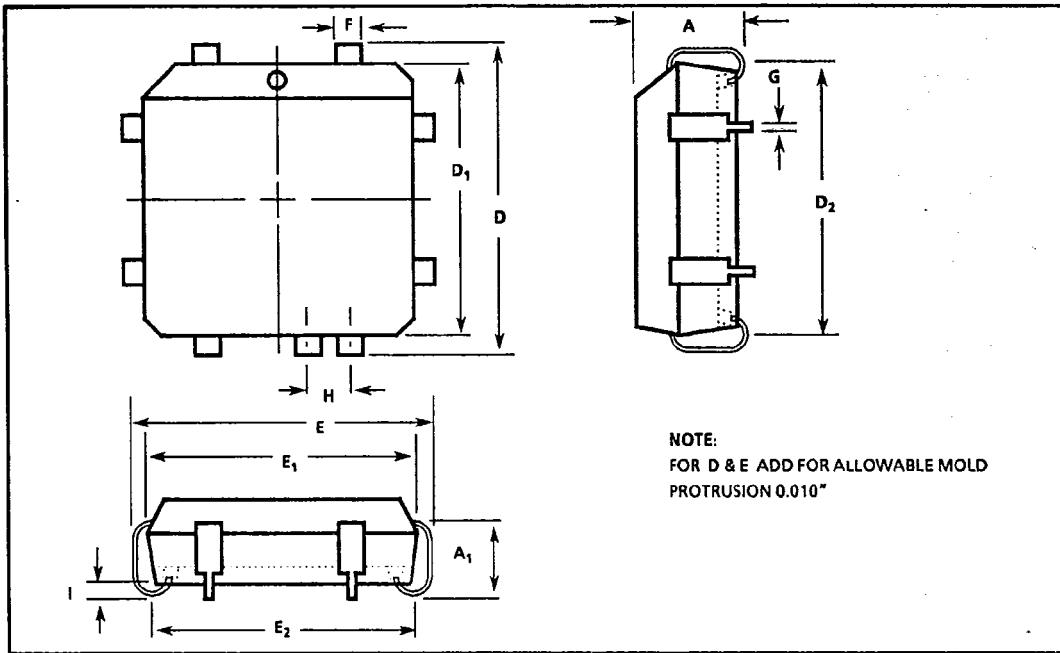
NOTE:
FOR D & E ADD FOR ALLOWABLE MOLD
PROTRUSION 0.010"

MITEL SEMICONDUCTOR   35E D ■ 6249370 0005783 T ═MITC

T-90-20

DIM	20-Pin PLCC		28-Pin PLCC		44-Pin PLCC		68-Pin PLCC		84-Pin PLCC	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.200 (5.08)	0.165 (4.20)	0.200 (5.08)
A_1	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.130 (3.30)	0.090 (2.29)	0.130 (3.30)
B			0.020 TP (0.511 TP)							
B_1										
B_2										
D/E	0.385 (9.78)	0.395 (10.03)	0.485 (12.32)	0.495 (12.57)	0.685 (17.40)	0.695 (17.65)	0.985 (25.02)	0.995 (25.27)	0.185 (30.10)	1.195 (30.35)
D_1/E_1	0.350 (8.890)	0.356 (9.042)	0.450 (11.430)	0.456 (11.582)	0.650 (16.510)	0.656 (16.662)	0.950 (24.130)	0.958 (24.333)	1.150 (29.210)	1.158 (29.413)
D_2/E_2	0.290 (7.37)	0.330 (8.38)	0.390 (9.91)	0.430 (10.92)	0.590 (14.99)	0.630 (16.00)	0.890 (22.61)	0.930 (23.62)	1.090 (27.69)	1.130 (28.70)
D_4/E_4										
e			0.050 BSC (1.27 BSC)							
F	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)
G	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)
H	0.050 BSC (1.27 BSC)				0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)	
h			0.040 BSC (1.02 BSC)							
h_1										
I	0.020 (0.51)		0.020 (0.51)		0.020 (0.51)		0.020 (0.51)		0.020 (0.51)	
L										
L_1										
R_1										

NOTE: ( ) Millimeters