

SRAM MODULE

256K x 32 SRAM LOW VOLTAGE

FEATURES

- High speed: 20*, 25 and 35ns
- High-density 1MB design
- High-performance, low-power, CMOS double-metal process
- Single +3.3V $\pm$ 0.3V power supply
- 5V-tolerant I/O
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ functions
- Industry-standard pinout
- All inputs and outputs are TTL-compatible
- Low profile

OPTIONS

- Timing
 - 17ns access
 - 20ns access
 - 25ns access
 - 35ns access
- Packages
 - 64-pin SIMM
 - 64-pin ZIP

MARKING

-17
-20
-25
-35

M
Z

- Optional, 2V data retention
- 2V data retention, low power

L
LP

- Part Number Example: MT8LS25632Z-20 LP

NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

GENERAL DESCRIPTION

The MT8LS25632 is a high-speed SRAM memory module containing 262,144 words organized in a x32-bit configuration. The module consists of eight low voltage 256K x 4 fast SRAMs mounted on a 64-pin, double-sided, FR4-printed circuit board.

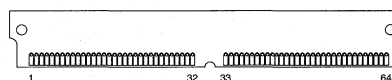
Data is written into the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ and/or $\overline{OE}$ can set the output in High-Z for additional flexibility in system design and memory expansion.

PD0 and PD1 identify the module's density allowing interchangeable use of alternate density, industry standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's 4 bytes independently.

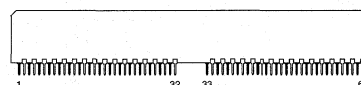
The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology.

PIN ASSIGNMENT (Top View)

64-Pin SIMM (SF-4)



64-Pin ZIP (SG-1)



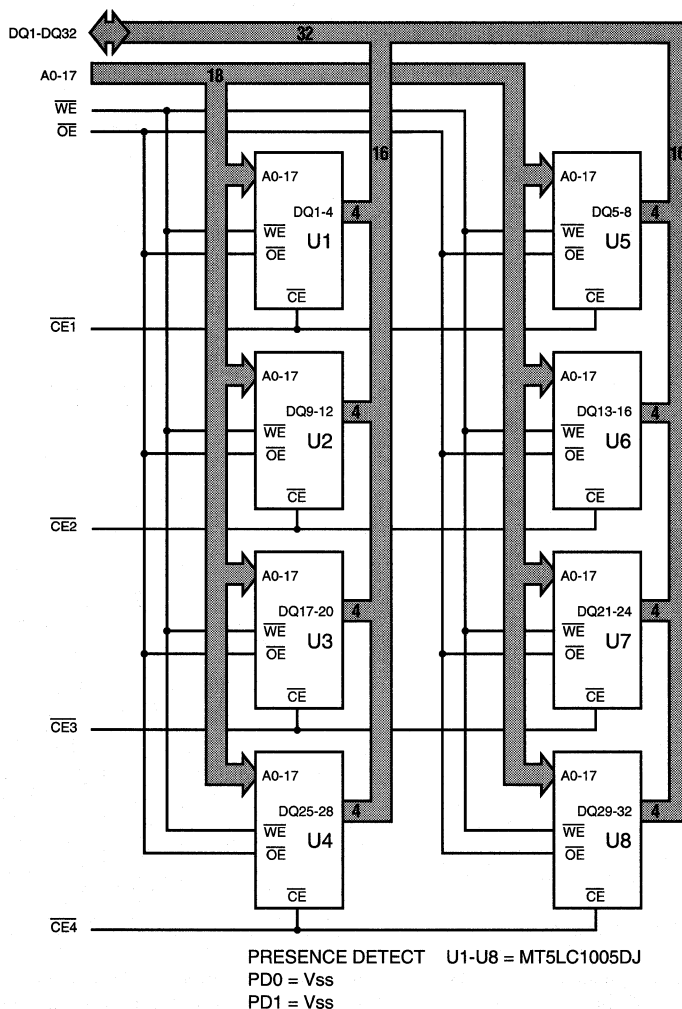
PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	17	A2	33	CE4	49	A4
2	PD0	18	A9	34	CE3	50	A11
3	PD1	19	DQ13	35	A17	51	A5
4	DQ1	20	DQ5	36	A16	52	A12
5	DQ9	21	DQ14	37	OE	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	WE	44	DQ19	60	DQ23
13	A0	29	A15	45	DQ28	61	DQ31
14	A7	30	A14	46	DQ20	62	DQ24
15	A1	31	CE2	47	A3	63	DQ32
16	A8	32	CE1	48	A10	64	Vss

All module components may be powered from a single +3.3V DC supply and all inputs and outputs are fully TTL-compatible.

The "L" and "LP" versions each provide a significant reduction in CMOS standby current (I_{SB2}) over the standard version. The "LP" version also provides a significant reduction in TTL standby current (I_{SB1}) through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

NEW
SRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss	-0.5V to +4.6V
V _{IN}	-0.5V to +6.0V
Storage temperature	-55°C to +125°C
Power dissipation	8W
Short circuit output current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{cc} = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V _{IH}	2.0	5.5V	V	1, 2
Input Low (Logic 0) Voltage		V _{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V _{IN} ≤ V _{CC}	I _{LI}	-8	8	μA	
Input/Output Leakage Current	Output(s) disabled 0V ≤ V _{OUT} ≤ V _{CC}	DQ1-DQ32 I _{LO}	-1	1	μA	
Output High Voltage	I _{OH} = -4.0mA	V _{OH}	2.4		V	1
Output Low Voltage	I _{OL} = 8.0mA	V _{OL}		0.4	V	1
Supply Voltage		V _{CC}	3.0	3.6	V	1

DESCRIPTION	CONDITIONS	SYMBOL	VER	MAX				UNITS	NOTES
				-17	-20	-25	-35		
Power Supply Current: Operating	$\overline{CE} \leq V_{IL}$; V _{CC} = MAX f = MAX = 1/ t _{RC} outputs open	I _{CC}	ALL	680	600	520	440	mA	3, 13
Power Supply Current: Standby	$\overline{CE} \geq V_{IH}$; V _{CC} = MAX f = MAX = 1/ t _{RC} outputs open	I _{SB1}	STD,L	160	144	112	96	mA	13
			LP	4	4	4	4	mA	13
	$\overline{CE} \geq V_{CC} - 0.2V$; V _{CC} = MAX V _{IN} ≤ V _{SS} +0.2V or V _{IN} ≥ V _{CC} -0.2V; f = 0	I _{SB2}	STD,L	2.4	2.4	2.4	2.4	mA	13
			LP	0.8	800	800	800	μA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A17, WE, $\overline{OE}$	T _A = 25°C; f = 1 MHz V _{CC} = 3.3V	C _{I1}	70	pF	4
Input Capacitance: $\overline{CE1}$ - $\overline{CE4}$		C _{I2}	15	pF	4
Input/Output Capacitance: DQ1-DQ32		C _{I/O}	10	pF	4



MT8LS25632

256K x 32 SRAM MODULE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$; $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$)

DESCRIPTION		-17		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^t RC	17		20		25		35		ns	
Address access time	^t AA		17		20		25		35	ns	
Chip Enable access time	^t ACE		17		20		25		35	ns	
Output hold from address change	^t OH	3		3		5		5		ns	
Chip Enable to output in Low-Z	^t LZCE	5		3		5		5		ns	7
Chip disable to output in High-Z	^t HZCE		7		8		10		15	ns	6, 7
Chip Enable to power-up time	^t PU	0		0		0		0		ns	
Chip disable to power-down time	^t PD		17		20		25		35	ns	
Output Enable access time	^t AOE		5		4		8		12	ns	
Output Enable to output in Low-Z	^t LZOE	0		0		0		0		ns	
Output disable to output in High-Z	^t HZOE		5		4		10		12	ns	6
WRITE Cycle											
WRITE cycle time	^t WC	17		20		25		35		ns	
Chip Enable to end of write	^t CW	12		12		15		20		ns	
Address valid to end of write	^t AW	12		12		15		20		ns	
Address setup time	^t AS	0		0		0		0		ns	
Address hold from end of write	^t AH	0		0		0		0		ns	
WRITE pulse width	^t WP1	12		12		15		20		ns	
WRITE pulse width	^t WP2	8		15		15		20		ns	
Data setup time	^t DS	7		8		10		15		ns	
Data hold time	^t DH	0		0		0		0		ns	
Write disable to output in Low-Z	^t LZWE	3		3		5		5		ns	7
Write Enable to output in High-Z	^t HZWE		7		8		10		15	ns	6, 7

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AC TEST CONDITIONS

Input pulse levels	V _{SS} to 2.8V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

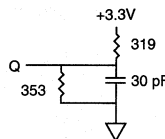


Fig. 1 OUTPUT LOAD EQUIVALENT

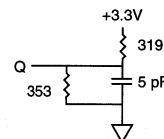


Fig. 2 OUTPUT LOAD EQUIVALENT

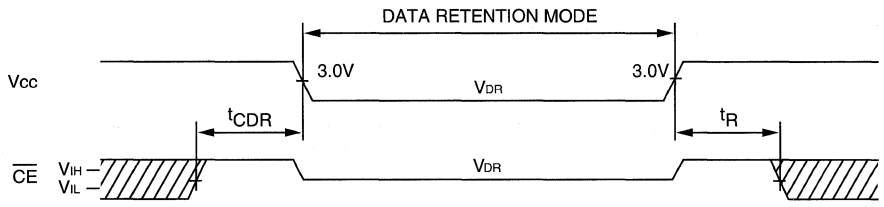
NOTES

- All voltages referenced to V_{SS} (GND).
- Overshoot: V_{IH} ≤ +6.0V for t ≤ t_{KC}/2
 Undershoot: V_{IL} ≥ -2.0V for t ≤ t_{KC}/2
 Power-up: V_{IH} ≥ +6.0V and V_{CC} ≤ 3.1V for t ≤ 200 msec.
- I_{CC} is dependent on output loading and cycle rates.
- This parameter is sampled.
- Test conditions as specified with the output loading as shown in Fig. 1, unless otherwise noted.
- t_{HZCE}, t_{HZOE} and t_{HZWE} are specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE}.
- $\overline{WE}$ is HIGH for READ cycle.
- Device is continuously selected. All chip enables are held in their active state.
- Address valid prior to, or coincident with, latest occurring chip enable.
- t_{RC}=READ cycle time
- Chip enable and write enable can initiate and terminate a WRITE cycle.
- Typical values are measured at 3.3V, 25°C and 25ns cycle time.
- Typical currents are measured at 25°C. MAX is over operating temperature range.
- Output enable ($\overline{OE}$) is inactive (HIGH).
- Output enable ($\overline{OE}$) is active (LOW).

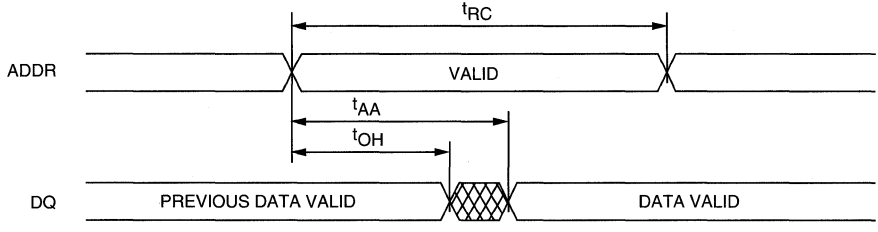
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V _{CC} for Retention Data		V _{DR}	2			V	
Data Retention Current L Version	$\overline{CE} \geq V_{CC} - 0.2V$ Other inputs: V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ V _{SS} + 0.2V V _{CC} = 2V	I _{CCDR}		TBD	400	μA	14
Data Retention Current LP Version	$\overline{CE} \geq V_{CC} - 0.2V$ V _{CC} = 2V	I _{CCDR}		TBD	400	μA	14
Chip Deselect to Data Retention Time		t _{CDR}	0			ns	4
Operation Recovery Time		t _R	t _{RC}			ns	4, 11

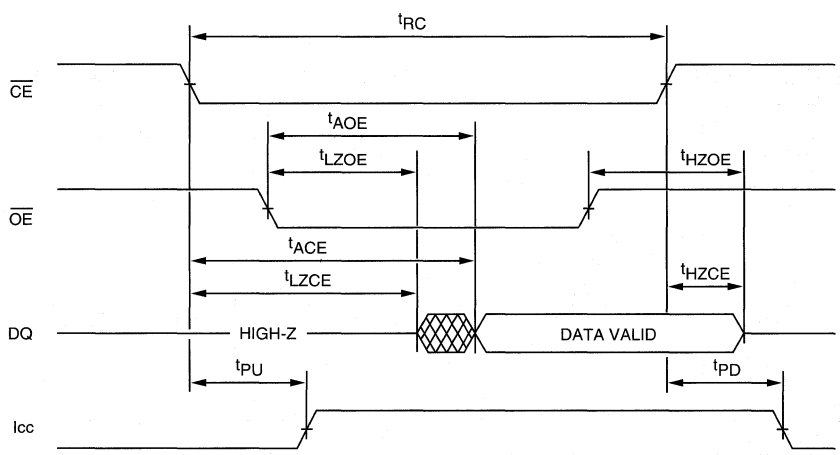
LOW V_{CC} DATA RETENTION WAVEFORM



READ CYCLE NO. 1 8, 9



READ CYCLE NO. 2 7, 8, 10

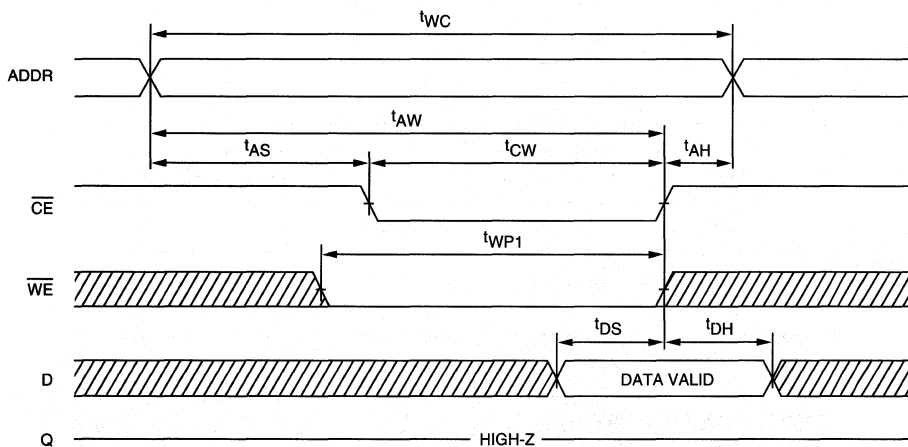


DON'T CARE

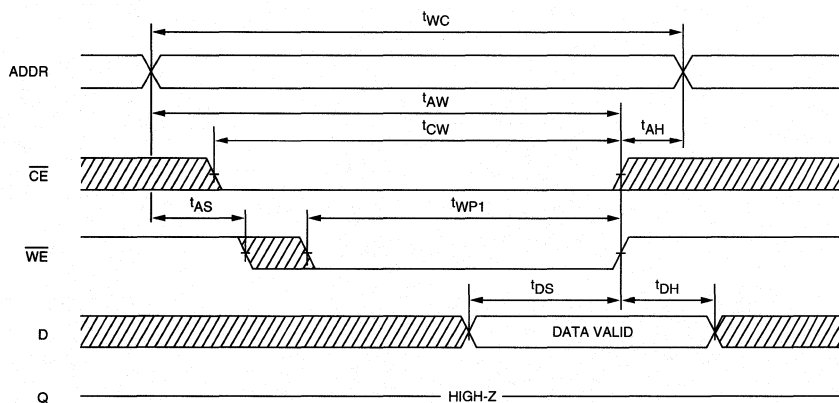
UNDEFINED

NEW ■ SRAM MODULE

WRITE CYCLE NO. 1 ¹²
(Chip Enable Controlled)



WRITE CYCLE NO. 2 ^{12, 15}
(Write Enable Controlled)



■ DON'T CARE
■ UNDEFINED

WRITE CYCLE NO. 3 7, 12, 16
 (Write Enable Controlled)
