SRAM MODULE

64K x 32 SRAM

FEATURES

- High speed: 15*, 20, 25, 30 and 35ns
- High-performance, low-power CMOS process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ functions
- Low profile
- Industry-standard pinout
- All inputs and outputs are TTL-compatible
- Upgradable with 128K x 32 and 256K x 32 modules

OPTIONS

	MARKING
• Timing	
12ns access	-12*
15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35
• Packages	
64-pin SIMM	M
64-pin ZIP	Z
• 2V data retention	L
• Low power	P

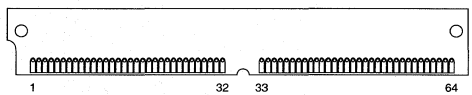
• Part Number Example: MT8S6432Z-15 P

*Consult factory

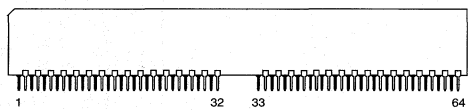
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

64-Pin SIMM
(SF-2)



64-Pin ZIP
(SG-3)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{CE4}$	49	A4
2	PD0	18	A9	34	$\overline{CE3}$	50	A11
3	PD1	19	DQ13	35	NC	51	A5
4	DQ1	20	DQ5	36	NC	52	A12
5	DQ9	21	DQ14	37	$\overline{OE}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{WE}$	44	DQ19	60	DQ23
13	A0	29	A15	45	DQ28	61	DQ31
14	A7	30	A14	46	DQ20	62	DQ24
15	A1	31	$\overline{CE2}$	47	A3	63	DQ32
16	A8	32	$\overline{CE1}$	48	A10	64	Vss

GENERAL DESCRIPTION

The MT8S6432 is a high-speed SRAM memory module containing 65,536 words organized in a x32-bit configuration. The module consists of eight 64K x 4 fast SRAMs mounted on a 64-pin, double-sided, FR4 printed circuit board.

Data is written into to the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ and/or $\overline{OE}$ can set the output in a High-Z state for additional flexibility in system design and memory expansion.

PD0 and PD1 identify the module's density, allowing interchangeable use of alternate density, industry-standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's 4 bytes independently.

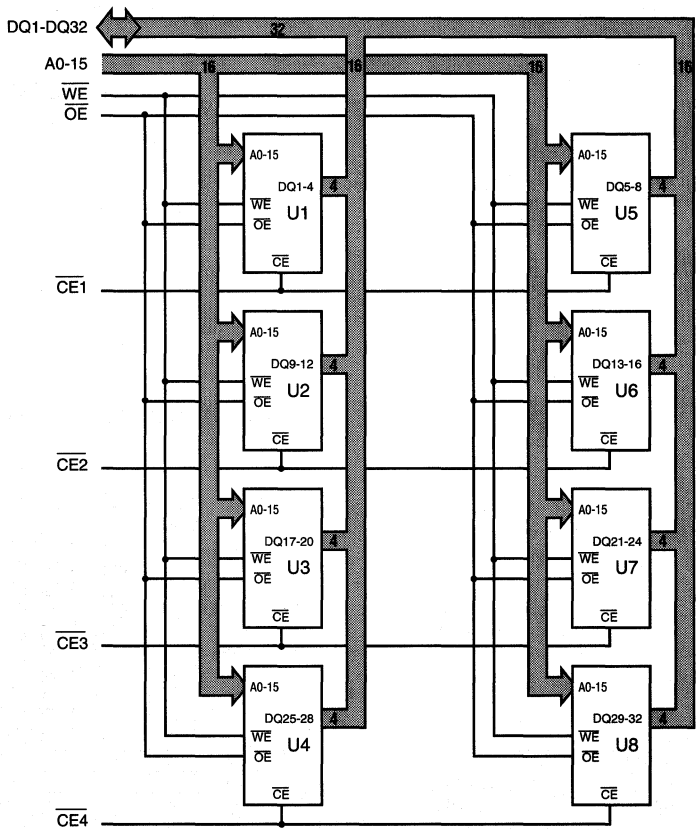
The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +5V DC supply and all inputs and outputs are fully TTL-compatible. The "L" option offers reduced-voltage operation for systems with low standby power requirements.

The "LP" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and

GENERAL DESCRIPTION (continued)

address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

FUNCTIONAL BLOCK DIAGRAM



PRESENCE DETECT
PD0 = No Connect
PD1 = Vss

U1-U8 = MT5C2565DJ

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature ..... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-40	40	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

					MAX						
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12	-15†	-20	-25	-35	UNITS	NOTES
Operating Current TTL Input Levels	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	824	1,520	1,360	1,200	1,040	1,000	mA	3, 13
	P Version	I_{CC}	768	-	-	1,080	1,000	920	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	192	440	400	360	320	280	mA	13
	P Version	I_{SB1}	11.2	-	-	32	32	32	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	4.8	40	40	40	40	56	mA	13
	P Version	I_{SB2}	3.2	-	3	3	3	3	mA	13

† LP version not available with this speed grade.

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A15, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz	C_I	70	pF	4
Input Capacitance: $\overline{CE}$1- $\overline{CE}$4	V_{CC} = 5V	C12	15	pF	4
Input/Output Capacitance: DQ1-DQ32		$C_{I/O}$	10	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

		-12*		-15		-20		-25		-35			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle													
READ cycle time	^tRC	12		15		20		25		35		ns	
Address access time	^tAA		12		15		20		25		35	ns	
Chip Enable access time	^tACE		12		15		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		3		3		ns	
Chip Enable LOW to output in Low-Z	^tLZCE	3		3		3		3		3		ns	7
Chip Enable to output in High-Z	^tHZCE		6		8		9		9		15	ns	6, 7
Chip Enable LOW to power-up time	^tPU	0		0		0		0		0		ns	
Chip Enable HIGH to power-down time	^tPD		12		15		20		25		35	ns	
Output Enable access time	^tAOE		6		8		8		8		12	ns	
Output Enable LOW to output in Low-Z	^tLZOE	0		0		0		0		0		ns	
Output Enable HIGH to output in High-Z	^tHZOE		6		6		7		7		12	ns	6
WRITE Cycle													
WRITE cycle time	^tWC	12		15		20		20		30		ns	
Chip Enable to end of write	^tCW	8		10		12		15		20		ns	
Address valid to end of write	^tAW	8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	1		1		1		1		1		ns	
WRITE pulse width	$^tWP1$	8		10		12		15		20		ns	
WRITE pulse width	$^tWP2$	12		12		15		15		20		ns	
Data setup time	^tDS	7		7		10		10		15		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write Enable LOW to output in Low-Z	^tLZWE	2		2		2		2		2		ns	7
Write Enable HIGH to output in High-Z	^tHZWE		6	0	7	0	8	0	10	0	12	ns	6, 7

*Consult factory

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

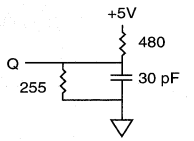


Fig. 1 OUTPUT LOAD EQUIVALENT

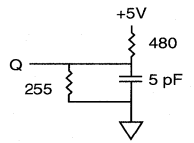


Fig. 2 OUTPUT LOAD EQUIVALENT

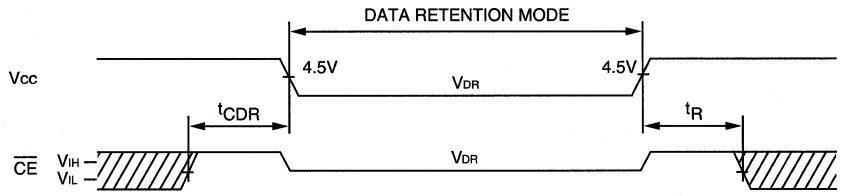
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC=Read Cycle Time
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 20ns cycle time.
14. Typical values are measured at 25°C.
15. Output enable ($\overline{OE}$) is inactive (HIGH).
16. Output enable ($\overline{OE}$) is active (LOW).

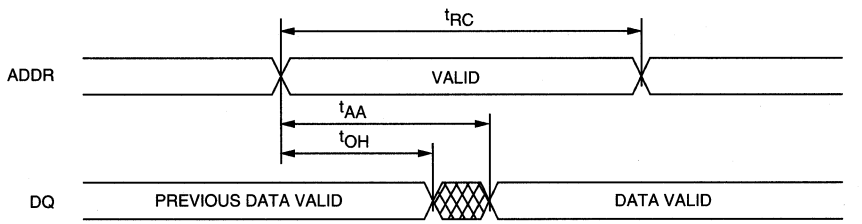
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current L Version	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		280	2,400	µA	14
		Vcc = 3V			720	4,000	µA	14
Data Retention Current LP Version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		280	2,400	µA	14
		Vcc = 3V	ICCDR		720	4,000	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4,11

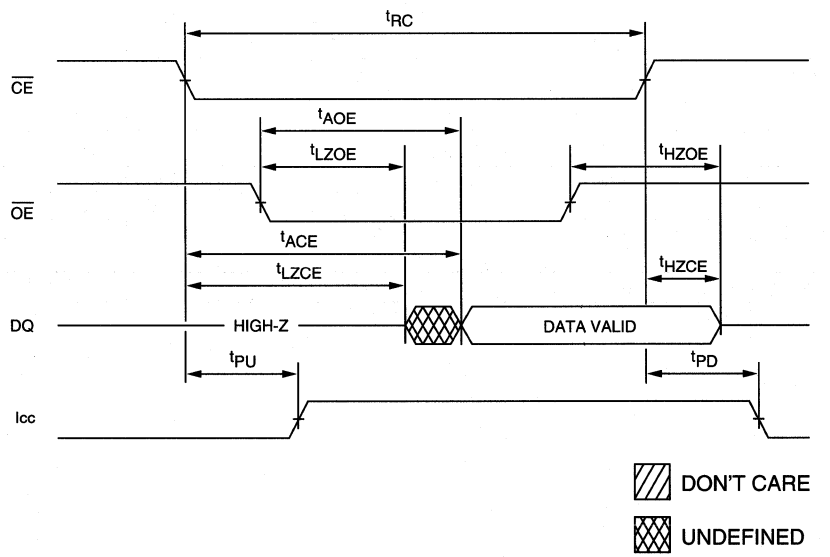
LOW Vcc DATA-RETENTION WAVEFORM



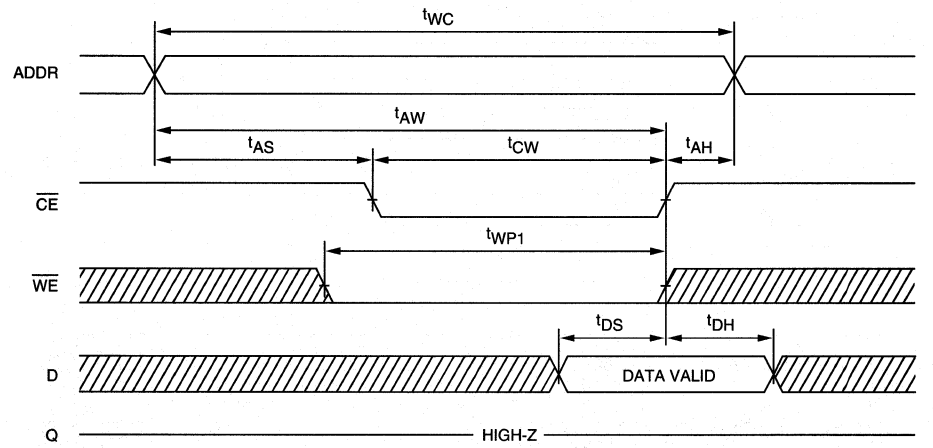
READ CYCLE NO. 1 [8, 9]



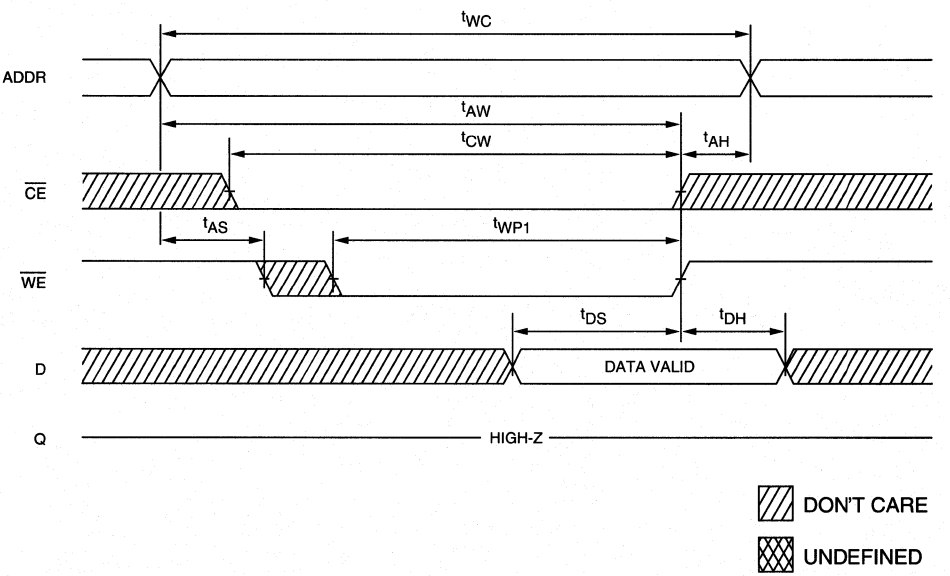
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12, 15]
(Write Enable Controlled)



WRITE CYCLE NO. 3 [7, 12, 16]
(Write Enable Controlled)