SMALL-OUTLINE DDR SDRAM MODULE

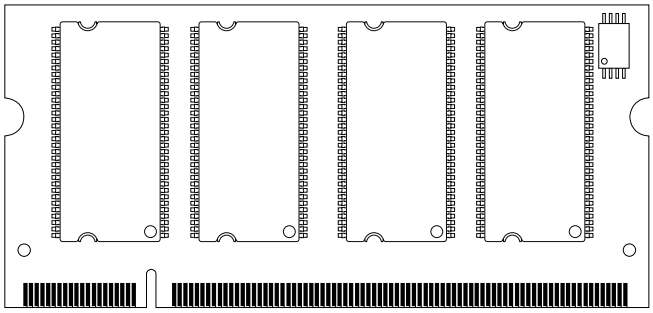
MT8VDDT1664H – 128MB
MT8VDDT3264H – 256MB

For the latest data sheet, please refer to the Micron® Web site: www.micron.com/moduleds

Features

- 200-pin, small-outline, dual in-line memory module (SODIMM)
- Fast data transfer rates PC1600, PC2100, or PC2700
- Utilizes 200 MT/s, 266 MT/s, and 333MT/s DDR SDRAM components
- 128MB (16 Meg x 64) or 256MB (32 Meg x 64)
- V_{DD} = $V_{DD}Q$ = +2.5V
- V_{DDSPD} = +2.3V to +3.6V
- 2.5V I/O (SSTL_2 compatible)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/received with data—i.e., source-synchronous data capture
- Differential clock inputs CK and CK#
- Four internal device banks for concurrent operation
- Programmable burst lengths: 2, 4, or 8
- Auto precharge option
- Serial Presence Detect (SPD) with EEPROM
- Programmable READ CAS latency
- Auto Refresh and Self Refresh Modes
- 15.625µs (128MB), 7.8125µs (256MB) maximum average periodic refresh interval
- Gold edge contacts

Figure 1: 200-Pin SODIMM (MO-224)



OPTIONS — MARKING

- Package
  - 200-pin SODIMM (Standard) — G
  - 200-pin SODIMM (Lead-free)[1] — Y
- Frequency/CAS Latency[2]
  - 6ns/166 MHz (333MT/s) CL = 2.5 — -335
  - 7.5ns/133 MHz (266 MT/s) CL = 2 — -262
  - 7.5ns/133 MHz (266 MT/s) CL = 2 — -26A
  - 7.5ns/133 MHz (266 MT/s) CL = 2.5 — -265
  - 10ns/100 MHz (200 MT/s) CL = 2 — -202

NOTE: 1. Consult with factory for availability of lead-free products.
2. CL = CAS (READ) Latency

Table 1: Address Table

	128MB	256MB
Refresh Count	4K	8K
Row Addressing	4K (A0–A11)	8K (A0–A12)
Device Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)
Device Configuration	16 Meg x 8	32 Meg x 8
Column Addressing	1K (A0–A9)	1K (A0–A9)
Module Rank Addressing	1 (S0#)	1 (S0#)

Table 2: Part Numbers and Timing Parameters

PART NUMBER	MODULE DENSITY	CONFIGURATION	MODULE BANDWIDTH	MEMORY CLOCK/ DATA BIT RATE	LATENCY (CL - ^{t}RCD - ^{t}RP)
MT8VDDT1664HG-335__	128MB	16 Meg x 64	2.7 GB/s	6ns/333 MT/s	2.5-3-3
MT8VDDT1664HY-335__	128MB	16 Meg x 64	2.7 GB/s	6ns/333 MT/s	2.5-3-3
MT8VDDT1664HG-262__	128MB	16 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT8VDDT1664HY-262__	128MB	16 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT8VDDT1664HG-26A__	128MB	16 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT8VDDT1664HY-26A__	128MB	16 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT8VDDT1664HG-265__	128MB	16 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT8VDDT1664HY-265__	128MB	16 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT8VDDT1664HG-202__	128MB	16 Meg x 64	1.6 GB/s	10ns/200 MT/s	2-2-2
MT8VDDT1664HY-202__	128MB	16 Meg x 64	1.6 GB/s	10ns/200 MT/s	2-2-2
MT8VDDT3264HG-335__	256MB	32 Meg x 64	2.7 GB/s	6ns/333 MT/s	2.5-3-3
MT8VDDT3264HY-335__	256MB	32 Meg x 64	2.7 GB/s	6ns/333 MT/s	2.5-3-3
MT8VDDT3264HG-262__	256MB	32 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT8VDDT3264HY-262__	256MB	32 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT8VDDT3264HG-26A__	256MB	32 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT8VDDT3264HY-26A__	256MB	32 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT8VDDT3264HG-265__	256MB	32 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT8VDDT3264HY-265__	256MB	32 Meg x 64	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT8VDDT3264HG-202__	256MB	32 Meg x 64	1.6 GB/s	10ns/200 MT/s	2-2-2
MT8VDDT3264HY-202__	256MB	32 Meg x 64	1.6 GB/s	10ns/200 MT/s	2-2-2

NOTE:

All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT8VDDT3264HG-265A1.

Table 3: Pin Assignment (200-Pin SODIMM Front)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VREF	51	VSS	101	A9	151	DQ42
3	VSS	53	DQ19	103	VSS	153	DQ43
5	DQ0	55	DQ24	105	A7	155	VDD
7	DQ1	57	VDD	107	A5	157	VDD
9	VDD	59	DQ25	109	A3	159	VSS
11	DQS0	61	DQS3	111	A1	161	VSS
13	DQ2	63	VSS	113	VDD	163	DQ48
15	VSS	65	DQ26	115	A10	165	DQ49
17	DQ3	67	DQ27	117	BA0	167	VDD
19	DQ8	69	VDD	119	WE#	169	DQS6
21	VDD	71	DNU	121	S0#	171	DQ50
23	DQ9	73	DNU	123	NC	173	VSS
25	DQS1	75	VSS	125	VSS	175	DQ51
27	VSS	77	DNU	127	DQ32	177	DQ56
29	DQ10	79	DNU	129	DQ33	179	VDD
31	DQ11	81	VDD	131	VDD	181	DQ57
33	VDD	83	DNU	133	DQS4	183	DQS7
35	CK0	85	NC	135	DQ34	185	VSS
37	CK0#	87	VSS	137	VSS	187	DQ58
39	VSS	89	DNU	139	DQ35	189	DQ59
41	DQ16	91	DNU	141	DQ40	191	VDD
43	DQ17	93	VDD	143	VDD	193	SDA
45	VDD	95	DNU	145	DQ41	195	SCL
47	DQS2	97	NC	147	DQS5	197	VDDSPD
49	DQ18	99	NC/A12	149	VSS	199	NC

Table 4: Pin Assignment (200-Pin SODIMM Back)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
2	VREF	52	VSS	102	A8	152	DQ46
4	VSS	54	DQ23	104	VSS	154	DQ47
6	DQ4	56	DQ28	106	A6	156	VDD
8	DQ5	58	VDD	108	A4	158	CK1#
10	VDD	60	DQ29	110	A2	160	CK1
12	DM0	62	DM3	112	A0	162	VSS
14	DQ6	64	VSS	114	VDD	164	DQ52
16	VSS	66	DQ30	116	BA1	166	DQ53
18	DQ7	68	DQ31	118	RAS#	168	VDD
20	DQ12	70	VDD	120	CAS#	170	DM6
22	VDD	72	DNU	122	DNU	172	DQ54
24	DQ13	74	DNU	124	NC	174	VSS
26	DM1	76	VSS	126	VSS	176	DQ55
28	VSS	78	DNU	128	DQ36	178	DQ60
30	DQ14	80	DNU	130	DQ37	180	VDD
32	DQ15	82	VDD	132	VDD	182	DQ61
34	VDD	84	DNU	134	DM4	184	DM7
36	VDD	86	NC	136	DQ38	186	VSS
38	VSS	88	VSS	138	VSS	188	DQ62
40	VSS	90	VSS	140	DQ39	190	DQ63
42	DQ20	92	VDD	142	DQ44	192	VDD
44	DQ21	94	VDD	144	VDD	194	SA0
46	VDD	96	CKE0	146	DQ45	196	SA1
48	DM2	98	NC	148	DM5	198	SA2
50	DQ22	100	A11	150	VSS	200	NC

NOTE:
Pin 99 is No Connect for 128MB, A12 for 256MB.

Figure 2: Module Layout

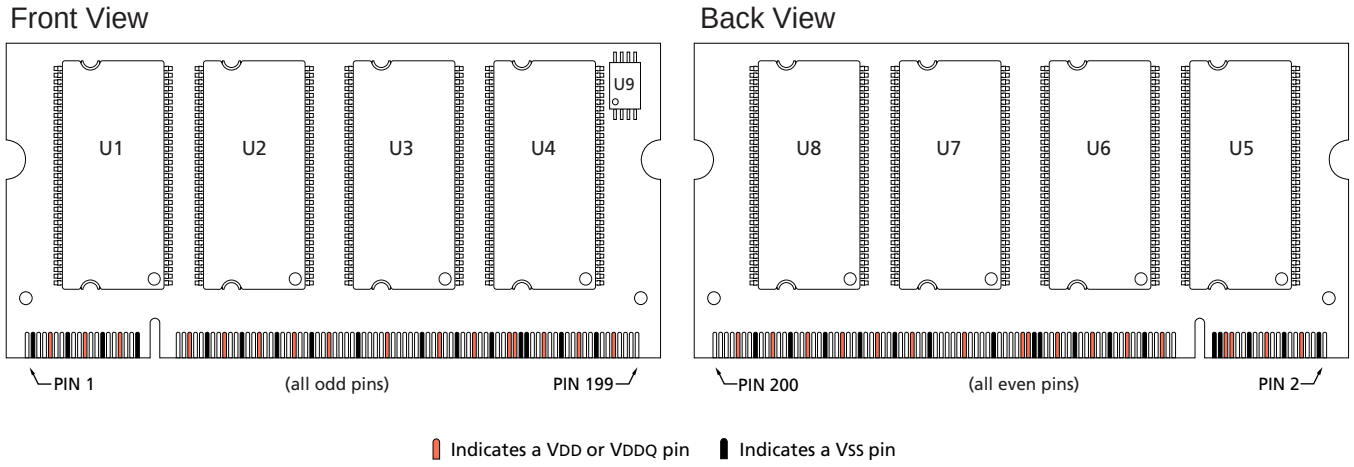


Table 5: Pin Descriptions

Pin numbers may not correlate with symbols. Refer to Pin Assignment tables on page 3 for more information

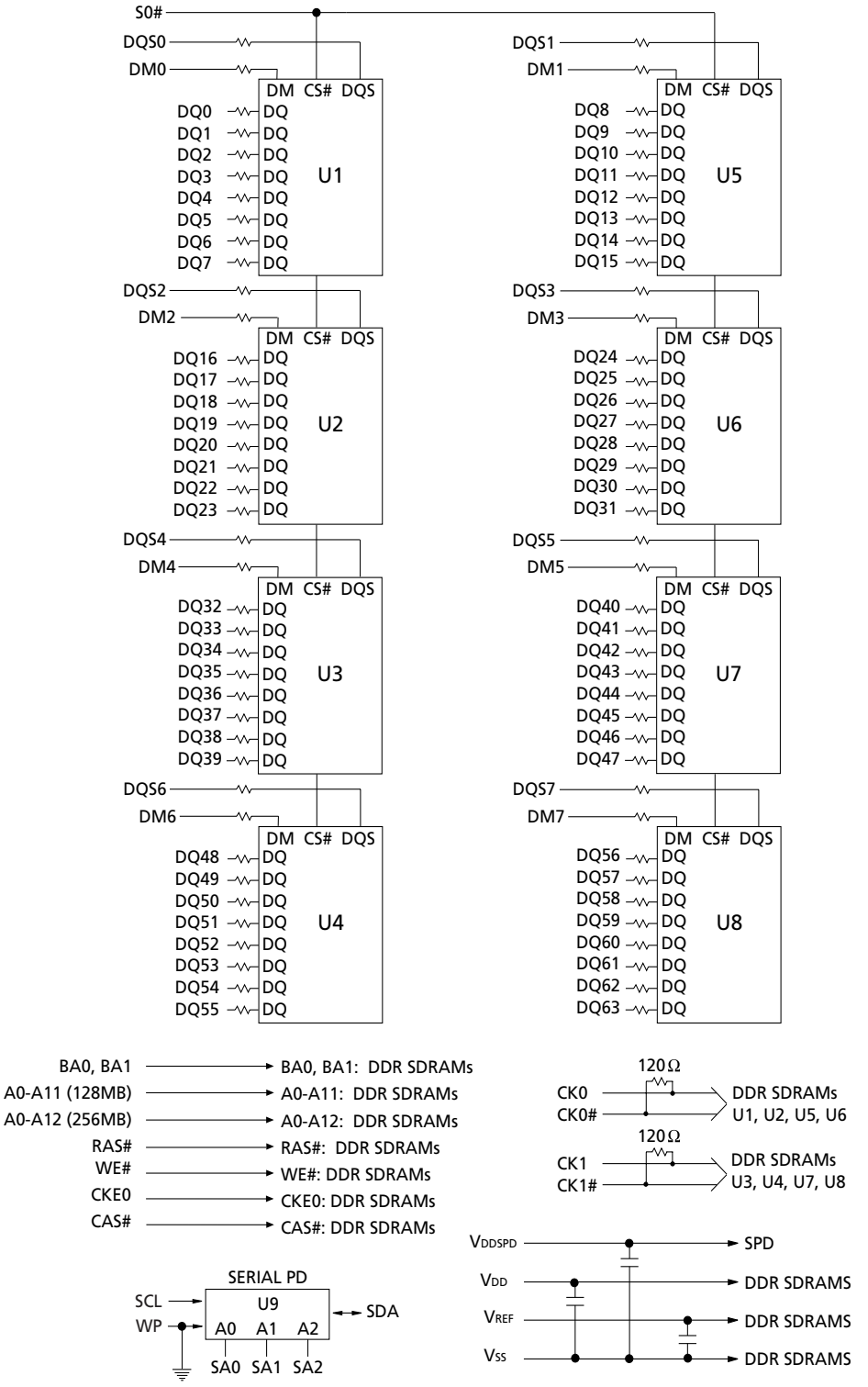
PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
118, 119, 120	WE#, CAS#, RAS#	Input	Command Inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
35, 37, 158, 160	CK0, CK0#, CK1, CK1#,	Input	Clock: CK, CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK,and negative edge of CK#. Output data (DQs and DQS) is referenced to the crossings of CK and CK#.
96	CKE0	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all device banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any device bank).CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK# and CKE) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V_{DD} is applied and until CKE is first brought HIGH. After CKE is brought HIGH, it becomes an SSTL_2 input only.
121	S0#	Input	Chip Selects: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# is considered part of the command code.
116, 117	BA0, BA1	Input	Bank Address: BA0 and BA1 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
99 (256MB), 100, 101, 102, 105, 106, 107, 108, 109, 110, 111, 112, 115	A0-A11 (128MB) A0-A12 (256MB)	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
11, 25, 47, 61, 133, 147, 169, 183	DQS0-DQS7	Input/ Output	Data Strobe: Output with READ data, input with WRITE data. DQS is edge-aligned with READ data, centered in WRITE data. Used to capture data.
12, 26, 48, 62, 134, 148, 170, 184	DM0-DM7	Input	Data Write Mask. DM LOW allows WRITE operation. DM HIGH blocks WRITE operation. DM lines do not affect READ operation.

Table 5: Pin Descriptions

Pin numbers may not correlate with symbols. Refer to Pin Assignment tables on page 3 for more information

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
5, 6, 7, 8, 13, 14, 17, 18, 19, 20, 23, 24, 29, 30, 31, 32, 41, 42, 43, 44, 49, 50, 53, 54, 55, 56, 59, 60, 65, 66, 67, 68, 127, 128, 129, 130, 135, 136, 139, 140, 141, 142, 145, 146, 151, 152, 153, 154, 163, 164, 165, 166, 171, 172, 175, 176, 177, 178, 181, 182, 187, 188, 189, 190	DQ0-DQ63	Input/ Output	Data I/Os: Data bus.
195	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
194, 196, 198	SA0-SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
193	SDA	Input/ Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
1, 2	V_{REF}	Input	SSTL_2 reference voltage.
9, 10, 21, 22, 33, 34, 36, 45, 46, 57, 58, 69, 70, 81, 82, 92, 93, 94, 113, 114, 131, 132, 143, 144, 155, 156, 157, 167, 168, 179, 180, 191, 192	V_{DD}	Supply	Power Supply: +2.5V ±0.2V. See note 49 on page 22.
3, 4, 15, 16, 27, 28, 38, 39, 40, 51, 52, 63, 64, 75, 76, 87, 88, 90, 103, 104, 125, 126, 137, 138, 149, 150, 159, 161, 162, 173, 174, 185, 186	V_{SS}	Supply	Ground.
197	V_{DDSPD}	Supply	Serial EEPROM positive power supply: +2.3V to +3.6V.
71, 72, 73, 74, 77, 78, 79, 80, 83, 84, 95, 122	DNU	—	Do Not Use: These pins are not connected on these modules, but are assigned pins on other modules in this product family.
85, 97, 99 (128MB), 123, 199, 98, 124, 200	NC	—	No Connect: These pins should be left unconnected.

Figure 3: Functional Block Diagram



DDR SDRAMS = MT46V16M8TG for 128MB module
DDR SDRAMS = MT46V32M8TG for 256MB module

NOTE:

1. Unless otherwise stated, all resistors are 22Ω.
2. Per industry standard, Micron utilizes various component speed grades as referenced in the Module Part Numbering Guide at www.micron.com/numberguide.

General Description

The MT8VDDT1664H and MT8VDDT3264H are high-speed CMOS, dynamic random-access, 128MB and 256MB memory modules organized in x64 configuration. DDR SDRAM modules use internally configured quad-bank DDR SDRAMs.

DDR SDRAM modules use a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-pre-fetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM module effectively consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR SDRAM modules operate from differential clock inputs (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to DDR SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed (BA0, BA1 select device bank; A0–A11 select device row (128MB), A0–A12 select device row (256MB). The address bits registered coincident with the READ or WRITE command are used to select the device bank and the starting device column location for the burst access.

DDR SDRAM modules provide for programmable READ or WRITE burst lengths of 2, 4, or 8 locations. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

The pipelined, multibank architecture of DDR SDRAM modules allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible. For more information regarding DDR SDRAM operation, refer to the 128Mb and 256Mb DDR SDRAM component data sheets.

Serial Presence-Detect Operation

These DDR SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

Mode Register Definition

The mode register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency and an operating mode, as shown in Figure 4, Mode Register Definition Diagram, on page 8. The mode register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

Reprogramming the mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded (reloaded) when all device banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Mode register bits A0–A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4–A6 specify the CAS latency, and A7–A11 (128MB) or A7–A12 (256MB) specify the operating mode.

Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 4, Mode Register Definition Diagram. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1–A*i* when the burst length is set to two, by A2–A*i* when the burst length is set to four and by A3–A*i* when the burst length is set to eight (where A*i* is the most significant column address bit for a given configuration; see Note 5 for Figure 6, Burst Definition Table, on page 9). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Figure 6, Burst Definition Table, on page 9.

Read Latency

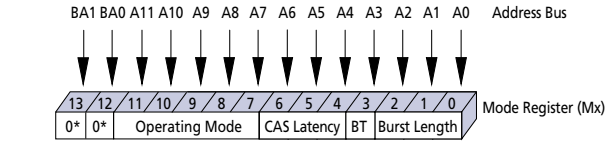
The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 2 or 2.5 clocks, as shown in Figure 5, CAS Latency Diagram.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m*. Table 7, CAS Latency (CL) Table, on page 9, indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

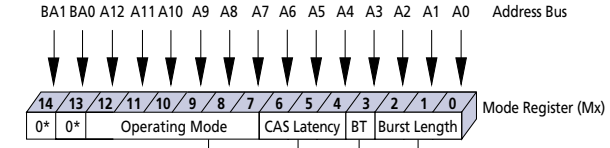
Figure 4: Mode Register Definition Diagram

128MB Module Address Bus



* M13 and M12 (BA1and BA0) must be "0, 0" to select the base mode register (vs. the extended mode register).

256MB Module Address Bus



* M14 and M13 (BA1 and BA0) must be "0, 0" to select the base mode register (vs. the extended mode register).

			Burst Length	
M2	M1	M0	M3 = 0	M3 = 1
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5
1	1	1	Reserved

M12	M11	M10	M9	M8	M7	M6-M0	Operating Mode
0	0	0	0	0	0	Valid	Normal Operation
0	0	0	0	1	0	Valid	Normal Operation/Reset DLL
-	-	-	-	-	-	-	All other states reserved

Table 6: Burst Definition Table

BURST LENGTH	STARTING COLUMN ADDRESS			ORDER OF ACCESSES WITHIN A BURST	
				TYPE = SEQUENTIAL	TYPE = INTERLEAVED
2			A0		
			0	0-1	0-1
			1	1-0	1-0
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

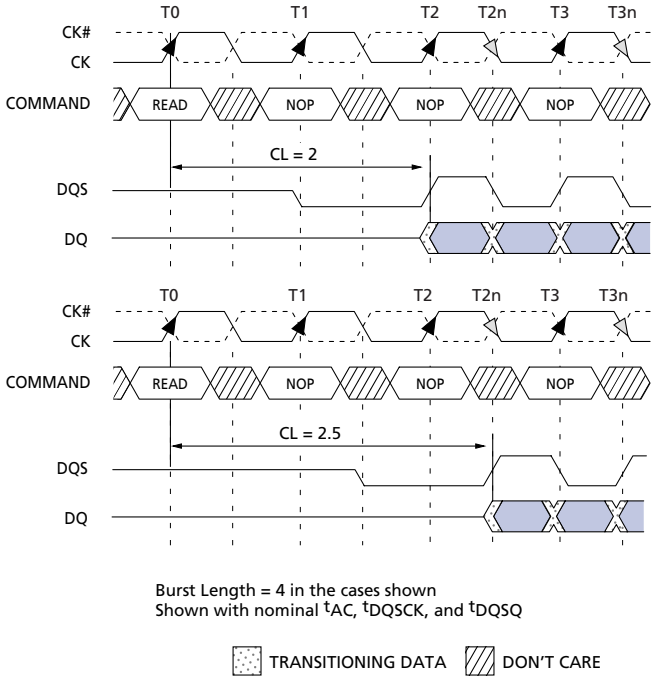
NOTE:

1. For a burst length of two, A1–A*i* select the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2–A*i* select the four-data-element block; A0–A1 select the first access within the block.
3. For a burst length of eight, A3–A*i* select the eight-data-element block; A0–A2 select the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
5. *i* = 9

Table 7: CAS Latency (CL) Table

	ALLOWABLE OPERATING CLOCK FREQUENCY (MHZ)	
SPEED	CL = 2	CL = 2.5
-335	75 ≤ f ≤ 133	75 ≤ f ≤ 166
-262	75 ≤ f ≤ 133	75 ≤ f ≤133
-26A	75 ≤ f ≤ 133	75 ≤ f ≤133
-265	75 ≤ f ≤ 100	75 ≤ f ≤ 133
-202	75 ≤ f ≤ 100	75 ≤ f ≤ 125

Figure 5: CAS Latency Diagram



Operating Mode

The normal operating mode is selected by issuing a MODE REGISTER SET command with bits A7–A11 (128MB), or A7–A12 (256MB) each set to zero, and bits A0–A6 set to the desired values. A DLL reset is initiated by issuing a MODE REGISTER SET command with bits A7 and A9–A11 (128MB), or A7 and A9–A12 (256MB) each set to zero, bit A8 set to one, and bits A0–A6 set to the desired values. Although not required by the Micron device, JEDEC specifications recommend when a LOAD MODE REGISTER command is issued to reset the DLL, it should always be followed by a LOAD MODE REGISTER command to select normal operating mode.

All other combinations of values for A7–A11, or A7–A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Extended Mode Register

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable and output drive strength. These functions are controlled via the bits shown in Figure 6, Extended Mode Register Definition Diagram, on page 10. The extended mode register is programmed via the LOAD MODE REGIS-

TER command to the mode register (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power. The enabling of the DLL should always be followed by a LOAD MODE REGISTER command to the mode register (BA0/BA1 both LOW) to reset the DLL.

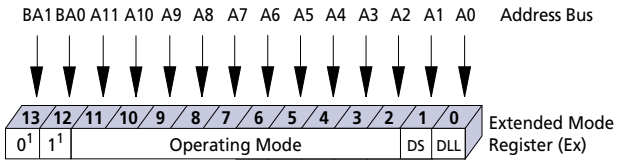
The extended mode register must be loaded when all device banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

DLL Enable/Disable

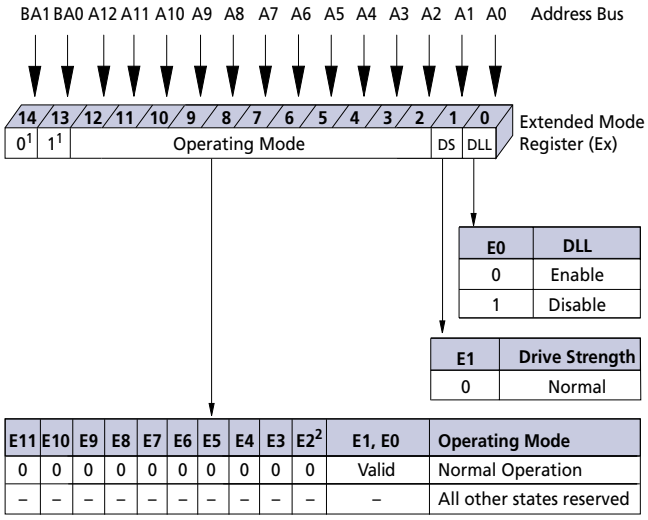
The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. (When the device exits self refresh mode, the DLL is enabled automatically.) Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.

Figure 6: Extended Mode Register Definition Diagram

128MB Module



256MB Module



NOTE:

1. BA1 and BA0 (E13 and E12 for 128MB, E14 and E13 for 256MB) must be "0, 1" to select the Extended Mode Register (vs. the base Mode Register).
2. The QFC# option is not supported.

Commands

The Truth Tables below provides a general reference of available commands. For a more detailed description of commands and operations, refer to the 128Mb or 256Mb DDR SDRAM component data sheet.

Table 8: Truth Table – Commands

CKE is HIGH for all commands shown except SELF REFRESH

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	1
NO OPERATION (NOP)	L	H	H	H	X	1
ACTIVE (Select device bank and activate row)	L	L	H	H	Bank/Row	2
READ (Select device bank and column, and start READ burst)	L	H	L	H	Bank/Col	3
WRITE (Select device bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	3
BURST TERMINATE	L	H	H	L	X	4
PRECHARGE (Deactivate row in device bank or banks)	L	L	H	L	Code	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	6, 7
LOAD MODE REGISTER	L	L	L	L	Op-Code	8

NOTE:

1. DESELECT and NOP are functionally interchangeable.
2. BA0–BA1 provide device bank address and A0–A11 (128MB) or A0–A12 (256MB) provide row address.
3. BA0–BA1 provide device bank address; A0–A9, provide column address; A10 HIGH enables the auto precharge feature (non-persistent), and A10 LOW disables the auto precharge feature.
4. Applies only to read bursts with auto precharge disabled; this command is undefined (and should not be used) for READ bursts with auto precharge enabled and for WRITE bursts.
5. A10 LOW: BA0–BA1 determine which device bank is precharged. A10 HIGH: all device banks are precharged and BA0-BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. BA0–BA1 select either the mode register or the extended mode register (BA0 = 0, BA1 = 0 select the mode register; BA0 = 1, BA1 = 0 select extended mode register; other combinations of BA0–BA1 are reserved).
   A0–A11 (128MB) or A0–A12 (256MB) provide the op-code to be written to the selected mode register.

Table 9: Truth Table – DM Operation

Used to mask write data; provided coincident with the corresponding data

NAME (FUNCTION)	DM	DQS
WRITE Enable	L	Valid
WRITE Inhibit	H	X

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Voltage on VDD Supply
Relative to VSS . . . . . -1V to +3.6V
Voltage on VDDQ Supply
Relative to VSS . . . . . -1V to +3.6V
Voltage on VREF and Inputs
Relative to VSS . . . . . -1V to +3.6V
Voltage on I/O Pins
Relative to VSS . . . . . -0.5V to VDDQ +0.5V

Operating Temperature,
T_A (ambient) . . . . . 0°C to +70°C
Storage Temperature (plastic) . . . . . -55°C to +150°C
Power Dissipation 8W
Short Circuit Output Current 50mA

Table 10: DC Electrical Characteristics and Operating Conditions

Notes: 1–5, 14, 49; notes appear on pages 19–22; 0°C ≤ T_A ≤ +70°C

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		VDD	2.3	2.7	V	32, 36
I/O Supply Voltage		VDDQ	2.3	2.7	V	32, 36, 39
I/O Reference Voltage		VREF	0.49 × VDDQ	0.51 × VDDQ	V	6, 39
I/O Termination Voltage (system)		VTT	VREF - 0.04	VREF + 0.04	V	7, 39
Input High (Logic 1) Voltage		VIH(DC)	VREF + 0.15	VDD + 0.3	V	25
Input Low (Logic 0) Voltage		VIL(DC)	-0.3	VREF - 0.15	V	25
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ VDD, Vref pin 0V ≤ VIN ≤ 1.35V (All other pins not under test = 0V)	Command/Address, RAS#, CAS#, WE#, CKE, S#	II	-16	16	µA	48
	CK, CK#		-8	8		
	DM		-2	2		
OUTPUT LEAKAGE CURRENT (DQ pins are disabled; 0V ≤ VOUT ≤ VDDQ)	DQ, DQS	IOZ	-5	5	µA	48
OUTPUT LEVELS High Current (VOUT = VDDQ-0.373V, minimum VREF, minimum VTT)		IOH	-16.8	–	mA	33, 34
Low Current (VOUT = 0.373V, maximum VREF, maximum VTT)		IOL	16.8	–	mA	

Table 11: AC Input Operating Conditions

Notes: 1–5, 14, 49; notes appear on pages 19–22; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.5V ±0.2V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	VIH(AC)	VREF + 0.310	–	V	12, 25, 35
Input Low (Logic 0) Voltage	VIL(AC)	–	VREF - 0.310	V	12, 25, 35
I/O Reference Voltage	VREF(AC)	0.49 × VDDQ	0.51 × VDDQ	V	6

Table 12: IDD Specifications and Conditions – 128MB Module

DDR SDRAM component values only

Notes: 1–5, 8, 10, 12, 49; notes appear on pages 19–22; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.5V ±0.2V

			MAX					
PARAMETER/CONDITION		SYM	-335	-262	-26A/ -265	-202	UNITS	NOTES
OPERATING CURRENT: One device bank; Active-Precharge; tRC = tRC (MIN); tCK = tCK (MIN); DQ, DM and DQS inputs changing once per clock cyle; Address and control inputs changing once every two clock cycles		IDD0	960	880	840	800	mA	20, 43
OPERATING CURRENT: One device bank; Active -Read Precharge; Burst = 2; tRC = tRC (MIN); tCK = tCK (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle		IDD1	1,080	960	960	880	mA	20, 43
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; tCK = tCK (MIN); CKE = (LOW)		IDD2P	24	24	24	24	mA	21, 28, 45
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; tCK = tCK MIN; CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM		IDD2F	360	360	360	280	mA	46
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; tCK = tCK (MIN); CKE = LOW		IDD3P	200	200	160	160	mA	21, 28, 45
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; tRC = tRAS (MAX); tCK = tCK (MIN); DQ, DM andDQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		IDD3N	360	360	360	280	mA	20
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); IOUT = 0mA		IDD4R	1,040	1,040	1,000	840	mA	20, 43
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W	1,080	1,000	920	840	mA	20, 42
AUTO REFRESH CURRENT	tRC = tRC (MIN)	IDD5	1,880	1,720	1,680	1,640	mA	24, 45
	tRC = 15.625µs	IDD5A	40	40	40	40	mA	24, 45
SELF REFRESH CURRENT: CKE ≤ 0.2V		IDD6	16	16	16	16	mA	9
OPERATING CURRENT: Four device bank interleaving READs (BL = 4) with auto precharge, tRC = tRC (MIN); tCK = tCK (MIN); Address and control inputs change only during Active READ or WRITE commands		IDD7	2,840	2,640	2,600	2,200	mA	20, 44

Table 13: IDD Specifications and Conditions – 256MB Module

DDR SDRAM component values only

Notes: 1–5, 8, 10, 12, 49; notes appear on pages 19–22; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.5V ±0.2V

			MAX					
PARAMETER/CONDITION		SYM	-335	-262	-26A/ -265	-202	UNITS	NOTES
OPERATING CURRENT: One device bank; Active-Precharge; tRC = tRC (MIN); tCK = tCK (MIN); DQ, DM and DQS inputs changing once per clock cyle; Address and control inputs changing once every two clock cycles		IDD0	1,000	1,000	840	960	mA	20, 43
OPERATING CURRENT: One device bank; Active -Read Precharge; Burst = 2; tRC = tRC (MIN); tCK = tCK (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle		IDD1	1,360	1,280	1,160	1,240	mA	20, 43
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; tCK = tCK (MIN); CKE = (LOW)		IDD2P	32	32	32	32	mA	21, 28, 45
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; tCK = tCK MIN; CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM		IDD2F	400	360	360	360	mA	46
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; tCK = tCK (MIN); CKE = LOW		IDD3P	240	200	200	240	mA	21, 28, 45
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; tRC = tRAS (MAX); tCK = tCK (MIN); DQ, DM andDQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		IDD3N	480	400	400	400	mA	20
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); IOUT = 0mA		IDD4R	1,400	1,200	1,200	1,400	mA	20, 43
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W	1,240	1,080	1,080	1,520	mA	20, 42
AUTO REFRESH CURRENT	tRC = tRC (MIN)	IDD5	2,040	1,880	1,880	1,960	mA	24, 45
	tRC = 7.8125µs	IDD5A	48	48	48	48	mA	24, 45
SELF REFRESH CURRENT: CKE ≤ 0.2V		IDD6	32	32	32	32	mA	9
OPERATING CURRENT: Four device bank interleaving READs (BL = 4) with auto precharge, tRC = tRC (MIN); tCK = tCK (MIN); Address and control inputs change only during Active READ or WRITE commands		IDD7	3,240	2,800	2,800	2,920	mA	20, 44

Table 14: Capacitance

Note: 11; notes appearon pages 19–22

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input/Output Capacitance: DQ, DQS, DM	C_{IO}	4	5	pF
Input Capacitance: Command and Address, S#, CKE	C_{I1}	16	24	pF
Input Capacitance: CK CK#	C_{I2}	8	12	pF

Table 15: DDR SDRAM Component Electrical Characteristics and Recommended AC Operating Conditions (-335 and -262 Speed Grades)

Notes: 1–5, 12-15, 29, 49; notes appear on pages 19–22; 0°C ≤ T_A ≤ +70°C; V_{DD} = $V_{DD}Q$ = +2.5V ±0.2V

AC CHARACTERISTICS			-335		-262			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Access window of DQs from CK/CK#		^tAC	-0.7	+0.75	-0.75	+0.75	ns	
CK high-level width		^tCH	0.45	0.55	0.45	0.55	^tCK	26
CK low-level width		^tCL	0.45	0.55	0.45	0.55	^tCK	26
Clock cycle time	CL=2.5	^tCK (2.5)	6	13	7.5	13	ns	40, 47
	CL=2	^tCK (2)	7.5	13	7.5	13	ns	40, 47
DQ and DM input hold time relative to DQS		^tDH	0.45		0.5		ns	23, 27
DQ and DM input setup time relative to DQS		^tDS	0.45		0.5		ns	23, 27
DQ and DM input pulse width (for each input)		^tDIPW	1.75		1.75		ns	27
Access window of DQS from CK/CK#		^tDQSCK	-0.60	+0.60	-0.75	+0.75	ns	
DQS input high pulse width		^tDQSH	0.35		0.35		^tCK	
DQS input low pulse width		^tDQSL	0.35		0.35		^tCK	
DQS-DQ skew, DQS to last DQ valid, per group, per access		^tDQSQ		0.45		0.5	ns	22, 23
Write command to first DQS latching transition		^tDQSS	0.75	1.25	0.75	1.25	^tCK	
DQS falling edge to CK rising - setup time		^tDSS	0.2		0.2		^tCK	
DQS falling edge from CK rising - hold time		^tDSH	0.2		0.2		^tCK	
Half clock period		^tHP	^tCH, ^tCL		^tCH, ^tCL		ns	30
Data-out high-impedance window from CK/CK#		^tHZ		+0.70		+0.75	ns	16, 37
Data-out low-impedance window from CK/CK#		^tLZ	-0.70		-0.75		ns	16, 38
Address and control input hold time (fast slew rate)		^tIH_F	0.75		0.90		ns	12
Address and control input setup time (fast slew rate)		^tIS_F	0.75		0.90		ns	12
Address and control input hold time (slow slew rate)		^tIH_S	0.80		1		ns	12
Address and control input setup time (slow slew rate)		^tIS_S	0.80		1		ns	12
LOAD MODE REGISTER command cycle time		^tMRD	12		15		ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access		^tQH	^tHP - ^tQHS		^tHP - ^tQHS		ns	22, 23
Data hold skew factor		^tQHS		0.55		0.75	ns	
ACTIVE to PRECHARGE command		^tRAS	42	70,000	40	120,000	ns	31
ACTIVE to READ with Auto precharge command	128MB	^tRAP	18		15		ns	41
	256MB		18		15		ns	
ACTIVE to ACTIVE/AUTO REFRESH command period		^tRC	60		65		ns	
AUTO REFRESH command period		^tRFC	72		75		ns	45
ACTIVE to READ or WRITE delay		^tRCD	18		15		ns	
PRECHARGE command period		^tRP	18		15		ns	
DQS read preamble		^tRPRE	0.9	1.1	0.9	1.1	^tCK	37

Table 15: DDR SDRAM Component Electrical Characteristics and Recommended AC Operating Conditions (-335 and -262 Speed Grades) (Continued)

Notes: 1–5, 12-15, 29, 49; notes appear on pages 19–22; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.5V ±0.2V

AC CHARACTERISTICS			-335		-262			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
DQS read postamble		^{t}RPST	0.4	0.6	0.4	0.6	^{t}CK	
ACTIVE bank a to ACTIVE bank b command		^{t}RRD	12		15		ns	
DQS write preamble		^{t}WPRE	0.25		0.25		^{t}CK	
DQS write preamble setup time		^{t}WPRES	0		0		ns	18, 19
DQS write postamble		^{t}WPST	0.4	0.6	0.4	0.6	^{t}CK	17
Write recovery time		^{t}WR	15		15		ns	
Internal WRITE to READ command delay		^{t}WTR	1		1		^{t}CK	
Data valid output window		na	^{t}QH - ^{t}DQSQ		^{t}QH - ^{t}DQSQ		ns	22
REFRESH to REFRESH command interval	128MB	^{t}REFC		140.6		140.6	µs	21
	256MB			70.3		70.3	µs	21
Average periodic refresh interval	128MB	^{t}REFI		15.6		15.6	µs	21
	256MB			7.8		7.8	µs	21
Terminating voltage delay to VDD		^{t}VTD	0		0		ns	
Exit SELF REFRESH to non-READ command		^{t}XSNR	75		75		ns	
Exit SELF REFRESH to READ command		^{t}XSRD	200		200		^{t}CK	

Table 16: DDR SDRAM Component Electrical Characteristics and Recommended AC Operating Conditions (-26A/-265 and -202 Speed Grades)

Notes: 1–5, 12-15, 29, 49; notes appear on pages 19–22; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.5V ±0.2V

AC CHARACTERISTICS			-26A/-265		-202			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Access window of DQs from CK/CK#		tAC	-0.75	+0.75	-0.8	+0.8	ns	
CK high-level width		tCH	0.45	0.55	0.45	0.55	tCK	26
CK low-level width		tCL	0.45	0.55	0.45	0.55	tCK	26
Clock cycle time	CL=2.5	tCK (2.5)	7.5	13	8	13	ns	40, 47
	CL=2	tCK (2)	7.5/10	13	10	13	ns	40, 47
DQ and DM input hold time relative to DQS		tDH	0.5		0.6		ns	23, 27
DQ and DM input setup time relative to DQS		tDS	0.5		0.6		ns	23, 27
DQ and DM input pulse width (for each input)		tDIPW	1.75		2		ns	27
Access window of DQS from CK/CK#		tDQSCK	-0.75	+0.75	-0.8	+0.8	ns	
DQS input high pulse width		tDQSH	0.35		0.35		tCK	
DQS input low pulse width		tDQSL	0.35		0.35		tCK	
DQS-DQ skew, DQS to last DQ valid, per group, per access		tDQSQ		0.5		0.6	ns	22, 23
Write command to first DQS latching transition		tDQSS	0.75	1.25	0.75	1.25	tCK	
DQS falling edge to CK rising - setup time		tDSS	0.2		0.2		tCK	
DQS falling edge from CK rising - hold time		tDSH	0.2		0.2		tCK	
Half clock period		tHP	tCH, tCL		tCH, tCL		ns	30
Data-out high-impedance window from CK/CK#		tHZ		+0.75		+0.8	ns	16, 37
Data-out low-impedance window from CK/CK#		tLZ	-0.75		-0.8		ns	16, 38
Address and control input hold time (fast slew rate)		tIHF	0.90		1.1		ns	12
Address and control input setup time (fast slew rate)		tISF	0.90		1.1		ns	12
Address and control input hold time (slow slew rate)		tIHS	1		1.1		ns	12
Address and control input setup time (slow slew rate)		tISS	1		1.1		ns	12
LOAD MODE REGISTER command cycle time		tMRD	15		16		ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access		tQH	tHP - tQHS		tHP - tQHS		ns	22, 23
Data hold skew factor		tQHS		0.75		1	ns	
ACTIVE to PRECHARGE command		tRAS	40	120,000	40	120,000	ns	31
ACTIVE to READ with Auto precharge command	128MB	tRAP	tRAS(MIN)-(burst length*tCK/2)				ns	41
	256MB		20		20		ns	
ACTIVE to ACTIVE/AUTO REFRESH command period		tRC	65		70		ns	
AUTO REFRESH command period		tRFC	75		80		ns	45
ACTIVE to READ or WRITE delay		tRCD	20		20		ns	
PRECHARGE command period		tRP	20		20		ns	
DQS read preamble		tRPRE	0.9	1.1	0.9	1.1	tCK	37
DQS read postamble		tRPST	0.4	0.6	0.4	0.6	tCK	
ACTIVE bank a to ACTIVE bank b command		tRRD	15		15		ns	
DQS write preamble		tWPRE	0.25		0.25		tCK	
DQS write preamble setup time		tWPRES	0		0		ns	18, 19
DQS write postamble		tWPST	0.4	0.6	0.4	0.6	tCK	17
Write recovery time		tWR	15		15		ns	
Internal WRITE to READ command delay		tWTR	1		1		tCK	
Data valid output window		na	tQH - tDQSQ		tQH - tDQSQ		ns	22

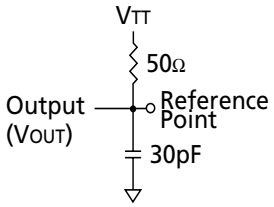
Table 16: DDR SDRAM Component Electrical Characteristics and Recommended AC Operating Conditions (-26A/-265 and -202 Speed Grades) (Continued)

Notes: 1–5, 12-15, 29, 49; notes appear on pages 19–22; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.5V ±0.2V

AC CHARACTERISTICS			-26A/-265		-202			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
REFRESH to REFRESH command interval	128MB	^{t}REFC		140.6		140.6	µs	21
	256MB			70.3		70.3	µs	21
Average periodic refresh interval	128MB	^{t}REFI		15.6		15.6	µs	21
	256MB			7.8		7.8	µs	21
Terminating voltage delay to VDD		^{t}VTD	0		0		ns	
Exit SELF REFRESH to non-READ command		^{t}XSNR	75		80		ns	
Exit SELF REFRESH to READ command		^{t}XSRD	200		200		^{t}CK	

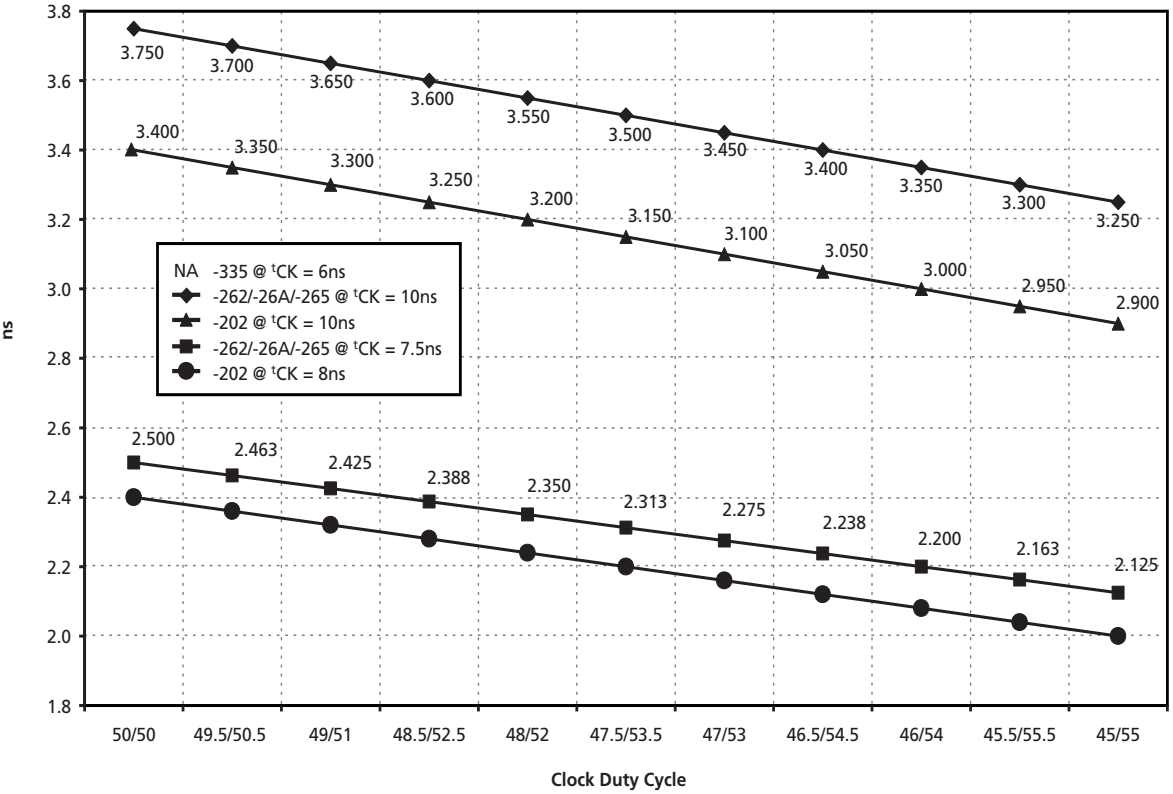
Notes

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:



4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between V_{IL} (ACV) and V_{IH} (AC).
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. V_{REF} is expected to equal V_{DDQ}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ±2 percent of the DC value. Thus, from V_{DDQ}/2, V_{REF} is allowed ±25mV for DC error and an additional ±25mV for AC noise. This measurement is to be taken at the nearest V_{REF} by-pass capacitor.
7. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
8. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time at CL = 2 for -262, -26A, and -202, CL = 2.5 for -335 and -265 with the outputs open.
9. Enables on-chip refresh and address counters.
10. I_{DD} specifications are tested after the device is properly initialized, and is averaged at the defined cycle rate.
11. This parameter is sampled. V_{DD} = +2.5V ±0.2V, V_{DDQ} = +2.5V ±0.2V, V_{REF} = V_{SS}, f = 100 MHz, T_A = 25°C, V_{OUT} (DC) = V_{DDQ}/2, V_{OUT} (peak to peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
12. Command/Address input slew rate = 0.5V/ns. For -335, -262, -26A, and -265 with slew rates 1V/ns and faster, ^{t}IS and ^{t}IH are reduced to 900ps. If the slew rate is less than 0.5V/ ns, timing must be derated: ^{t}IS has an additional 50ps per each 100mV/ns reduction in slew rate from the 500mV/ns, while ^{t}IH remains constant. If the slew rate exceeds 4.5V/ns, functionality is uncertain.
13. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference level for signals other than CK/CK# is V_{REF}.
14. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before V_{REF} stabilizes, CKE ≤ 0.3 x V_{DDQ} is recognized as LOW.
15. The output timing reference level, as measured at the timing reference point indicated in Note 3, is V_{TT}.
16. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
17. If DQS transitions to HIGH above V_{IH} (DC) MIN, then it must not transition to LOW below V_{IH} (DC) MIN prior to ^{t}DQSH (MIN).
18. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
19. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on ^{t}DQSS.
20. MIN (^{t}RC or ^{t}RFC) for I_{DD} measurements is the smallest multiple of ^{t}CK that meets the minimum absolute value for the respective parameter. ^{t}RAS (MAX) for I_{DD} measurements is the largest multiple of ^{t}CK that meets the maximum absolute value for ^{t}RAS.

Figure 7: Derating Data Valid Window



21. The refresh period is 64ms. This equates to an average refresh rate of 15.625µs (128MB) or 7.8125µs (256MB). However, an AUTO REFRESH command must be asserted at least once every 140.6µs (128MB) or 70.3µs (256MB); burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.
22. The valid data window is derived by achieving other specifications: ^{t}HP (^{t}CK/2), ^{t}DQSQ, and ^{t}QH (^{t}QH = ^{t}HP - ^{t}QHS). The data valid window derates directly porportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55. Functionality is uncertain when operating beyond a 45/55 ratio. Figure 7, Derating Data Valid Window, shows the derating curves for duty cycles ranging between 50/50 and 45/55.
23. Each byte lane has a corresponding DQS.
24. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period (^{t}RFC [MIN]) else CKE is LOW (i.e., during standby).
25. To maintain a valid level, the transitioning edge of the input must:
    a. Sustain a constant slew rate from the current AC level through to the target AC level, VIL (AC) or VIH (AC).
    b. Reach at least the target AC level.
    c. After the AC target level is reached, continue to maintain at least the target DC level, VIL (DC) or VIH (DC).
26. JEDEC specifies CK and CK# input slew rate must be ≥ 1V/ns (2V/ns differentially).
27. DQ and DM input slew rates must not deviate from DQS by more than 10 percent. If the DQ/DM/DQS slew rate is less than 0.5V/ns, timing must be derated: 50ps must be added to ^{t}DS and ^{t}DH for each 100mv/ns reduction in slew rate. If slew rate exceeds 4V/ns, functionality is uncertain.
28. VDD must not vary more than 4 percent if CKE is not active while any device bank is active.
29. The clock is allowed up to ±150ps of jitter. Each timing parameter is allowed to vary by the same amount.

30. tHP min is the lesser of tCL minimum and tCH minimum actually applied to the device CK and CK/ inputs, collectively during device bank active.
31. READs and WRITEs with auto precharge are not allowed to be issued until tRAS(MIN) can be satisfied prior to the internal precharge command being issued.
32. Any positive glitch in the nominal voltage must be less than 1/3 of the clock and not more than +400mV or 2.9V maximum, whichever is less. Any negative glitch must be less than 1/3 of the clock cycle and not exceed either -300mV or 2.2V minimum, whichever is more positive.
33. Normal Output Drive Curves:
    a. The full variation in driver pull-down current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 8, Pull-Down Characteristics.
    b. The variation in driver pull-down current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 8, Pull-Down Characteristics.
    c. The full variation in driver pull-up current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 9, Pull-Up Characteristics.
    d. The variation in driver pull-up current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 9, Pull-Up Characteristics.
    e. The full variation in the ratio of the maximum to minimum pull-up and pull-down current should be between 0.71 and 1.4, for device drain-to-source voltages from 0.1V to 1.0V, and at the same voltage and temperature.
    f. The full variation in the ratio of the nominal pull-up to pull-down current should be unity ±10 percent, for device drain-to-source voltages from 0.1V to 1.0V.
34. The voltage levels used are derived from a minimum VDD level and the referenced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.
35. VIH overshoot: VIH (MAX) = VDDQ + 1.5V for a pulse width ≤ 3ns and the pulse width can not be greater than 1/3 of the cycle rate. VIL undershoot: VIL (MIN) = -1.5V for a pulse width ≤ 3ns and the pulse width can not be greater than 1/3 of the cycle rate.
36. VDD and VDDQ must track each other.
37. This maximum value is derived from the referenced test load. In practice, the values obtained in a typical terminated design may reflect up to 310ps less for tHZ(MAX) and the last DVW. tHZ (MAX) will prevail over tDQSCK (MAX) + tRPST (MAX) condition. tLZ (MIN) will prevail over tDQSCK (MIN) + tRPRE (MAX) condition.
38. For slew rates greater than 1V/ns the (LZ) transition will start about 310ps earlier.
39. During initialization, VDDQ, VTT, and VREF must be equal to or less than VDD + 0.3V. Alternatively, VTT may be 1.35V maximum during power up, even if VDD/VDDQ are 0V, provided a minimum of 42Ω of series resistance is used between the VTT supply and the input pin.

Figure 8: Pull-Down Characteristics

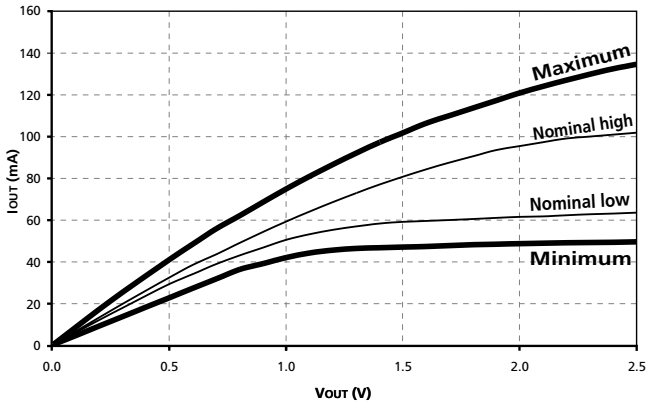
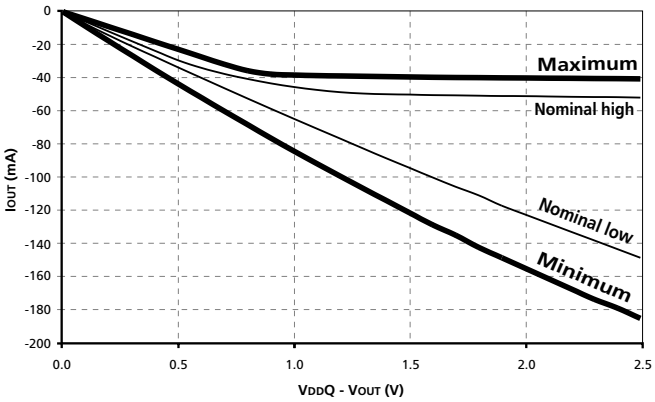


Figure 9: Pull-Up Characteristics



40. The current Micron part operates below the slowest JEDEC operating frequency of 83 MHz. As such, future die may not reflect this option.
41. ^{t}RAP ≥ ^{t}RCD. Does not apply to -335 speed grade.
42. For the -335, -262, -26A and -265, IDD3N is specified to be 35mA at 100 MHz.
43. Random addressing changing and 50 percent of data changing at every transfer.
44. Random addressing changing and 100 percent of data changing at every transfer.
45. CKE must be active (high) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until ^{t}REF later.
46. IDD2N specifies the DQ, DQS, and DM to be driven to a valid high or low logic level. IDD2Q is similar to IDD2F except IDD2Q specifies the address and control inputs to remain stable. Although IDD2F, IDD2N, and IDD2Q are similar, IDD2F is "worst case."
47. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset. This is followed by 200 clock cycles (before READ commands).
48. Leakage number reflects the worst case leakage possible through the module pin, not what each memory device contributes.
49. The -335 module speed grade, using the -6R speed device, has VDD (MIN) = 2.4V.

SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (as shown in Figure 10, Data Validity, and Figure 11, Definition of Start and Stop).

SPD Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD Stop Condition

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (as shown in Figure 12, Acknowledge Response from Receiver).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 10: Data Validity

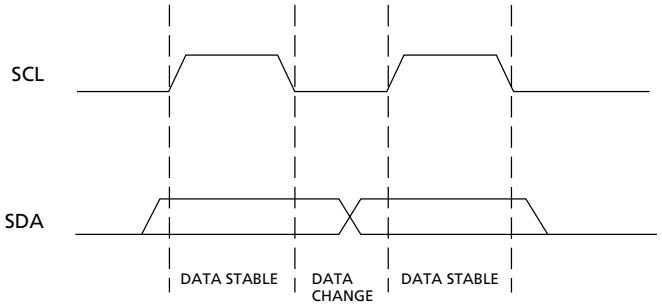


Figure 11: Definition of Start and Stop

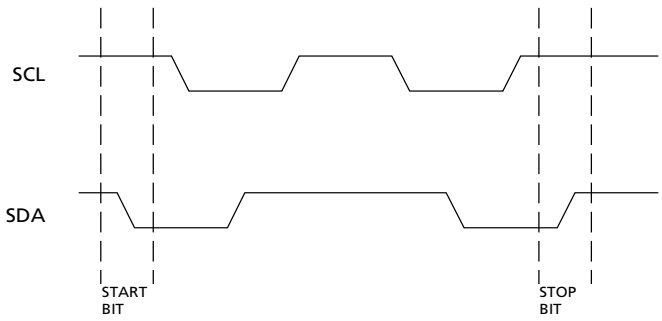


Figure 12: Acknowledge Response from Receiver

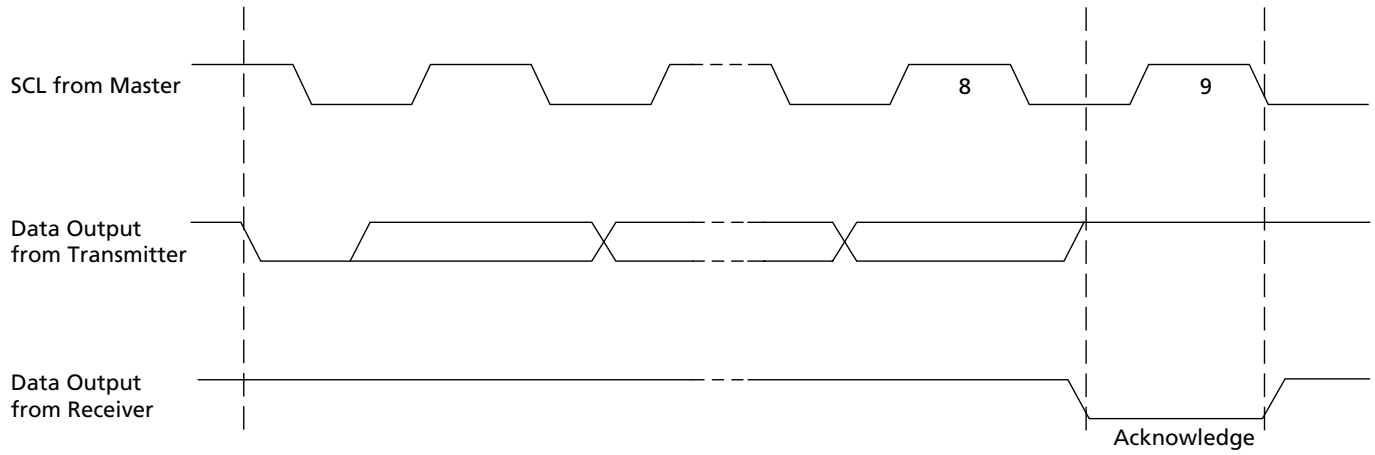


Table 17: EEPROM Device Select Code

Most significant bit (b7) is sent first

SELECT CODE	DEVICE TYPE IDENTIFIER				CHIP ENABLE			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Select Code (two arrays)	1	0	1	0	SA2	SA1	SA0	RW
Protection Register Select Code	0	1	1	0	SA2	SA1	SA0	RW

Table 18: EEPROM Operating Modes

MODE	RW BIT	WC	BYTES	INITIAL SEQUENCE
Current Address Read	1	VIH or VIL	1	START, Device Select, RW = '1'
Random Address Read	0	VIH or VIL	1	START, Device Select, RW = '0', Address
	1	VIH or VIL	1	reSTART, Device Select, RW = '1'
Sequential Read	1	VIH or VIL	≥ 1	Similar to Current or Random Address Read
Byte Write	0	VIL	1	START, Device Select, RW = '0'
Page Write	0	VIL	≤ 16	START, Device Select, RW = '0'

Figure 13: SPD EEPROM Timing Diagram

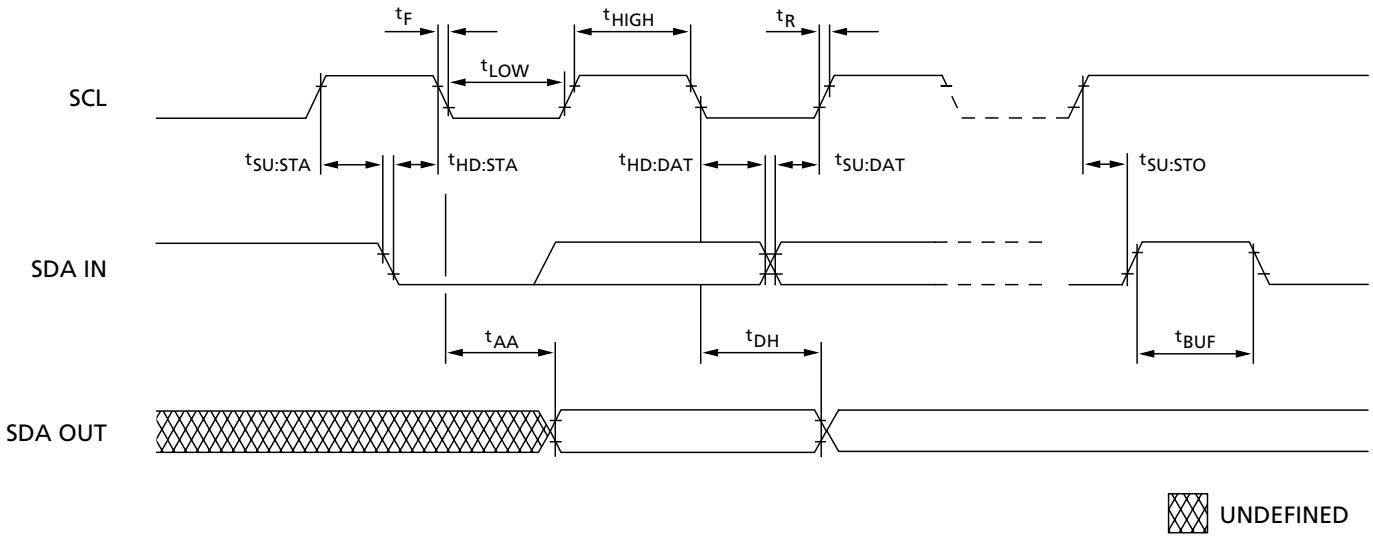


Table 19: Serial Presence-Detect EEPROM DC Operating Conditions

All voltages referenced to V_{SS}; V_{DDSPD} = +2.3V to +3.6V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE	V_{DDSPD}	2.3	3.6	V
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	$V_{DDSPD} \times 0.7$	V_{DDSPD} + 0.5	V
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	$V_{DDSPD} \times 0.3$	V
OUTPUT LOW VOLTAGE: I_{OUT} = 3mA	V_{OL}	–	0.4	V
INPUT LEAKAGE CURRENT: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA
OUTPUT LEAKAGE CURRENT: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA
STANDBY CURRENT: SCL = SDA = V_{DD} - 0.3V; All other inputs = V_{SS} or V_{DD}	I_{SB}	–	30	µA
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{CC}	–	2	mA

Table 20: Serial Presence-Detect EEPROM AC Operating Conditions

All voltages referenced to V_{SS}; V_{DDSPD} = +2.3V to +3.6V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	^{t}AA	0.3	3.5	µs	
Time the bus must be free before a new transition can start	^{t}BUF	4.7		µs	
Data-out hold time	^{t}DH	300		ns	
SDA and SCL fall time	^{t}F		300	ns	
Data-in hold time	$^{t}HD:DAT$	0		µs	
Start condition hold time	$^{t}HD:STA$	4		µs	
Clock HIGH period	$^{t}HIGH$	4		µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I		100	ns	
Clock LOW period	^{t}LOW	4.7		µs	
SDA and SCL rise time	^{t}R		1	µs	
SCL clock frequency	^{t}SCL		100	KHz	
Data-in setup time	$^{t}SU:DAT$	250		ns	
Start condition setup time	$^{t}SU:STA$	4.7		µs	
Stop condition setup time	$^{t}SU:STO$	4.7		µs	
WRITE cycle time	^{t}WRC		10	ms	1

NOTE:

1. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

Table 21: Serial Presence-Detect Matrix

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; notes appear following matrix

BYTE	DESCRIPTION	ENTRY (VERSION)	MT8VDDT1664H	MT8VDDT3264H
0	Number of SPD Bytes Used by Micron	128	80	80
1	Total Number of Bytes in SPD Device	256	08	08
2	Fundamental Memory Type	DDR SDRAM	07	07
3	Number of Row Addresses on Assembly	12,13	0C	0D
4	Number of Column Addresses on Assembly	10	0A	0A
5	Number of Physical Ranks on DIMM	1	01	01
6	Module Data Width	64	40	40
7	Module Data Width (Continued)	0	00	00
8	Module Voltage Interface Levels	SSTL 2.5V	04	04
9	SDRAM Cycle Time, (^{t}CK) CAS Latency = 2.5 (See note 1)	6ns(-335) 7ns (-262/-26A) 7.5ns (-265) 8ns (-202)	60 70 75 80	60 70 75 80
10	SDRAM Access From Clock (^{t}AC) CAS Latency = 2.5	0.7ns (-335) 0.75ns (-262/-26A/-265) 0.8ns (-202)	70 75 80	70 75 80
11	Module Configuration Type	None	00	00
12	Refresh Rate/Type	15.62µs, 7.8µs/SELF	80	82
13	SDRAM Device Width (Primary DDR SDRAM)	8	08	08
14	Error-checking DDR SDRAM Data Width	None	00	00
15	Minimum Clock Delay, Back-to-Back Random Column Access	1 clock	01	01
16	Burst Lengths Supported	2, 4, 8	0E	0E
17	Number of Banks on DDR SDRAM Device	4	04	04
18	CAS Latencies Supported	2, 2.5	0C	0C
19	CS Latency	0	01	01
20	WE Latency	1	02	02
21	SDRAM Module Attributes	Unbuffered/Diff. Clock	20	20
22	SDRAM Device Attributes: General	Fast/Concurrent AP	C0	C0
23	SDRAM Cycle Time, (^{t}CK) CAS Latency = 2	7.5ns (-335/-262/-26A) 10ns (-265/-202)	75 A0	75 A0
24	SDRAM Access from Clock (^{t}AC) CAS Latency = 2	0.7ns (-335) 0.75ns (-262/-26A/-265) 0.8ns (-202)	70 75 80	70 75 80
25	SDRAM Cycle Time, (^{t}CK) CAS Latency = 1.5	N/A	00	00
26	SDRAM Access from CK , (^{t}AC) CAS Latency = 1.5	N/A	00	00
27	Minimum Row Precharge Time, (^{t}RP)	18ns (-335) 15ns (-262) 20ns (-26A/-265/-202)	48 3C 50	48 3C 50
28	Minimum Row Active to Row Active, (^{t}RRD)	12ns (-335) 15ns (-262/-26A/-265/-202)	30 3C	30 3C
29	Minimum RAS# to CAS# Delay, (^{t}RCD)	18ns (-335) 15ns (-262) 20ns (-26A/-265/-202)	48 3C 50	48 3C 50

Table 21: Serial Presence-Detect Matrix (Continued)

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; notes appear following matrix

BYTE	DESCRIPTION	ENTRY (VERSION)	MT8VDDT1664H	MT8VDDT3264H
30	Minimum RAS# Pulse Width, (^{t}RAS), (See note 3)	42ns (-335) 45ns (-262/-26A/-265) 40ns (-202)	2A 2D 28	2A 2D 28
31	Module Rank Density	128MB, 256MB	20	40
32	Address and Command Setup Time, (^{t}IS), (See note 4)	0.8ns (-335) 1.0ns (-262/-26A/-265) 1.1ns (-202)	80 A0 B0	80 A0 B0
33	Address and Command Hold Time, (^{t}IH), (See note 4)	0.8ns (-335) 1.0ns (-262/-26A/-265) 1.1ns (-202)	80 A0 B0	80 A0 B0
34	Data/Data Mask Input Setup Time, (^{t}DS)	0.45ns (-335) 0.5ns (-262/-26A/-265) 0.6ns (-202)	45 50 60	45 50 60
35	Data/Data Mask Input Hold Time, (^{t}DH)	0.45ns (-335) 0.5ns (-262/-26A/-265) 0.6ns (-202)	45 50 60	45 50 60
36-40	Reserved		00	00
41	Min Active Auto Refresh Time (^{t}RC)	60ns (-335/-262) 65ns (-26A/-265) 70ns (-202)	3C 41 46	3C 41 46
42	Minimum Auto Refresh to Active/Auto Refresh Command Period, (^{t}RFC)	72ns (-335) 75ns (-262-26A/-265) 80ns (-202)	48 4B 50	48 4B 50
43	SDRAM Device Max Cycle Time (^{t}CKMAX)	12ns (-335) 13ns (-262-26A/265/202)	30 34	30 34
44	SDRAM Device Max DQS-DQ Skew Time (^{t}DQSQ)	0.45ns (-335) 0.5ns (-262/-26A/-265) 0.6ns (-202)	2D 32 3C	2D 32 3C
45	SDRAM Device Max Read Data Hold Skew Factor (^{t}QHS)	0.55ns (-335) 0.75ns (-262/-26A/-265) 1.0ns (-202)	55 75 A0	55 75 A0
46	Reserved		00	00
47	DIMM Height		01	01
48–61	Reserved		00	00
62	SPD Revision	Release 1.0	10	10
63	Checksum for Bytes 0-62	-335 -262 -26A -265 -202	04 D7 04 34 CF	27 BA E7 17 B2
64	Manufacturer's JEDEC ID Code	MICRON	2C	2C
65-71	Manufacturer's JEDEC IDCode	(Continued)	FF	FF
72	Manufacturing Location	01–12	01–0C	01–0C
73-90	Module Part Number (ASCII)		Variable Data	Variable Data
91	PCB Identification Code	1-9	01-09	01-09
92	Identification Code (Continued)	0	00	00
93	Year of Manufacture in BCD		Variable Data	Variable Data

Table 21: Serial Presence-Detect Matrix (Continued)

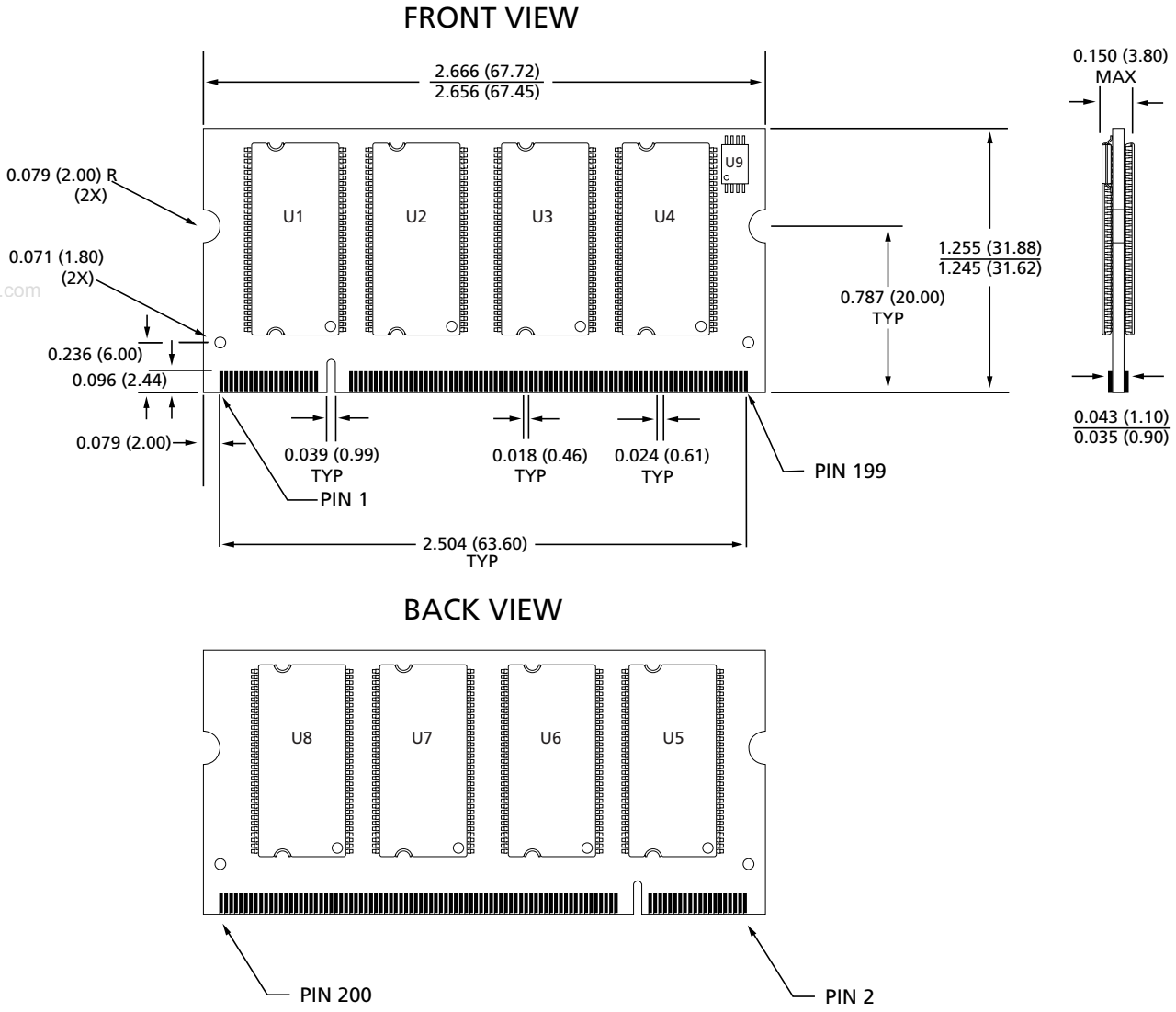
"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; notes appear following matrix

BYTE	DESCRIPTION	ENTRY (VERSION)	MT8VDDT1664H	MT8VDDT3264H
94	Week of Manufacturein BCD		Variable Data	Variable Data
95-98	Module Serial Number		Variable Data	Variable Data
99-127	Manufacturer-Specific Data (RSVD)		–	–

NOTE:

1. Value for -262 and -26A ^{t}CK set to 7ns (0x70) for optimum BIOS compatibility. Actual device spec. value is 7.5ns.
2. The value of ^{t}RAS used for -262/-26A/-265 modules is calculated from ^{t}RC - ^{t}RP. Actual device spec. value is 40 ns.
3. The JEDEC SPD specification allows fast or slow slew rate values for these bytes. The worst-case (slow slew rate) value is represented here. Systems requiring the fast slew rate setup and hold values are supported, provided the faster minimum slew rate is met.

Figure 14: 200-Pin DDR SODIMM Dimensions



NOTE:

All dimensions are in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

Data Sheet Designation

Released (No Mark): This data sheet contains minimum and maximum limits specified over the complete power supply and temrperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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