CMOS MT90810

Flexible MVIP Interface Circuit

Data Sheet

August 2005

Features

- MVIP™ and ST-BUS™ compliant
- MVIP Enhanced Switching with 384x384 channel capacity (256 MVIP channels; 128 local channels)
- On-chip PLL for MVIP master/slave operation
- Local output clocks of 2.048,4.096,8.192 MHz with programmable polarity
- Local serial interface is programmable to 2.048, 4.096 or 8.192 Mb/s with associated clock outputs
- Additional control output stream
- Per-channel message mode
- Two independently programmable groups of up to 12 framing signals each
- Motorola non-multiplexed or Intel multiplexed/non-multiplexed microprocessor interface

Applications

- Medium size digital switch matrices
- MVIP interface functions
- Serial bus control and monitoring

Ordering Information

MT90810AK3 100 Pin PQFP* Trays
*Pb Free Sn-Bi Plating

0°C to +70°C

- Centralized voice processing systems
- Voice/Data multiplexer

Description

Zarlink's MT90810 is a Flexible MVIP Interface Circuit (FMIC). The MVIP (Multi-Vendor Integration Protocol) compliant device provides a complete MVIP compliant interface between the MVIP Bus and a wide variety of processors, telephony interfaces and other circuits. A built-in digital time-slot switch provides MVIP enhanced switching between the full MVIP Bus and any combination of up to 128 full duplex local channels of 64 kbps each. An 8 bit microprocessor port allows real-time control of switching and programming of device configuration. On-board clock circuitry, including both analog and digital phase-locked loops, supports all MVIP clock modes. The local interface supports PCM rates of 2.048, 4.096 and 8.192 Mb/s, as well as parallel DMA through the microprocessor port.

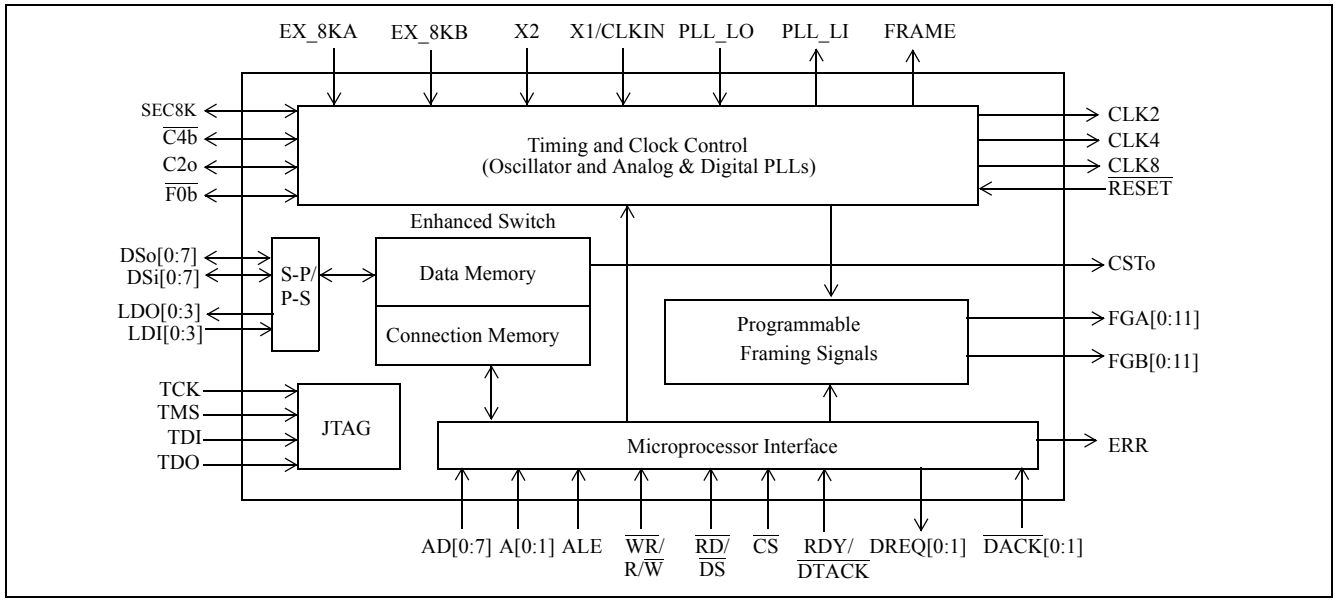

Figure 1 - Functional Block Diagram

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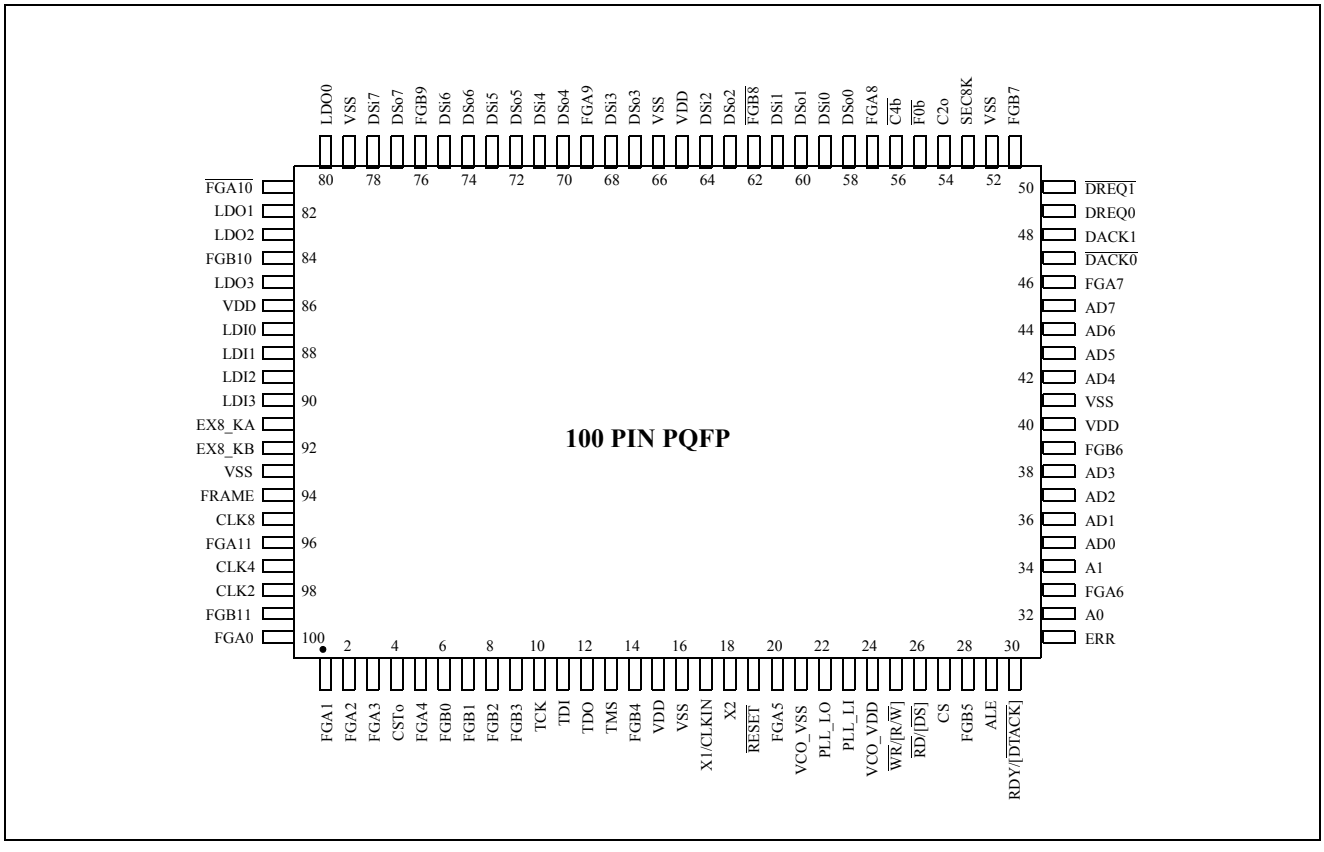


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
58, 60, 63, 67, 70, 72, 74, 77	DSo[0:7]	**MVIP DSo Streams (Bidirectional CMOS).** 2.048 Mb/s serial data streams conforming to ST-BUS serial data stream specifications.
59, 61, 64, 68, 71, 73, 75, 78	DSi[0:7]	**MVIP DSi Streams** (Bidirectional CMOS). 2.048 Mb/s serial data streams conforming to ST-BUS serial data stream specifications.
80, 82, 83, 85	LDO[0:3]	**Local Output Serial Streams (Output).** Serial data streams programmable to 2.048, 4.096 or 8.192 Mb/s data rates.
87, 88, 89, 90	LDI[0:3]	**Local Input Serial Streams (TTL Input).** Serial data streams programmable to 2.048, 4.096 or 8.192 Mb/s data rates.
4	CSTo	**Control ST-BUS Output (Output).** This is a 1.024 Mb/s output. The state of each bit in this stream is determined by the CSTo bit in connection memory high.
55	$\overline{\text{F0b}}$	**MVIP F0 signal (CMOS Input/Output).** ST-BUS 8 kHz framing signal
56	$\overline{\text{C4b}}$	**MVIP C4 signal (CMOS Input/Output).** ST-BUS 4.096 MHz clock
54	C2o	**MVIP C2 signal (Output).** ST-BUS 2.048 MHz clock. This pin is automatically set to high impedance when it is not driven.
53	SEC8K	**MVIP SEC8K signal (CMOS Input/Output).** A secondary 8 kHz signal used either as an input source to the on-chip digital PLL or as an output to the MVIP bus.
91	EX_8KA	External 8 kHz input A (TTL Input).
92	EX_8KB	External 8 kHz input B (TTL Input).
94	FRAME	**Local Frame Output Signal (Output).** This 8 kHz framing signal has a duty cycle and period equal to the MVIP $\overline{\text{F0}}$ signal.
95	CLK8	8 MHz Local Output Clock (Output). This is a 8 MHz clock.
97	CLK4	4 MHz Local Output Clock (Output). This 4 MHz clock has a duty cycle and period equal to the MVIP $\overline{\text{C4}}$ signal.
98	CLK2	2 MHz Local Output Clock (Output). This 2 MHz clock has a duty cycle and period equal to the MVIP $\overline{\text{C2}}$ signal.
100, 1, 2, 3, 5, 20, 33, 46, 57, 69, 81, 96	FGA[0:11]	**Frame Group A framing signals (Output).** Programmable framing signals. The frame group outputs are determined by mode bits in the frame register to be either programmed outputs, output drive enables for DSo, or output framing pulses for use with local serial data streams.
6, 7, 8, 9, 14, 28, 39, 51, 62, 76, 84, 99	FGB[0:11]	**Frame Group B framing signals (Output).** Programmable framing signals. The frame group outputs are determined by mode bits in the frame register to be either programmed outputs, output drive enables for DSi, or output framing pulses for use with local serial data streams.

Pin Description (continued)

Pin #	Name	Description
19	$\overline{\text{RESET}}$	**Chip Reset (Schmitt Input).** This active low reset clears all internal registers, except connection memory and data memory.
35, 36, 37, 38, 42, 43, 44, 45	AD[0:7]	**Microprocessor Address/Data Bus (Bidirectional TTL).** Microprocessor access to internal registers, connection and data memories. In non-multiplexed mode: data bus. In multiplexed mode: multiplexed address and data bus.
32, 34	A[0:1]	**Microprocessor Address (TTL Input).** In non-multiplexed mode: address to FMIC internal registers In multiplexed mode: unused (leave unconnected).
29	ALE	**Microprocessor Address Latch Enable (TTL Input).** Selects the microprocessor mode. In Intel multiplexed mode, the falling edge of this signal is used to sample the address.
27	$\overline{\text{CS}}$	**Microprocessor Bus Chip Select (TTL Input).** This active low input enables microprocessor access to connection and data memory and internal registers.
26	$\overline{\text{RD}}$/[$\overline{\text{DS}}$]	**Read/Data Strobe (TTL Input).** In Intel mode ($\overline{\text{RD}}$), this active low input configures the data bus lines as output. In Motorola mode ($\overline{\text{DS}}$), this active low input operates with $\overline{\text{CS}}$ to enable read and write operation.
25	$\overline{\text{WR}}$/[R/$\overline{\text{W}}$]	**Write\ Read/Write Strobe (TTL Input).** In Intel mode ($\overline{\text{WR}}$), this active low input configures the data bus lines as inputs. In Motorola mode (R/$\overline{\text{W}}$), this input controls the direction of the data bus D[0:7] during a microprocessor access.
30	RDY [$\overline{\text{DTACK}}$]	**Ready/Data Acknowledge (Open Drain Output).** In Intel mode (RDY), this output acts as IOCHRDY. A 10 K pull up is required. In Motorola mode ($\overline{\text{DTACK}}$), this active low output indicates a successful data bus transfer. A 10 K pull up is required.
31	ERR	**Error Status (Output).** This pin is asserted high if either a clock error (loss of $\overline{\text{C4b}}$ clock), DMA overrun condition or PLL unlock occurs.
49, 50	DREQ[0:1]	**DMA Request (Output).** When DMA operations on the device are enabled, this pin requests transfers for DMA reads/writes from/to the device.
47, 48	$\overline{\text{DACK}}$[0:1]	**DMA Acknowledge (TTL Input).** When DMA operations on the device are enabled, this pin receives acknowledgement for DMA reads/writes from/to the device.
10	TCK	**JTAG Input Clock (TTL Input).** Maximum recommended clock rate is 16 MHz. If not used, this pin should be left unconnected.
11	TDI	**JTAG Serial Input Data (TTL Input).** If not used, this pin should be left unconnected.

Pin Description (continued)

Pin #	Name	Description
12	TDO	**JTAG Serial Output Data (Output).** If not used, this pin should be left unconnected.
13	TMS	**JTAG Mode Control Input (TTL Input).** If not used, this pin should be left unconnected.
17	X1/CLKIN	**Clock Input Pin/ Crystal Oscillator Pin1.**
18	X2	**Crystal Oscillator Pin 2 (Input).** If X1 is clock input, this pin should be left unconnected.
22	PLL_LO	**PLL Loop Filter Output.** (Output 6 mA drive).
23	PLL_LI	**PLL Loop Filter Input.** (1 μA Low level/High level Input current).
21	VCO_VSS	Ground for On-chip VCO.
24	VCO_VDD	+5 Volt Power Supply for On-chip VCO.
15, 40, 65, 86	VDD[0:3]	+5 Volt Power Supply.
16, 41, 52, 66, 79, 93	VSS[0:5]	Ground.

Device Overview

Zarlink's MT90810 is a MVIP compliant device. It provides a complete, cost effective, MVIP compliant interface between the MVIP Bus and a wide variety of processors, telephony interfaces and other circuits. The FMIC supports 384 full duplex, time division multiplexed (TDM), channels. These channels are divided into 256 full duplex MVIP channels and 128 full duplex local channels. The sample rate for each channel is 8 kHz and the width of each channel is 8 bits for a total data rate of 64 kbits/s per channel.

The FMIC's internal clock circuitry includes both an analog and a digital PLL and supports all MVIP clock modes. The device can be configured as a timing master whereby an external 16.384 MHz crystal or 4.096, 8.192 or 16.384 MHz external clock source is used to generate MVIP clock signals. The device can also operate as a slave to the MVIP bus, synchronizing its master clock to the MVIP 4 MHz bus clock.

The device's local serial interface supports PCM rates of 2.048, 4.096 and 8.192 Mb/s, per channel message mode, an additional control stream, as well as parallel DMA through the microprocessor port. Furthermore, the FMIC's programmable group of output framing signals and local output clocks may be used to provide the appropriate frame and clock pulses to drive other local serial buses such as GCI.

A microprocessor interface permits reading and writing of the data memory, connection memory and all internal control registers. The Connection and Data memory can be read and updated while the MVIP bus is active, that is, connections can be made without interrupting bus activities.

Functional Description

Switching

The FMIC provides for switching of data from any input channel to any output channel. This is accomplished by buffering a single sample of each channel in an on-chip 384 byte static RAM. Samples are written into this data RAM in a fixed order and read out in an order determined by the programming of the connection memory. An input shift register and holding latch for each input stream make up the serial to parallel conversion blocks on the input of

the FMIC and an output holding register an shift register make up the parallel to serial conversion blocks on the output of the FMIC.

Data Memory

Data memory is a 384 byte static RAM block which provides one sample of buffering for each of the 384 channels. An input shift register and holding latch for each input stream make up the serial to parallel conversion blocks on the input. Each input channel is mapped to a unique location in the RAM, as shown Table 18 - “Data Memory Mapping”.

Data memory can be read and written by the microprocessor (See “Software Control” for further details). Note that writing to data memory may be futile since the contents will be overwritten by incoming data on the serial input streams.

Connection Memory

Connection memory is comprised of a static RAM block 384 locations by 12 bits. Each location in connection memory corresponds to one of the 384 output channels. The mapping of memory location to output channel is the same as the mapping of input channel to data memory location and is shown in Table 19 - “Connection Memory Mapping”.

The lower 8 bits of connection memory form connection memory low byte as shown in Figure 10 - “Connection Memory Low Byte”. The bits are defined in Table 20, “Connection Memory Low Bits”.

The upper 4 bits of connection memory form connection memory high (refer to Figure 11 - “Connection memory high byte”). Connection memory low byte, together with the least significant bit of connection memory high form an address to point to in data memory. The location pointed to in data memory provides the data for a given output channel. The remaining three bits in connection memory high are control bits. These bits perform slightly different functions for MVIP and local channels. The control bits in connection memory high for MVIP streams enable/disable output drivers, specify message or connection mode for individual output channels, and determine the direction of the DSi/DSo channel pair (see Table 21 - “Connection Memory High Bits for MVIP channels” for further details). The control bits in connection memory high for local streams enable/disable DMA transfer, specify message or connection mode for individual output channels, and control CSTo timing (see Table 22 - “Connection Memory High Bits for Local channels” for further details).

Connection memory can be read and written by the microprocessor (see “Software Control” for further details). When writing to connection memory, it is necessary to first write the low bits and then the high bits. The low bits are held in a temporary register until the high bits are written. The complete write of all 12 bits (to connection memory) is only performed when the high bits are being written.

Connection and Message Modes

In connection mode, the connection memory low byte and the least significant bit of connection memory high form a 9 bit address to point to in data memory. The location pointed to specifies which source/input channel to connect to the respective output channel and stream. The same source channel can be routed to various output channels, thus providing broadcast facility within the switch.

In message mode, the connection memory low byte is sent directly out the corresponding output channel and stream. The least significant bit of connection memory high is not used.

Direction Control Bit

The direction control (DC) bit in connection memory high determines the direction of the associated DSi-DSo channel pair. If the DSi or DSo channel is programmed as an input, the corresponding DSo or DSi channel will automatically be configured as an output. Thus, there are always 256 MVIP input and 256 MVIP output channels or 256 full duplex MVIP channels on the MVIP bus. Figure 3 - “Per channel direction control” illustrates the use of DC

bit for direction control on stream 0 channel 1 and channel 29. When DC bit is set, DSo channel is output from the FMIC and DSi is input to the FMIC. When DC bit is cleared, the channel directions are reversed.

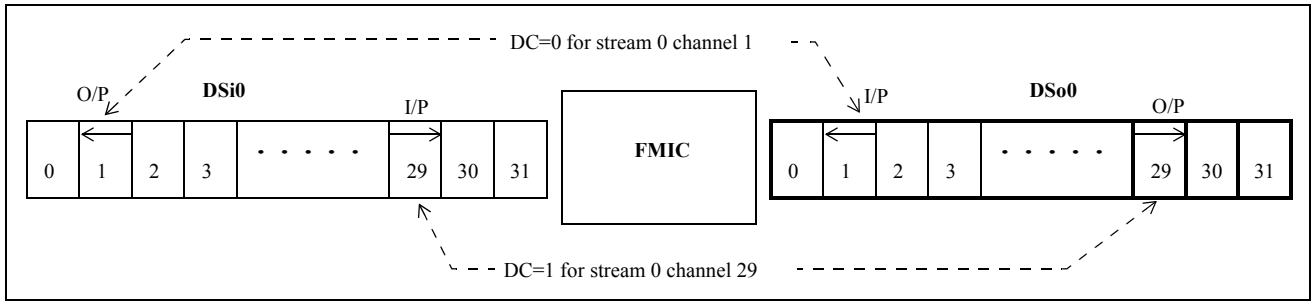


Figure 3 - Per-channel Direction Control

Timing and Clock Control

The FMIC clock control circuitry contains an on-chip analog PLL (with external loop filter) which is designed to phase lock to a 4.096 MHz clock. The on-chip VCO runs at eight times this rate yielding a 32 MHz clock which is divided by two. The resulting 16.384 MHz is used as the internal master clock of the FMIC.

The input to the analog PLL can be selected from among several different sources including, the MVIP C4 clock which is used as the internal master clock of the FMIC.

The on-chip digital PLL generates a 4.096 MHz clock which is phase locked to an externally generated 8 kHz clock. The digital PLL state machine is clocked at 16.384 MHz. The digital PLL maintains lock by occasionally dropping or repeating a 16.384 MHz clock period on the generated 4.096 MHz clock. Consequently, the 4.096 MHz clock has jitter equal to about 60 ns. If the output of the digital PLL is chosen as the input to the analog PLL, a slow loop filter with a time constant greater than several 8 kHz frames will smooth out the jitter.

The clock oscillator pins X1 and X2 can be used with an external 16.384 MHz crystal or pin X1 can be used directly as a clock input with X2 left unconnected. When X1 is used as a clock input, the frequency of the clock can be selected to be either 16.384 MHz or 8.192 MHz or 4.096 MHz by changing the XCLK_SEL bits in the CLK_CNTL register.

The overall FMIC state machine from which all timing is derived, is clocked by the 16.384 MHz output of the analog PLL, the device's master clock. The state machine controls all timing in the FMIC and has a period equal to one MVIP frame (8 kHz). This state machine can either free run or synchronize to an 8 kHz source such as the MVIP F0 signal or an external 8 kHz reference.

Refer to Figure 4 - "Clock Control Functional Block Diagram" for further details.

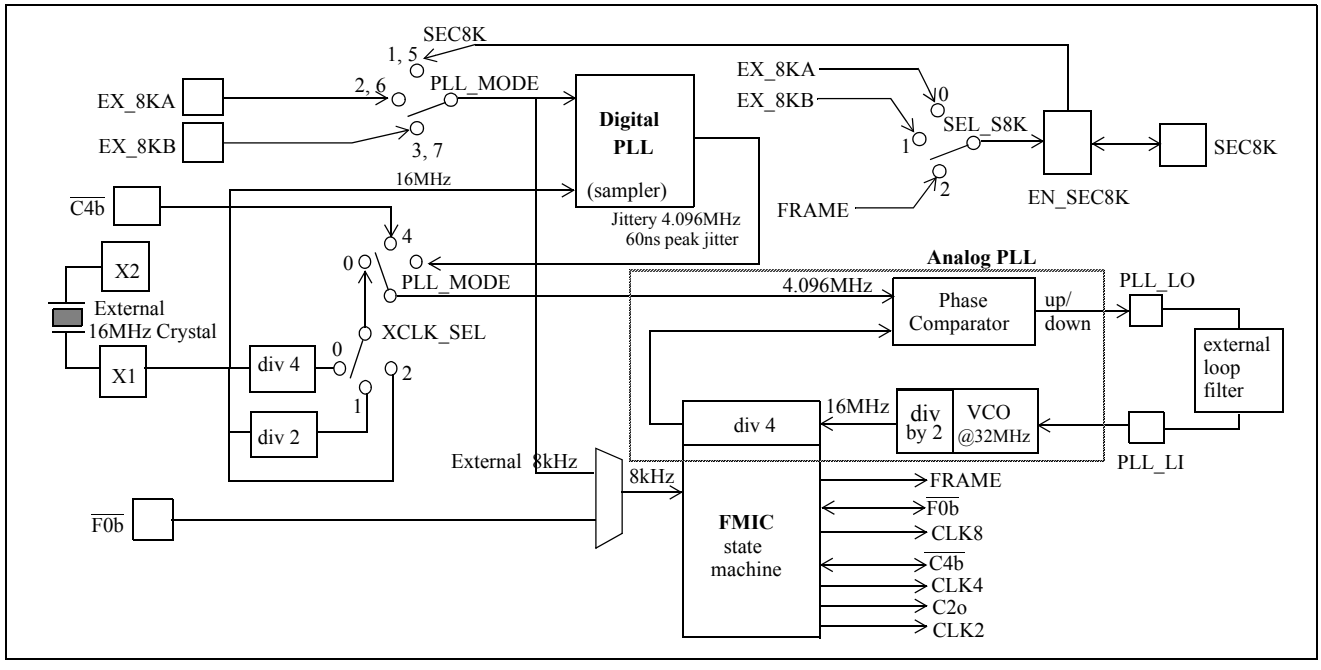


Figure 4 - Clock Control Functional Block Diagram

The operation of the PLLs and the state machine is controlled by the clock control register as described in Figure 6 - “Clock Control (CLK_CNTRL) Register” and Tables 8 to 10. The clock circuitry (PLLs and state machine) operates in eight different modes.

1. FMIC as Timing Master (Mode 0)

The FMIC is configured as the timing master (CLK_CNTRL register cleared, PLL mode 0 selected) after reset. The external 16.384 MHz input is divided by four and used as the input to the analog PLL so the internal master clock is phase locked to the 16.384 MHz oscillator. The FMIC state machine is free-running and does not synchronize to any external 8 kHz source.

In this mode, the XLCK_SEL bits of the clock control register can be programmed to accommodate an 8.192 MHz or 4.096 MHz external clock instead of the default 16.384 MHz.

The FMIC becomes MVIP master when MVIP_MST bit is set in the Control/Status register. This mode can be used when the FMIC chip is to become timing master in a system which has no digital network connections (T1 or E1).

2. FMIC as MVIP Slave (Mode 4)

When this mode is selected, MVIP $\overline{C4}$ clock is selected as the input to the analog PLL. The FMIC internal master clock is then synchronized to the MVIP bus timing. The FMIC state machine is also synchronized to the MVIP $\overline{F0}$ framing signal.

The MVIP_MST bit in the Control/Status register should never be set when the device is in mode 4 as the FMIC is entirely slave to the MVIP bus timing.

3. FMIC as MVIP Master (Mode 1,2,3)

In modes 1 through 3, the output of the device’s digital PLL is selected as the input to the analog PLL. The source to the digital PLL is selected as either SEC8K, EX_8KA or EX_8KB depending on the particular mode (1, 2 or 3) chosen.

In these modes, the FMIC state machine is not synchronized to the external 8 kHz input selected, that is, the state machine output 8 kHz FRAME and $\overline{F0b}$ signals may not be phase aligned with the external 8 kHz input but will always be frequency locked.

In modes 1, 2 and 3, the external clock X1 must be 16.384MHz. This is required for proper operation of the digital PLL.

The FMIC becomes MVIP master when MVIP_MST bit is set in the Control/Status register.

4. FMIC as MVIP Master (Mode 5,6,7)

In modes 5 through 7, the output of the device's digital PLL is selected as the input to the analog PLL. The source to the digital PLL is selected as either SEC8K, EX_8KA or EX_8KB depending on the particular mode (5, 6 or 7) chosen.

In these modes, the FMIC state machine is synchronized to the external 8kHz input selected, that is, the state machine output 8 kHz FRAME and $\overline{F0b}$ signals are phase aligned with the external 8kHz input as well as frequency locked. Here lies the difference between these modes (5, 6 and 7) and the above mentioned modes (1, 2 and 3). In these modes, the external 8 kHz input signal is used to synchronize the FMIC state machine.

In modes 5, 6 and 7, the external clock X1 must be 16.384 MHz. This is required for proper operation of the digital PLL.

The FMIC becomes MVIP master when MVIP_MST bit is set in the Control/Status register.

5. PLL Jitter Performance

To measure the intrinsic jitter of the analog PLL, the FMIC is set to slave mode, slave to a clean MVIP $\overline{C4}$ clock (no jitter). A resulting jitter of 0.004UI p-p is measured on the C2o clock.

The jitter transfer function of the analog PLL, which is the ratio of the output jitter to the input jitter, is shown in "Figure 5 - Jitter Transfer Function of the Analog PLL". The measurements are made with a controlled sinusoidal jitter modulating the MVIP $\overline{C4}$ clock.

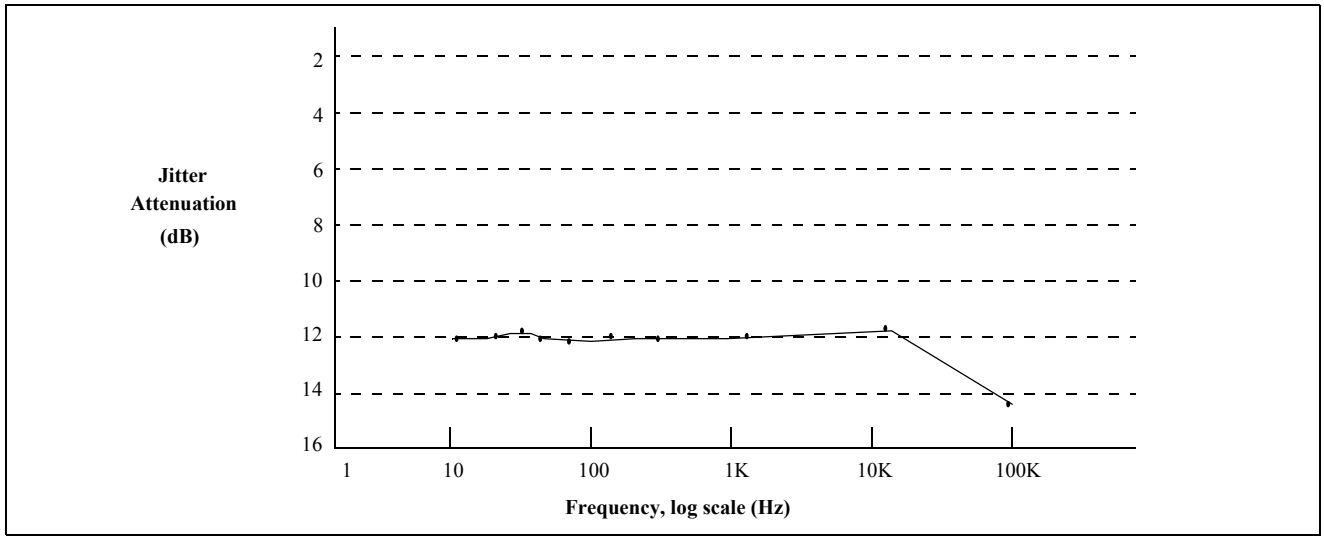


Figure 5 - Jitter Transfer Function of the Analog PLL

To measure the intrinsic jitter of the two PLLs combined, the FMIC is set to master mode, slave to a clean external 8 kHz clock SEC8K (no jitter). A resulting jitter of 0.206UI p-p is measured on the C2o clock.

Jitter transfer function of the digital PLL and analog PLL combination is determined primarily by the digital PLL. The digital PLL is essentially a digital sampler which samples on the nearest rising or falling edge of its 16 MHz clock and therefore has a 60 ns jitter on the output.

Please note that the digital PLL and analog PLL combination may not meet some international standards for jitter performance. In cases where strict idle jitter specifications must be met, an external custom PLL may be required and the internal analog PLL should be disabled (refer to PLL Diagnostic section for further details).

6. Local Output Clock Control

The FMIC provides four output clocks which are always driven off of the device. The FRAME output clock has a duty cycle and period equal to the MVIP F0 signal. The CLK2 and CLK4 output clocks are identical to the MVIP C2 and C4 clocks, respectively. The CLK8 output provides a 8.192 MHz clock. The frame pulse and output clocks may be used to provide framing and clocking signals to serial interfaces other than ST-BUS, such as, GCI bus. Timing diagrams and parameters are provided in Figures 19 and 20 along with the associated table.

The local output clock control register is defined in Table 11 - “Local Clock Control (LOC_CLK) Register”. The register allows the user to program the polarity of the four local output clocks. In addition, the register contains four read-only bits which indicate the logic levels on EX_8KA, EX_8KB, DACK0 and DACK1 input pins of the device.

7. Local Serial Interface

The local serial interface is implemented on 4 input pins LDI[0:3] and four output pins LDO[0:3]. It can be programmed in one of four different configurations by setting the appropriate bits in the SER_MODE register (refer to Figure 7 - “Serial Mode (SER_MODE) Register”).

In serial configuration one, the data rate is set to 2 Mb/s. Each input stream is associated with a serial input pin and each serial output stream is associated with a serial output pin. There are 32 channels per pin.

In serial configuration two, the data rate is set to 4 Mb/s. Local streams 0 and 1 are multiplexed onto input and output pins LDI[0] and LDO[0] and streams 2 and 3 are multiplexed onto input and output pins LDI[2] and LDO[2]. There are 64 channels per pin and the streams are multiplexed onto the pins as shown in Table 12 - “SER_CNFG bits (control configuration of local serial streams)”.

In serial configuration three, the data rate is set to 8 Mb/s. All four local streams are multiplexed onto pins LDI[0] and LDO[0]. There are 128 channels per pin and the streams are multiplexed onto the pins as shown in Table 12 - “SER_CNFG bits (control configuration of local serial streams)”.

In serial configuration four, the data rate is set to 2 Mb/s for streams 0 and 1 and 4 Mb/s for streams 2 and 3. Streams 0 and 1 are associated with serial pins LDI/O[0] and LDI/O[1], respectively. Streams 2 and 3 are multiplexed onto pin LDI[2] and LDO[2]. The streams are multiplexed onto the pins as shown in Table 12 - “SER_CNFG bits (control configuration of local serial streams)”.

8. Programmable Framing Signals

The FMIC provides two groups of independently programmable output framing signals:

FGA[0:11] group A output framing signals are programmed by frame start register A (FRMA_STRT) and frame mode register A (FRMA_MODE). FGB[0:11] group B output framing signals are programmed by frame start register B (FRMB_STRT) and frame mode register B (FRMB_MODE).

The framing signals may be used to drive serial buses interfaces other than ST-BUS.

The functional characteristics of a group of framing output signals is controlled by MODE bits in the frame mode register. Table 13 - “Frame Group Mode bits” defines the various modes.

In mode 0, the frame group output depends on the status of bits in the frame start and frame mode registers. The values of the bits in frame start register x (x is either A for group A or B for group B) are driven out on pins FGx[0:7] and the values of bits 0 to 3 in frame mode register x are driven out on pins FGx[8:11]. This mode is selected after device reset when all bits in both registers are cleared.

In mode 1, the first four outputs of the frame group FGx[0:3] are available for programmed output as in mode 0. The other 8 outputs of each frame group are available as output drive enables for the MVIP DSI/DSO channels within the streams. FGA4 to FGA11 outputs correspond to output drive enables for the MVIP DSo channels within streams

0 to 7, respectively. For example, if only two DSo channels, 0 and 2 on stream 0, are enabled then the corresponding channels 0 and 2 on FGA4 will be pulled low and the remaining channels will be left high. Similarly, FGB4 to FGB11 outputs correspond to output drive enables for the MVIP DSi channels within streams 0 to 7, respectively.

In mode 2, frame groups A&B are programmed as output framing pulses for use with the local serial data streams (refer to Figure 16 - “Frame Pulse Timing for Mode 2” for further details). The position of the first framing signal in a group is determined by an 11 bit quantity. The quantity is the FMIC state number (the number of 16 MHz clock cycles during one frame) minus one. The lower eight bits of this quantity are located in the frame start register, and the upper three bits are located in the frame mode register.The width of the framing signal is determined by the state of the FRM_TYPE bit in the frame mode register and can be either a single bit cell time or 8 bit cell times. All framing signals in the same group (A or B) follow each other sequentially, that is, the first FGx[0] is asserted then exactly 8 bit cell times later FGx[1] is asserted and so on until the last framing signal in the group is asserted. The distance between consecutive frame pulses within a frame group can be one 2, 4 or 8 Mb/s channel time and can be specified by two bits in the frame mode register.

Mode 3 is identical to mode 2 except the polarity of the framing pulses is logically inverted.

Refer to Tables 13 to 16 for details on the frame start and frame mode registers.

All the framing signals FGA[0:11] and FGB[0:11] are available in the 100 pin PQFP package.

Delay through the MT90810

Switching delay through the FMIC is dependent on input and output stream, source and destination channel, as well as, I/O data rate. A summary of throughput delay values for the device is provided in Table 1, “Throughput Delay Values”. The minimum delay achievable in the MT90810 depends on the data rate selected for the streams. When switching from a slower input data rate to a faster output data rate, the minimum delay is set by the faster output data rate and the maximum delay is set by the slower input data rate. When switching from a faster input data rate to a slower output data rate, the minimum delay is set by the slower output data rate and the maximum delay is set by the faster input data rate.

Input - Output Rate	Throughput Delay	
	min	max
2.048 - 2.048 Mb/s	2 x 2 Mb/s t.s.	1 fr. + 2 x 2 Mb/s t.s.
4.096 - 4.096 Mb/s	3 x 4 Mb/s t.s.	1 fr. + 5 x 4 Mb/s t.s.
8.192 - 8.192 Mb/s	5 x 8 Mb/s t.s.	1 fr. + 11 x 8 Mb/s t.s.
2.048 - 4.096 Mb/s	3 x 4 Mb/s t.s.	1 fr. + 2 x 2 Mb/s t.s.
2.048 - 8.192 Mb/s	5 x 8 Mb/s t.s.	1 fr. + 2 x 2 Mb/s t.s.
4.096 - 2.048 Mb/s	2 x 2 Mb/s t.s.	1 fr. + 5 x 4 Mb/s t.s.
8.192 - 2.048 Mb/s	2 x 2 Mb/s t.s.	1 fr. + 11 x 8 Mb/s t.s.

Table 1 - Throughput Delay Values

t.s.=timeslot is used synonymously with channel
fr.=125 μs frame
2 Mb/s t.s.=3.9 μs
4 Mb/s t.s.=1.95 μs
8 Mb/s t.s.=0.975 μs

Initialization of the MT90810

The $\overline{\text{RESET}}$ pin should be hold low during initialization and power-up to ensure that all internal registers and connection and data memories are cleared.

Microprocessor Interface

The FMIC is configured and controlled via a microprocessor interface. The microprocessor interface consists of the combined address/data bus AD[0:7], address bits A[0:1], the chip select bit $\overline{\text{CS}}$, the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals, the address latch enable (ALE) signal and the RDY signal. If ALE is tied to VSS, the interface acts as an Intel non multiplexed interface with the AD[0:7] bus carrying only data and pins A[0:1] serving as the address lines. If ALE is tied to VCC the interface acts as a Motorola non multiplexed interface using A[0:1] as address lines with $\overline{\text{RD}}$ becoming $\overline{\text{DS}}$ and $\overline{\text{WR}}$ becoming R/$\overline{\text{W}}$. If ALE is active (switching during accesses), the interface acts as in Intel multiplexed interface with the AD[0:7] bus carrying both address and data and the A[0:1] pins unused. The RDY signal acts as IOCHRDY in Intel mode and as $\overline{\text{DTACK}}$ in Motorola mode.

In all modes the FMIC decodes four read/write registers in the microprocessor's address space according to Table 2, "FMIC I/O Addresses".

Address A[1:0]	Register
0 [00]	MCS - Master Control/Status Register
1 [01]	LAR - Low Address Register
2 [10]	AMR - Address Mode Register
3 [11]	IDR - Indirect Data Register

Table 2 - FMIC I/O Addresses

The microprocessor interface provides read and write access to all the registers. When the microprocessor performs a read or write to the registers, the microprocessor cycle is a fast cycle (In Intel mode, the RDY bit is not pulled low, and in Motorola mode, $\overline{\text{DTACK}}$ is asserted immediately). When the microprocessor performs a read or write to data memory or connection memory, the microprocessor cycle is a slow cycle (In Intel mode, the RDY is pulled low until the cycle is complete, in Motorola mode $\overline{\text{DTACK}}$ is not asserted until the cycle is complete).

Software Control

The FMIC control registers as well as the connection memory and data memory are accessible through indirect addressing.

To perform a write operation to an indirect location, the Low Address Register (LAR) and Address Mode Register (AMR) registers must first be initialized. The lower 8 bits of the indirect address are written to the LAR, and then the upper bit of the indirect address along with the appropriate bit settings to select the memory and auto increment/decrement mode is written to the AMR. Finally, the write operation is performed when data is written to the Indirect Data Register(IDR). Similarly, to perform a read operation from an indirect location, the LAR and AMR must be initialized and then the data can be read from the IDR.

Data memory can be read and written by the microprocessor. This is accomplished by first initializing the LAR and AMR register to select data memory and then either reading from or writing to the Indirect Data Register.

Connection memory can be read and written by the microprocessor. This is accomplished by first initializing the LAR and AMR register to select high or low connection memory and then either reading from or writing to the IDR.

The indirect address can be programmed to auto-increment after reads or writes to the indirect data register by setting bits 6 and 7 in the AMR accordingly. The auto-increment occurs only when the indirect address register points to either data memory or the high byte of connection memory.

If auto-increment on read/write is enabled, and connection memory is selected, then consecutive reads/writes to the IDR will toggle between selection of low to high then back to low byte of connection memory and continue on toggling until the reads/writes to IDR stop. Note that when reading/writing connection memory with auto increment disabled, the reads/writes to IDR will toggle from low to high byte connection memory once only.

Using the auto-increment feature, the connection memory can be quickly initialized by resetting the LAR and initializing the AMR for auto-increment on write with connection memory low byte selected. Writing a stream of bytes to IDR will then fill connection memory. The first byte written to the IDR will go to the low byte of the first connection memory location. The memory space selection will be automatically toggled to select connection memory high. The second byte written to the IDR will then be written to connection memory high of the first connection memory location. The memory space will automatically toggle back to the low byte connection memory and the address pointer will be incremented to prepare for writing to the next location in connection memory. Similarly, the contents of connection memory can also be read back quickly by setting the auto-increment on read bit of AMR and reading from the IDR continuously.

Writing to a data memory of connection memory when the address register contains an indirect RAM address of greater than 383 will cause unpredictable results.

DMA Interface

The DMA interface to the FMIC is accessible only when the microprocessor interface is in INTEL mode. All 128 local channels can be DMA'ed out to/in from external memory. MVIP channels can be DMA'ed by switching to local channels.

The DMA_EN bit in the FMIC Control/Status register enables DMA mode. This bit should be set only after the desired local channels have been enabled for DMA. The DMA_EN bit does not take effect until after the beginning of the next MVIP frame. This assures that when the DMA transactions begin, that they begin on a frame boundary.

An individual local channel is enabled for DMA by setting the CE bit in connection memory high for that channel. When a channel is enabled for DMA, both input and output are enabled for DMA. The local output data is also driven out on the programmed serial output stream. It is not possible to enable input without output or vice versa. If channels in time slot 0 are enabled for DMA, there will be no DMA requests for those channels in the first frame after DMA is enabled. Instead, setup and preparation for the DMA will occur in that first frame, in the timeslot preceding. DMA transfer will actually occur in the second frame after DMA is enabled. It is, therefore, recommended that channels in time slot 0 not be enabled for DMA.

The DMA signals DREQ[1] and $\overline{\text{DACK}}$[1] control transfers for DMA reads from the FMIC while DREQ[0] and $\overline{\text{DACK}}$[0] control transfers for DMA writes to the FMIC. For every 2 Mb/s timeslot where a channel is enabled for DMA, the FMIC will assert DREQ and wait for a $\overline{\text{DACK}}$ from an external controller. Upon receiving the acknowledgement, $\overline{\text{DACK}}$, it would proceed with one DMA burst transfer.

DMA read requests always occur at the beginning of the 2 Mb/s time slot during which, all channels enabled for DMA in the timeslot will be DMA'ed out in a burst, onto the local serial data stream. One burst implies one DREQ cycle, whereby DREQ is held low for the duration of the transfer. The maximum number of 8 bit channels that can be DMA'ed out during one burst is 4, since, regardless of the serial interface mode, there can be only four 8 bit channels per 2 Mb/s time slot, whether it be one channel per stream (on 4 streams) at 2 Mb/s, 2 channels per stream (on 2 streams) at 4 Mb/s or 4 channels all on one stream at 8 Mb/s.

DMA write requests occur at the end of the 2 Mb/s time slot during which, all channels enabled for DMA in the timeslot will be DMA'ed from the local serial data stream. DMA write requests can also occur in bursts of up to four 8 bit channels. The data for write requests is actually staggered by one DMA request for each stream. This means that the data written into the device due to a DMA write request of a given channel, is not actually written to that channel but to the next channel enabled for DMA on the same stream.

If a DMA read or write request is not completely served by the time the next request needs to be asserted, a DMA overrun error occurs. This causes the corresponding overrun bit in the MCS register, as well as, the ERR bit to be set. DMA access can be throttled by disabling DMA for several timeslots in between channels that have DMA enabled.

Bit	Name	Description (This register is cleared upon reset)
7	PLL_UNLCK	The bit will be asserted if the on-chip PLL goes out of lock. The ERR pin of the FMIC will also be asserted high. The PLL_UNLCK bit will remain asserted until a zero is written to it.
6	DMAW_OV	When asserted, the bits indicate that a DMA overrun condition occurred on the DMA Read/Write channel, respectively. The ERR pin of the FMIC will also be asserted. The DMAR/W_OV bits will remain asserted until zeros are written to them.
5	DMAR_OV	
4	CLK_ERR	The bit monitors activity on the $\overline{C4b}$ pin of the MVIP bus and is asserted if there has been no activity on the $\overline{C4b}$ pin for 4 ms. The ERR pin of the FMIC will also be asserted high. The CLK_ERR bit will remain asserted until a zero is written to it
3	MVIP_MST	When set, enables the FMIC to drive the MVIP clock signals and consequently to become master of the MVIP bus. When cleared, FMIC becomes slave of MVIP bus.
2	DMA_EN	The bit should be set to enable DMA operations only after the DMA control registers have been initialized
1	FMIC_EN	When cleared, all MVIP signals are high impedance and LD0&2 are set to logic 1, LD1&3 are set to logic 0. The bit should be set to enable the FMIC to drive data onto the streams only after the chip has been initialized
0	RESET	When set, clears all registers in the FMIC control space but does NOT clear connection and data memory. The bit must be cleared for normal operation

Table 3 - Master Control/Status Register [00]

Bit	Bit Function
7:0	Bits 0 to 7 of the Indirect Address

Table 4 - Low Address Register [01]

LL Diagnostic

Diagnostic for the PLL is available via a diagnostic register. The register contains bits which should never be set under normal operating conditions. Two bits in the register SEL_XIN or VCO_BYP may be set if the user wishes to bypass the internal analog PLL or VCO, respectively. The bits are defined in Table 17 - “Diagnostic (DIAG_REG) Register”.

Bits	Bit Function
7:6	Auto increment/decrement mode [00] Normal Mode - indirect address not auto incremented [01] Auto increment indirect address after indirect read of IDR [10] Auto increment indirect address after indirect write of IDR [11] Auto increment indirect address after indirect read or write of IDR
5:4	Selects the memory space: [00] FMIC Control Registers [01] Data Memory [10] Connection Memory Low Byte [11] Connection Memory High Byte
3:1	Reserved
0	Bit 8 of the Indirect Address

Table 5 - Address Mode Register [10]

Bits	Bit Function
7:0	All bits are written into the indirect address location specified by the LAR and AMR registers. If auto increment on write/read is enabled, and connection memory is selected, then consecutive writes/reads to/from the IDR will toggle between selection of high byte and low byte connection memory.

Table 6 - Indirect Data Register [1]

Indirect Address	Name	Function
0	CLK_CNTRL	Clock Control Register
1	LOC_CLK	Local Output Clock Control
2	SER_MODE	Local Serial Configuration Register
3		RESERVED
4	FRMA_STRT	Frame Group A start register
5	FRMA_MODE	Frame Group A mode register
6	FRMB_STRT	Frame Group B start register
7	FRMB_MODE	Frame Group B mode register
8:11		RESERVED
12	DIAG_REG	Chip diagnostic bits
13:511	RESERVED	

Table 7 - FMIC Control Register (read/write)

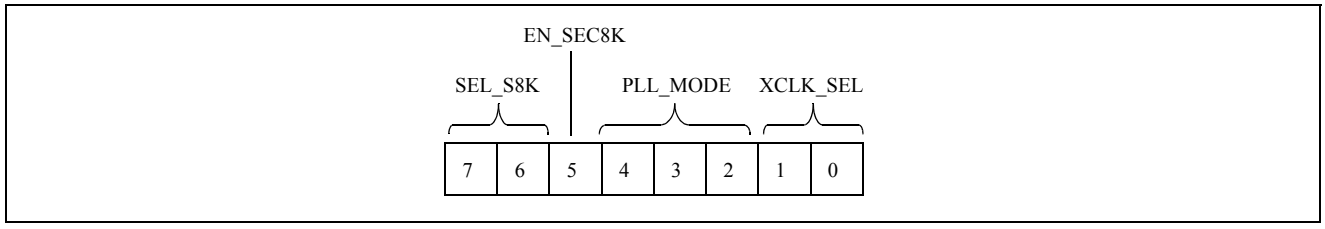


Figure 6 - Clock Control (CLK_CNTRL) Register

Name	Description	
	Mode [bits]	Function
SEL_S8K	Selects source of 8kHz signal driven out on SEC8K pin	
	0 [00]	Select EX_8KA as SEC8K output
	1 [01]	Select EX_8KB as SEC8K output
	2 [10]	Select FRAME as SEC8K output
	3 [11]	RESERVED
EN_SEC8K	Enables SEC8K as output	

Table 8 - EN_SEC8K and SEL_S8K Bits

Mode [bits]	Description		
	APLL source	Frame Sync.	Function
0 [000]	X1 divided by 1,2, or 4	no frame sync.	**FMIC as Timing Master** • FMIC defaults to this mode after reset (Clock Control Register is cleared). • X1 divided by 1,2 or 4 is used as the input to the APLL. • State machine is free running and does not synchronize to any external 8 kHz source. • XCLK_SEL can be programmed to any mode. • MVIP_MST bit in MCS is set. • Used when the FMIC is to become the timing master in a system which has no digital network connections (T1 or E1).
1 [001]	SEC8K >DPLL	no frame sync.	**FMIC as MVIP Master** (Slaved to external 8 kHz) • DPLL is selected as the source to the APLL. Input to the DPLL is either SEC8K,EX8KA/EX8KB. • State machine is not synchronized to external 8 kHz (SEC8K/EX8KA/B); that is, FRAME signal is freq locked but not necessarily phase aligned with external 8 kHz. • XCLK_SEL must be programmed to mode 0. • MVIP_MST bit in MCS is set.
2 [010]	EX8KA >DPLL		
3 [011]	EX8KB >DPLL		
4 [100]	MVIP $\overline{C4}$	frame sync. to $\overline{F0}$	**FMIC as MVIP Slave** • FMIC is entirely slaved to MVIP bus timing. • MVIP $\overline{C4}$ is selected as input to APLL. • State machine is synchronized to MVIP $\overline{C4}$ and $\overline{F0}$ inputs. • MVIP_MST bit in MCS register must be cleared.

Table 9 - PLL_MODE Bits (control PLL and frame synchronization)

Mode [bits]	Description		
	APLL source	Frame Sync.	Function
5 [101]	SEC8K >DPLL	frame sync. to SEC8K	**FMIC as MVIP Master** (Slaved to external 8 kHz) • DPLL is selected as the source to the APLL. Input to the DPLL is either SEC8K,EX8KA/EX8KB. • State machine is synchronized to external 8 kHz (SEC8K/EX8KA/B); that is, FRAME signal is freq locked and phase aligned with external 8 kHz. • XCLK_SEL must be programmed to mode 0. • MVIP_MST bit in MCS must be set.
6 [110]	EX8KA >DPLL	frame sync. to EX8KA	
7 [111]	EX8KB >DPLL	frame sync. to EX_8KB	

Table 9 - PLL_MODE Bits (control PLL and frame synchronization)

Mode [bits]	Description	
	X1 =	Comments
0 [00]	16.384MHz	X1 must be 16.384 MHz when PLL is in modes 1-3 or 5-7
1 [01]	8.192MHz	
2 [10]	4.096MHz	
3 [11]	RESERVED	

Table 10 - XCLK_SEL bits (control divide ratio of X1 clock)

Bit	Name	Bit Function
7	$\overline{\text{DACK1}}$	Read-only, reads logic value on $\overline{\text{DACK1}}$ pin
6	$\overline{\text{DACK0}}$	Read-only, reads logic value on $\overline{\text{DACK0}}$ pin
5	EX8KB	Read-only, reads logic value on EX8KB pin
4	EX8KA	Read-only, reads logic value on EX8KA pin
3	INV_CLK8	When set, inverts 8.192 MHz CLK8 output pin
2	INV_CLK4	When set, inverts 4.096 MHz CLK4 output pin
1	INV_CLK2	When set, inverts 2.048 MHz CLK2 output pin
0	INV_FRM	When set, inverts FRAME output signal

Table 11 - Local Clock Control (LOC_CLK) Register

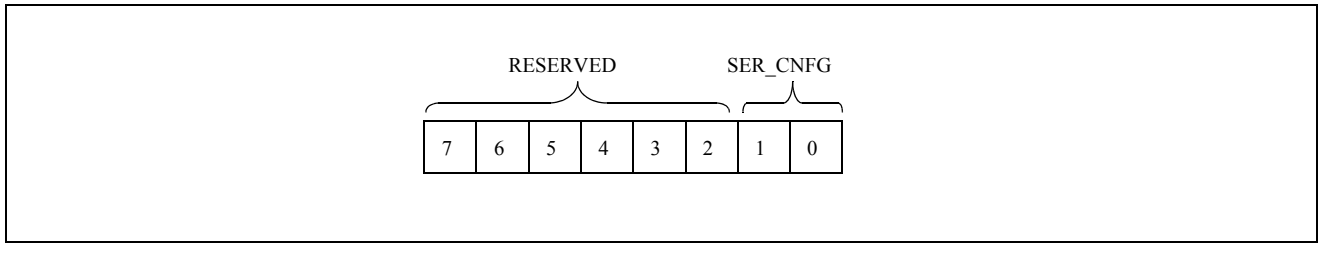


Figure 7 - Serial Mode (SER_MODE) Register

<table>
<tr><th>Mode [bits]</th><th>Description</th><th colspan="3">Multiplexing of streams onto pins LDI/O[str] where str=stream (0-3)</th></tr>
<tr><td>0 [00]</td><td>2 MHz streams
All local streams are configured to run at 2 MHz.
Each channel occupies a 2 Mb/s timeslot of 3.9 ms.</td><td colspan="3">2MHz, 32 channels
LDI/O[0] = local stream 0
LDI/O[1] = local stream 1
LDI/O[2] = local stream 2
LDI/O[3] = local stream 3</td></tr>
<tr><td rowspan="8">1 [01]</td><td rowspan="8">4 MHz streams
local streams 0&1 are multiplexed onto pin LDI/O[0]
local streams 2&3 are multiplexed onto pin LDI/O[2]
Each channel occupies a 4 Mb/s timeslot of 1.95 ms.</td><td></td><td>LDI/O[0]
(4 MHz, 64 channels)</td><td>LDI/O[2]
(4 MHz, 64 channels)</td></tr>
<tr><td>channel 0</td><td>stream0, ch0</td><td>stream2, ch0</td></tr>
<tr><td>channel 1</td><td>stream1, ch0</td><td>stream3, ch0</td></tr>
<tr><td>channel 2</td><td>stream0, ch1</td><td>stream2, ch1</td></tr>
<tr><td>channel 3</td><td>stream1, ch1</td><td>stream3, ch1</td></tr>
<tr><td>etc....</td><td></td><td></td></tr>
<tr><td rowspan="8">2 [10]</td><td rowspan="8">8 MHz streams
all four local streams are multiplexed onto pins LDI/O[0]
Each channel occupies a 8 Mb/s timeslot of 0.975 ms.</td><td></td><td>LDI/O[0]
(8 MHz, 128 channels)</td><td></td></tr>
<tr><td>channel 0</td><td>stream0, ch0</td><td></td></tr>
<tr><td>channel 1</td><td>stream1, ch0</td><td></td></tr>
<tr><td>channel 2</td><td>stream2, ch0</td><td></td></tr>
<tr><td>channel 3</td><td>stream3, ch0</td><td></td></tr>
<tr><td>channel 4</td><td>stream0, ch1</td><td></td></tr>
<tr><td>etc....</td><td></td><td></td></tr>
<tr><td rowspan="8">3 [11]</td><td rowspan="8">Split 2 MHz/4 MHz streams
Local streams 0&1 are each configured to run at 2 MHz on pins LDI/O[0] and LDI/O[1], respectively.
Local streams 2&3 are multiplexed onto pin LDI/O[2].</td><td colspan="3">LDI/O[0] = local stream 0
LDI/O[1] = local stream 1</td></tr>
<tr><td></td><td>LDI/O[2]
(4 MHz, 64 channels)</td><td></td></tr>
<tr><td>channel 0</td><td>stream2, ch0</td><td></td></tr>
<tr><td>channel 1</td><td>stream3, ch0</td><td></td></tr>
<tr><td>channel 2</td><td>stream2, ch1</td><td></td></tr>
<tr><td>channel 3</td><td>stream3, ch1</td><td></td></tr>
<tr><td>etc....</td><td></td><td></td></tr>
</table>

Table 12 - SER_CNFG bits (control configuration of local serial streams)

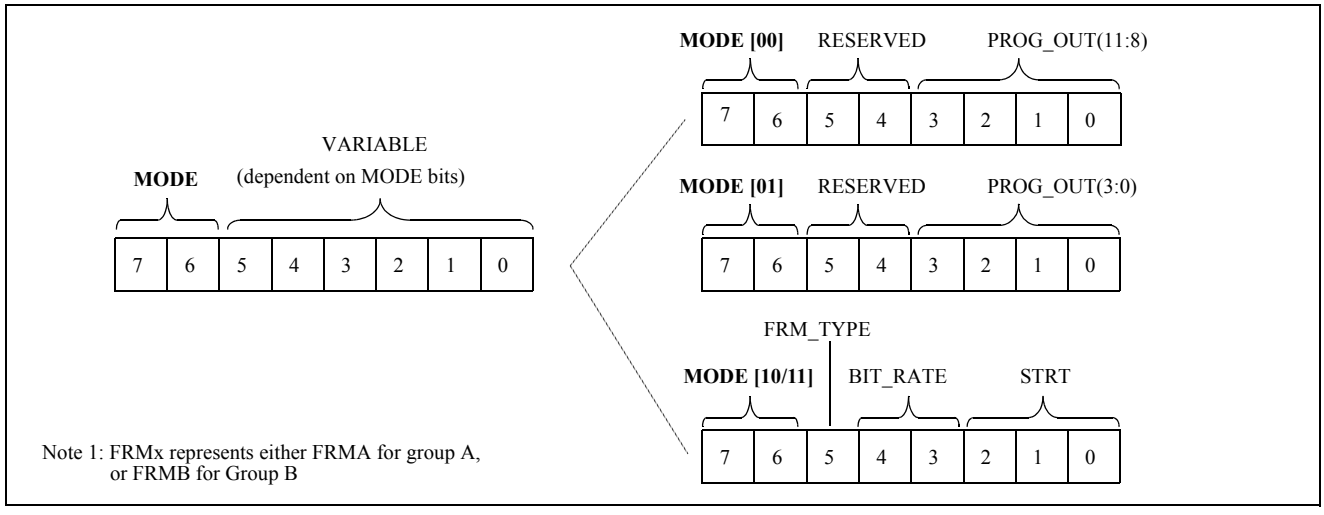


Figure 8 - Frame Mode (FRMx_MODE) Register

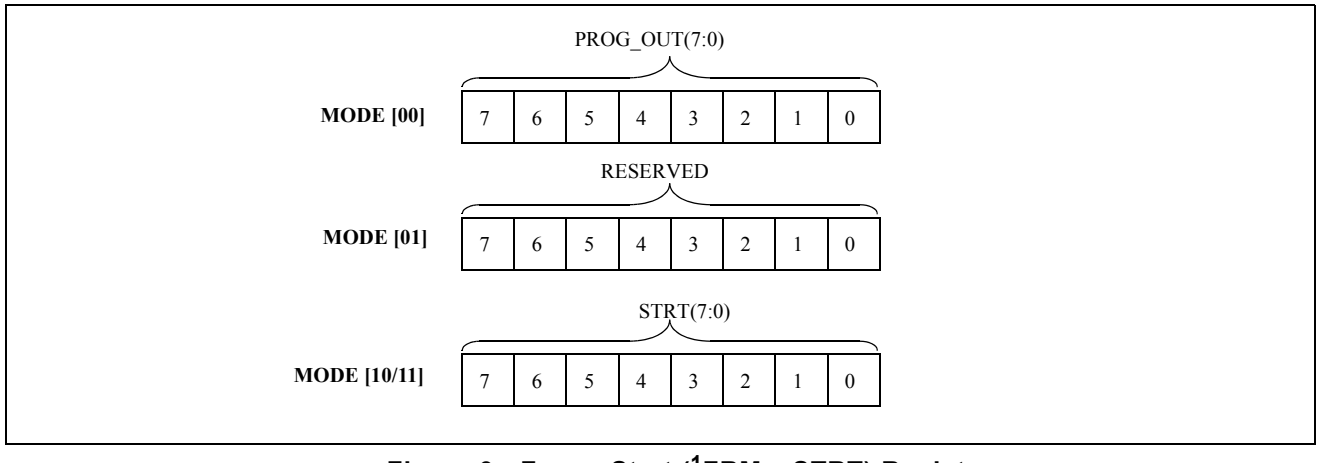


Figure 9 - Frame Start ([1]FRMx_STRT) Register

Mode [bits]	Description
0 [00]	**Programmed output** FGx[0:11] are programmable output pins. All 8 bits of FRMx_START register are driven out pins FGx[0:7] (with bit 0 corresponding to pin FGx[0] etc.) and bits 0-3 of FRMx_MODE register are driven out pin FGx[8:11] (with bit 0 corresponding to pin FGx[8] etc.).
1 [01]	**DSi/DSo output enables** FGA[4:11] pins correspond to output drive enables for the MVIP DSo streams 0 to 7, respectively. FGB[4:11] pins correspond to output drive enables for the MVIP DSi streams 0 to 7, respectively. FGx[0:3] are programmable output pins. The least significant four bits of FRMx_MODE register are driven out pins FGx[0:3] (with bit 0 corresponding to pin FGx[0] etc.).

Table 13 - Frame Group Mode Bits

Mode [bits]	Description
2 [10]	**Normal Framing** Frame groups A&B (FGx[0:11]) are programmed as output framing pulses for use with the local serial data streams (see Figure 16 - “Frame Pulse Timing for Mode 2”). The position of the first framing signal in a group is determined by an 11 bit quantity. The quantity is the FMIC state number minus one. The quantity determines when the first framing signal in a group is to be asserted high.
3 [11]	**Inverted Framing** Identical to Normal Framing except the polarity of the framing pulses is logically inverted.

Table 13 - Frame Group Mode Bits

Notes: FRMx represents either FRMA for frame group A, or FRMB for group B

Bit	Name	Description
Frame Start (FRMx_STRT) Register x		
7:0	PROG_OUT(7:0)	All 8 bits are driven out FGx[7:0]
Frame Mode (FRMx_MODE) Register x		
7:6	MODE	Frame Group Mode 0 [00] Programmed Output
5:4	RESERVED	
3:0	PROG_OUT(11:8)	All 4 bits are driven out FGx[11:8]

Table 14 - Frame Register Bits for Mode 0

Bit	Name	Description
Frame Start (FRMx_STRT) Register x		
7:0	RESERVED	
Frame Mode (FRMx_MODE) Register x		
7:6	MODE	Frame Group Mode 1 [01] DSi/DSo output enable
5:4	RESERVED	
3:0	PROG_OUT(3:0)	All 4 bits are driven out FGx[3:0]

Table 15 - Frame Register Bits for mode 1

Bit	Name	Description
Frame Start (FRMx_STRT) Register x		
7:0	STRT(7:0)	Lower 8 bits of the 11 bit quantity specified in Table 13 - “Frame Group Mode bits”
Frame Mode (FRMx_STRT) Register x		
7:6	MODE	Frame Group Mode 2 [10] Normal Framing 3 [11] Inverted Framing
5	FRM_TYPE	Type of framing signal for this group 0 Frame pulse is one bit cell wide 1 Frame pulse is eight bit cell wide
4:3	BIT_RATE	Frame Group bit rate register Spacing for the framing pulses is for: 0 [00] 2 Mb/s data rate 1 [01] 4 Mb/s data rate 2 [10] 8 Mb/s data rate 3 [11] Reserved
2:0	STRT(11:8)	Upper three bits of the 11 bit quantity specified in Table 13 - “Frame Group Mode bits”

Table 16 - Frame Register Bits for modes 2 & 3

Bit	Name	Description
7:3	RESERVED	Should NEVER be set under normal operating conditions
2	VCO_BYP	Bypass On-chip VCO External VCO may be used in place of FMIC VCO
1	RESERVED	Should NEVER be set under normal operating conditions
0	SEL_XIN	Select X1 as chip master clock, direct input to FMIC state machine. Bypass entire On-chip APLL (including VCO)

Table 17 - Diagnostic (DIAG_REG) Register

Streams	Channels	Indirect RAM Address	
		decimal	hex
MVIP Stream 0	0:31	0:31	0x00:0x1f
MVIP Stream 1	0:31	32:63	0x20:0x3f
MVIP Stream 2	0:31	64:95	0x40:0x5f
MVIP Stream 3	0:31	96:127	0x60:0x7f
MVIP Stream 4	0:31	128:159	0x80:0x9f
MVIP Stream 5	0:31	160:191	0xa0:0xbf
MVIP Stream 6	0:31	192:223	0xc0:0xdf
MVIP Stream 7	0:31	224:255	0xe0:0xff
Local Stream 0	0:31	256:287	0x100:0x11f
Local Stream 1	0:31	288:319	0x120:0x13f

Table 18 - Data Memory Mapping

Streams	Channels	Indirect RAM Address	
		decimal	hex
Local Stream 2	0:31	320:351	0x140:0x15f
Local Stream 3	0:31	352:383	0x160:0x17f

Table 18 - Data Memory Mapping

Indirect RAM Address		Streams	Channels
decimal	hex		
0:31	0x00:0x1f	MVIP Stream 0	0:31
32:63	0x20:0x3f	MVIP Stream 1	0:31
64:95	0x40:0x5f	MVIP Stream 2	0:31
96:127	0x60:0x7f	MVIP Stream 3	0:31
128:159	0x80:0x9f	MVIP Stream 4	0:31
160:191	0xa0:0xbf	MVIP Stream 5	0:31
192:223	0xc0:0xdf	MVIP Stream 6	0:31
224:255	0xe0:0xff	MVIP Stream 7	0:31
256:287	0x100:0x11f	Local Stream 0	0:31
288:319	0x120:0x13f	Local Stream 1	0:31
320:351	0x140:0x15f	Local Stream 2	0:31
352:383	0x160:0x17f	Local Stream 3	0:31

Table 19 - Connection Memory Mapping

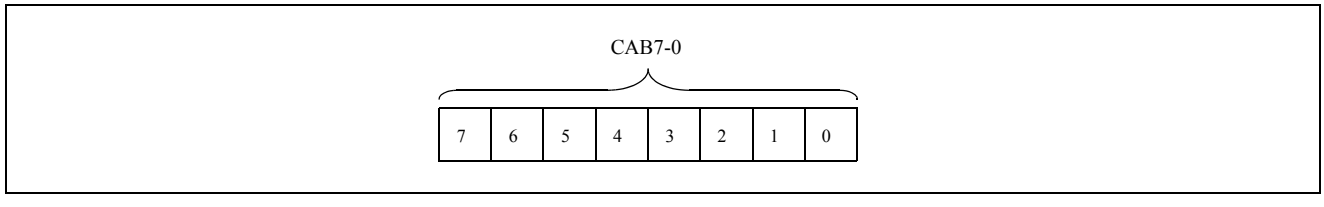


Figure 10 - Connection Memory Low Byte

Bit	Name	Description
7-0	CAB7-0	**Source Channel Address bits 0-7.** These eight bits, together with CAB8 in connection memory high, are used to select any one of the 384 source input channels for the connection.

Table 20 - Connection Memory Low Bits

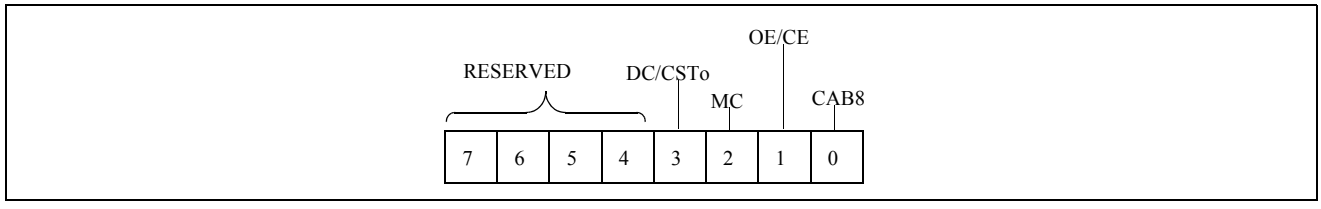


Figure 11 - Connection Memory High Byte

Bit	Name	Description
7:4	RESERVED	
3	DC	**Direction Control.** controls the direction of the MVIP DSi/DSo channel pair. When DC is set, DSi is the input channel and DSo is the output channel. When DC is clear the direction is reversed.
2	MC	**Message Channel.** This bit, when set, will send the eight bits of connection memory low directly out the corresponding output channel and stream. When the bit is cleared, the contents of the programmed location in connection memory low act as an address for the data memory and so determine the source of the corresponding output channels and stream.
1	OE	**Output Enable.** This bit, when set, enables the output drivers on a per-channel basis. This allows individual channels on individual streams to be made high-impedance, permitting the construction of switch matrices. When this bit is cleared, the drivers are disable.
0	CAB8	**Source Channel Address Bit 8.** This bit, together with bits CAB0-7 in connection memory low, is used to select one of 384 different source input channels for the connection.

Table 21 - Connection Memory High Bits for MVIP Channels

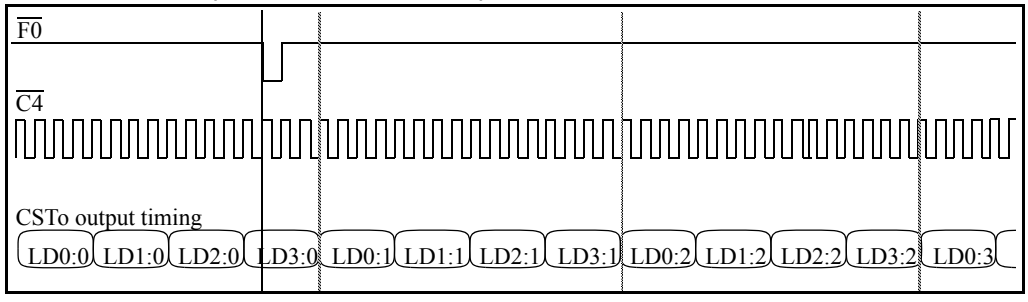
Bit	Name	Description
7-4	RESERVED	
3	CSTo	**CSTo.** The inverted value of this bit is output on the CSTo pin and is available for general purpose system timing functions. The CSTo bit for each of the local output channels is multiplexed onto the CSTo pin as illustrated below: 

Table 22 - Connection Memory High Bits for Local Channels

Bit	Name	Description
2	MC	**Message Channel.** This bit, when set, will send the eight bits of connection memory low directly out the corresponding output channel and stream. When the bit is cleared, the contents of the programmed location in connection memory low act as an address for the data memory and so determine the source of the corresponding output channels and stream.
1	CE	**Channel Enable.** If the DMA_EN bit in the Control/Status register is set, then this bit flags the control logic to perform a bidirectional DMA transfer for this input/output channel pair. When the bit is clear, the DMA transfer for this channel pair is disabled. If DMA operations are not enabled then this bit must be cleared.
0	CAB8	**Source Channel Address Bit 8.** This bit, together with bits CAB0-7 in connection memory low, is used to select one of 384 different source input channels for the connection.

Table 22 - Connection Memory High Bits for Local Channels

JTAG Support

The FMIC JTAG interface is designed to the Boundary-Scan standard IEEE1149.1. The standard specifies a design-for-testability technique called Boundary-Scan Test (BST). A boundary-scan IC has a shift-register stage or 'Boundary-Scan Cell' (BSC) in between the core logic and the I/O buffers adjacent to each I/O pin. The BSCs can control and observe what happens at each I/O pin of the IC. The operation of the boundary-scan circuitry is controlled by a Test Access Port (TAP) Controller.

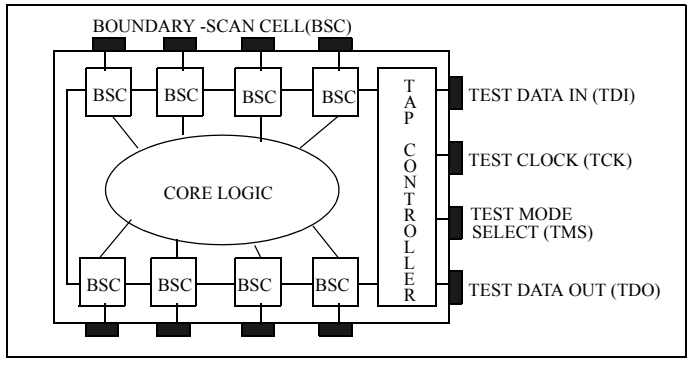


Figure 12 - A Typical Boundary-Scan IC

Test Access Port (TAP)

The Test Access Port (TAP) provides access to many test support functions built into the FMIC. It consists of three input connections and one output connection. The following connections form the TAP:

- Test Clock Input (TCK)
  TCK provides the clock for the test logic. The TCK must not interfere with any on-chip clock and thus remain independent. This permits shifting of test data into or out of the Boundary-Scan register cells concurrently with the operation of the device without interfering with on-chip logic.

- Test Mode Select Input (TMS)
  The logic signal (0's and 1's) received at the TMS input are interpreted by the TAP Controller to control the test operations. The TMS signals are sampled at the rising edge of the TCK pulses. When TMS is not driven from an external source, the test logic perceives a logic 1.

- The Test Data Input (TDI)
  Serial input data applied to this port is fed either into the instruction register or into a test data register, depending on the sequence previously applied to the TMS input. Both registers are described in a subsequent section. The received input data is sampled at the rising edge of the TCK pulses. When TDI is not driven from an external source, the test logic perceives a logic 1.

- The Test Data Output (TDO)
  Depending on the sequence previously applied to the TMS input, the contents of either the instruction register or a data register are serially shifted out towards the TDO. The data out of the TDO is clocked at the falling edge of the TCK pulses. When no data is shifted through the cells, the TDO driver is set to an inactive state.

I[0:1]	Instruction	Description	
[00]	EXTEST	Boundary-Scan register selected, Test Enabled	This instruction is specifically provided to allow board-level interconnect testing of opens, bridging errors etc. When the EXTEST instruction is selected, the on-chip logic is isolated from the FMIC's I/O pin such that the value of the I/O pins is determined by its boundary-scan register. Data for the execution of this instruction can be preloaded into the boundary-scan register with the SAMPLE/PRELOAD instruction.
[01]	SAMPLE/PRELOAD	Boundary-Scan register selected, Test Disabled	Two functions can be performed by the use of this instruction. It allows a SAMPLE ('snapshot') of the normal operation of the FMIC to be taken for examination. And, prior to the selection of another test operation, a PRELOAD can place data values into the latched parallel outputs of the Boundary-Scan cells. During the execution of the instruction, the on-chip logic operation is not hampered in any way.
[10]	BYPASS/TEST	Bypass register selected, Test Enabled	This instruction is used to BYPASS the FMIC while sampling or loading the data registers in other devices with scan registers in the same serial register chain. The FMIC is in test mode and the value of it's I/O pins is determined by its boundary-scan register.
[11]	BYPASS/NOTEST	Bypass register selected, Test Disabled	This instruction is used to BYPASS the FMIC while performing boundary-scan testing on other devices with scan registers in the same serial register chain. The FMIC is allowed to function normally. This instruction is automatically loaded upon reset of the FMIC, as specified in IEEE1149.1

Table 23 - Instruction Register

Instruction Register

In accordance with the IEEE 1149.1 standard, the FMIC uses public instructions listed in Table 23 - "Instruction Register". The FMIC JTAG Interface contains a two bit instruction register. Instructions are serially loaded into the Instruction Register from the TDI when the TAP Controller is in its Shift-IR state. Subsequently, the instructions are decoded to achieve two basic functions: to select the test data register that may operate while the instruction is current and to define the serial test data register path that is used to shift data between TDI and TDO during data register scanning.

Test Data Registers

As specified in the IEEE 1149.1 Standard, the FMIC JTAG interface contains two test data registers:

- The Boundary Scan Register
  The Boundary-Scan Register consists of a series of Boundary-Scan Cells arranged to form a scan path around the boundary of the core logic of the FMIC.

- The Bypass Register
  The Bypass Register is a single stage shift-register that provides a one-bit path that minimizes the distance for test data shifting from the FMIC's TDI to its TDO.

The FMIC boundary-scan register contains 84 bits. Bit 0 in Table 24 - "Boundary Scan Register" is the first bit clocked out. All tristate enable bits are asserted high i.e., a logic 1 enables the corresponding group of outputs/bidirectionals. Note that clocking all zeros into the scan path register will set all outputs to tristate.

Bits	Definition
0:11	FGB[11:0]
12:23	FGA[11:0]
24:31	DSo[7:0]
32	tristate enable for DSo[7:0]
33:40	DSi[7:0]
41	tristate enable for DSi[7:0]
42:45	$\overline{F0}$, $\overline{C4}$, C2, SEC8K
46	tristate enable for
47:51	FRAME, CLK8, CLK4, CLK2, CSTo
52	tristate enable for ALL output only pins
53:54	EX8KA, EX8KB
55:58	LDO[3:0]
59:62	LDI[3:0]
63:70	D[7:0]
71	tristate enable for D[7:0]
72:75	RDY, ERR, DREQ[1:0]
76:83	$\overline{RD}$, $\overline{WR}$, $\overline{CS}$, ALE, A[1:0], $\overline{DACK}$[1:0]

Table 24 - Boundary Scan Register

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply Voltage	V_{DD} - V_{SS}	- 0.3	6	V
2	Voltage on any I/O pin	$V_{I/O}$	V_{SS} - 0.3	V_{DD} + 0.3	V
3	Storage Temperature	T_S	- 65	+ 125	°C
4	Thermal Resistance	Theta Ja	80	90	°C/W

* Exceeding these figures may cause permanent damage. Functional operation under these conditions is not guaranteed.

Recommended Operating Conditions

	Characteristics	Sym.	Min.	Typ.*	Max.	Units	Test Conditions
1	Input Voltage	V_{DD}	4.75		5.25	V	
2	Operating Temperature	T_{OP}	0		+70	°C	
3	Input Voltage Low	V_I	V_{SS}		V_{DD}		

* Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

DC Characteristics: Clocked operation (T_{OP}=0 to 70°C; V_{DD}=5V±5%)

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Supply Current	I_{DD}		30		mA	
2	Input High Voltage for CMOS Inputs	V_{IH}	3.5			V	
3	Input Low Voltage for CMOS pins	V_{IL}			1	V	
4	Input High Voltage for TTL Inputs	V_{IH}	2			V	
5	Input Low Voltage for TTL Inputs	V_{IL}			0.8	V	
6	Low Level Input Leakage Current	I_{IL}			1.0	mA	V_I= V_{SS}
7	High Level Input Leakage Current	I_{IH}			1.0	mA	V_I= V_{DD}
8	Input Pin Capacitance	C_I		4		pF	
9	Output High Voltage (MVIP streams)	V_{OH}	V_{DD} -0.4			V	I_{OH}= 4mA
10	Output Low Voltage (MVIP streams)	V_{OL}			V_{SS}+0.4	V	I_{OL}= 12mA
11	Output High Voltage (Local streams)	V_{OH}	V_{DD} -0.4				I_{OH}= 2mA
12	Output Low Voltage (Local streams)	V_{OL}			V_{SS}+0.4		I_{OL}= 6mA
13	High Impedance Leakage	I_{OZ}			1.0	mA	
14	Output Pin Capacitance	C_O		10		pF	
15	Schmidt Trigger Positive Threshold	V_{t+}			3	V	
16	Schmidt Trigger Negative Threshold	V_{t-}	0.6			V	

AC Electrical Characteristics- Clock and Stream Timing

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Data Propagation Delay	t_{PD}	0		30	ns	Load Cap =200pF For all Timing
2	Data Setup Time	t_S	30			ns	
3	Data Hold Time	t_H	10			ns	
4	Data bit 7 Tristate	t_{D7}	60		90	ns	
5	$\overline{F0b}$/FRAME Setup Time	t_{FS}	50		150	ns	
6	$\overline{F0b}$/FRAME Hold Time	t_{FH}	50		150	ns	
7	$\overline{F0b}$/FRAME Pulse Width	t_{FW}	200		300	ns	
8	CLK8 Period	t_{C8P}	110	122	134	ns	
9	CLK8 High Width	t_{C8H}	55	61	67	ns	
10	CLK8 Low Width	t_{C8L}	55	61	67	ns	
11	$\overline{C4b}$/CLK4 Period	t_{C4P}	232	244	256	ns	
12	$\overline{C4b}$/CLK4 High Width	t_{C4H}	110	122	134	ns	
13	$\overline{C4b}$/CLK4 Low Width	t_{C4L}	110	122	134	ns	
14	C2o/CLK2 Period	t_{C2P}	474	488	502	ns	
15	C2o/CLK2 High Width	t_{C2H}	220	244	268	ns	
16	C2o/CLK2 Low Width	t_{C2L}	220	244	268	ns	

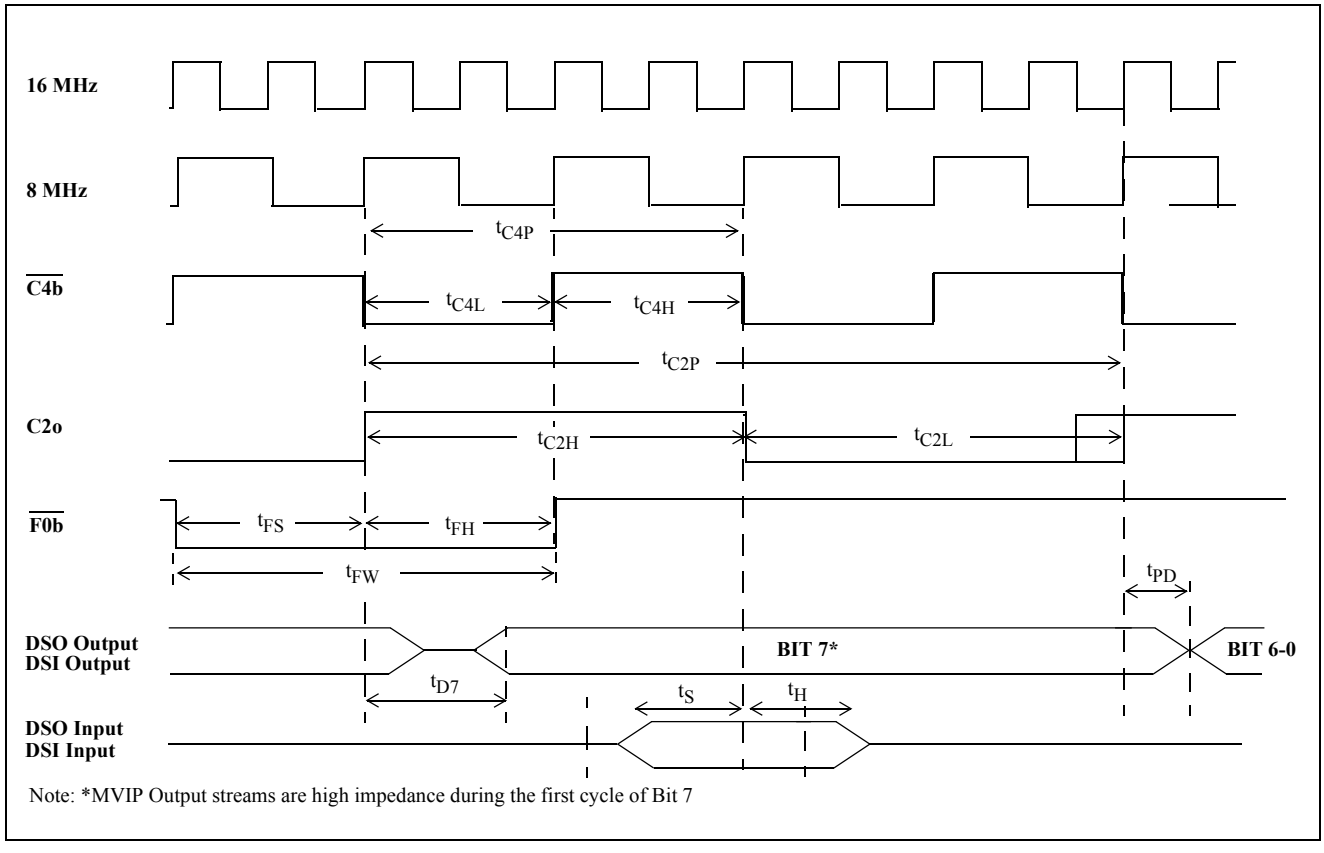


Figure 13 - MVIP Stream Timing

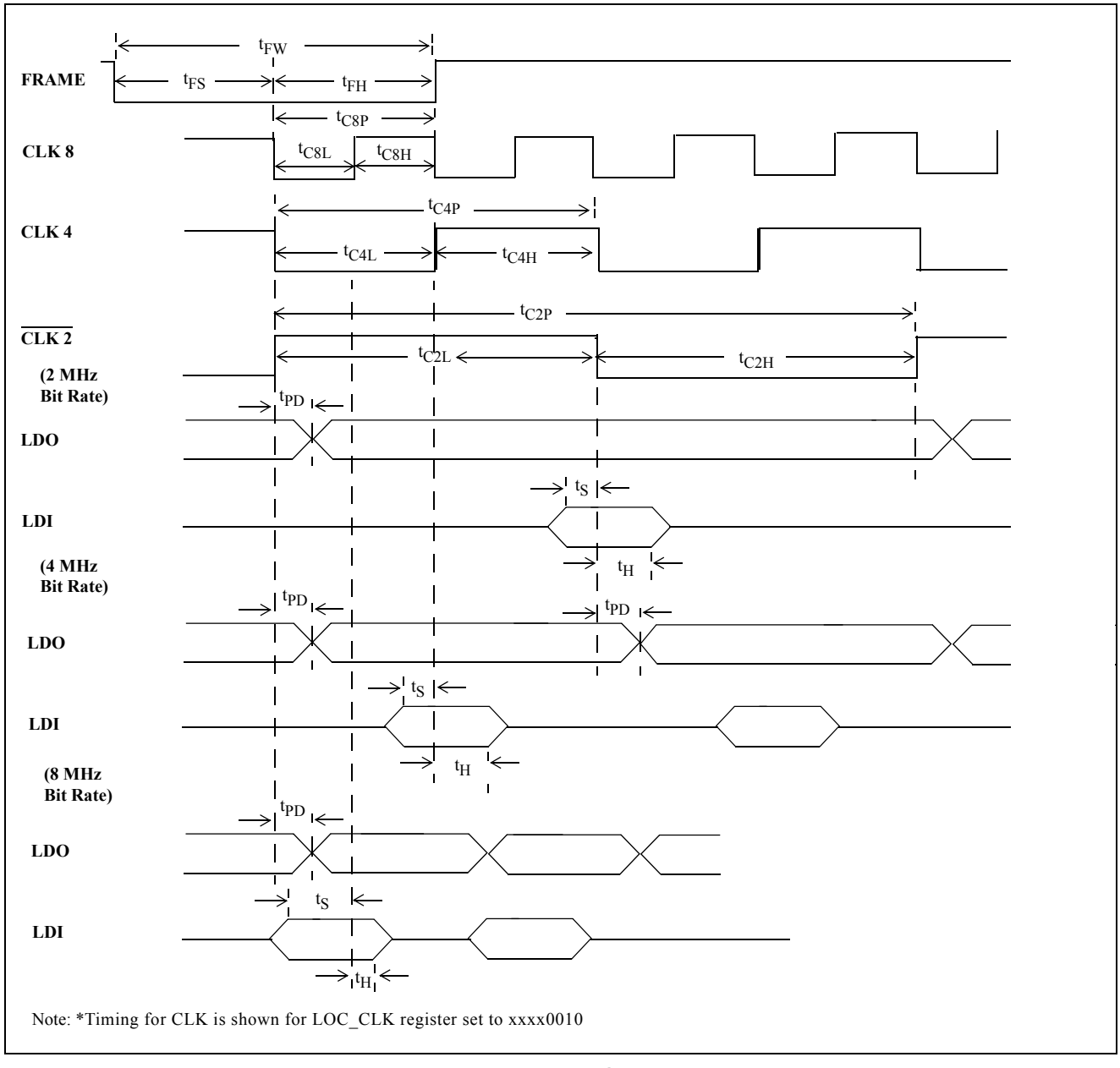


Figure 14 - Local Stream Timing

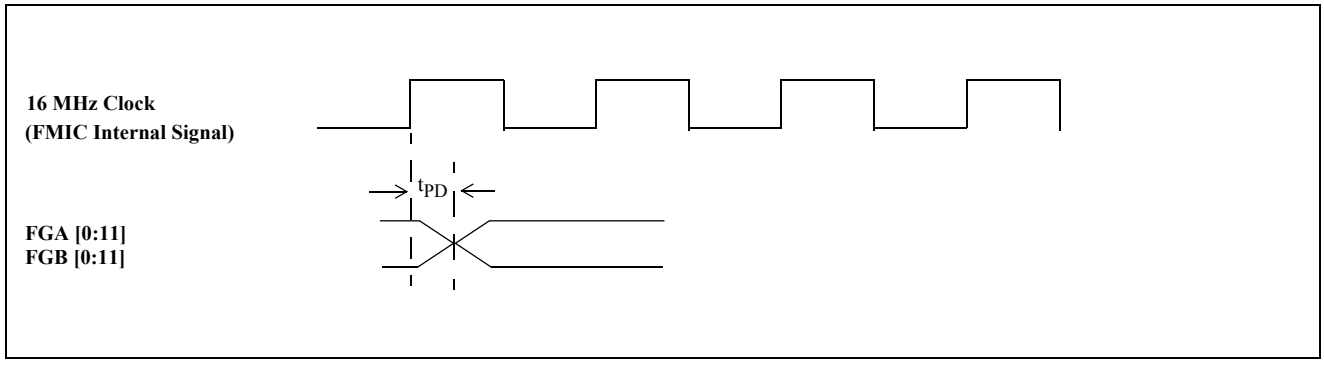
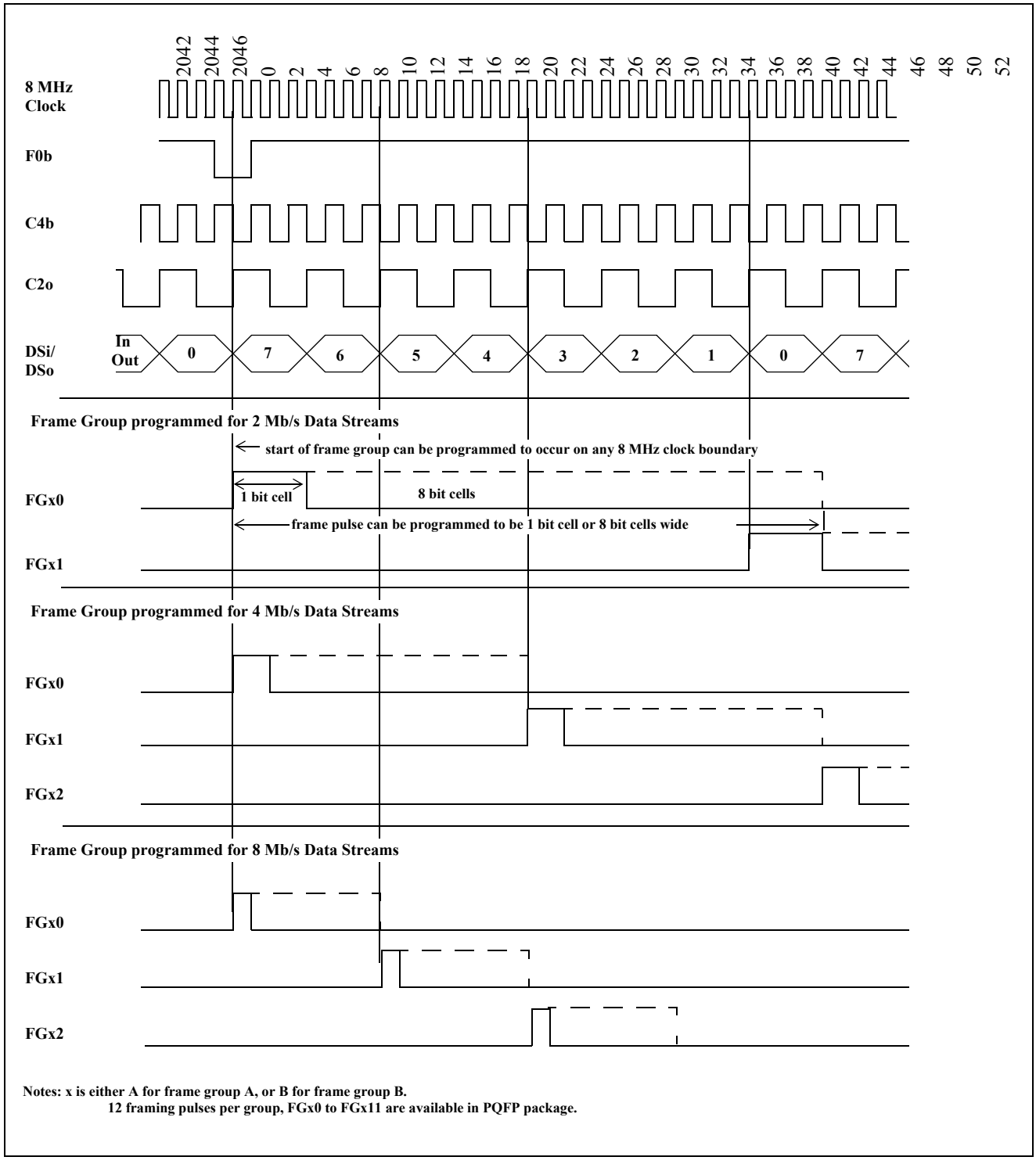


Figure 15 - Local Frame Timing



Notes: x is either A for frame group A, or B for frame group B.
12 framing pulses per group, FGx0 to FGx11 are available in PQFP package.

Figure 16 - Frame Pulse Timing for Mode 2

AC Electrical Characteristics - GCI Timing

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Clock Period	t_{CK}	232	244	256	ns	Load Cap = 200pF for all timing
2	Clock High/Low Width	$t_{CH,}$ t_{CL}	110	122	134	ns	
3	Frame Setup	t_{FRS}	50		150	ns	
4	Frame Hold	t_{FRH}	50		150	ns	
5	Clock Edge to Data Valid	t_{PD}			30	ns	
6	Data Setup	t_{LDS}	30			ns	
7	Data Hold	t_{LDH}	10			ns	

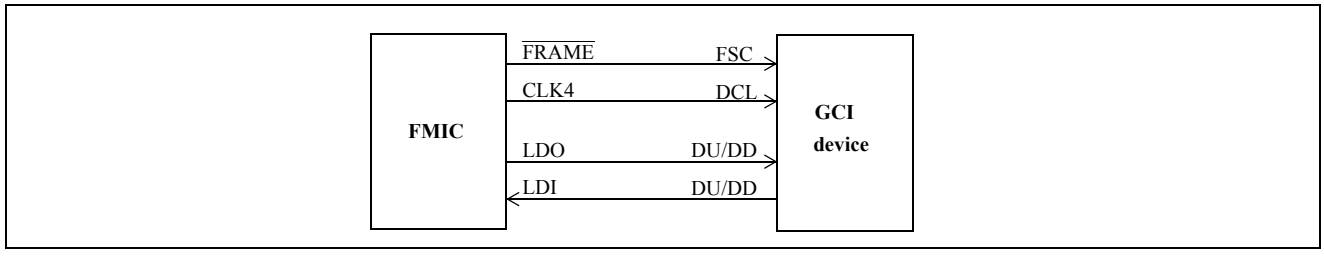


Figure 17 - FMIC to GCI Connections

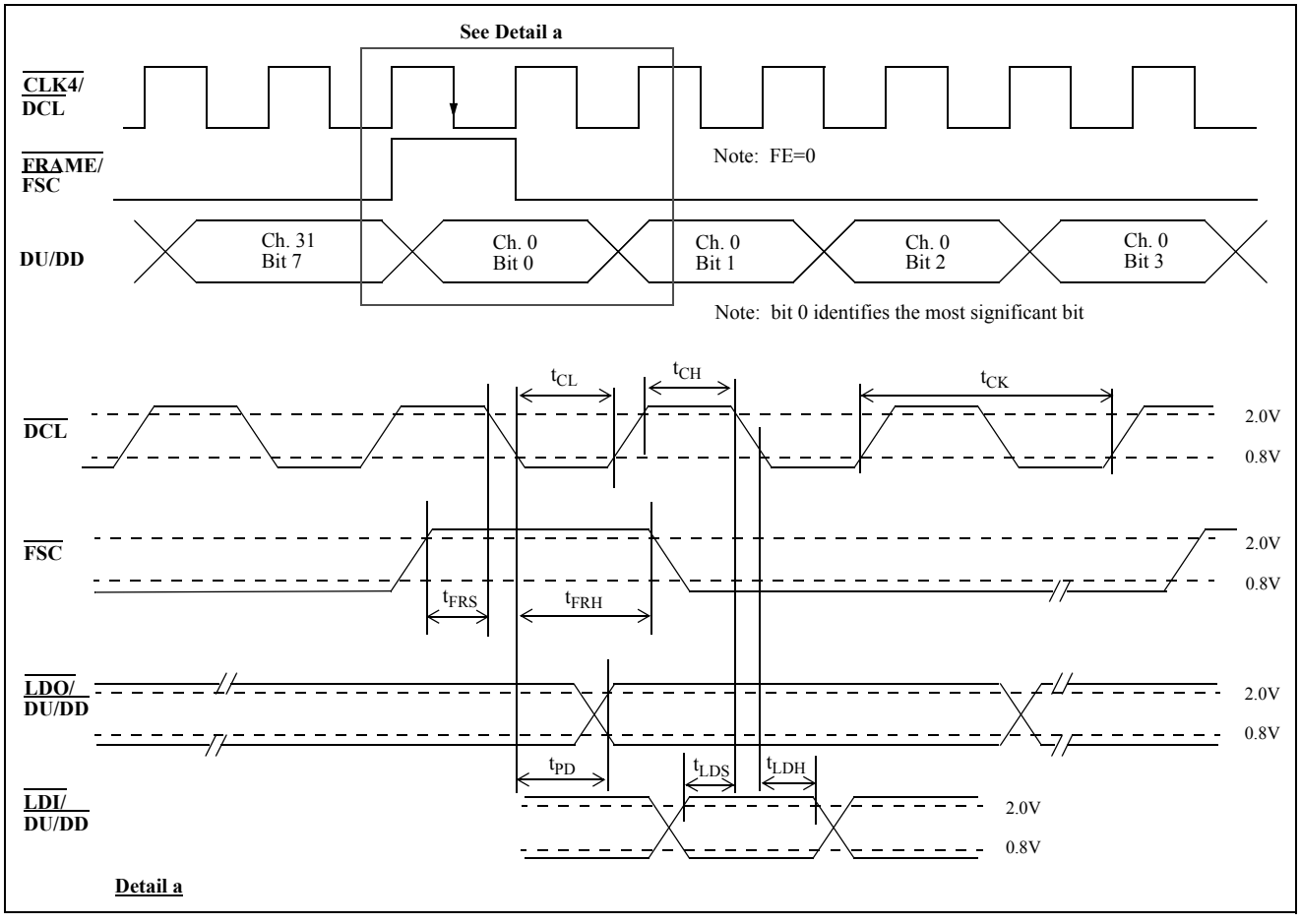
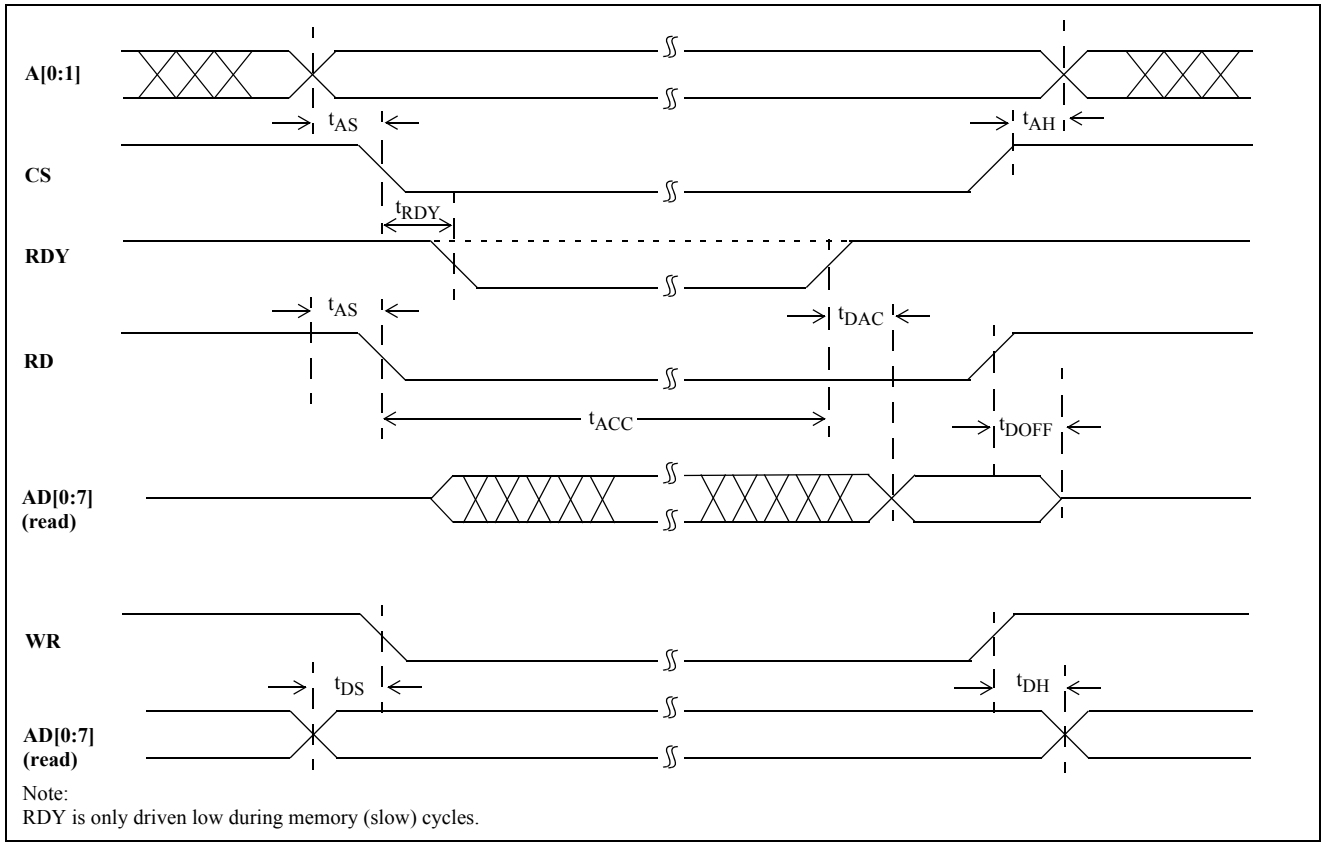


Figure 18 - GCI Timing

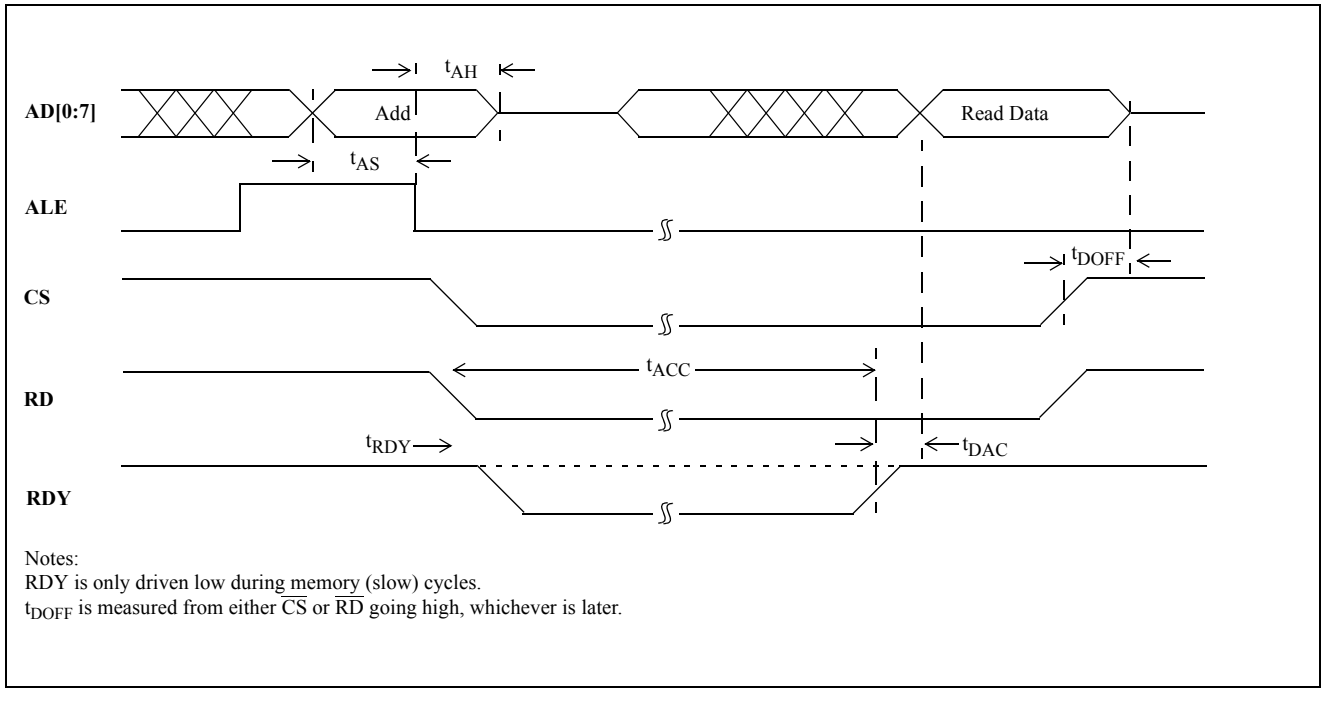
AC Electrical Characteristics - Microprocessor Timing

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Address Setup	t_{AS}	5			ns	Load Cap = 100pF for all timing
2	Address Hold	$t_{AH,}$	5			ns	
3	Data Access from RDY High	t_{DAC}			25	ns	
4	Microprocessor Access to Data Ready Register (Fast) Access Memory (Slow) Access	t_{ACC}			 50 800	 ns ns	
5	Microprocessor to RDY low	t_{RDY}			25	ns	
7	Data Hold	t_{DH}	5			ns	
6	Data Setup	t_{DS}	5			ns	
8	Data Enable Off	t_{DOFF}	20			ns	



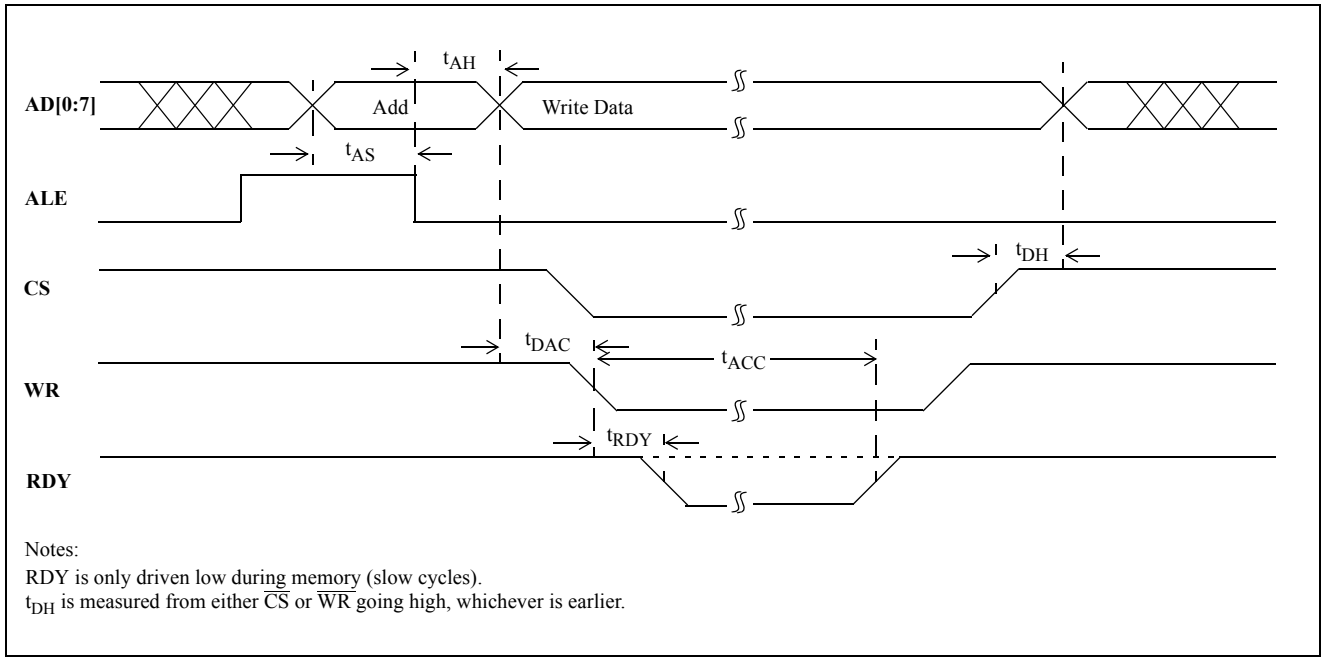
Note:
RDY is only driven low during memory (slow) cycles.

Figure 19 - Intel Non-multiplexed Bus Timing (ALE=VSS)



Notes:
RDY is only driven low during memory (slow) cycles.
t_{DOFF} is measured from either $\overline{CS}$ or $\overline{RD}$ going high, whichever is later.

Figure 20 - Intel Multiplexed Bus Timing for Read Cycle (ALE is active)



Notes:
RDY is only driven low during memory (slow cycles).
t_{DH} is measured from either $\overline{CS}$ or $\overline{WR}$ going high, whichever is earlier.

Figure 21 - Intel Multiplexed Bus Timing for Write Cycle (ALE is active)

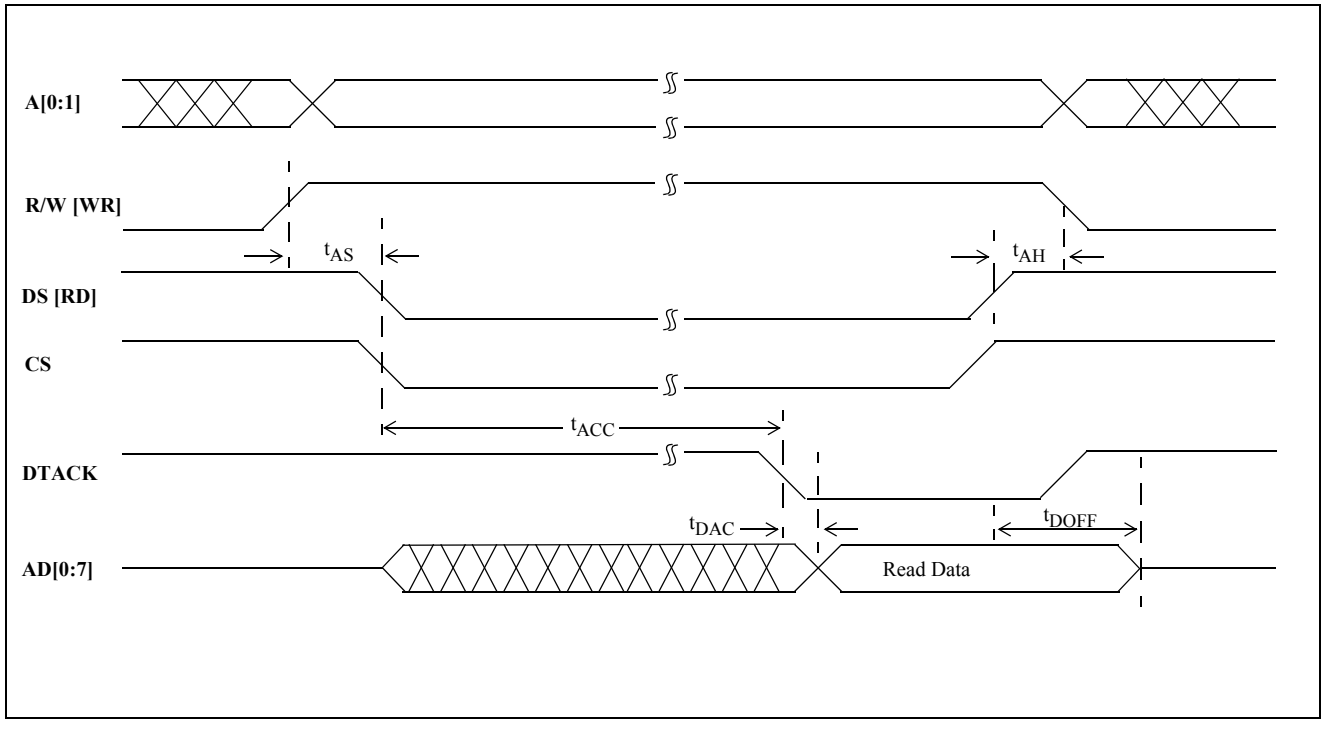


Figure 22 - Motorola Non-multiplexed Bus Timing for Read Cycle (ALE=VDD)

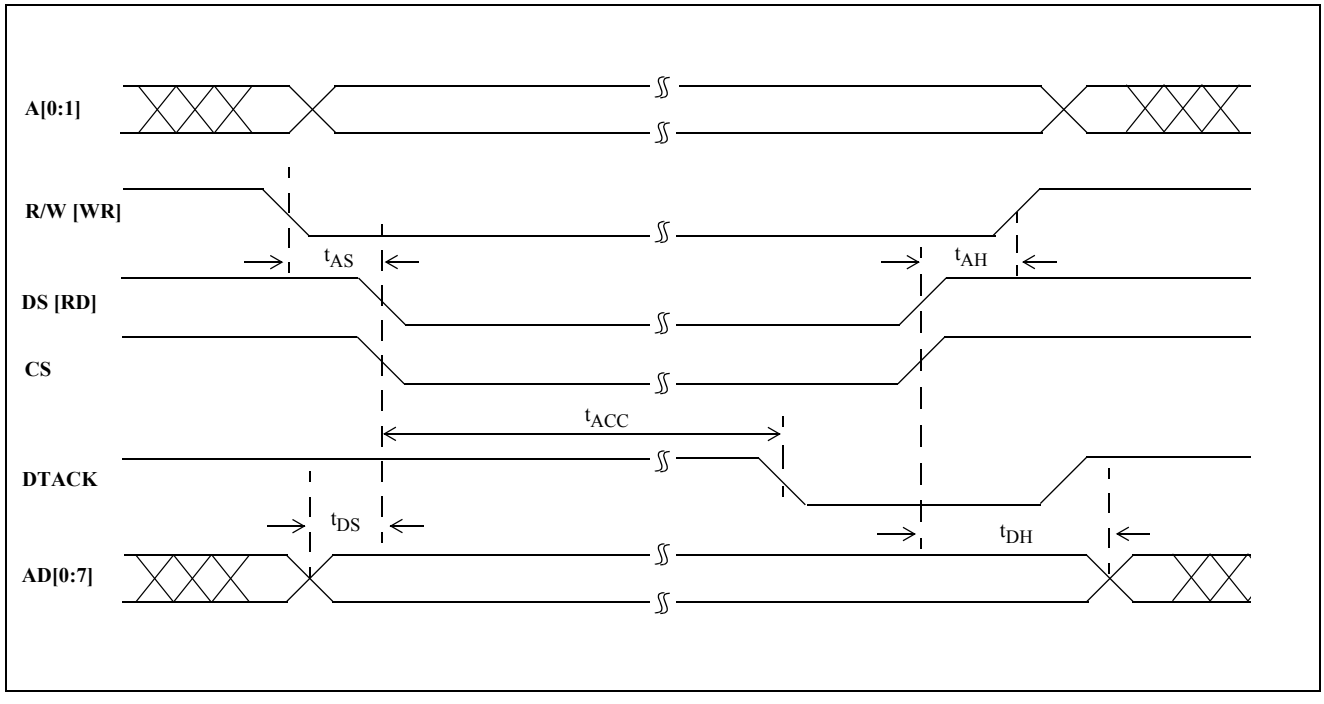


Figure 23 - Motorola Non-multiplexed Bus Timing for Write Cycle (ALE=VDD)

AC Electrical Characteristics - DMA Timing

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	C2o low to $\overline{\text{DACK1}}$ asserted	t_{CDAK1}	DMA controller dependent			ns	
2	C2o low to $\overline{\text{DACK0}}$ asserted	t_{CDAK0}				ns	
3	$\overline{\text{DACK1}}$ asserted to $\overline{\text{RD}}$ low	t_{DAKR}				ns	
4	$\overline{\text{DACK0}}$ asserted to $\overline{\text{WR}}$ low	t_{DAKW}				ns	
5	C2 low to DREQ1 asserted	t_{CDRQ1}	0		30	ns	
6	C2 low to DREQ0 asserted	t_{CDRQ0}	0		30	ns	
7	$\overline{\text{RD}}$ low (on 4th DMA read pulse) to DREQ1 removed	t_{RDRQ}	0		30	ns	
8	$\overline{\text{WR}}$ low (on 4th DMA write pulse) to DREQ0 removed	t_{WDRQ}	0		30	ns	
9	$\overline{\text{RD}}$ pulse width (DMA=fast read)	t_{RW}	100			ns	
8	$\overline{\text{WR}}$ pulse width (DMA=fast write)	t_{WW}	100			ns	

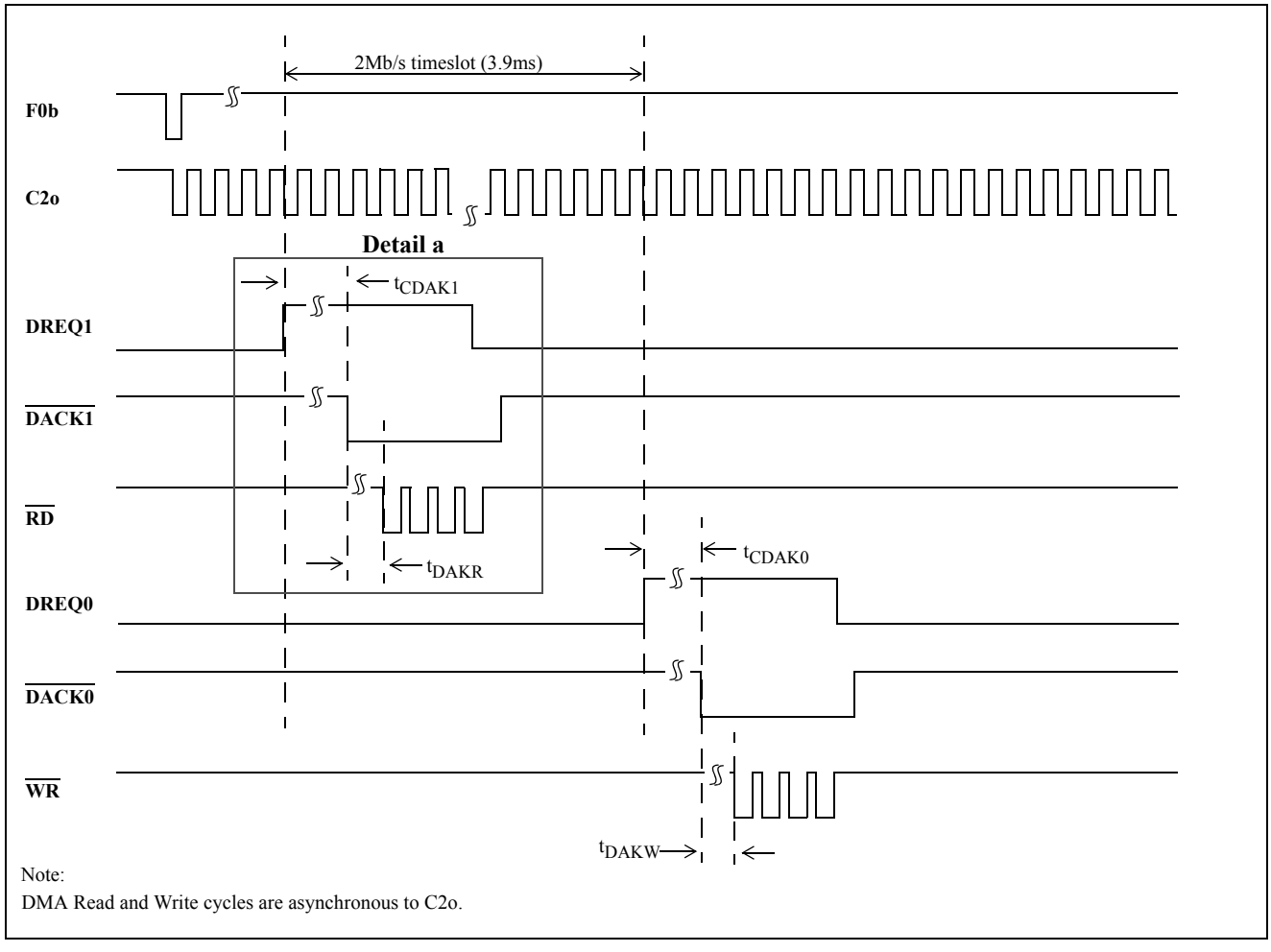


Figure 24 - DMA Interface Timing

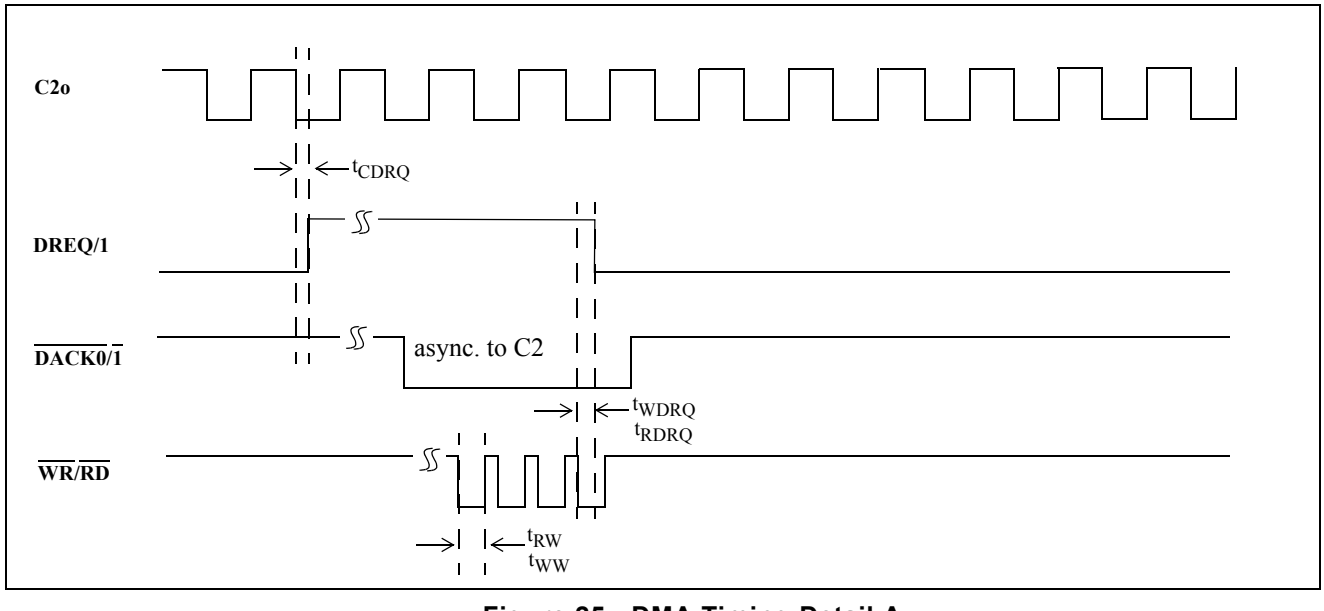
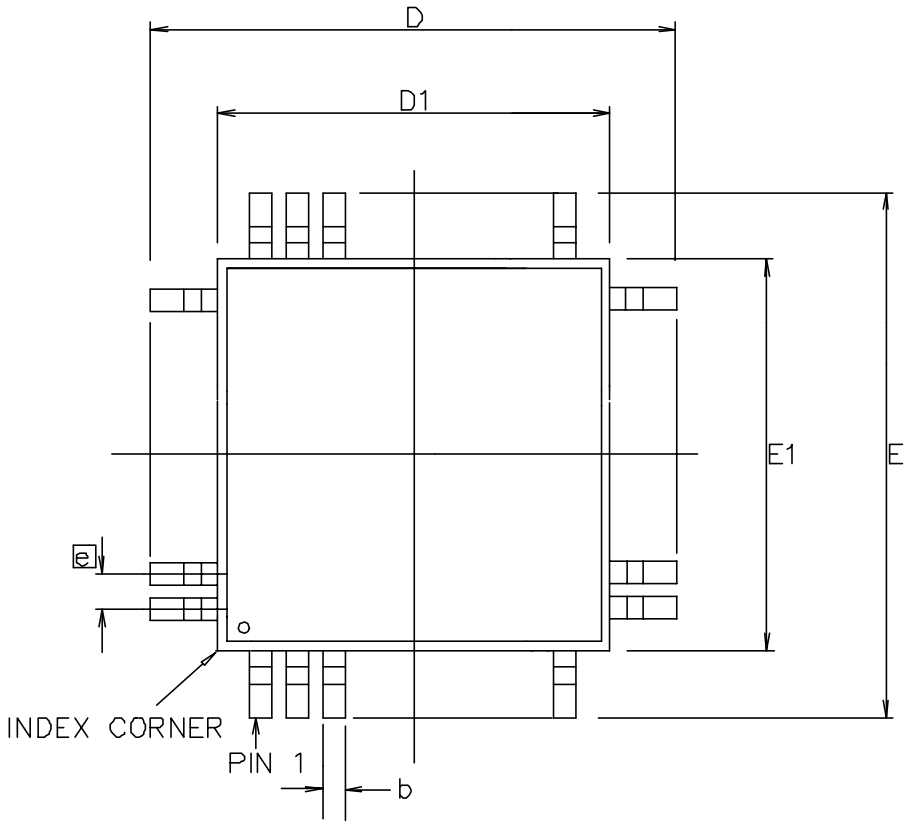
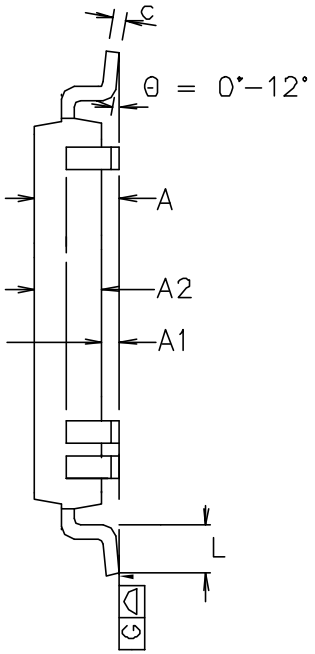


Figure 25 - DMA Timing Detail A





Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	2.6	2.8		.102	0.110
A1	---	---		---	---
A2	---	---		---	---
D	25.20	26.00		0.99	1.024
D1	19.90	20.10		0.783	0.791
E	19.2	20.00		0.756	0.787
E1	13.90	14.10		0.547	0.555
L	1.2	1.8		0.047	0.071
e	0.55	0.75		0.022	0.029
b	0.20	0.40		0.008	0.016
c	0.10	0.20		0.004	0.008
	Pin features				
N	100				
ND	30				
NE	20				
NOTE	RECTANGULAR				

Notes:
1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. Dimension D1 and E1 do not include mould protrusion.
4. Dimension b does not include dambar protrusion.
5. Coplanarity, measured at seating plane G, to be 0.15 mm (0.006 inch) max.

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ZARLINK SEMICONDUCTOR

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