MT90812

Integrated Digital Switch (IDX)

Advance Information

DS5219 ISSUE 2 December 1999

Ordering Information

MT90812AP	68 Pin PLCC
MT90812AL	64 Pin MQFP

-40 to +85°C

Features

- 192 channel x 192 channel non-blocking switching
- 2 local bus streams @ 2Mb/s supports up to 64 channels
- In TDM mode, the expansion bus supports up to 128 channels at 8.192 Mb/s
- Rate conversion capability between local and expansion bus streams
- Integrated conference bridge, supporting 15 parties over 5 bridges
- Integrated PLL
- Frequency Shift Keying (FSK) 1200 baud transmitter, meeting Bell 202 or CCITT V.23 standards
- 32 channel dual tone generator, including 16 standard DTMF tones and tone ringer
- Expansion bus in IDX Link mode, allows the interconnection of up to 4 IDX devices
- Programmable per channel gain control from +3 to -27dB, increments of 1dB for output channels
- Supervisory signalling cadence detection capability
- HDLC resource allocator
- D-channel buffering of message information
- C-channel access for control and status registers
- Provides both variable and constant delay modes
- Parallel microprocessor port, compatible to Intel and Motorola and National CPU's
- Supports both A-law or u-law operation
- Supports both ST-BUS, GCI and HMVIP framing formats

Applications

- Computer Telephony Integration (CTI)
- Key Telephone Systems
- Private Branch Exchange (PBX) Systems

Description

By integrating key functions needed in voice telecom application, the Integrated Digital Switch (IDX) provides a solution-on-a-chip for key telephone systems, PBX applications or CTI designs. Figure 2 shows a typical configuration.

The MT90812 provides non-blocking timeslot interchange capability for B, C and D channels, up to a maximum of 192 channels. It offers conference call capability for 15 parties over a maximum of 5 conference bridges. With its integrated PLL, the MT90812 provides the necessary clocks to support peripheral devices, such as codecs or interconnected IDX devices. Integrated into the IDX is the capability to detect supervisory signalling and to generate FSK 1200-baud signals. In addition, an integrated digital tone generator produces continuous dual tones, including standard DTMF.

With its programmable gain control, the IDX allows users to use codecs without gain control and also centrally manage conference calls.

To support both small and large switching platforms, a built-in expansion Bus allows the interconnection of up to 4 IDX devices or external components such as digital switches. When 4 IDX devices are interconnected, the array is capable of switching 256 channels (64x4), handling 60 conference parties (15x4) and generating additional tones including programmable ones. Other functions are also increased in this configuration. The functional block diagram is shown in Figure 1.

An evaluation board, MEB90812, is available complete with software and a user manual, which demonstrates the layout of a typical application board and facilitates the use of the MT90812, and peripheral devices such as Mitel's DNIC products.

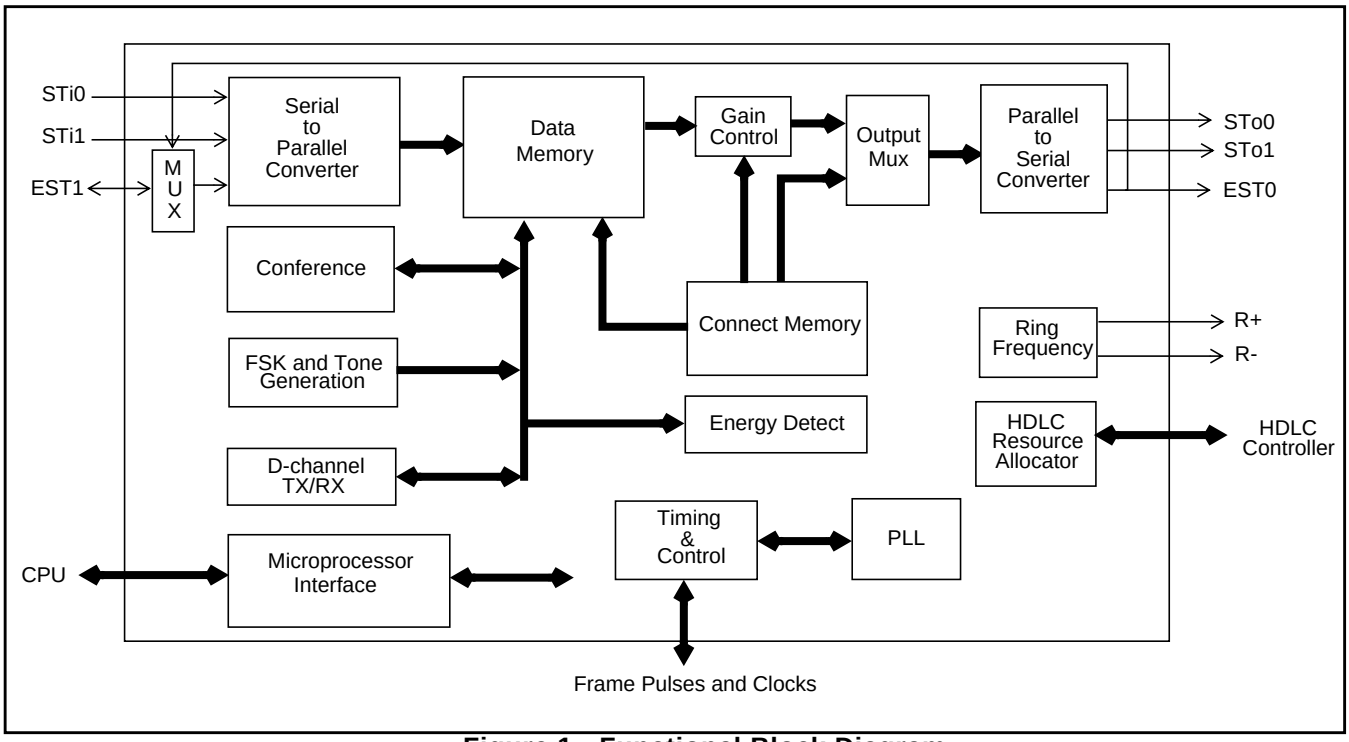


Figure 1 - Functional Block Diagram

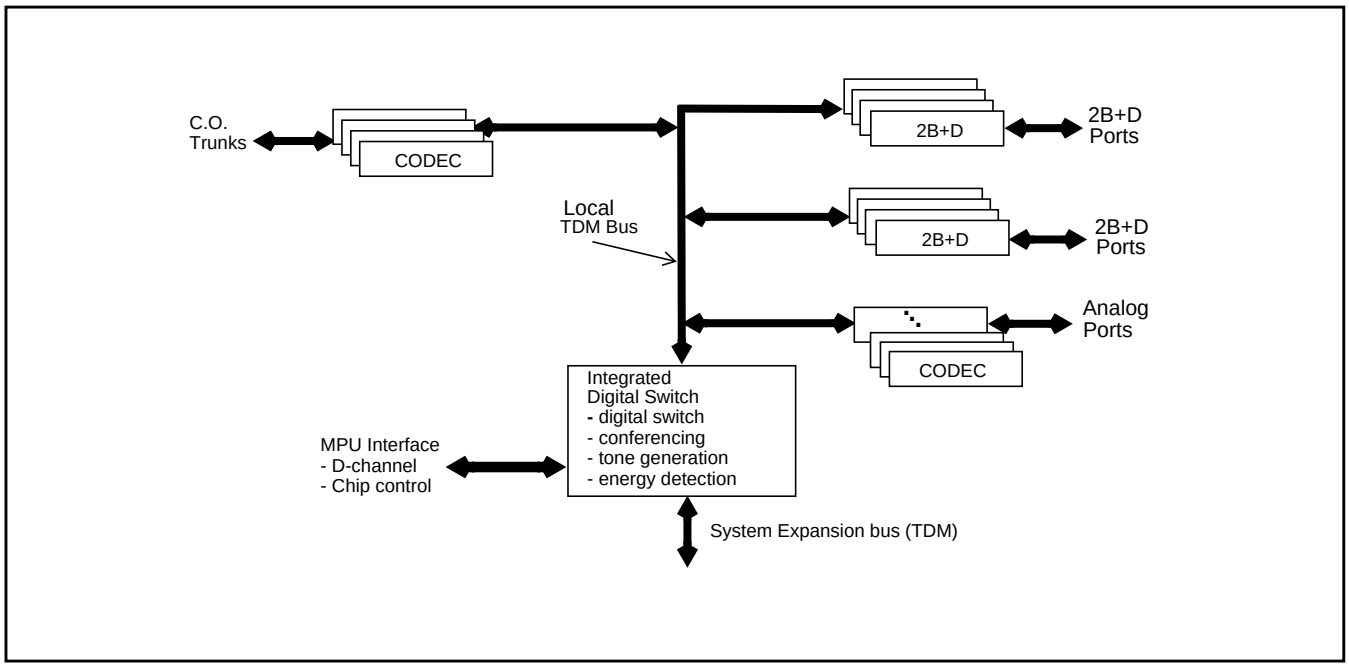
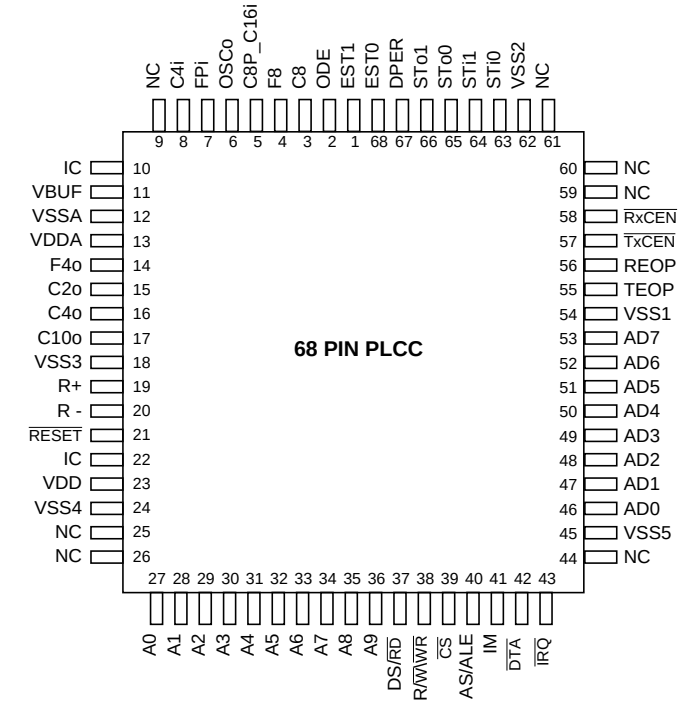


Figure 2 - System Blocks - Typical Configuration



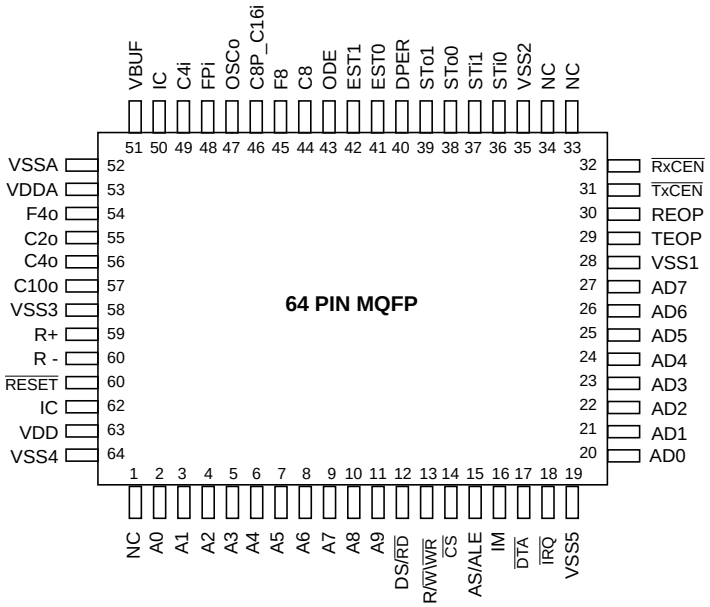


Figure 3 - Pin Connections

Pin Description

Pin #		Name	Description
64 Pin MQFP	68 Pin PLCC		
1	25-26	NC	**No Connect**. Ground
2-11	27-36	A0 - A9	**Address 0 - 9(Input)**. When non-multiplexed CPU bus is selected, these lines provide the A0 - A9 address lines to IDX internal memories.
12	37	DS/$\overline{RD}$	**Data Strobe/$\overline{Read}$ (Input)**. For Motorola multiplexed bus operation, this active high DS input works with $\overline{CS}$ to enable the read and write operations. For Motorola non-multiplexed CPU bus operation, this input is $\overline{DS}$. This active low input works in conjunction with $\overline{CS}$ to enable the read and write operations. For Intel/National multiplexed bus operations, this input is $\overline{RD}$. This active low input sets the data bus lines (AD0-AD7) as outputs.
13	38	R/$\overline{W}$ \ $\overline{WR}$	**Read/$\overline{Write}$ \ $\overline{Write}$ (Input)**. In case of non-multiplexed and Motorola multiplexed buses, this input is Read/$\overline{Write}$. This input controls the direction of the data bus lines (AD0 - AD7) during a microprocessor access. For Intel/National multiplexed bus, this input is $\overline{WR}$. This active low signal configures the data bus lines (AD0-AD7) as inputs.
14	39	$\overline{CS}$	**Chip Select (Input)**. Active low input enabling a microprocessor read or write of internal memories.
15	40	AS/ALE	**Address Strobe or Latch Enable (Input)**. This input is only used if multiplexed bus is selected via IM input pin.
16	41	IM	**CPU Interface Mode (Input)**. If High, this input sets the device in the multiplexed microprocessor mode. If this input is grounded, the device resumes non-multiplexed CPU interface.
17	42	$\overline{DTA}$	**Data Acknowledgment (Open Drain Output)**. This active low output indicates that a data bus transfer is complete. A 10Kohm pull-up resistor is required at this output.
18	43	$\overline{IRQ}$	**Interrupt Request Output (Open Drain Output)**. This active low output notifies the controlling microprocessor of an interrupt request. It goes Low only when the bits in the Interrupt Enable Register are programmed to acknowledge the source of the interrupt as defined in the Interrupt Status Register.
-	44	NC	**No Connect**. Ground
19	45	VSS5	**Ground**.
20-27	46-53	AD0 - AD7	**Data Bus (Bidirectional)**. These pins provide microprocessor access to the internal memories. In the multiplexed bus mode, these pins also provide the input address to the internal Address Latch circuit.
28	54	VSS1	**Ground**.
29	55	TEOP	**Transmit End of Packet (Input)**. This is a strobe that is generated by the HDLC controller chip for one bit period during the last bit of the closing flag of the transmit packet.
30	56	REOP	**Receive End of Packet (Input)**. A receive packet will normally be terminated when the HDLC controller asserts the REOP strobe for one bit period, one bit time after the closing flag is received.
31	57	$\overline{TxCEN}$	**Transmit Clock Enable (Output)**. The HDLC transmitter is controlled by the IDX-generated Transmit Clock Enable signal, $\overline{TxCEN}$.
32	58	$\overline{RxCEN}$	**Receive Clock Enable (Output)**. The HDLC receiver is controlled by the IDX-generated Receive Clock Enable signal, $\overline{RxCEN}$.

Pin Description (continued)

Pin #		Name	Description
64 Pin MQFP	68 Pin PLCC		
33-34	59-61	NC	**No Connect**. Ground
35	62	VSS2	**Ground**.
36-37	63-64	STi0-1	**Serial TDM input streams 0 and 1 (Input)**. Serial data input streams which have data rates of 2.048 Mb/s with 32 channels.
38-39	65-66	STo0-1	**Serial TDM output streams 0 and 1 (Three-state output)**. Serial data output streams which have data rates of 2.048 Mb/s with 32 channels.
40	67	DPER	**D-Channel Input in ST-BUS format (Input)**. The MT8952B CDSTo stream containing formatted D-channel data.
41	68	EST0	**Expansion Bus Serial data stream 0 (Three-state output/input)**. This is a bi-directional pin at 8.192 Mb/s in IDX Link mode. In TDM Link mode this is a 2.048, 4.096 or 8.192 Mb/s output stream.
42	1	EST1	**Expansion Bus Serial data stream 1 (Three-state output/input)**. This is a bi-directional pin at 8.192 Mb/s in IDX Link mode. In TDM Link mode this is a 2.048, 4.096 or 8.192 Mb/s input stream.
43	2	ODE	**Output Device Enable (Input)**. This is the output enable input for the serial outputs. If this input is low, STo0, STo1, EST0, EST1 are high impedance. If this input is high, each channel may still be put into high impedance state by using per channel control bit in the Connection Memory.
44	3	C8	**Clock 8.192 (Bidirectional)**. As an input this signal is used for Expansion bus and/or internal clock source at 8.192 MHz depending on the timing mode selected. As an output this signal is an 8.192 MHz output clock locked to the reference input signal.
45	4	F8	**Frame Pulse for 8.192 MHz (Bidirectional)**. As an input accepts and automatically identifies frame synchronization signals formatted according to ST-BUS and GCI interface specifications. As an output is an 8 KHz frame pulse that indicates the start of the active frame. Either F8 or FPi are used for frame synchronization depending on the timing mode selected
46	5	C8P_C16i	**Oscillator Master Clock (CMOS Input)**. For crystal operation, a 8.192MHz crystal is connected to this pin from OSCo. For clock oscillator operation, this pin is connected to a clock source. The clock source of either 8.192 MHz or 16.384 MHz can be used as selected in the Timing Control Register (TC).
47	6	OSCo	**Oscillator Master Clock (CMOS Output)**. For crystal operation, a 8.192MHz crystal is connected from this pin to C8P_C16i. For clock oscillator operation, this pin is left unconnected.
48	7	FPi	**Frame Pulse (Input).** This input accepts and automatically identifies frame synchronization signals formatted according to ST-BUS and GCI interface specifications. Either F8 or FPi are used for frame synchronization depending on the timing mode selected.
49	8	C4i	**Clock 4.096 MHz (Input)**. This input is the 4.096 MHz clock input.
-	9	NC	**No Connect**. Ground
50-51	10-11	IC	**Internal Connect**. Open.
52	12	VSSA	**Analog Ground**.
53	13	VDDA	**+5 Volt Power Supply (Analog)**.

Pin Description (continued)

Pin #		Name	Description
64 Pin MQFP	68 Pin PLCC		
54	14	F4o	**Frame Pulse for 4.096 MHz (Output)**. This is an 8 KHz output frame pulse that indicates the start of the active ST-Bus/GCI frame. The pulse width is based upon the period of the C4o clock.
55	15	C2o	**Clock 2.048 MHz (Output)**. This output is an 2.048 MHz output clock locked to the reference input signal.
56	16	C4o	**Clock 4.096 MHz (Output)**. This output is an 4.096 MHz output clock locked to the reference input signal.
57	17	C10o	**Clock 10.24MHz (Output)**. This output is a 10.24 MHz clock locked to the reference input signal.
58	18	VSS3	**Ground**.
59	19	R+	**Ringing Generator +ve Output**. This output is a 16, 20, 25 or 50 Hz square wave.
60	20	R-	**Ringing Generator -ve Output**. Square wave output 180 degrees out of phase with R+.
61	21	$\overline{\text{RESET}}$	**Device Reset (Input).** When 0, reset the device internal counters, registers and tri-states STo0, STo1, EST0, EST1 and data outputs from the microport.
62	22	IC	**Internal Connection**. Tie to Vss for normal operation.
63	23	VDD	**+5 Volt Power Supply**.
64	24	VSS4	**Ground**.

Overview

The MT90812 Integrated Digital Switch (IDX) provides the integration of several functions required in a telecom application. The IDX includes a digital switch for switching up to 192 x 192 channels, five conference bridges, a DTMF/supervisory-tone bus and two digital energy detector circuits for trunk call progress tone detection. There are two 2.048 Mbit/s Serial Links and an Expansion Bus that can operate at 2.048, 4.096 or 8.192 Mb/s. A digital Frequency Shift Keying (FSK) transmitter, compatible to Bell 202 or CCITT V.23 1200 baud is provided. D-Channel control is realized by microprocessor access to the MT90812. D-Channel messages are relayed to and from the 2B+D line transceivers via the local TDM link. In D-channel Basic Receive/Transmit mode a 32 byte buffer is provided for each of the transmit and receive directions, and these can be independently assigned to specific D-channels. Alternatively, the HDLC controller mode can be selected, providing an interface to the MT8952 HDLC. The HDLC controller mode provides the necessary control signals to operate the MT8952 HDLC in external timing mode, allowing multiplexing of the MT8952 over the local TDM links.

The MT90812 also provides an interface to the Expansion Bus capable of linking a number of MT90812 devices together directly or in a larger matrix through other digital switches. Each MT90812 can route any of the 64 channels associated with the local TDM streams onto the Expansion Bus. Thus, system growth is easily achieved via the addition of a MT90812 device onto the Expansion Bus. Very little hardware overhead is required to enable cost effective system growth.

In a multi-IDX system functions including Conferencing, Tone generation, Supervisory Signal Detection, D-channel Receiver and Transmitter, Tone Ringer and FSK Transmitter can be shared across the system. For example, in a system consisting of four MT90812 devices, 20 three party conferences can be supported, independent of which MT90812 the party originated. For Tone Generation, 6 programmable tones per MT90812 translates to 24 programmable tones in a four MT90812 system, all of which can be routed to any channel in the system.

1.0 Functional Description

The functional block diagram of Fig. 1 depicts the main operations performed by the MT90812. The integrated digital switch has three TDM streams. The two local TDM serial streams, STi/o0 and STi/o1, operate at 2048kbit/s and are arranged in 125us wide frames each containing 32 8-bit channels. The third TDM stream, comprised of EST0 and EST1 can be used as an additional serial stream at 2.048, 4.096 or 8.192 Mb/s, supporting 32, 64 or 128 channels, respectively.

The expansion bus, EST0/1 operates in two modes, TDM Link and IDX Link modes. IDX Link mode allows multiple MT90812 devices to be linked together very efficiently. In IDX Link mode, the incoming data on the local TDM streams of each MT90812 is transferred onto the expansion bus to enable switching channels between a maximum of four MT90812 devices. For TDM Link mode, the expansion bus is configured as a TDM serial stream which can run at 2.048, 4.096 or 8.192 Mb/s. In TDM Link mode, the MT90812 can be connected to more peripheral devices or to other digital switches (i.e. MT8980/1/2 or MT8985/6) to support larger matrices of MT90812 devices.

The MT90812 can switch data from channels on the local and expansion input streams to channels on the local and expansion output streams. The controlling microprocessor can simultaneously read channels on TDM inputs or write to channels on TDM outputs (Message Mode). To the microprocessor, the MT90812 looks like a memory peripheral. The microprocessor can write to the MT90812 to establish switched connections between input TDM channels and output TDM channels, or to transmit messages on output TDM channels. By reading from the MT90812, the microprocessor can receive messages from TDM input channels or check which switched connections have already been established.

The MT90812 provides conference call capability and supports a total of 15 parties, distributed over a maximum of 5 conferences. (i.e. 1x15 parties, 3x5 parties, 5x3 parties etc.). Conference parties can be from any of the incoming channels on the local or expansion TDM streams.

Gain Control is provided on the outgoing channels, with a range of +3 to -27 dB in steps of 1dB, as well as -∞dB. If a channel is in a conference, incoming and/or outgoing gain control is provided. Conference incoming gain also ranges from +3 to -27 dB in steps of 1dB, as well as -∞dB. Conference outgoing gain can range from 0 to -9 dB in steps of 3 dB.

A tone source of 32 dual tones is generated from the tone generator block and stored in Data Memory. Outgoing gain control of +3 to -27 dB in steps of 1dB, as well as -∞dB, is provided for each tone. Seven of the thirty-two tones are programmable in frequency. The 32 locations can be switched to outgoing channels or accessed by the microprocessor.

A phase coherent FSK transmitter generates two output frequencies, representing the ‘marks’ and ‘spaces’, selectable to Bell 202 or CCITT V.23 standards at 1200 baud. The FSK transmitter output is a PCM coded signal that can be directed to any outgoing local TDM channel.

Two energy detect blocks provide monitoring capability of supervisory signalling for any of the TDM channels. D-Channel access is provided to link the microprocessor to the transceivers. There are two modes of message formats that can be selected. The D-Channel Basic Receive Transmit (DBRT) mode provides basic formatting of the data, which includes start and stop signalling and parity checking. In DBRT mode there are RX and TX buffers, 32 bytes in length, which can be allocated to any of the incoming/outgoing channels of the TDM streams. The HDLC mode provides a control interface to facilitate the multiplexing of an external HDLC controller (MT8952) over any of the local TDM streams’ D-Channels.

C-Channel access for control of ST-BUS family of devices (e.g. MT9160B, MT9171/72, MT8930, MT8910) is provided through Message Mode.

Each of the programmable parameters within the functional blocks are accessed through a parallel microprocessor port compatible with CPU non-multiplexed bus and Intel®, Motorola® and National®

multiplexed bus specifications. The MT90812 can operate in either A-Law or μ–Law as defined in Control register as specified in section “Control Register (CTL)” on page 54.

2.0 Local TDM Streams

There are two local serial Time Division Multiplexed (TDM) streams. These streams at STi/o0 and STi/o1 provide a link between the MT90812 and other peripheral devices, including those in the ST-BUS family (e.g. MT9160B, MT9171/72, MT8930, MT8910). The two serial streams operate at 2.048 Mbit/s and are arranged in 125us wide frames, each comprising 32 8-bit channels. Refer to Section 9.2, “Serial Data Interface Timing”.

The MT90812 can support Primary Rate or Basic Rate devices. Using the Basic Rate devices (e.g. MT9171/72 DNIC) in dual port mode the D-Channel should be assigned to STi/o1 streams. D-channel signalling support is provided for any timeslot on the STi/o1 streams for the HDLC Controller mode. The DBRT can access any timeslot and stream. Refer to “D-Channel Signalling Support” on page 30 and “Local TDM Channel Assignment” on page 76.

3.0 Expansion Bus

The expansion bus operates in 2 modes, IDX Link and TDM Link modes. The modes will be described in the following sections. Section 24.1 describes the timing references used for both Expansion bus modes.

3.1 TDM Link Mode

In this mode, the expansion bus at EST0 and EST1, are regular output and input serial streams, respectively. They operate at either 2.048, 4.096 or 8.192 Mbit/s. Refer to Fig. 4.

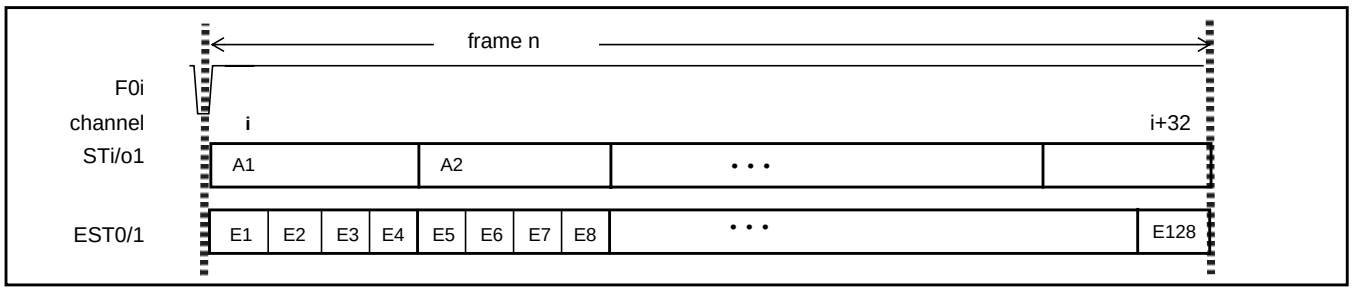


Figure 4 - Expansion Bus (TDM Link mode)

At 2.048Mb/s, the first block of 32 locations of Data Memory reserved for the expansion bus are used. The 32 incoming channels on EST1 are placed in expansion block 1 of Data Memory. At 4.096 Mb/s the 64 bytes are utilized in expansion block 1 and 2. At 8.192Mb/s all 128 locations of Data Memory reserved for the expansion bus are used. Refer to the description of the memory allocation in Section 5, “Address Memory Map”.

This mode allows linking larger matrices of MT90812 devices together. For example, at 2.048 Mb/s, eight MT90812 devices can be connected together via a MT8980D (DX) switch, as shown in Fig. 5.

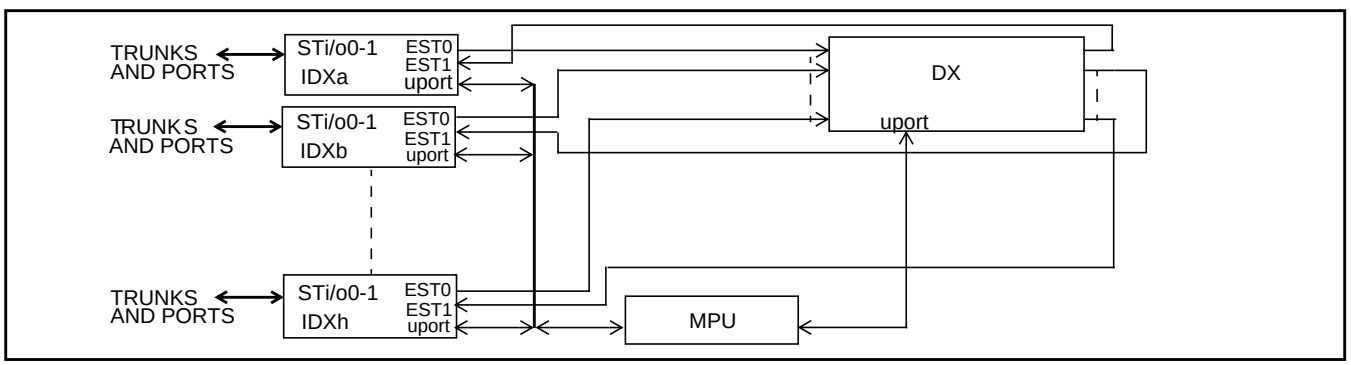


Figure 5 - Eight IDX Configuration using Expansion Bus TDM Link mode

Each of the 32 channels of the 8 streams connecting the DX and IDX devices can be switched to any outgoing channel and stream. This provides switching across all eight of the MT90812 devices.

3.2 IDX Link Mode

In IDX Link mode the expansion bus allows up to four IDX devices to be connected together as shown in Fig. 6. The data flow between each MT90812 is supported on EST0 and EST1, two serial streams which operate at 8.192Mbit/s and each consist of 128 8-bit channels. The four MT90812 devices are labelled A, B, C and D. TDM Link Mode can be used to link more than four MT90812 devices, refer to Section 3.1.

The expansion bus channel assignment for EST0 and EST1 in IDX Link mode is shown in Fig. 7. For the EST0 stream, each of the four MT90812 devices place data into 32 timeslots and read in data from the other 96 timeslots. The EBUS position, as defined in section “Control Register (CTL)” on page 54, designates which timeslots the MT90812 writes to and which timeslots it reads from. For example, IDX A would output Channel 1 at the timeslot shown as A1 in Fig. 7 and input data during timeslots B1, C1 and D1.

For the EST1 stream, each MT90812 reads in 32 channels and can output data to the other 96 channels. Which channels are read are also determined from the EBUS position bits. For example, IDX A will read data during timeslots EA1, EA2,... EA32.

Each MT90812 will receive a total of 128 channels from the two streams EST0 and EST1. For IDX A, the 96 channels, B1-B32, C1-C32, D1-D32 will be taken from EST0 and 32 channels EA1-EA32 will be taken from EST1.

A description of programming the switch in IDX Link mode is given in “Connection Memory” on page 10. The Data Memory allocation is described in Section 5, “Address Memory Map”.

On power up, the EBUS is set to high impedance and the EBUS position bits must be programmed to avoid any contention on the two streams.

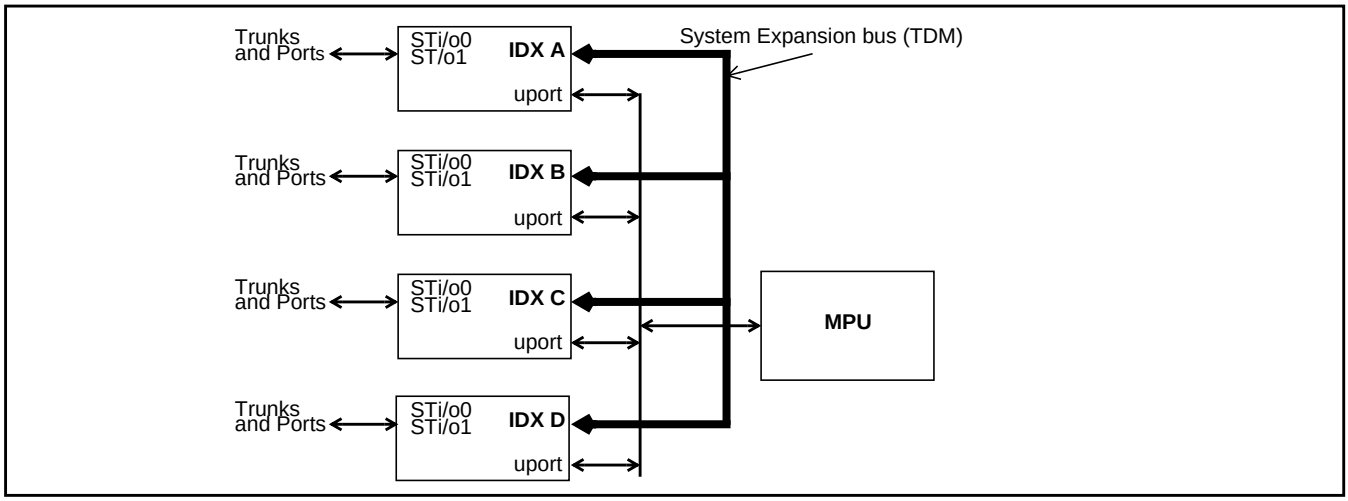


Figure 6 - Four IDX Configuration using Expansion Bus IDX Link mode

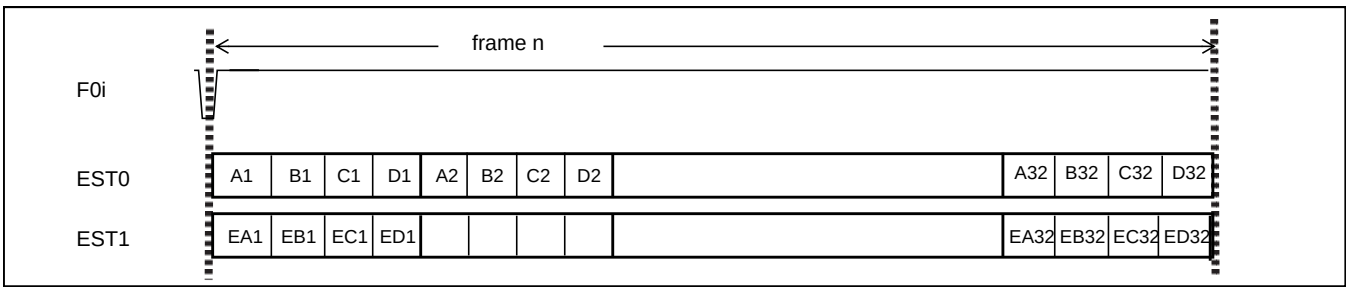


Figure 7 - Expansion Bus - IDX Link mode

4.0 Switching

The switching function of the MT90812 is described in four parts:

- How incoming data from the Local TDM streams are transferred to Data Memory.
- How incoming data from the Expansion Bus is transferred to Data Memory for both IDX Link and TDM Link modes.
- Connect Memory and Data Memory structure.
- How output data can be switched from either Data Memory or Connect Memory.

Each will be described below with reference to Figure 1 - “Functional Block Diagram”. This is followed by a more detailed description of Connect Memory in Section 4.2.

4.1 Switching Functions

4.1.1 Data Transfer from Local TDM Streams to Data Memory

The serial data incoming to the MT90812 is converted into parallel format (8 bits per channel) with the parallel to serial converters for both the Local and Expansion Bus streams. This data is written to consecutive locations in Data Memory.

The two local TDM streams, STi/o0 and STi/o1, operate at 2.048 Mb/s for a total of 64 channels per frame. The 64 bytes are stored in the Local Data Memory page in locations 00_H to $3F_H$. Refer to the Memory Map in Table 2.

4.1.2 Data Transfer from the Expansion Bus to Data Memory

In TDM Link mode, the expansion bus rate can be set to 2.048, 4.096 or 8.192 Mb/s, where the number of channels used for the expansion bus stream are 32, 64 and 128, respectively. In Data Memory, 128 bytes are reserved in the Expansion Data Memory page. If there are only 32 or 64 channels (i.e. at 2.048 or 4.096 Mb/s) then the first 32 or 64 locations of the 128 reserved for the expansion bus are used.

In IDX Link mode, the Expansion Bus rate is set to 8.192 Mb/s. There are 96 channels incoming from EST0 and 32 channels from ESTI, for a total of 128 incoming channels read into Expansion Data Memory.

4.1.3 Connect Memory and Data Memory Structure

There are 64 locations in Local Data Memory reserved for the incoming channels of the Local TDM streams and 128 locations in Expansion Data Memory, for the incoming channels of the Expansion Bus. In addition, there are another 32 locations of Local Data Memory reserved for the Tone generator. Refer to the Memory Map in Table 2.

For each output channel there is an associated Connect Memory location. There are 128 locations for the outgoing expansion bus channels and 64 for the local TDM streams.

4.1.4 Switching Output Data from Either Data Memory or Connect Memory

When the MT90812 switches data from input channels to outgoing channels, the address for Data Memory is read from the Connection Memory location corresponding to the desired output channel. In Message Mode, output data is read directly from the Connection Memory location corresponding to the output channel. The details for setting up the connections are given in the following section.

4.2 Connection Memory

The use of Connection Memory in the MT90812 is described in three parts:

- Connection Memory usage for Switch Connection or Message Mode

- Control Register and the use of Connection Memory
- Connect Memory Configurations for Expansion Bus Modes

Each will be described below. A full description of addressing memory in the MT90812 is given in “Address Memory Map” starting on page 12. Refer to Section 21.0 for a definition of the Connection Memory High and Low bits.

4.2.1 Connection Memory Usage for Switch Connection or Message Mode

Locations in the Connection Memory, which is split into high and low parts, are associated with particular TDM output streams. When a channel is due to be transmitted on an TDM output stream, the data for the channel can either be switched from an TDM input stream or it can originate from the microprocessor. If the data is switched from an input, then the contents of the Connection Memory Low location associated with the output channel is used to address the Data Memory.

The Data Memory address corresponds to the channel on the input stream on which the data for switching arrived. If the data for the output channel originates from the microprocessor (Message Mode), then the contents of the Connection Memory Low location associated with the output channel are output directly, and this data is output repetitively on the channel once every frame until the microprocessor intervenes.

The Connection Memory High determines whether individual output channels are in Message Mode, controls individual output channels to go into a high-impedance state and specifies the gain for each outgoing channel.

4.2.2 Connection Memory Select

If the microport is operating in multiplexed mode, addressing the high and low sections of Connection Memory is done by setting the Memory Select Bits in Control Register. If the microport is operating in non-multiplexed mode, addressing the high and low sections of connection memory is done by setting the external address bits A9,A8,A7. Refer to “Address Memory Select Register (AMS)” on page 53, and “Microprocessor Port” on page 49.

The Control Register also consists of mode control bits that allows the chip to broadcast messages on all TDM output channels (i.e., to put every channel into Message Mode). Mode control bit 5, CT2:MSG bit, puts every output channel on every output stream into active Message Mode; i.e., the contents of the Connection Memory Low are output on the TDM output streams once every frame unless the ODE pin is low. In this mode the chip behaves as if bits 2 and 0 of every Connection Memory High location were 1, regardless of the actual values.

If CAR:MSG bit is 0, then bits 2 and 0 of each Connection Memory High location function as follows. If CMH:bit 2 is set to 1, the associated TDM output channel is in Message Mode; i.e., the byte in the corresponding Connection Memory Low location is transmitted on the stream at that channel. Otherwise, the serial input is transmitted and the Connection Memory Low defines the associated input stream and channel where the byte is to be found.

If the ODE pin is low, then all serial outputs are high-impedance. If the ODE pin is high and CAR:MSG bit is 1, then all outputs are active. If the ODE pin is high and CAR:MSG bit is 0, then the bit 0 in the Connection Memory High location enables the output driver for the corresponding individual output stream and channel. CMH:bit 0=1 enables the driver and CMH:bit 0=0 disables it.

4.2.3 Connect Memory Configurations for Expansion Bus Modes

In TDM Link mode, the 128 Connect Memory locations reserved for the expansion bus are associated with the outgoing channels of EST0.

In IDX Link mode, there are 32 outgoing channels for the EST0 stream. For the EST1 stream there are 96 outgoing channels. In this mode the Connection Memory is configured such that the first 32 locations are used for the EST0 stream. The next 96 locations are for the EST1 stream as selected by the Expansion Bus Position bits as described in “Address Memory Map” on page 12.

5.0 Address Memory Map

The MT90812 memory is accessed via the microport. The microport can operate in multiplexed or non-multiplexed mode as described in “Microprocessor Port” on page 49 The access to the MT90812 memory for multiplexed and non-multiplexed mode is described below.

5.1 Memory Page Select

The MT90812 memory is divided into 7 pages, as listed in Table 1.

Non-Multiplexed Mode	Multiplexed Mode		Memory Pages
External Address A9,A8,A7	Memory Select Bits	External Address A7	
111	XXX	0	Control Registers (Section 22.0)
000	000	1	Local Data Memory
001	001	1	Expansion Data Memory
010	010	1	Local Connect Memory Low
011	011	1	Expansion Connect Memory Low
100	100	1	Local Connect Memory High
101	101	1	Expansion Connect Memory High

Table 1 - MT90812 Memory Page Select

In multiplexed mode, the Memory Select bits in the Address Memory Select register (AMS) determine the page that is addressed. In non-multiplexed mode, the external address bits A9,A8,A7, determine the page that is addressed, eliminating the need to access the AMS register for memory page select.

The control registers, described in “Detailed Register Descriptions” on page 52, consist of one page of 128 locations. In multiplexed mode the control registers are accessed independent of the setting of the memory select bits in the AMS register, by setting the external address bit A7 to low. In non-multiplexed model the control registers are accessed by setting address bits A9, A8, and A7 to High. **The control register at location 61_H ($3E1_H$ in motorola non-muxed, 061_H in in multiplexed mode) must be initialized to 080_H.**

The addressing of the other blocks and memory pages are described below. Each Data and Connect Memory page consists of 128 locations, as shown in Table 2.

5.1.1 Addressing Memory Pages in Multiplexed Microport Mode

An MT90812 memory address, in multiplexed microport mode, consists of two portions. The higher order bits(3) originate from the Control Address Memory Select (AMS) register, which may be written to or read from via the Control Interface. The Control Interface receives address information at A7 to A0, data information at D7 to D0 and handles the microprocessor control signals $\overline{CS}$, $\overline{DTA}$, R/$\overline{W}$ and DS. The lower order bits(8) originate from the address lines directly. The address lines A6-A0, on the Control Interface, give access to the MT90812 registers directly if A7 is zero, or depending on the contents of AMS register, to the High or Low sections of the Connection Memory, or to the Data Memory.

5.1.2 Addressing Memory Pages in Non-Multiplexed Microport Mode.

A MT90812 memory address, in **non-multiplexed** microport mode, consists of A9 to A0. The higher order bits(3) originating from the external address bits A9,A8,A7, control which page is accessed. The Control Interface receives address information at A9 to A0, data information at D7 to D0 and handles the microprocessor control signals $\overline{CS}$, $\overline{DTA}$, R/$\overline{W}$ and DS. The lower order bits(7) originating from the external

address bits A6-A0, give access to the Control Registers if A9,A8,A7=111, or depending on the high order bits A9,A8,A7, to the High or Low sections of the Connection Memory, or to the Data Memory, as shown in Table 1.

5.2 Data Memory and Connect Memory

The Data Memory and Connect Memory Map, as shown in Table 2, illustrates the direct relationship between DM and CM for each of the channels. As described earlier in “Switching” on page 10, the data from the incoming TDM streams are written to Data Memory and the data is switched to the outgoing streams as programmed in CM.

	Address A6-A0	Memory Pages		
		Data Memory Pages	Connect Memory High Pages	Connect Memory Low Pages
Local Memory Page	00-1F	Sti0 32 Channels	Sto0 Outgoing Gain	Sto0 32 Channels
	20-3F	Sti1 32 Channels	Sto1 Outgoing Gain	Sto1 32 Channels
	40-5F	Tones(32), FSK	Tone Gain	(Not used)
	60-7F	Confout(15), unused(1) DCHout(1) unused(15)	Conf - Incoming Gain(15) IT - Incoming Gain(1) DCH - Incoming Gain(1) EDA -Incoming Gain(1) EDB -Incoming Gain(1) unused(13)	Conf Incoming Channel(15) Insertion Tone - Channel(1) DCH Incoming Channel(1) EDA -Incoming Channel(1) EDB -Incoming Channel(1) unused(13)
Expansion Memory Page	00-1F	Ei1 32 Channels	Ei1 Outgoing Gain	Ei1 32 Channels
	20-3F	Ei2 32 Channels	Ei2 Outgoing Gain	Ei2 32 Channels
	40-5F	Ei3 32 Channels	Ei3 Outgoing Gain	Ei3 32 Channels
	60-7F	Ei4 32 Channels	Ei4 Outgoing Gain	Ei4 32 Channels

Table 2 - Data Memory and Connect Memory Pages

In addition to holding the incoming data from the TDM streams, Data Memory holds the output of the other MT90812 blocks. This is described below in the following section. Expansion Memory page is used to hold the incoming data for the expansion bus TDM streams. Refer to “Use of Data Memory Reserved for Expansion Bus Streams” on page 15 for further description.

Connection Memory is used to specify the source for the outgoing channels and to connect the Conference, Energy Detect and DBRT blocks to incoming channels. In addition CM is used to specify the gain for the outgoing streams and the gain for the tones.

5.2.1 Local Data Memory

Table 3 details the mapping for Local Data Memory. The first block of 32 locations in Data Memory is used to store the 32 bytes of data from the STi0 stream. Locations 20-3F are used for the 32 bytes of data from the STi1 stream. The third block of 32 locations in Data Memory is used for output of the tone generator block as described in “Tone Generation” on page 42 The next 32-bytes consist of conference outputs(15), DCHout(1), and some unused locations(14).

Address A6-A0	Local Data Memory	Description
00-1F	Sti0 32 Channels	Sti0 32 Channels
20-3F	STi1 32 Channels	STi1 32 Channels

Address A6-A0	Local Data Memory	Description
40-59	DTMF Tones(26)	DTMF Tone generator output
59-5A	Tone Ringer or DTMF	Tone Ringer or Tone Generator output
5B-5E	Tones(4)	Tone generator output
5F	FSK or DTMF	FSK Transmitter output or Tone generator output
60-6E	CONFout(15)	Conference Output
6F	unused	
70	DCHout(1)	Output from the D-channel TX FIFO buffer. Allows D-channel TX buffer to be directed to any outgoing channel.
71-7F	unused(14)	unused(14)

Table 3 - Local Data Memory

5.3 Connection Memory use in Conferencing, Gain Control and specifying Incoming Sources for Energy Detect and DBR

Connection Memory is used to specify the source and gain for the 64 outgoing channels of STo0 and STo1 and the 128 outgoing channels of the expansion bus. Message mode, Minimum or Constant Delay and Output Enable are specified in CMH for each of these channels.

The conference circuit incoming channels are specified in CML 60-6E. The incoming conference gain, inversion bit and noise suppression are specified in CMH. Message mode, Minimum or Constant Delay and Output Enable are not used for locations 60-6E reserved for conference control. See the description of “Connection Memory High” on page 50. Channels are transferred from Data Memory with Constant Delay to the conference circuit.

Channels that can be included in a conference include; the 64 channels of STi0 and STi1, and the channels of the four expansion bus blocks. In fact any location in Local or Expansion Data Memory can be specified as in incoming conference source, including the 32 tones or the DBT output. The Conference Party Control registers specify which conference the channel is participating in, output attenuation levels, tone insertion and conference initialization. See the description of “Conference Party Control Register (CPC1-15)” on page 65.

CM is also used to connect the Energy detect and DBRT blocks to incoming channels. The incoming channels are specified in CML. The locations are listed below in Table 4. Channels can be transferred from Data Memory in either Minimum or Constant Delay to the Energy Detect and DBRT blocks as specified in CMH. CMH Message Mode and Output Enable bits are ignored for locations 70-72 of CM.

In addition CMH is used to specify the gain for the outgoing streams and the gain for the tones.

Hex Address A6-A0	Connect Memory Low	Description
60-6E	CONFin	Conference Incoming
6F	Insertion Tone	Insertion Tone Incoming Channel
70	DCH in(1)	Incoming channel to be transferred to the DBR FIFO.
71	EDA	Incoming channel to be transferred to the Energy Detect A block
72	EDB	Incoming channel to be transferred to the Energy Detect B block
72-7F	unused(14)	unused(14)

Table 4 - Connect Memory

Channels can be transferred from Data Memory in either Minimum or Constant Delay to the Energy Detect and DBRT blocks as specified in CMH. CMH Message Mode and Output Enable bits are ignored for locations 70-72 of CM.

In addition, CMH is used to specify the gain for the outgoing streams and the gain for the tones.

5.4 Use of Data Memory Reserved for Expansion Bus Streams

The use of the four blocks reserved for the expansion bus is dependent on the expansion bus mode set for the device. The two expansion bus modes, TDM Link and IDX Link, are described on page 8. In TDM Link mode, the four blocks are used according to the data rate set for the expansion bus. At 2.048 Mb/s the first 32 bytes, 00-1F, are used to store the incoming data. At 4.096 Mb/s the first 64 bytes, 00-3F are used. At 8.192 Mb/s all 128 locations, 00-7F, are used.

In IDX Link mode, 128 channels are read, 32 from EST1 and 96 from EST0. The positions that the MT90812 will read and write to the expansion bus are controlled by the EP1 and EP0 bits in Control Register B.

For example, a group of four MT90812 devices are labelled A, B, C, and D. The 128 channels on the expansion bus streams are identified as A1, B1, C1, D1, A2, B2, C2, D2,...., A128, B128, C128, D128. The MT90812 with EP1,EP0 set to 0,0 will read and write to EST0 and EST1 as listed in Table 5.

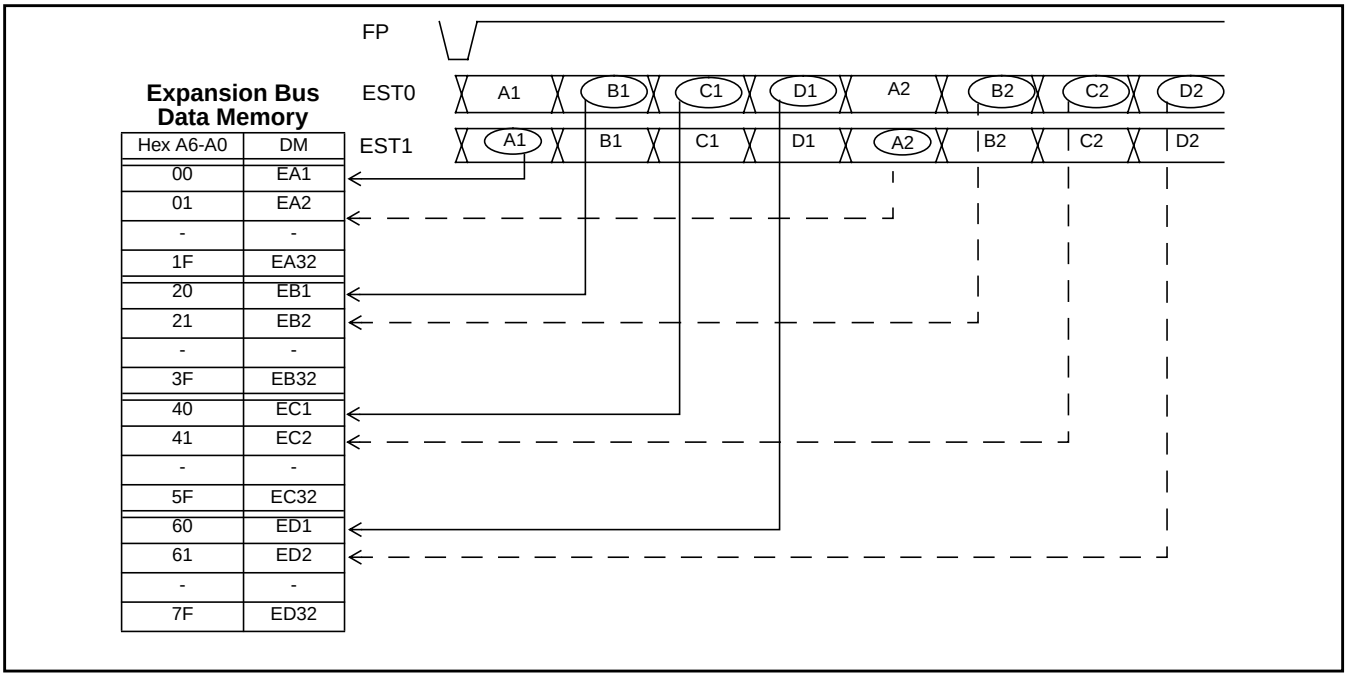
	Expansion Bus Channel (i=1,32)			
	Ai	**Bi**	**Ci**	**Di**
EST0	Write	Read	Read	Read
EST1	Read	Write	Write	Write

Table 5 - Expansion Bus Read/Write timeslots for IDX A

The MT90812 with EP1,EP0 set to 0,0 will output on EST0 during channel Ai and will read the next three channels Bi, Ci and Di. Channels Bi, Ci and Di go into Data Memory at Expansion Block 2, 3 and 4 respectively, as shown in Table 2. Expansion block 1 will contain incoming channels on EST1 sent to IDX A in timeslots labelled EA1,...,EA32 as shown in Figure 7 on page 9.

The MT90812 with EP1,EP0 set to 0,1 will output on EST0 and read EST1 during channel Bi and will read EST0 and output on EST1 for channels Ai, Ci and Di.

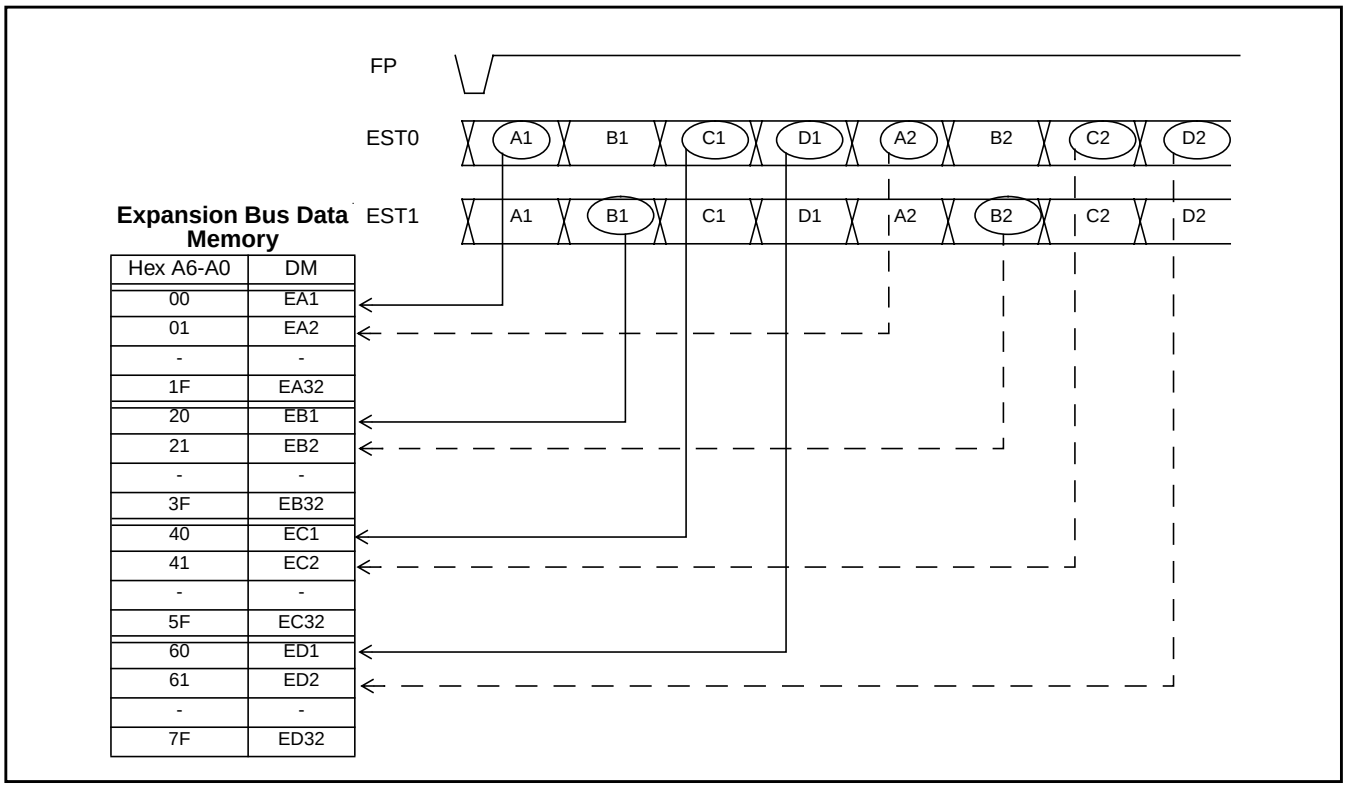
The memory map for the expansion bus timeslots are shown in the Figures 8 - 12 for each of the four settings of EP1 and EP0.



Expansion Bus Data Memory

Hex A6-A0	DM
00	EA1
01	EA2
-	-
1F	EA32
20	EB1
21	EB2
-	-
3F	EB32
40	EC1
41	EC2
-	-
5F	EC32
60	ED1
61	ED2
-	-
7F	ED32

Figure 8 - Data Memory Assignment for Expansion Bus Timeslots for EP1,EP0 = 00



Expansion Bus Data Memory

Hex A6-A0	DM
00	EA1
01	EA2
-	-
1F	EA32
20	EB1
21	EB2
-	-
3F	EB32
40	EC1
41	EC2
-	-
5F	EC32
60	ED1
61	ED2
-	-
7F	ED32

Figure 9 - Data Memory Assignment for Expansion Bus Timeslots for EP1,EP0 = 01

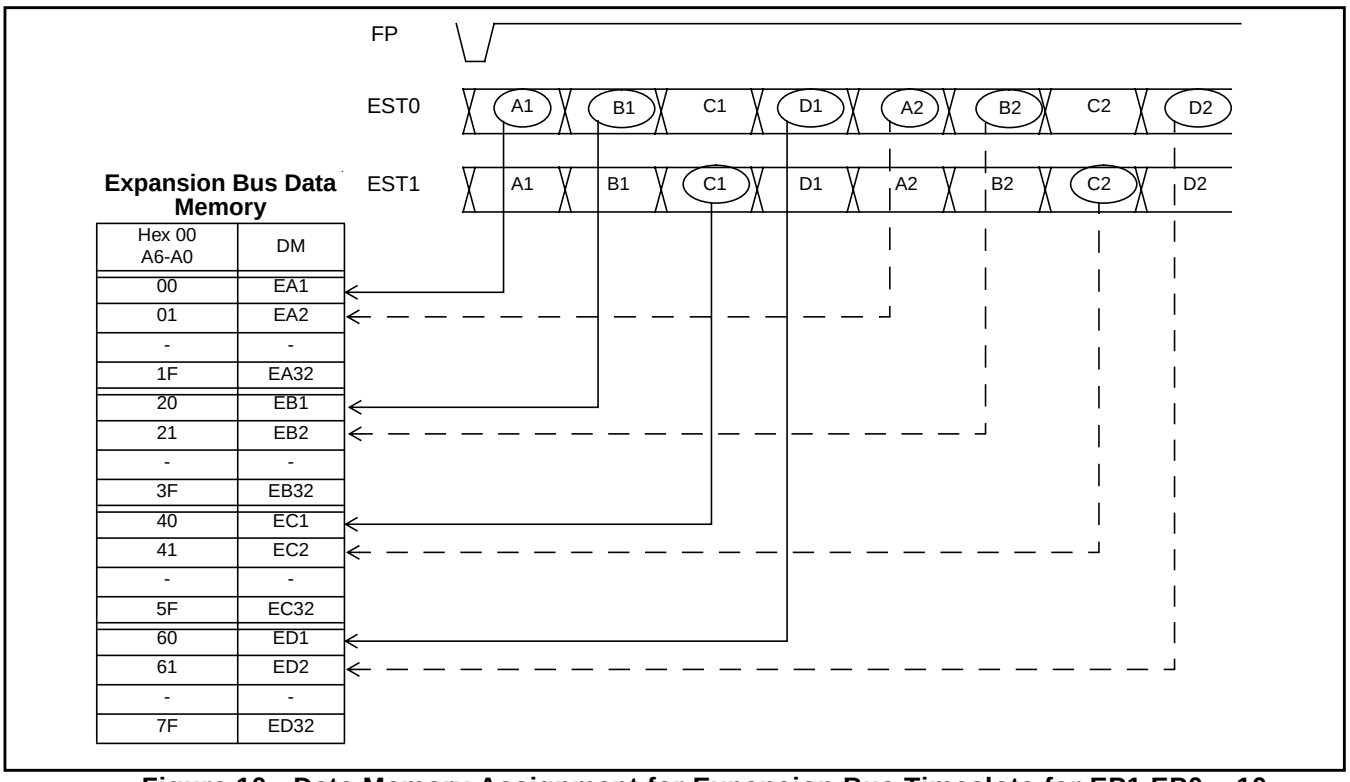


Figure 10 - Data Memory Assignment for Expansion Bus Timeslots for EP1,EP0 = 10

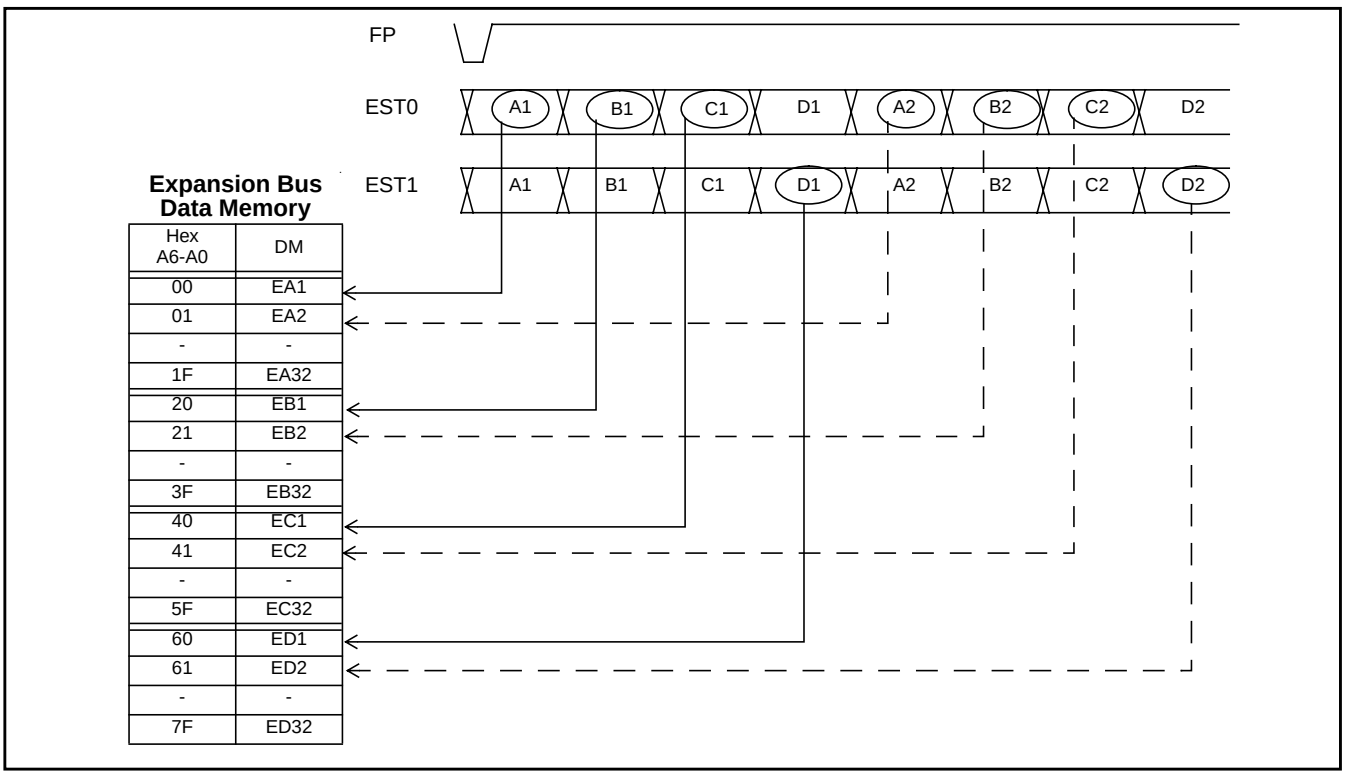


Figure 11 - Data Memory Assignment for Expansion Bus Timeslots for EP1,EP0 = 11

The previous diagrams illustrate the Data Memory allocation for the timeslots on EST0 and EST1. Fig. 12 illustrates Connect Memory allocation for the timeslots on EST0 and EST1. For the IDX A, which has EP0,EP1 = 00, the circled timeslots are read as incoming data to Data Memory. The other timeslots are outgoing

timeslots, where IDX A can either write to EST0 and EST1 during these channels or place EST0 or EST1 in high impedance.

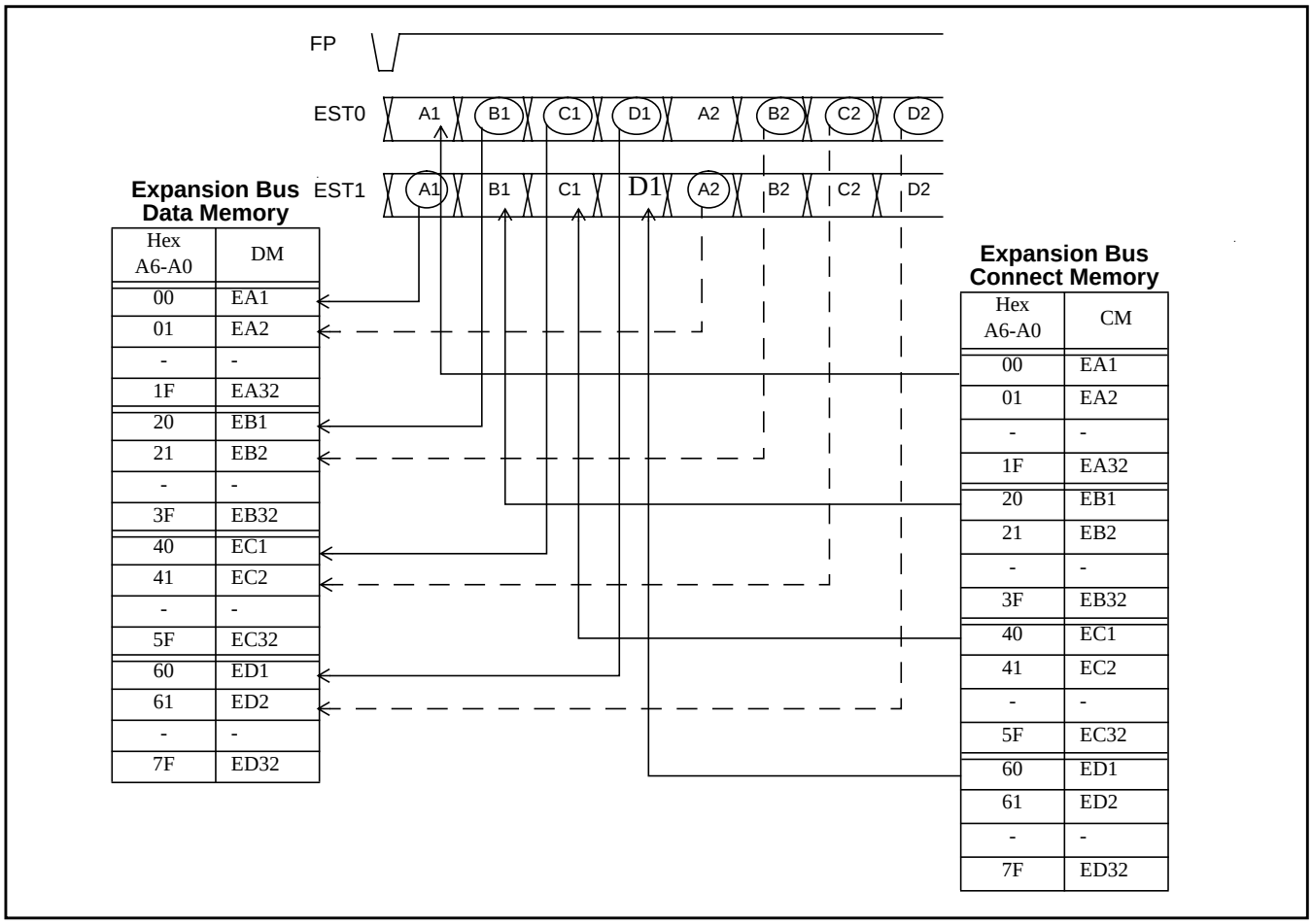


Figure 12 - Data Memory Assignment for Expansion Bus Timeslots for EP1,EP0 = 00

6.0 Conferencing

The conference block provides conference call capability in the MT90812 and supports a total of 15 parties, distributed over a maximum of 5 conferences. (i.e. 1x15 parties, 3x5 parties, 5x3 parties etc.). A/m-Law companded data from an incoming channel is converted to linear format, applied incoming gain, processed by a dedicated arithmetic unit, applied outgoing conference gain and stored in Data Memory in linear format. The output signal contains all the information of each channel connected in conference except its own.

For each of the 15 conference parties there is a Conference Party Control Register. The **Conference Party Control Register** contains the conference ID, start bit, insertion tone enable and outgoing channel attenuation. Refer to “Conference Party Control Register (CPC1-15)” on page 65.

The output for each conference is stored in 1 of 15 Data Memory locations which can be switched to any outgoing channel. For each of the 15 DM locations the corresponding Connect Memory Low byte is used to specify the incoming source channel.

The conference circuit incoming channels are specified in CML 60-6E. The incoming conference gain, inversion bit and noise suppression are specified in CMH. Message mode, Minimum or Constant Delay and Output Enable are not used for locations 60-6E reserved for conference control. See the description of “Connection Memory High” on page 50. Channels are transferred from Data Memory with Constant Delay to the conference circuit.

Channels that can be included in a conference include; the 64 channels of STi0 and STi1, and the channels of the four expansion bus blocks. In fact any location in Local or Expansion Data Memory can be specified as in incoming conference source, including the 32 tones or the DBT output.

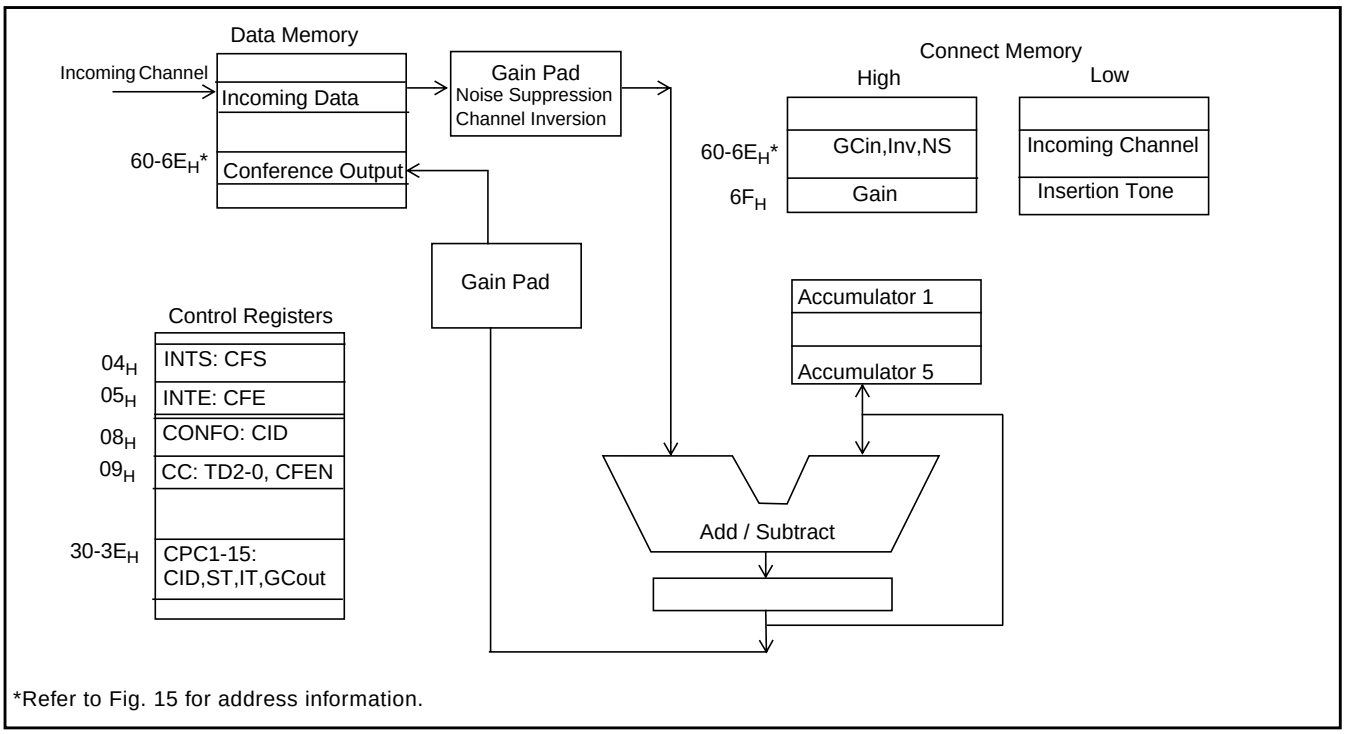


Figure 13 - Conference Circuit Block Diagram

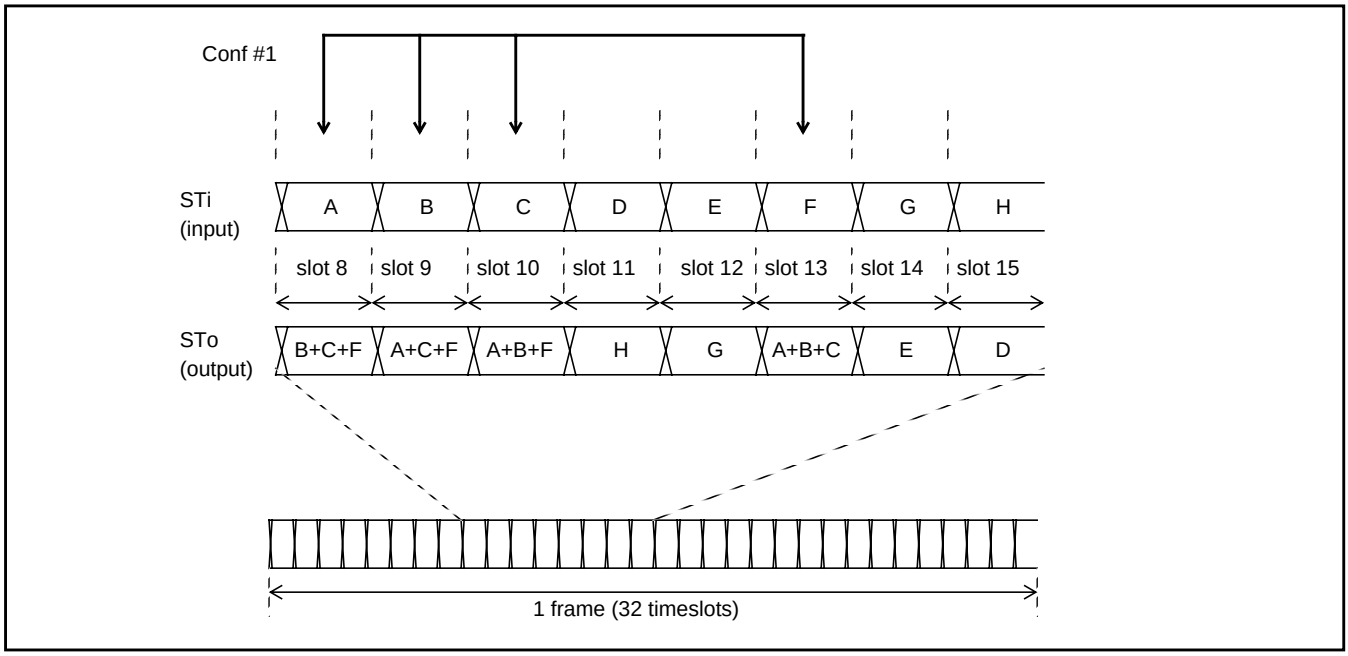


Figure 14 - Four Party Conference Example

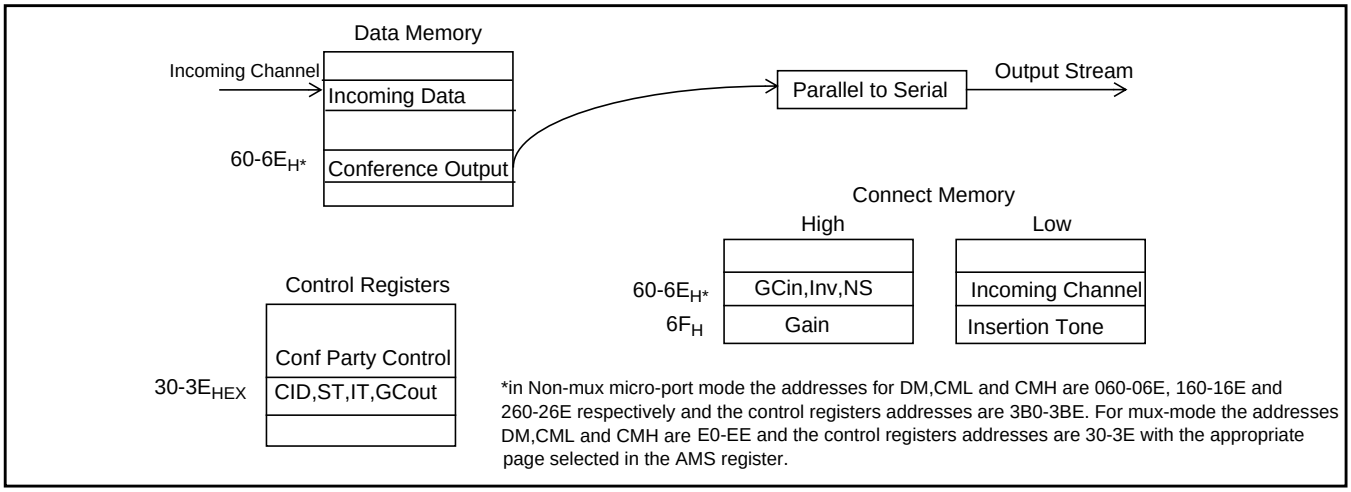


Figure 15 - Conference Control with Conference Party Control Registers and Connect Memory

6.1 Channel Attenuation

Channel Attenuation is provided on incoming and outgoing channels that are in a conference. The gain can range from +3 to -27 dB in steps of 1dB, as well as -∞ dB for the incoming PCM data and +0 to -9 dB in steps of 3dB for outgoing PCM data. If an overflow condition occurs, then the input from each channel in a conference can be independently attenuated, by setting the incoming channel attenuation bits in CMH for the specific conference party. The outgoing gain bits are in the Conference Party Control register.

6.2 Noise Suppression and Channel Inversion

Channel inversion and noise suppression bits are specified in Connect Memory High for locations 60-6E$_H$.

When noise suppression is enabled for a specific input channel, then the PCM bytes for this channel, when below the selected threshold level, are converted to PCM bytes corresponding to the minimum PCM code level before being added to the conference sum. The four threshold levels available correspond to the first, fifth, ninth, and sixteenth step of the first segment. These are 1/4096, 9/4096, 16/4096, and 32/4096 with respect to full scale A-law, and 1/8159, 9/8159, 16/8159, and 32/8159 with respect to full scale ulaw. The threshold level is set using the threshold bits NS1, NS0.

The inversion bit allows for every other channel in a conference to be inverted. This reduces noise due to reflections and line impedance mismatch.

6.3 Tone Insertion

As a party is added to a conference, if the insertion tone bit (IT) is set, all channels connected in a conference will have the tone added to the conference output. This allows for conference users to be informed of a new party being added to the conference, or to be reminded that they are in a conference.

The DM address of the desired tone must be programmed at location 6F$_H$ of CML, (16F$_H$ non-mux mode, EF$_H$ for mux-mode addressing). The tone source may be from any location in DM, including any of the 32 tones from the Tone Generation block. The PCM data from the specified Data Memory location will be added to the conference output for a specified tone duration.

The tone duration is specified in the Conference Control Register (CC). Refer to Section 22.10 for a description of the Conference Control Register (CC). The tone duration can be set from 0.125 to 1.0 seconds in steps of 0.125 seconds. The tone duration is from the time the party is added to the conference by writing the Conference Party Control Register.

6.4 Conference Overflow

A peak clipping indicator identifies the conference causing conference bridge overflow whenever a 14-bit two complement overflow occurs[1]. Once a conference bridge overflow occurs an interrupt is asserted, the Conference Overflow bit in the Interrupt Status Register (INTS) is set and the conference ID is placed in the Conference Overflow Status Register (CONFO). Refer to the CONFO register description on page 59.

Reading the Interrupt Status Register (INTS) will clear the Conference Overflow bit. A conference overflow will not trigger an interrupt until the conference overflow bit is cleared. The conference overflow interrupt is maskable using the Interrupt Enable Register (INTE). The conference interrupt mask does not disable updates of the CONFO register. The Conference ID in this register will not be updated again until it is reset. The register is reset following a read of the register or resetting the conference block or Mt90812 device.

Note 1 - The overflow limit is the same whether Ulaw or Alaw companding is used. Following gain adjustment companding will then implement clipping to the Ulaw and Alaw max values of 8031 and 4032 respectively.

6.5 Starting a New Conference

In order to initiate a conference, the Conference Party Control register as well as Connection Memory Low/ High must be programmed. Setting the **ST** bit for the **first** party programmed for a conference will remove any other parties that may have been previously programmed for that conference. The following steps outline initialization of a conference.

Conference Block Initialization

1) Perform MT90812 reset or conference reset. The Conference Party Control registers are reset and all conference ID numbers are set to null.
2) Disable the conference overflow interrupt until after a conference is set up. Set CFE bit LOW in the Interrupt Enable Register (INTE).
3) Enable the conference block by writing to the conference control register, setting CFEN=1 and setting the tone duration.
4) Set up Tone Insertion: program the tone by writing the tone coefficient registers if a different programmable tone is required. Refer to “Tone Generation” on page 42 Identify the tone by writing CML location 6F with the DM address of the Tone. Write CMH location 6F with the gain setting for the insertion tone.

Conference Party Initialization

5) Write CMH with the Incoming gain, inversion bit and noise suppression for the first party.
6) Write CML with the Incoming channel DM address for the first party.
7) Write the Conference Party Control register with a conference ID from 1-5. Set the **ST** bit for the **first** party programmed for a conference. Setting the ST bit will remove any other parties that may have been previously programmed for that conference. Set the Insertion Tone bit and outgoing conference gain control required.
8) Write CML of the Incoming channel with DM address of the conference output location ($60\text{-}6E_H$). Write CMH of the location with the required outgoing gain if it has not been previously set. Also set the OE bit.
9) Repeat steps 5 to 8 for each additional party in the conference.
10) Enable the conference overflow interrupt if required, by setting CFE, bit 1 in the Interrupt Enable Register (INTE). Read the CONFO register to ensure it is reset allowing the next overflow to update the conference ID value.

6.6 Removing a channel from a Conference

Setting the Conference ID number, in Conference Party Control register, to ‘0’ will disconnect the selected channel from the conference. Once the selected channel is removed from the conference, the Output Enable

(OE) bit of Local (or Expansion depending on the output stream number) Connect Memory High must be set to 0 in order to put the output driver of the corresponding stream into high-impedance state during the selected timeslot.

7.0 Gain Control

Gain Control is provided on the outgoing channels, with a range of +3 to -27 dB in steps of 1dB, as well as -∞dB. If a channel is in a conference, incoming and/or outgoing gain control is provided, with a range of 0 to -9 dB in steps of 3 dB. Refer to Section 6.0 for a description of gain control for a conference.

Outgoing gain control of +3 to -27 dB in steps of 1dB, as well as -∞dB is also provided on the 32 tones from the Tone generator.

The gain for each outgoing channel is specified in Connect Memory High. Refer to “Connection Memory High” on page 50. There are five bits G4-G0 which are used to set the gain. If 0 dB value is selected then the gain control circuitry is bypassed. Otherwise the 8 bit PCM value for the outgoing channel is read from Data Memory, expanded to a 14 bit linear PCM value, multiplied by the appropriate gain factor, and compressed to an 8 bit PCM value, before being output on the outgoing serial stream.

The output of the tone generator and conference blocks are multiplied by the gain factor specified for the tone or conference party and stored as a 14 bit linear PCM value in Data Memory. When the outgoing channel is connected to a tone or conference output location, the 14 bit linear PCM value is then read from DM, multiplied by the gain factor specified for the outgoing channel, and compressed to an 8 bit PCM value, before being output on the outgoing serial stream.

8.0 Delays Through the MT90812

A delay results when transferring channel information from a MT90812 local input stream to an output stream. This delay varies according to the switch mode programmed in the CST bit of connect memory high; i.e. Minimum or Constant Throughput Delay Mode.

8.1 Minimum Delay Mode (CST bit=0)

In Minimum Delay Mode the delay is dependent on the combination of source and destination channels, the input and output streams and the data rate of the expansion bus.

Data transfers between streams operating at the same data rate (i.e. Sti1 to Sto1, Est1 to Est0, etc.) can be described as follows. Channel information for a particular timeslot **n** from the input stream is sent to Data Memory in timeslot **n+1**. Channel information is queued for an output channel **n** in timeslot **n-1**. Thus, information entering the MT90812 from timeslot **n**, cannot be transmitted in the same timeslot **n** or timeslot **n+1**, without a frame delay. Information switched to a timeslot of **m=n+2** or later will be switched within the same frame. The relationship that is required between incoming and outgoing timeslots are shown in Table 6. For all but four cases, if the outgoing timeslot, m, is greater than or equal to n+2, the data is switched within the same frame. The throughput delay is m-n timeslots.

There are four cases where there are data transfers between streams operating at different data rates. This occurs when the expansion bus is running at 4.096Mb/s or 8.192 Mb/s and the data is transferred between the expansion bus and either Sto0 or Sto1. The channel numbers range from 0 to 31 for a stream operating at 2.048Mb/s, and from 0 to 63 and 0 to 127 for streams operating at 4.096Mb/s and 8.192 Mb/s, respectively.

Source and Destination Streams	Expansion Bus Data Rate		
	2.048 Mb/s	4.096 Mb/s	8.192 Mb/s
Sti0/1 -> Sto0/1	m>=n+2	N/A	N/A
Est0/1 -> Est0/1		m>=n+2	
Sti0/1 -> Est0/1		m>=2n+3	m>=4n+5
Est0/1 -> Sto0/1		m>=(n+3)/2	m>=(n+5)/4

Table 6 - Output Channels for Minimum Delay

The output channel number m, specified for minimum delay in these four cases account for there being two 4.096Mb/s channels and four 8.192Mb/s channels for every one 2.048Mb/s channel.

Table 7 lists the condition required for a throughput delay of less than one frame period, the throughput delay if this condition is met and the throughput delay expressed in timeslots when switching is made in the following frame. For cases where there are different data rates the delay is expressed in timeslots associated with the fastest data rate. i.e. with the source channel from Est1 (@8Mb/s) and destination channel on STo1 (@2Mb/s) the delay is expressed in 8Mb/s timeslots. If the incoming 8Mb/s channel, n = 119, outgoing 2Mb/s channel m =31, then the delay = 4m-n = 4(31)-119= five 8Mb/s timeslots. If m=1 the delay=128-(n-4m)=128-(119-4)=thirteen 8Mb/s timeslots.

Source and Destination Streams	Input channel, n, range	Output channel, m, range	Condition for switching within same frame	Throughput Delay within same frame	Throughput Delay if condition not met
Sti0/1 -> Sto0/1	0-31	0-31	m>=n+2	m-n $t.s_2$.	32-(n-m) $t.s_2$.
Est0/1 -> Est0/1 2.048 Mb/s	0-31	0-31	m>=n+2	m-n $t.s_2$.	32-(n-m) $t.s_2$.
Est0/1 -> Est0/1 4.096 Mb/s	0-64	0-64		m-n $t.s_4$.	64-(n-m) $t.s_4$.
Est0/1 -> Est0/1 8.192 Mb/s	0-127	0-127		m-n $t.s_8$.	128-(n-m) $t.s_8$.
Sti0/1 -> Est0/1 2.048 Mb/s	0-31	0-31	m>=n+2	m-n $t.s_2$.	32-(n-m) $t.s_2$.
Sti0/1 -> Est0/1 4.096 Mb/s	0-31	0-64	m>=2n+3	m-2n $t.s_4$.	64-(2n-m) $t.s_4$.
Sti0/1 -> Est0/1 8.192 Mb/s	0-31	0-127	m>=4n+5	m-4n $t.s_8$.	128-(4n-m) $t.s_8$.
Est0/1 2.048 Mb/s -> Sti0/1	0-31	0-31	m>=n+2	m-n $t.s_2$.	32-(n-m) $t.s_2$.
Est0/1 4.096 Mb/s -> Sti0/1	0-64	0-31	m>=(n+3)/2	2m-n $t.s_4$.	64-(n-2m) $t.s_4$.
Est0/1 8.192 Mb/s -> Sti0/1	0-127	0-31	m>=(n+5)/4	4m-n $t.s_8$.	128-(n-4m) $t.s_8$.

Table 7 - Throughput Delay for Minimum Delay Mode

Notes: t.s. = time-slot. $t.s_2$. =2Mb/s t.s. = 3.9 us. $t.s_4$. =4Mb/s t.s.=1.95 us. $t.s_8$.=8Mb/s t.s.=0.975 us.
Delays are measured in timeslots and at the point in time from when the input channel is completely shifted in and when the output channel is completely shifted out.

8.2 Constant Delay Mode (CST bit=1)

In Constant Delay mode, channel integrity is maintained by making use of a multiple Data Memory buffer technique. The input channels written in any of the buffers during frame N will be read out during frame N+2. Table 8 lists the throughput delay for Constant Delay mode for all combinations of source and destination streams.

Source and Destination streams	Input channel, n, range	Output channel, m, range	Throughput Delay
Sti0/1 -> Sto0/1	0-31	0-31	2x32-(n-m) $t.s_2$.
Est0/1 -> Est0/1 2.048 Mb/s	0-31	0-31	2x32-(n-m) $t.s_2$.
Est0/1 -> Est0/1 4.096 Mb/s	0-64	0-64	2x64-(n-m) $t.s_4$.
Est0/1 -> Est0/1 8.192 Mb/s	0-127	0-127	2x128-(n-m) $t.s_8$.
Sti0/1 -> Est0/1 2.048 Mb/s	0-31	0-31	2x32-(n-m) $t.s_2$.
Sti0/1 -> Est0/1 4.096 Mb/s	0-31	0-64	2x64-(2n-m) $t.s_4$.
Sti0/1 -> Est0/1 8.192 Mb/s	0-31	0-127	2x128-(4n-m) $t.s_8$.
Est0/1 2.048 Mb/s -> Sti0/1	0-31	0-31	2x32-(n-m) $t.s_2$.
Est0/1 4.096 Mb/s -> Sti0/1	0-64	0-31	2x64-(n-2m) $t.s_4$.
Est0/1 8.192 Mb/s -> Sti0/1	0-127	0-31	2x128-(n-4m) $t.s_8$.

Table 8 - Throughput Delay for Constant Delay Mode

Notes: t.s. = time-slot. $t.s_2$. =2Mb/s t.s. = 3.9 us. $t.s_4$. =4Mb/s t.s.=1.95 us. $t.s_8$.=8Mb/s t.s.=0.975 us.
Delays are measured in timeslots and at the point in time from when the input channel is completely shifted in and when the output channel is completely shifted out.

8.3 Delays in Conferencing

In a conference the data is read from Data Memory and transferred to the conference block as in constant delay mode, with a 2 frame delay. If the incoming data is in frame N, then within the first half of frame N+2 the conference output is calculated and stored in the conference output locations in Data Memory. The conference output data is then switched to the outgoing data channel in Minimum Delay mode.

The minimum delay possible in a conference is one frame + two 2Mb/s-timeslots = 34 2Mb/s-timeslots. The maximum delay possible is approximately 2 frames + 1.5 frames + two 2Mb/s-timeslots = 82 2Mb/s-timeslots.

9.0 Timing and Clock Control

The MT90812 clock control circuitry selects one of five possible input clock and frame pulse references. The input clock can be either 4.092, 8.192, or 16.384 MHz as described in Section 9.1, “Input Timing Reference”. Fig. 16 shows the Clock Control Functional diagram. The clock control circuitry provides an internal master clock of 8.192 MHz, generates 2.048, 4.096, 8.192, and 10.24 MHz output clocks, F4 and F8 frame pulse signals, as well as the serial interface timing for STi/o0, STi/o1 and EST0/1 serial streams. These signals are either generated directly from the input clock source or from an on-chip analog PLL.

The on-chip analog PLL may be used to generate 2.048, 4.096, 8.192, and 10.24 MHz clocks. The PLL operates in Master and Slave modes. Master mode provides more jitter attenuation while Slave mode minimizes Phase delay. The PLL can provide the required 4.096 and 10.24 MHz clocks (C4 and C10) to be supplied to the MT9171/72 DNIC devices. The C4 and C10 clocks meet the requirement that they be frequency locked and maintain a jitter of less than or equal to 15ns with respect to each other, while maintaining at least 40/60 duty cycle for C10o. Refer to Section 9.3.1, “Master and Slave PLL Modes”.

Multiple IDX systems are supported by allowing the IDX to either drive or receive an 8.192 MHz clock. The master IDX in the system may supply C8 while the slave IDX derive their timing from the master. In a multi-chassis application a slave IDX may be required to generate its own C10. C8 is distributed between master and slave IDX devices and the PLL is then used to phase lock C10, C4 and C2 to the C8 input.

The MT90812 Expansion Bus can be supported with either an 8.192 MHz or 16.384 MHz clock when operating at 8.192 Mb/s. When the input clock source is selected as 16.384 MHz either HMVIP and non-HMVIP mode may be used.

In a multiple IDX system the slave IDX devices are supplied C8 from a master IDX. A watchdog timer on the IDX allows the slave IDX to monitor the C8 input. In the event of the loss of the C8 clock the slave IDX can be switched to be master IDX and supply C8 to the system. This provides redundancy for the clock source allowing IDX operation to remain independent of the other IDX devices if necessary.

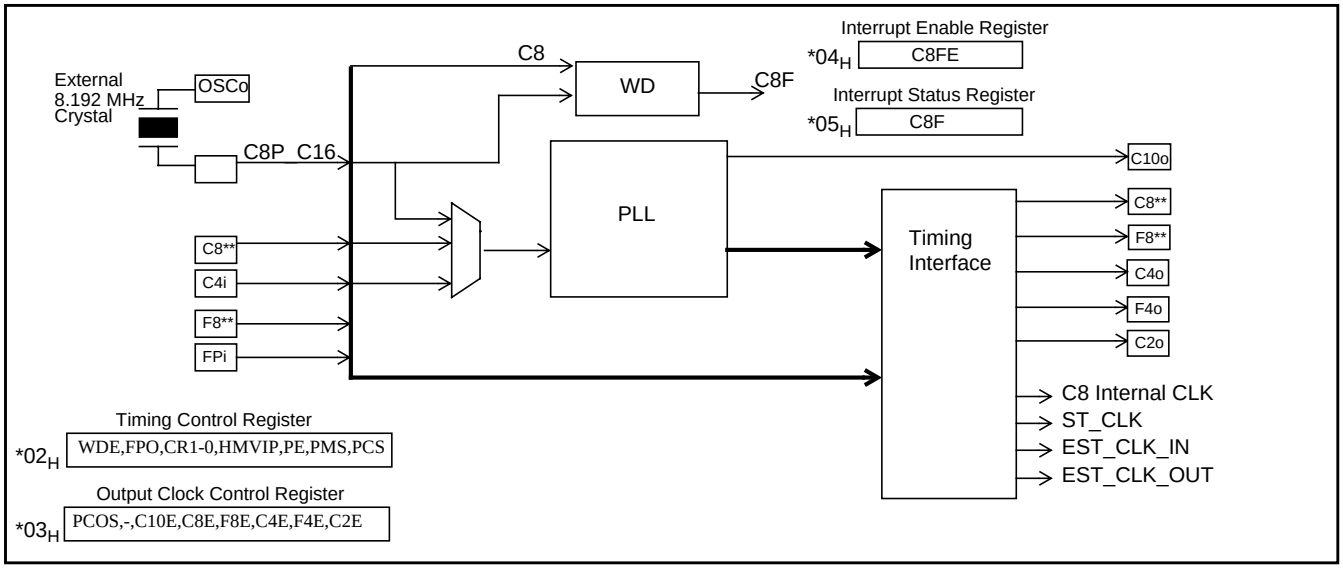


Figure 16 - Clock Control Functional Diagram

*Non-mux mode addresses for TCR, OCCR, INTE and INTS are 382_H, 383_H, 384_H and 385_H, respectively.
**C8 and F8 are bi-directional pads. They are used as inputs in C8 timing mode, otherwise as output pads.

9.1 Input Timing Reference

The Input Timing Reference is selected setting CR1-0 and HMVIP bits in the Timing Control Register (TC) described on page 55. One of five possible clock and frame pulse references, C4/F4, C8/F8, C8P, or C16/F8, C16/HMVIP, can be selected, as listed in Table 9.

CR1,0	HMVIP	Clock Reference	Frame Pulse Reference
00	x	C4	FPi(F4)
01	x	C8	F8i
10	x	C8P (default)	No Frame Pulse
11	0	C16 Non-HMVIP	FPi (F8)
11	1	C16 HMVIP	FPi(F4)

Table 9 - Clock Modes

The MT90812 requires at least an 8.192 MHz clock internally. When the C4 input clock is selected the 8.192 MHz clock is derived from the PLL. C4 is not a valid clock reference when the PLL is disabled.

The MT90812 defaults to C8P input clock reference when reset. When C8P is selected as the input clock reference the clock oscillator pins C8P_C16 and OSC can be used with an external 8.192 MHz crystal or pin C8P_C16 can be used directly as a clock input with OSC left unconnected. Refer to Section 9.5, “C8P Pin Timing Source”. When C8P is selected, no frame pulse is used and the MT90812 generates F4o and F8o. F4o and F8o can be disabled by setting F4E and F8E bits low in the Output Clocking Control Register (OCC).

With C16 as the clock reference the HMVIP Frame Alignment Interface can be selected with the HMVIP bit in the Timing Control Register (TC).

9.2 Serial Data Interface Timing

ST-Bus, GCI or HMVIP Serial Data Interface timing modes are supported on the serial streams of the MT90812. The two local streams, STi/o0, STi/o1 operate at 2.048 Mb/s. The Expansion Bus can operate in two modes, TDM Link and IDX Link, as described in Section 3.0. In TDM Link, EST0/1 can operate at 2, 4 or 8 Mb/s. In IDX Link, EST0/1 operates at 8 Mb/s. The incoming 8kHz frame pulse used for frame synchronization for both local and expansion bus streams can be either ST-Bus, GCI or HMVIP format. In all timing modes except C16-HMVIP mode, the MT90812 automatically detects the presence of an input frame pulse on F8 or FPi pins and identifies it as either ST-Bus or GCI. For C16-HMVIP mode, the frame pulse must be in ST-Bus format.

9.2.1 Local Streams, STi/o0 and STi/o1

For STi/o0, STi/o1 2.048 Mb/s streams a 4.096 MHz clock is used for the serial interface timing and is generated in the Clock Control block. The PCS bit in the TC register selects the source of this clock as either derived from the input clock or from the PLL and is described below. In ST-Bus format, every second edge of the 4.096 MHz clock marks the bit boundary and the data is clocked in on the rising edge the 4.096 MHz clock, three quarters of the way into the bit cell, see Figure 40 on page 86. In GCI format, every second rising edge of the 4.096 MHz clock marks the bit boundary and data is clocked in on the falling edge of the 4.096 MHz clock at three quarters of the way into the bit cell, see Figure 41 on page 87.

9.2.2 Expansion Bus, EST0/1

The Expansion Bus can run at 2, 4 or 8Mb/s. In TDMLink, bits EP0 and EP1 of the TC register define the data rate. In IDX Link the date rate is always 8Mb/s. In both modes the timing is similar to that used for ST0/1 streams when double rate clock is used. For example at 2, 4 and 8 MB/s rates, CLK is 4.096, 8.192 or 16.384 MHz, respectively. Refer to Figure 40 on page 86 for ST-Bus timing and Figure 41 on page 87 for GCI.

When C8 timing mode is selected, the incoming data, on the Expansion bus running at 8Mb/s, is clocked at either the 1/2 bit time or 3/4 bit time. Fig. 42 and Fig. 43 shows the expansion bus timing with the data clocked at the 1/2 bit time for ST-Bus and GCI, respectively. Without the presence of a 16.384 MHz input clock reference, the PLL must be used to clock data at the 3/4 bit time. The PLL must be enabled and the PCS bit set to 1. For further description see Section 9.2.5.

9.2.3 HMVIP Frame Alignment

When C16 timing mode is selected, the HMVIP bit in the Timing Control Register (TC) enables the HMVIP Frame Alignment Interface. The C8P_C16i input must be at 16.384 MHz, C4i must be 4.096MHz. C4i is used to sample the 8kHz ST-Bus frame pulse. The timing relationship between the two clocks and the frame pulse is defined in Figure 44 on page 88. In C16 Non-HMVIP mode frame synchronization is made using F8. C16/F8 timing is shown in Figure 37 on page 84 for ST-Bus and Figure 38 on page 84 for GCI.

9.2.4 Output Clock and Frame Pulse Signals

The MT90812 generates C2o, F4o, C4o, F8, C8, and C10o signals. These outputs are enabled by setting the corresponding bits in the Output Clocking Control Register (OCC) described on page 56. F8 and C8 signals are bi-directional pins. When the C8/F8 input clock reference mode is selected they are used as inputs and the C8E and F8E output enables of the OCC register are ignored.

The MT90812 generates C4o, F4o, C8, and F8 signals in either ST-Bus or GCI formats as selected by the FPO bit in the Timing Control Register (TC). This selection is independent of the incoming frame synchronization used.

9.2.5 Selecting Timing from the Input Clock Reference or from the PLL

As mention above, the clocks used for the local and expansion bus streams can be derived directly from the input clock reference or from the PLL. Two bits are used to control this, the **PLL Clock Select** (**PCS**) bit in the TC register and the **PLL Clock Output Select** (**PCOS**) bit in the Output Clocking Control Register (OCC).

Referring to Figure 16, “Clock Control Functional Diagram,” on page 25, the clock used for the STi/o0 and STi/o1 serial streams, is STCLK. The clocks used for clocking in data and clocking out data on the Expansion Bus are EST_CLK_IN and EST_CLK_OUT, respectively.

With PCS set high, EST_CLK_IN, STCLK and C4o are generated from the PLL. Otherwise they are derived from the input clock. With the PCS set high, C4o and C10 are both supplied from the PLL for clock supply to the MT9171/72/73 DNIC devices. The other advantage with PCS high allows for clocking in data at three quarters into the bit cell on the 8Mb/s Expansion Bus.

With PCOS set high, EST_CLK_OUT and C8 (output) are generated from the PLL. Otherwise, they are derived from the input clock. For example, with PCOS=0 in C8P timing mode, C8P is used to generate C8 (output) and in C16 timing modes, C8 (output) is C16 divided by 2. When C4F4 is used as the timing reference, EST0/1, 4 and 8 Mb/s timing, as well as F8o and C8o, are generated from the PLL independent of the PCS and PCOS settings.

9.3 Phase Lock Loop (PLL)

As shown in Fig. 17, the PLL of the MT90812 consists of a Phase and Frequency Detector, Loop Filter, Voltage Controlled Oscillator and Divider Circuit.

The **Phase and Frequency Detector** compares the reference signal selected by CR0-1 bits in the TC register, with the feedback signal from the Divider circuit, and provides an error signal corresponding to the phase difference between the two. This error signal is passed to the Loop Filter.

The **Loop Filter** is a second order low pass filter which operates in two modes, Master and Slave. These modes are described in Section 9.3.1. The **Voltage Controlled Oscillator** receives the filtered signal from the Loop Filter and based on its value, generates a corresponding digital output signal.

The **Divider** circuit uses the VCO output to generate five clock outputs, C10, C8, C8_75, C4 and C4_75. C10, C8 and C4 are 10.29 MHz, 8.192 MHz and 4.096 MHz signals respectively. C8_75 and C4_75 are 8.192 MHZ and 4.096 MHz signals with a 75/25% duty cycle. These two clock signals are used in the Serial Interface Circuit for the Expansion Bus. Refer to Section 9.2.

The PLL is enabled with PE bit set in the Timing Control Register (TC). With the PLL off, C10 is disabled and C4 as an input clock reference is not valid.

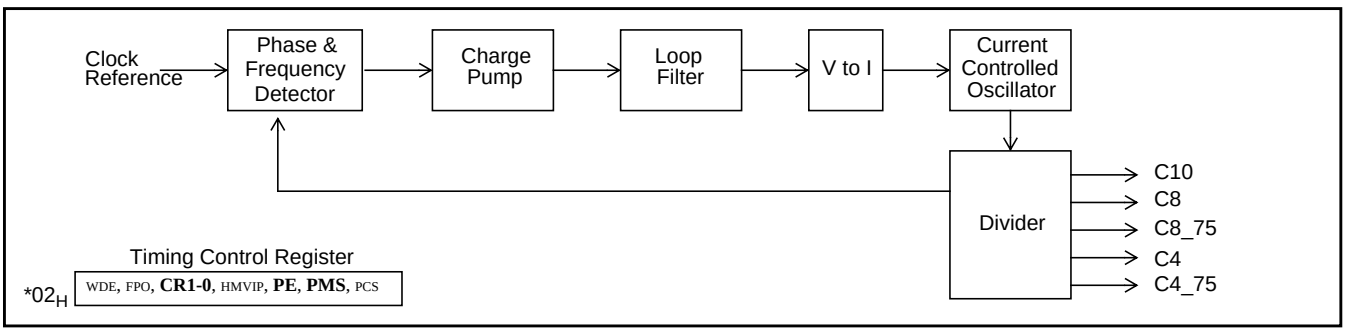


Figure 17 - PLL Block Diagram

9.3.1 Master and Slave PLL Modes

The PLL Master/Slave (PMS) bit in the TC register selects the PLL mode. In Master mode the PLL loop filter is selected to minimize the magnitude of any one clock correction. This preserves the C10o 40/60 duty cycle given the input jitter as specified on page 95. For example this provides the 10.24 MHz clock required for DNIC operation with up to 32ns of clock correction on the input clock once per 125us frame. Refer to Intrinsic Jitter for Master and Slave modes on page 93 and typical Input to Output Jitter Transfer for Master Mode on page 93.

In Slave mode the PLL loop filter is selected to minimize the phase delay on the output clock with respect to the input clock reference. The typical Input to Output Jitter Transfer for Slave Mode is shown on page 94. In Slave mode the Loop Filter ensures a phase difference of less than 15 ns. This is assuming an input clock reference from the Master IDX, where the Master IDX has up to 32 ns of clock correction on the input clock once per 125 us. In an application where the clock reference does not require jitter attenuation the PLL can be used in Slave mode. For example in a multi-IDX application the Master IDX could have its PLL in Master Mode, and generate clocks for the other IDX devices. Setting the PLLs of these Slave IDX devices in Slave mode lessens phase delay while taking advantage of the clock source from the Master IDX. Note: the Master IDX PLL maybe placed in Slave mode as well if jitter attenuation is not required.

9.4 Watchdog Timer

A watchdog timer monitors C8 input. This requires the presence of a 8.192 MHz clock at C8P_C16. In the event of the loss of the C8 clock an interrupt is generated and the C8F bit in the Interrupt Status Register (INTS) is set. The system can service the interrupt and maintain operation of the MT90812 by switching clock input reference from C8 (CR0-1=01) to C8P (CR0-1=10) and enable the MT90812 to supply C8 output.

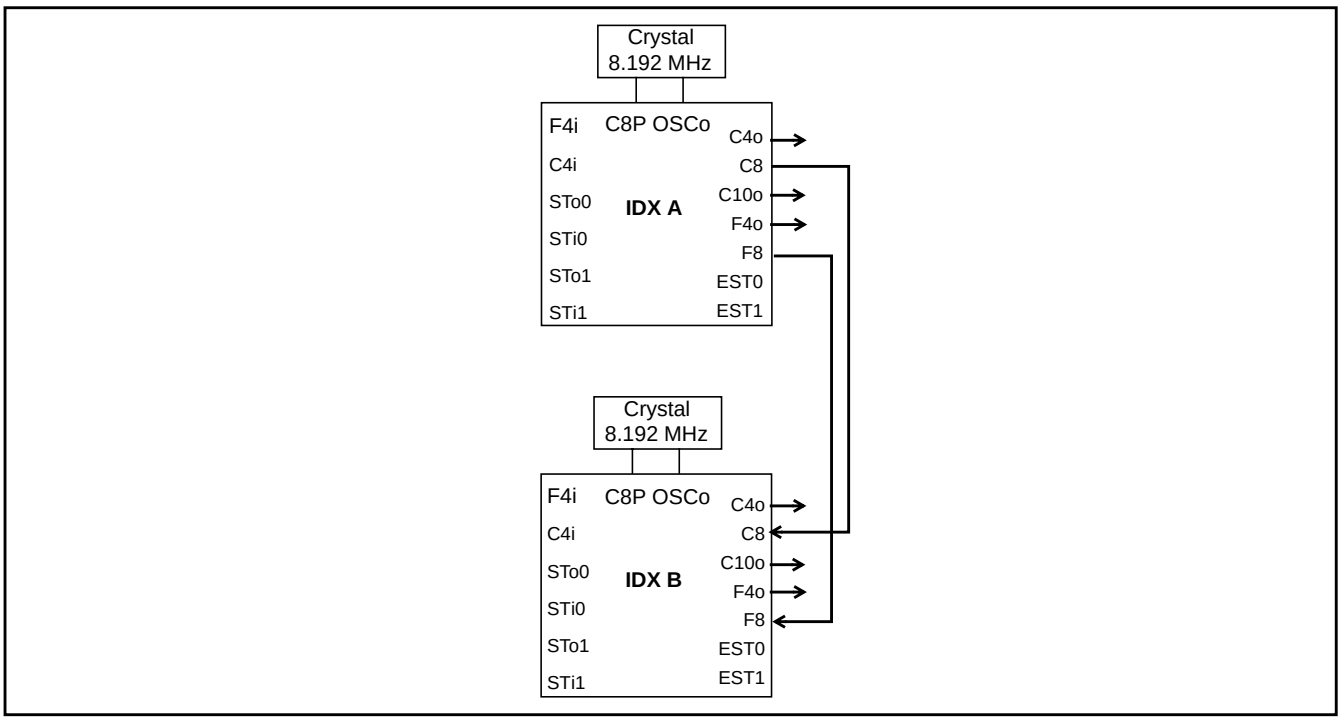


Figure 18 - Watchdog Configuration

This provides redundancy for the clock source in a multiple IDX system. The watchdog timer is enabled by setting WDE bit in Timing Control Register (TC).The interrupt is enabled by setting C8FE bit in Interrupt Enable Register (INTE).

9.5 C8P Pin Timing Source

The MT90812 can use either a clock or crystal, connecting to pins C8P_C16i and OSCo, as a reference timing source.

9.5.1 Clock Oscillator

Fig. 19 shows a 8.192MHz clock oscillator, with 32 ppm tolerance, directly connected to C8P_C16i pin of the MT90812. The output clock should be connected directly (not AC coupled) to the C8P_C16i pin, and the OSCo output should be left open.

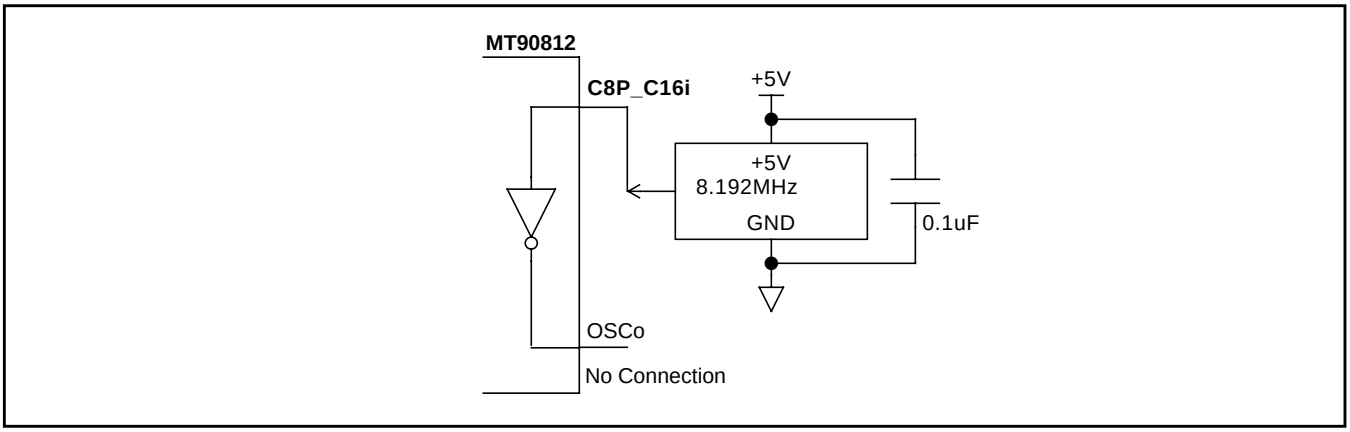


Figure 19 - Clock Oscillator Circuit

9.5.2 Crystal Oscillator

Alternatively, a Crystal Oscillator may be used. A complete oscillator circuit made up of a crystal, resistor and capacitors is shown in Fig. 20.

The accuracy of a crystal oscillator depends on the crystal tolerance as well as the load capacitance tolerance. Typically, for a 8.192MHz crystal specified with a 32pF load capacitance, each 1pF change in load capacitance contributes approximately 9ppm to the frequency deviation. Consequently, capacitor tolerances, and stray capacitances have a major effect on the accuracy of the oscillator frequency.

The trimmer capacitor shown in Fig. 20 may be used to compensate for capacitive effects. If accuracy is not a concern, then the trimmer may be removed, the 39pF capacitor may be increased to 56pF, and a wider tolerance crystal may be substituted.

The crystal should be a fundamental mode type. The fundamental mode crystal permits a simpler oscillator circuit with no additional filter components and is less likely to generate spurious responses. The crystal specification is as follows:

Frequency:	8.192MHz
Tolerance:	As required
Oscillation Mode:	Fundamental
Resonance Mode:	Parallel
Load Capacitance:	20pF
Maximum Series Resistance:	35Ω
Approximate Drive Level:	1mW

e.g. CTS R1B23B32-8.192MHz
(20ppm absolute 6 ppm 0C to 50C, 32pF, 25

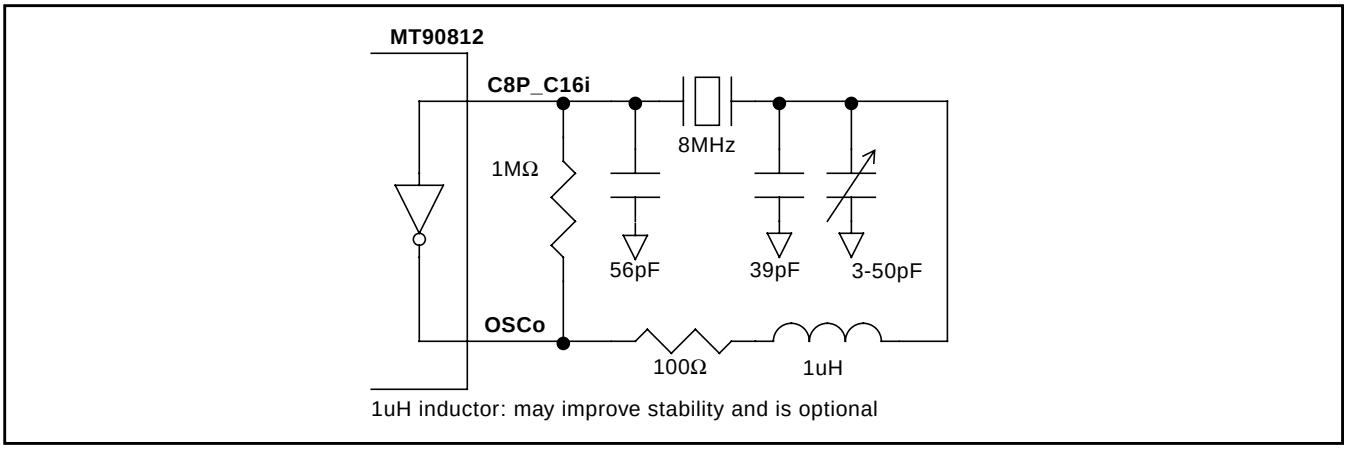


Figure 20 - Crystal Oscillator Circuit

10.0 D-Channel Signalling Support

The MT90812 can support communications over the D-channel in one of the following methods:

- Basic Receive Transmit Method
- Shared HDLC Resource Method

The first method is supported by the D-channel Basic Receive Transmit (DBRT) block. The DBRT supports the communication over the D-channel with the use of start and stop signalling and buffering of messages for both receive and transmit directions.

The second method supports the use of the MT8952 HDLC Protocol Controller for communication over the D-Channel. The HDLC Resource Allocator (HRA) block in the MT90812 provides an interface to the MT8952 HDLC Protocol Controller. Refer to the MSAN-122 note for a description of how voice/data channels and signalling information channels on a digital communications link are supported. MSAN-178 note provides a programming example for the HRA.

Each of the blocks are described in the following sections.

11.0 D-Channel Basic Receive Transmit Block

The MT90812 can support communications over the D-channel with the use of the D-channel Basic Receiver/ Transmitter (DBRT). The D-Channel Basic Receiver and Transmitter are used to transfer data between a channel on a serial stream and the parallel micro-port with the use of two 32 byte FIFOs.

There are two modes which the receiver or transmitter may be placed in: Message Length Interrupt Mode (MLIM) and FIFO Level Interrupt Mode (FLIM). MLI is suited to smaller messages, where efficient use of bandwidth is important and interrupts are generated on the completion of a message. FLI mode is suited to the transfer of large amount of data, where due to the size of the message, start, parity and stop bits are required more often and interrupt generation can support a large data transfer through the FIFO. The bit formatting for these two modes are summarized in Table 10 and Fig. 21.

In MLI mode a start bit is sent, followed by the message bits and parity (if enabled) and stop bit. In FLI mode start, parity and stop bits are added to every 8 bits. It is also possible to send unframed data in FLI mode.

The bit rate can be set to 1, 2, or 8 bits per frame for any mode.

Mode name	Interrupt Mode	Mode Bit (M)	Start-Stop bits	Parity bit	Bit Rate
Message oriented	MLIM	1	X	0	1, 2, or 8 bits/frame
Message oriented with parity	MLIM	1	X	1	1, 2, or 8 bits/frame
Unframed	FLIM	0	0	x	1, 2, or 8 bits/frame
Byte oriented	FLIM	0	1	0	1, 2, or 8 bits/frame
Byte oriented with parity	FLIM	0	1	1	1, 2, or 8 bits/frame

Table 10 - DBRT Modes of Operation

*X = don't care

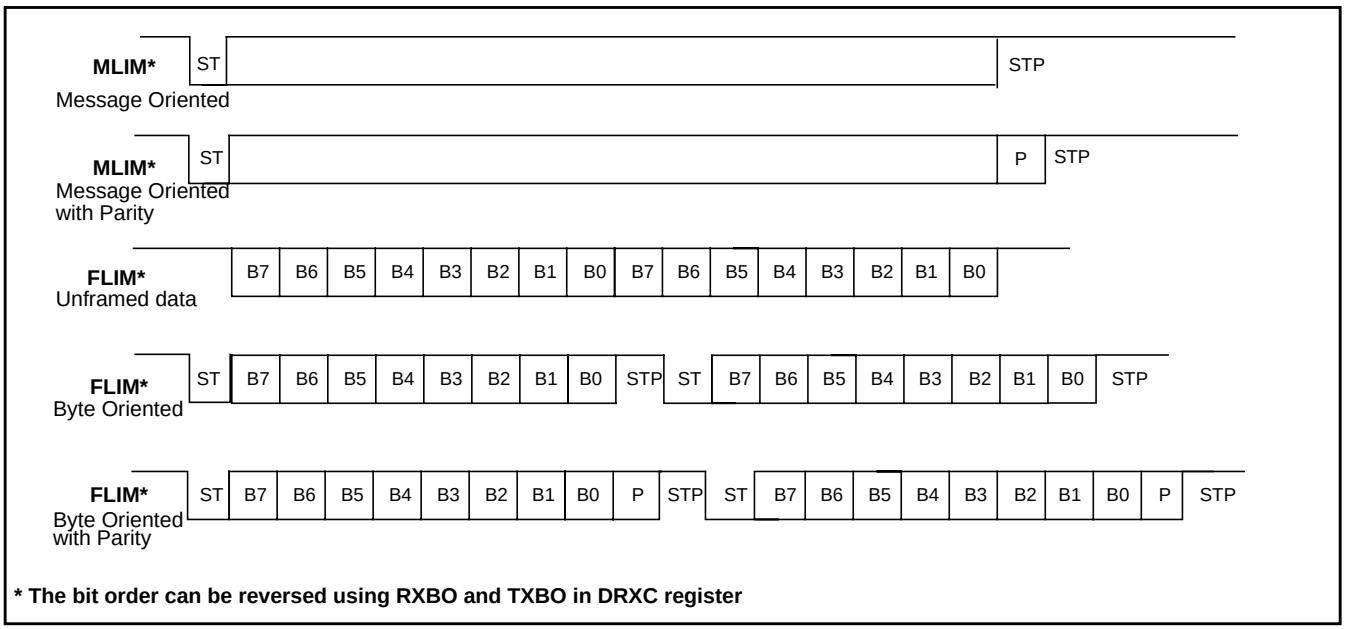


Figure 21 - DBRT modes

11.1 Receiver Operation

The receiver transfers incoming data for a specified channel, identified in CM location 70_H, to the RX FIFO. The system read of "D-Channel RX FIFO Output (DRXOUT)" register at 43_H accesses the next data byte in the RX FIFO buffer. The following diagram illustrates the data flow for the D-channel data.

The RX control register "D-channel RX FIFO Control Bits (DRXC)" at 41_H is used to specify the receiver bit order, data rate at 1, 2 or 8 bits per frame, Message Length or FIFO Level Interrupt Mode, select start and stop bits, enable parity, and activate the receiver. Refer to page 66 for more description. The receiver bit order defines whether the first bit received on the TDM channel is the LSB or MSB read on the microport data bus (D0 or D7, respectively).

In MLI Mode, when the data is transferred to the RX FIFO the start and stop bits are automatically stripped off. The start and stop enable (SE) bit in DRXC register is not used and the received message (1 to 256 bits) is always assumed to be framed by the start and stop bits. The received data is only transferred to the RX FIFO following the reception of the start bit (the first '0'). The status of the parity enable (PE) bit in the DRXC register

will specify whether the received data will have a parity bit and consequently the receiver will perform a parity check on the received data.

In FLI Mode, the start and stop bits and the parity bit can be enabled or disabled with the SE and PE bits in the DRXC Control register, respectively. With the start and stop bits enabled, the start of the message is identified by the first '0' received after the DBR is enabled. When the start and stop bits are disabled, no parity check will be performed (regardless of the status of PE bit) and the data will be transferred from the incoming TDM stream to the RX FIFO following the RX being enabled.

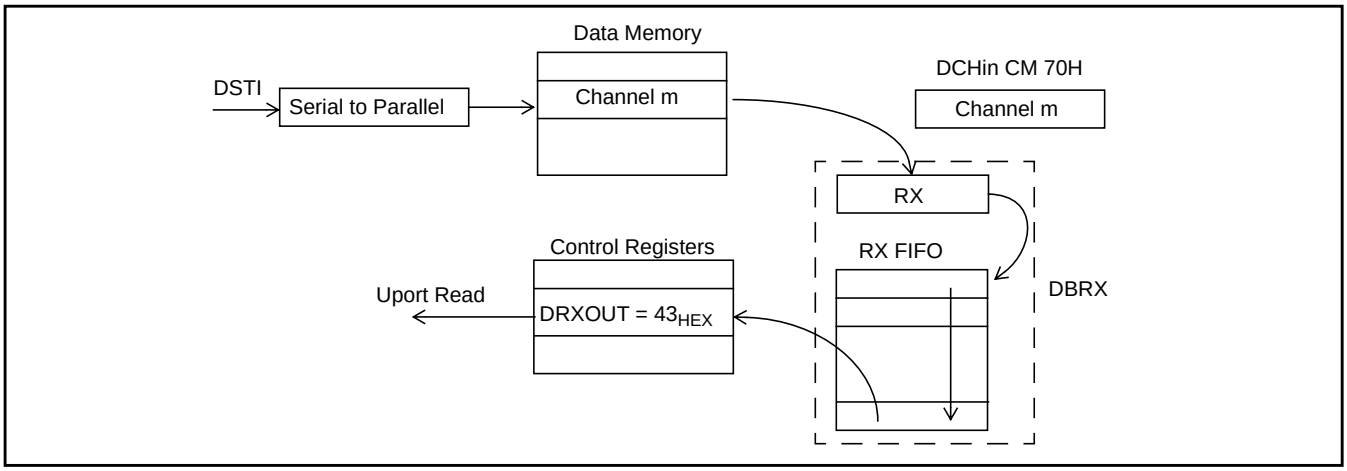


Figure 22 - Data Flow for D-channel Receiver

11.1.1 Receiver Interrupt Handling

There are four interrupts associated with the D-channel Receiver. They are listed in Table 11.

Interrupts	Register	Reference Page	Description
DRX	INTS	page 56	D-Channel Receive Message Length or FIFO Level interrupt
DRE	INTS	page 56	D-Channel Receive FIFO Error. Status of error in DCHS register.
OE	DRXS	page 68	Receive Overrun Error
PE	DRXS	page 68	Receive Parity Error
SE	DRXS	page 68	Receive Stop Bit Error

Table 11 - D-Channel Receive Interrupts

The DREE and DRXE bits in the "Interrupt Enable Register (INTE)" on page 57 enable/disable the above interrupts.

The main difference in MLI and FLI modes is in determining when the interrupt occurs. In MLI mode the interrupt occurs when the full message has been received. In FLI mode the interrupt occurs when the number of bytes in the FIFO equals the trigger level. The "D-Channel Receive Interrupt Threshold (DRXIT)" register is used to program when an interrupt occurs for either MLI or FLI Mode. In the latter mode, the interrupt is to indicate that the FIFO level is attained and not necessarily the end of the message. In the former mode, the interrupt solely indicates the end of the message.

As listed in Table 11 an interrupt is also triggered when one of the following error conditions occurs:

- The RX FIFO is full and the next byte of data has been received and is to be transferred to the FIFO then the overrun status bit is set and an interrupt occurs (RX overrun error).

- The stop bit was not detected (RX stop bit error).
- The status of the received parity bit did not equate to the calculated parity (RX parity bit error).

12.0 Transmitter Operation

Fig. 23 illustrates the data flow for the D-channel data in the transmit direction. A system write to the TX FIFO buffer is performed by addressing the “D-Channel TX FIFO Input (DTXIN)” register at location 44_{HEX} of the Control Register page. Up to 32 bytes can be written to the FIFO. The output of the DBTX is memory mapped to Data Memory location 70_{HEX}. The output of the Transmitter can then be directed to the specified output channel by programming Connect Memory Low as 70_{HEX} for the intended output channel.

As with the Receiver, the Transmitter also operates in two modes: MLIM and FLIM. The TX control register “D-Channel TX Control (DTXC)” at location 45_{HEX} of the Control Register page is used to program the Transmitter for interrupt select, transmission rate at 1, 2, or 8 bits per frame, MLI or FLI mode, start and stop bit enable (SE), parity enable (PE), and start transmission (ST). The transmission sequence starts when bit ST is set followed by writing the first byte to the FIFO. The transmission bit order is determined from TXB0 bit in the “D-Channel Receive Interrupt Threshold (DRXIT)” register. Refer to page 66 for a description on the transmission bit order.

In MLI Mode, the Transmitter automatically appends the start and stop bits to an N byte message with an optional parity bit. The status of SE bit has no effect on this mode but the PE bit specifies whether the message to be transmitted requires a parity bit.

In FLI Mode, the status of SE and PE bits can provide three transmission methods. If the SE bit is disabled, the Transmitter does not include start, parity and stop bits to the message regardless of the status of PE bit. If SE is enabled, the user has the option of enabling or disabling the PE bit. The start, parity, and stop bits are applied on a per byte basis.

The transmitted messages are always padded with stop bits for any remaining bits. For example in the case where a byte long message is to be sent with start and stop bits and a data rate at 8 bits per frame, the transmission of the message will take two frames and the stop bit will be in the second bit of the second frame and the 3rd to 8th bits will be padded with stop bits.

The Transmitter operation also provides a message to be broadcast to several channels simultaneously. This is accomplished by programming the Connect Memory of the intended outgoing channels all to 70_{HEX}. One application for broadcasting messages might be to update displays on all phone sets.

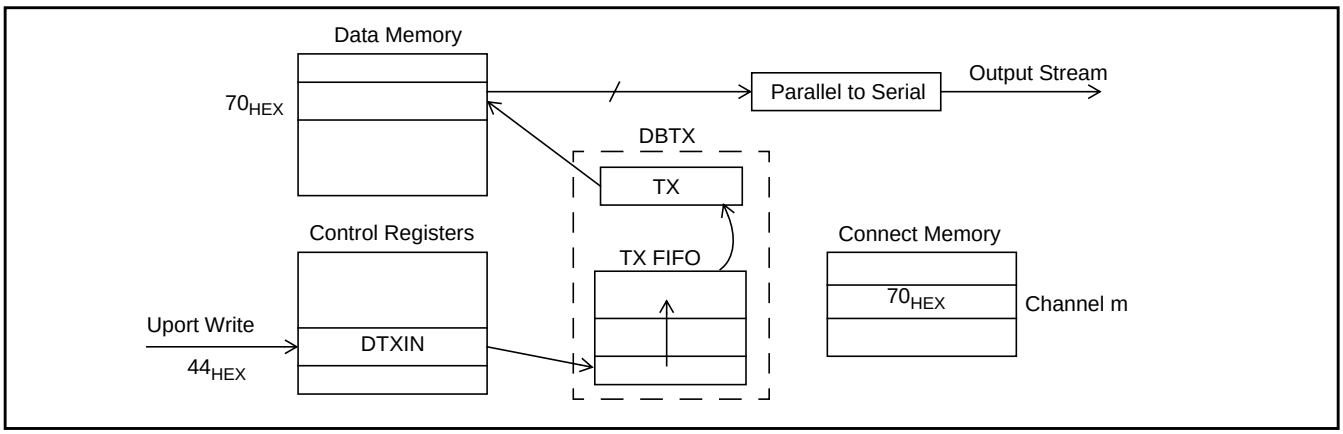


Figure 23 - Data Flow for D-channel Transmitter

12.1 Transmitter Interrupt Handling

In either MLI or FLI modes interrupts are generated on TX FIFO empty or 3/4 empty, or end of transmission. The TX FIFO Interrupt Select (IS) and Interrupt Level (IL) bits in the DTXC register specify the condition for an interrupt to occur. If the IS bit is set high, then the interrupt occurs when transmission is complete.

Mode name	Interrupt Mode	Bit Rate		
		1 bit/frame	2 bits/frame	8 bits/frame
Message oriented	MLIM	8 frames	4 frames	1 frame
Message oriented with parity	MLIM	8 frames	4 frames	1 frame
Unframed	FLIM	8 frames	4 frames	1 frame
Byte oriented	FLIM	10 frames	5 frames	1 frame
Byte oriented with parity	FLIM	11 frames	6 frames	1 frame

Table 12 - Number of available frames to continue the message following TX FIFO empty interrupt

If the IS bit is zero, then an interrupt occurs when either the TX FIFO is empty or 3/4 empty depending on the status of the IL bit. This type of interrupt can be used to continue the message. Therefore, to continue a message after the TX FIFO empty interrupt occurs, the user can write to the TX FIFO within the number of frames as shown in Table 12.

The D-Channel TX Enable Interrupt (DTXE) bit in the “Interrupt Enable Register (INTE)” on page 57 enables or disables the Transmitter interrupts.

13.0 HDLC Resource Allocator Module

The HDLC Resource Allocator (HRA) block in the MT90812 provides an interface to the MT8952 HDLC Protocol Controller. This interface supports the sharing of the HDLC resource across several MT9171/72 DNIC devices for communication over the D-Channel. The MSAN-122 application note describes how voice/data channels and signalling information channels on a digital communications link are supported. Refer to the MSAN-122 note for a general description of:

- MT8952 HDLC Protocol Controller
- MT9171/72 Digital Network Interface Circuit
- Shared HDLC Resource Method

The HRA block is described in the following sections.

- General Description of MT90812 and Shared HDLC Configuration
- Connection to MT8952 HDLC Controller and MT9171/72 DNIC
  - Connection to MT8952B HDLC Controller
  - Connection to MT9171/72 DNIC
  - Data Stream Flow
- TX Control
  - Generation of TxCEN
  - End of the Transmission of a Packet
  - TX and RX Handshaking
  - Merging of D and C-channels
- RX Control
  - Generation of RxCEN

- Dedicated Receive Mode
- Multiplexed Receive Mode
- CTS Generation
- Receive Packet Termination

- RX Channel Auto-hunt
  - Auto-hunt Monitoring
  - Circumstances When Monitoring a Channel is Stopped

Refer to the HDLC control and status registers starting on page 70. Refer to MSAN-178 note for a programming example for the HRA.

13.1 General Description of MT90812 and Shared HDLC Configuration

The HRA provides the capability to multiplex the HDLC controller over a maximum of 16 channels of the STo1 link. Signalling information can be passed to and from the far end through the 8, 16, or 64 kb/s D-channels. The microprocessor uses the MT8952 to send and receive the signalling information in the HDLC protocol. To send information, the microprocessor writes to the HDLC transmit buffer. The message will then be sent out 1,2, or 8 bits per channel to the far end. Messages from the peripherals can be received through the RX and the Auto-hunt blocks of the HRA.

The HRA is used to specify which channel, and hence which of the DNICs, the message is intended. The HRA allows the transmit and receive sections of the MT8952 to act independently. When the microprocessor is transmitting to one peripheral it may receive from another simultaneously. To specify the receive and transmit channels the channel number is written to the DRX4-1 bits in HRA CTRL Register 2 (HC2) and NTX4-1 bits in HRA CTRL Register 3 (HC3). The channel number for the RX circuit may also be supplied from the Auto-hunt circuit of the HRA. The Auto-hunt circuit supplies the channel number when the RX circuit is in multiplexed mode. When in dedicated mode the channel number is supplied by a system write to the DRX4-1 bits in HRA CTRL Register 2 (HC2).

When in multiplexed mode the HRA supports polling of the peripherals. In this mode, sharing of the single HDLC amongst several peripherals (i.e. MT9171/72 DNIC devices) is simplified through the use of the Auto-hunt circuit. When it is necessary for a peripheral to send a message to the central processor, the peripheral continually sends a “Request-to-Send” (RTS) message. The Auto-hunt block in the HRA monitors each incoming channel in turn and checks for a RTS message. Upon detection of a RTS from the peripheral the HRA latches the channel number to be used as the next receive channel by the RX circuit of the HRA.

The Auto-hunt circuit functions independently of the TX and RX circuits, thereby reducing the workload demanded of the MT8952 HDLC controller. There is some handshaking that is required between the TX, RX and Auto-hunt blocks and will be described further in the next sections.

13.2 Connection to MT8952 HDLC Controller and MT9171/72B DNIC

Fig. 24 shows a typical application of the MT90812 connected to a MT8952 HDLC Protocol Controller and several MT9171/72 DNICs. Placing the MT8952B in the External Timing mode and the DNICs in the dual-port digital-network mode allows for easy interface through the HRA block.

13.2.1 Connection to MT8952B HDLC Controller

The multiplex timing for the HDLC-channel is performed by the HRA block. The MT8952B transmit and receive sections, in External Timing mode, are independently controlled by the hardware pins $\overline{\text{TxCEN}}$ and $\overline{\text{RxCEN}}$, respectively. To assist in multiplexing, the MT8952B outputs TEOP and REOP indicate when it has finished transmitting or receiving a packet.

The $\overline{\text{TxCEN}}$ and $\overline{\text{RxCEN}}$ clock enable strobes are generated by the HRA during the specified-channel and bit times to allow the HDLC controller to transmit to, and receive from, any channel.

The MT90812 output C2o is a 2.048 MHz clock provided for the MT8952 HDLC controller bit rate clock input.

13.2.2 Connection to MT9171/72B DNIC

The DNIC, as mentioned earlier, is used in dual-port mode. The B1 and B2 channels are input/output at DNIC port DSTi/DSTo in timeslots 0 (B1) and 16 (B2) relative to $\overline{F0i}$. The D and C information is input/output at port CDSTi/CDSTo on channels 0 (D) and 16 (C). The DNICs are 'daisy-chained' together using the delayed frame pulse output $\overline{F0o}$. In dual-port mode the signal $\overline{F0o}$ comes at the end of channel 0. Supplying it to the next DNIC in the chain skews its active channels by one channel.

Because two TDM links are used to support these 'daisy-chained' DNICs, up to 16 line circuits may be served by one HDLC Protocol Controller with this configuration.

13.2.3 Data Stream Flow

Fig. 24 shows five numbered streams which connect a MT90812 to the DNICs and the MT8952 HDLC Protocol Controller. They are:

1. The STo0 stream from the MT90812 to the DNICs' DSTi containing B channels.
2. The STo1 stream from the MT90812 to the DNICs' CDSTi containing D/C-channels.
3. The STi0 stream of the MT90812 from the DNICs' DSTo containing B channels.
4. The DNICs' CDSTo containing D/C-channels to the MT90812 STi1 and the MT8952B CDSTi.
5. The MT8952B CDSTo stream to the MT90812 DPER containing formatted D-channel data.

Streams 1 and 3 contain only B channel information. **Stream 1** originates from the STo0 of the MT90812 and is input to DSTi of the DNIC devices. **Stream 3** is the opposite direction of stream 1, transferring B-channel information from DSTo of the DNICs to STi0 of the MT90812.

Streams 2, 4 and 5 are used to pass D- and C-channel information from the microprocessor to the DNICs through the MT90812 and HDLC protocol controller. D-channel information starting at the microprocessor is written to the MT8952 transmit buffer. It is formatted and sent out **stream 5. Stream 5** connects CDSTo of the MT8952B to the DPER input of the MT90812.

In the MT90812 the D-channel and C-channel information are merged to form **stream 2**. The C-channel information is written by the microprocessor to the Connect Memory of the MT90812. The C-channel information from Connect Memory is sent out STo1 of the MT90812 along with the D-Channel information from DPER. **Stream 2** connects STo1 from the MT90812 to CDSTi of the DNICs. The merging of the D- and C-channels is described in Section 13.3.4.

The D- and C-channel information is transferred from the DNICs' CDSTo on **stream 4**, to both the MT90812 and the HDLC. The C-channel information is transferred to the Data Memory of the MT90812, where it may be read directly by the microprocessor. The D-channel information is transferred to the microprocessor through the MT8952 HDLC Protocol Controller. The MT8952 stores the D-channel information in the 19-byte buffer to be read by the microprocessor.

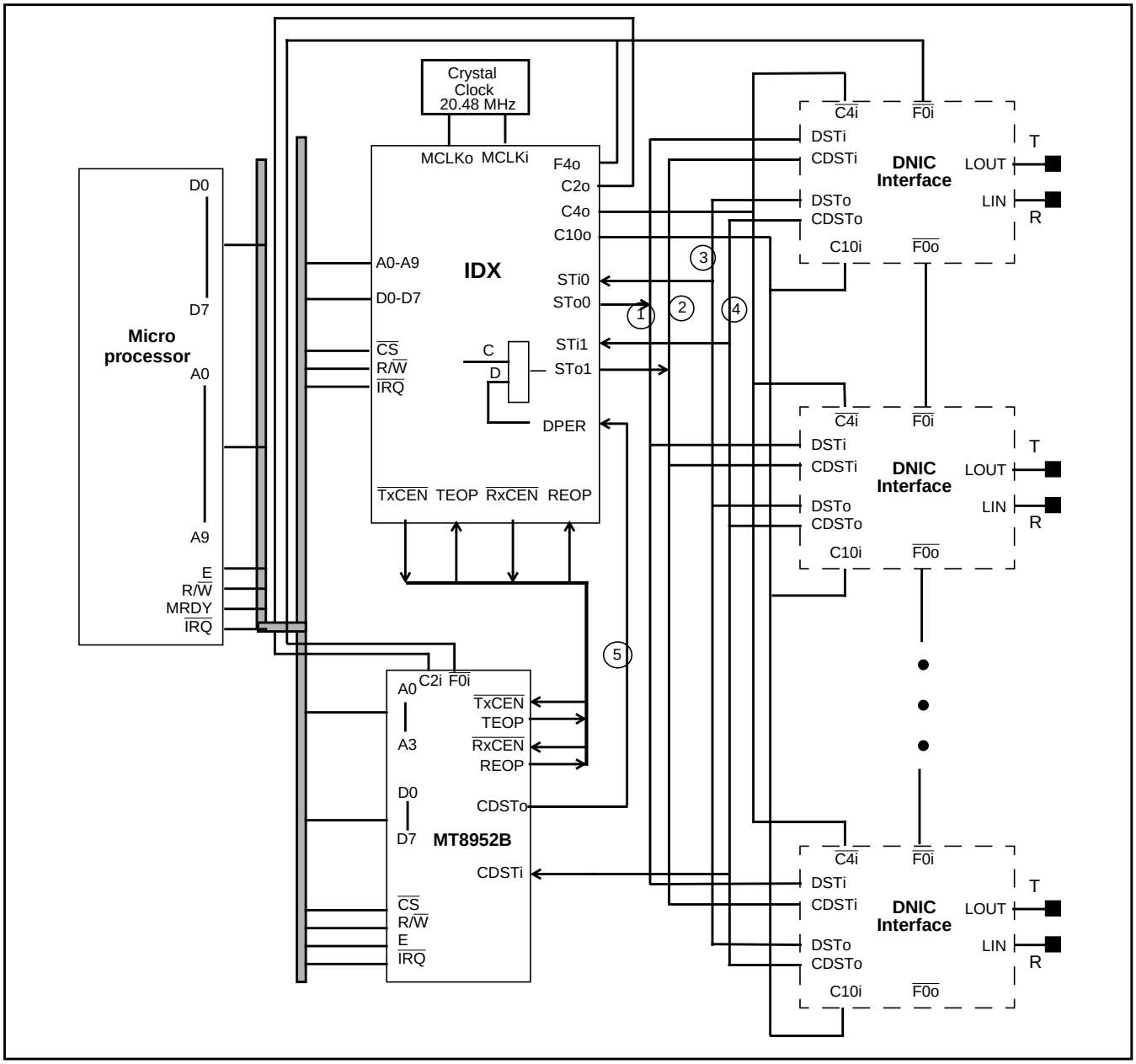


Figure 24 - Typical Application Using the HDLC Resource Allocator

13.3 TX Control

The TX circuit performs the following functions:

- generate TxCEN to enable the HDLC transmitter.
- handle Transmit Packet Termination.
- allow RX and TX Handshaking
- merge D-Channel data from the HDLC controller into the local TDM stream.

These functions will be described in the sections below.

13.3.1 Generation of $\overline{\text{TxCEN}}$

The HDLC transmitter is controlled by the MT90812 generated Transmit Clock Enable signal, $\overline{\text{TxCEN}}$. The $\overline{\text{TxCEN}}$ output signal enables the HDLC transmitter in the appropriate channel as specified by the system, via

the MT90812 microport. $\overline{\text{TxCEN}}$ output signal is enabled for one to eight bits per channel per frame, depending upon the selected baud rate.

The desired active channel is selected by the system via a write to the MT90812 device's Next Transmit Channel (NTX) bits defined in HRA CTRL Register 3 (HC3). A write to this register will start $\overline{\text{TxCEN}}$ to be enabled for the channel specified as soon as the transmitter becomes inactive.

The NTX bits are double buffered which allows the system to specify the next transmit packet at any time, without concern for whether the present transmit packet is finished.

At the start of the transmission of a packet the following three actions are taken:

- the NTX bits are latched into the PTX (present transmit channel) bits in HRA Status 4 (HS4) register.
- status bit TXCHNL is set,
- a transmitter-active flag (TXACT) is set

Latching the system's NTX request into the PTX (present transmit channel) register redefines the active transmit channel time. When the status bit TXCHNL is set, this informs the system that its transmit channel request has been satisfied. When the transmitter-active flag (TXACT) is set, this allows $\overline{\text{TxCEN}}$ to be enabled during the appropriate bit times.

13.3.2 End of the Transmission of a Packet

A transmit packet will be terminated by a transmit end-of-packet (TEOP) strobe from the HDLC controller chip or by setting the STEOP flag through the HRA CTRL Register 2 (HC2). The HDLC controller chip asserts TEOP for one bit period during the last bit of the closing flag of the transmit packet. The system may, at any time, raise its own STEOP flag through the HRA CTRL Register 2 (HC2). When the STEOP flag has been read by the system, it will be automatically cleared.

In either case, the end-of-packet signal will cause the transmitter to go inactive, thus allowing another packet transmission to be initiated (if desired). Whenever TXACT is low, the HDLC controller's transmit clock enable $\overline{\text{TxCEN}}$ is disabled, and idles are transmitted for the unused remainder (if any) of the D-channel time.

13.3.3 TX and RX Handshaking

Transmit and receive functions are generally independent of each other. But there is a coupling of the two functions caused by the requirement for a go-ahead handshake. This handshake must be sent by the MT90812 when a peripheral requests to transmit to the system. While the MT90812 is generating and transmitting this go-ahead on the channel reserved for the specific peripheral, it pre-empts the system's D-channel transmit time. This interference occurs for that particular peripheral only, for the duration of the clear-to-send (CTS) nine-bit go-ahead pattern.

If the system transmits a packet to a peripheral which is also currently being sent a go-ahead this would result in the loss of data from the system transmit packet. To prevent data loss a number of approaches can be taken.

After specifying the NTX channel, and waiting until TXCHNL goes high, the system can read the present receive channel (PRX). If PRX is the same as NTX, then the system may either:

- send the packet anyway and retransmit on request,
- assert a software transmit end-of-packet (STEOP) to terminate the system's request for that particular transmit channel,
- wait for a maximum of five frames (at a 16K baud rate) for the CTS to complete,
- or monitor CTSACT until it goes low.

In dedicated receive mode, where the generation and transmission of CTS by the MT90812 is inhibited, no possibility of contention exists between the system and the MT90812. So such restrictions need not apply.

13.3.4 Merging of D and C-channels.

The HRA block multiplexes the D-channel, originating at the HDLC Protocol Controller, and the C-channels into a common output stream. C-channel and D-channel information destined for the line circuit are also fed through a multiplexer controlled by $\overline{\text{TxCEN}}$ and a half-frame count. This does the merging of the outgoing D- and C-channel information and produces a high ('all-ones') pattern on the unused D-channels.

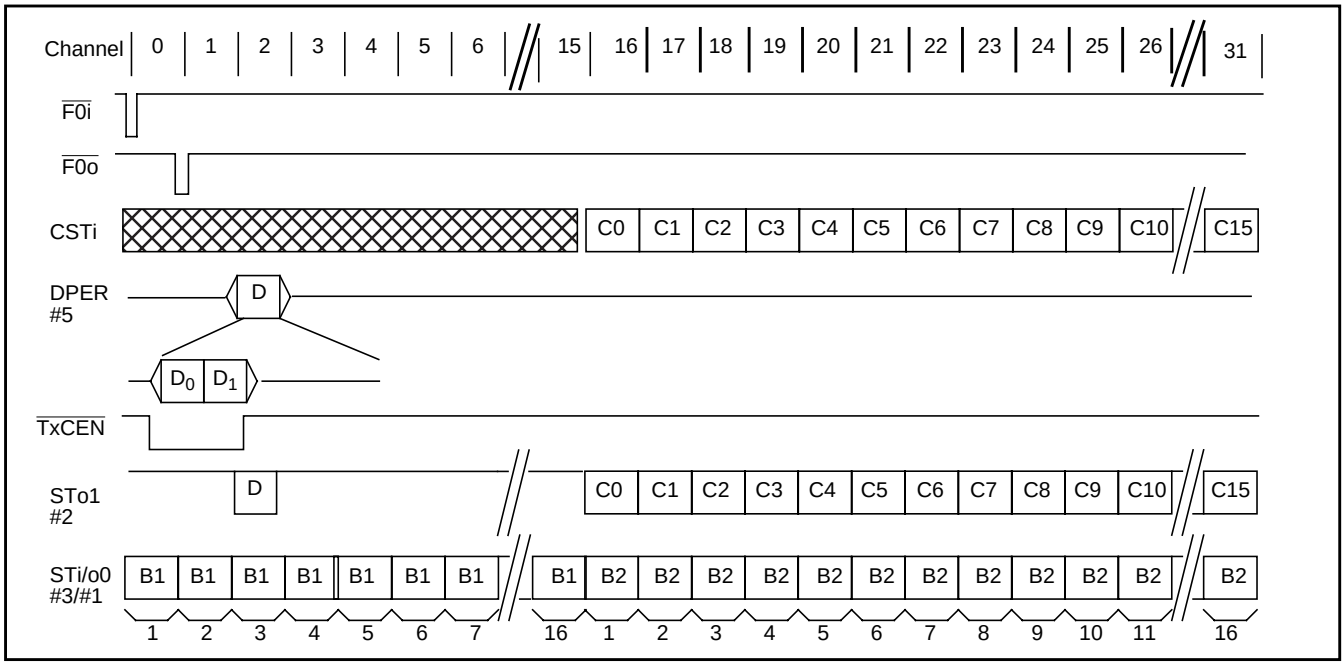


Figure 25 - Composite ST-BUS Frame for HRA Application

Fig. 25 shows the composition of the ST-BUS in the transmit direction. The streams are also labelled according to the numbers assigned as in Fig. 24.

The B1 and B2 channels for up to 16 line circuits arrive at STi0 **stream #3** and depart at STo0 **stream #1**. All DNIC line circuits are connected in parallel to this bus. The channel assignments and line destination addresses are shown in Fig. 24. The C-channel information, which have been written to the MT90812 Connect Memory, are assigned to the first 16 channels of STo1, **stream #2**.

The D-channel from the MT8952B is input to the HRA block of the MT90812 at DPER, **stream #5**, during the times enabled by $\overline{\text{TxCEN}}$. The C and D-channels are combined to produce STo1, **stream #2**, which is then routed to the DNICs. The composition of CDSTo is shown, in Fig. 24, with the D-channel enabled for line circuit 3 (channel 18).

In the opposite direction, C-channel information from the line circuits arrives at STi1, **stream #4**, in the first 16 channels. The MT8952B, enabled by $\overline{\text{RxCEN}}$, receives the active incoming D-channel directly from the same bus.

14.0 RX Control

14.1 RX Circuit Functions

The RX circuit performs the following functions:

- generate $\overline{\text{RxCEN}}$ to enable the HDLC receiver
- operate in dedicated mode or multiplexed modes
- handle Receive Packet Termination
- generate the CTS pattern to be transmitted

14.1.1 Generation of $\overline{\text{RxCEN}}$

The RX circuit performs two functions. As with the TX circuit, it must generate the proper HDLC receive clock enable signal ($\overline{\text{RxCEN}}$). This signal has the same characteristics as $\overline{\text{TxCEN}}$.

The $\overline{\text{RxCEN}}$ signal enables the HDLC receiver in the appropriate channel as specified by the system, via the MT90812 microport. $\overline{\text{RxCEN}}$ is enabled for one to eight bits per channel per frame, depending upon the selected baud rate, specified in HRA CTRL Register 1(HC1).

The desired active channel corresponding to a specific D-Channel is determined from either the Dedicated RX Channel (DRX) bits in HRA CTRL Register 2 (HC2) or the Present Receive Channel (PRX) bits in HRA Status registers in dedicated and multiplexed modes, respectively.

14.1.2 Dedicated Receive Mode

When the receiver is operated in Dedicated Receive mode, the Auto-hunt circuitry is ignored and the system provides the channel number. Dedicated Receive mode is selected by setting DDRX bit in HRA CTRL Register 2 (HC2). When DDRX bit is set high it enables dedicated reception from the channel selected by the DRXi bits in HRA CTRL Register 2 (HC2).

In Dedicated Receive mode RXCHNL and RXACT bits will be held high. The CTSACT bit will be held low, disabling the CTS generator. These three status bits are in HRA Status 1 (HS1).

A write to the DRX bits will start $\overline{\text{RxCEN}}$ to be enabled for the channel specified as soon as the receiver becomes inactive.The DRX bits are double buffered which allows the next receive channel to be specified at any time, without a concern for whether the present receive packet is finished.

14.1.3 Multiplexed Receive Mode

The primary function of the RX channel Auto-hunt circuit is to provide the RX circuit with the next receive channel number. The Auto-hunt circuit has to interface with both the RX and TX circuits as described in Section 13.3.3. The main function of the Auto-hunt circuit is described in the following sections.

14.1.4 Auto-hunt Monitoring

The Auto-hunt circuit scans each of the 16 incoming D-Channels on stream STi1 to determine if any one of them is requesting to send a packet to the system. The Auto-hunt circuit will scan the channels which are enabled for receive activity. On reset, all 16 channels are locked out, and the system must specify which channels are to be scanned for request-to-send (RTS) flags. The two HRA Lockout registers described in Section 22.30 and Section 22.31 are used to specify the channels. The Auto-hunt circuit will stop monitoring a channel for flags in three other circumstances which are described in Section 14.1.6.

The HDLC flag control character '01111110', ($7E_{HEX}$), is used to indicate an RTS to the system. For each D-Channel which is not disabled, the Auto-hunt circuit monitors during the appropriate bit times for flags. If a flag is undetected after 15 consecutive bit times on the currently scanned D-Channel, the Auto-hunt circuit moves to the next channel. The amount of time required to accumulate 15 “consecutive” bits is dependent on the selected baud rate; for a 16K baud rate, each non-disabled-channel is monitored for up to eight frames before being rejected. This hunt sequence continues until a flag is detected, at which point the scanning stops and the FLAG bit is set high in the HRA Status register.

Scanning for flags, at least until an RTS is actually detected, is independent of RX circuit activity or inactivity. The Auto-hunt circuitry cycles endlessly through all available (non-disabled) channels, listening for a peripheral's request to send. The more channels there are with RTS, the faster the Auto-hunt circuit finds the next receive channel number, thereby keeping the receiver inactive time to a minimum.

At the start of receiving a packet the RX circuit will latch the NRX channel number, clearing the FLAG bit, and moving the Auto-hunt circuit on to begin scanning the next potential receive channel.

In multiplexed operation, the receiver obtains the next RX channel (NRX) number from the RX channel Auto-hunt circuit. Three conditions must be met before the RX circuitry will initiate receiving a packet:

- The Auto-hunt circuit must have detected a request-to-send (RTS) flag.
- The system must have read the channel number for the most recently active receive channel. This condition is not required if the received RTS flag is the first detected flag after reset.
- The receiver must currently be inactive.

The order in which these three conditions are satisfied is not important. For the first condition to be true the Auto-hunt circuit must detect the RTS pattern '01111110' on the current D-channel.

The second condition is met by setting the status bit (RXCHNL) high in HRA Status 1 (HS1) register when a new receive channel number is latched. This disables subsequent receive channel number latching until the system clears that bit by reading PRX in HRA Status 3 (HS3) register. If the system wants to stop the HDLC receiver, it may do so by not reading PRX.

The third condition, that the HDLC receiver be inactive, is achieved by the detection of a receive end-of-packet strobe (REOP) from the HDLC controller chip.

At the start of the reception of a packet the following five actions are taken:

- the NRX channel number will be latched into the PRX (present receive channel) bits, where it will define the active receive channel time;
- an internal receive-active flag (RXACT) will be set, allowing $\overline{\text{RxCEN}}$ to be enabled during the appropriate channel time;
- the RXCHNL status bit will be set, to inform the system that a new PRX channel number is available;
- the Auto-hunt circuitry will be cleared, and forced to move on to the next channel to be scanned;
- and a CTS go-ahead pattern will be initiated (CTSACT high).

14.1.5 CTS Generation

Clear-to-Send Active (CTSACT) is in HRA Status 1 (HS1) register. CTSACT set high indicates that the receiver is currently transmitting a clear-to-send go-ahead pattern to the peripheral on the transmit channel denoted by PRXi. The CTS pattern generated is the 9-bit HDLC go-ahead character '011111110' (7F +’0’). For a 16k baud rate, this bit pattern is sent out 2 bits/frame in the appropriate D-Channel. When the go-ahead is complete, CTSACT will be forced low, and control of the particular D-Channel used for the go-ahead transmission will be returned to the system.

The CTS generator can be re-triggered by the system, if desired, by setting the Re-initiate Clear To Send (RECTS) bit in “HRA CTRL Register 2 (HC2)” on page 71. Once a new CTS pattern has been initiated, the RECTS control bit will automatically be cleared by the RX circuitry. RECTS is acted upon with the same timing as the normal source of CTS initiation.

14.1.6 Circumstances When Monitoring a Channel is Stopped

There are four conditions which will cause the Auto-hunt circuit to stop monitoring a particular channel for flags. They are:

- RTS is not detected
- the channel is the current active receive channel
- the channel is locked out
- the channel is the current active transmit channel

The first, which was described above, is when a flag has not been detected within 15 valid bit times.

The second condition occurs if the Auto-hunt circuit manages to cycle back to monitor a peripheral which is already the currently active receive channel. Because the peripheral continues to send request-to-sends during the time when it is being acknowledged with a go-ahead from the RX circuitry, it is important that flags not be detected twice for the same request. This condition is prevented by disabling scanning on a currently active receive channel.

The third condition that causes the Auto-hunt circuit to skip a channel, is if it has been locked out by the system. This allows the system to independently disable reception from any channel. On reset, all 16 D-channels are locked out, and the system must specify which channels are to be enabled for receive activity. The two HDLC CTRL Lockout registers are described in Section 22.30 and Section 22.31.

The fourth condition that will cause the Auto-hunt circuit to skip a channel occurs when the scanned-channel number is the same as an active TX channel. The channel is skipped in this case to reduce the contention between a system transmit packet and the transmission of a CTS. If a flag has been detected before the transmitter goes active on the same channel, then the contention, described in “TX and RX Handshaking” on page 38, will occur. However, if the transmitter goes active at any point before a flag is detected, then contention will be avoided.

14.1.7 Receive Packet Termination

A receive packet will be terminated when the HDLC controller asserts the REOP strobe for one bit period, one bit time after the closing flag is received. If desired, the system may assert its own SREOP flag via the micro interface. The SREOP bit is in “HRA CTRL Register 2 (HC2)” on page 71. This flag has the same effect as the normal REOP strobe, but may be written asynchronously and will be cleared by the RX circuit after it has been acted upon. In either case, a receive end-of-packet will cause RXACT to go low, disabling $\overline{\text{RxCE}}$N.

15.0 C-Channel Data

C-Channel access for Codec or DNIC control is provided through Message Mode (refer to “Connection Memory” on page 10). The C-Channel information can be read from Data Memory or written to Connect Memory.

C-Channel data status information is very static. Therefore, the interface as provided via Message Mode is single buffered. Hence, the C-channel information may change every frame.

16.0 Tone Generation

The MT90812 generates the standard 16 DTMF frequencies within +/- 0.6% of the nominal standard frequencies. Table 13 shows the standard DTMF frequencies, the coefficient used to generate the closest frequency, the actual frequency generated and the percent deviation of the generated tone from the nominal.

Tone Group	Frequency Hz	Coefficient	Actual Frequency	% Deviation
Low	697	59H	695.31	-0.24%
	770	62H	765.63	-0.56%
	852	6DH	851.56	-0.05%
	941	78H	937.50	-0.37%
High	1209	8DH	1203.12	-0.49%
	1336	96H	1343.75	+0.58%
	1477	9FH	1484.38	+0.50%
	1633	A9H	1640.62	+0.47%

Table 13 - DTMF Frequencies

A further 9 other standard tones are available for use as call progress and supervisory tones. Also available are 7 programmable tones, which may be single or dual frequency. This totals 32 available tone outputs.

The composite signal output level in the transmit direction is -4 dBm0 (μ-Law) and -10 dBm0 (A-law), when the programmable gains are set at zero dB. Pre-twist of 2.0 dB is incorporated into the composite signal resulting in a low tone output level of -8.12 dBm0 and a high group level of -6.12dBm0 (for μ-Law, 6 dB lower for A-Law). Note that the digitally generated signals will be gain adjusted as programmed in the Connect Memory High for each outgoing channel. Refer to Section 7.0 for a description of gain control.

Each of the seven programmable locations has two 8-bit registers accessible via the parallel microprocessor interface used to program the two tone frequencies. If a single tone is desired then one of the registers is programmed to zero. A tone output is disabled if both low and high coefficient registers are programmed to zero. The register descriptions of the coefficient registers, Low Tone Coefficient 1-7, and High Tone Coefficient 1-7 (LTC1-7, HTC1-7) are listed on page 64. Of the 7 programmable tone generators the first two can also be used to provide dual frequency squarewave ringing signals. Tone Ringer enable bits, TRE1 and TRE2, in the TEDC register, enable the generation of the squarewave ringing signals by the two Tone Ringer circuits. The Tone Ringer function is described in Section 16.1.

The Tone Generation circuit can be enabled with TGE bit set to 1 in the Tone Generation and Energy Detect Control Register (TEDC) listed on page 61. With the DTMF circuit reset there is no output generated for all the 32 tones including the Tone ringers and FSK transmitter output.

Frequencies in the fixed and programmable locations tone locations are generated according to one of three formula's, depending on what range the coefficient value is in, as shown in Table 14. The coefficients of the fixed tones cannot be changed. The coefficient is an integer value from 0 to 255.

These single and dual frequency tones are written to the Local Data Memory page at the Tone Block Addresses. The tones will be selected by writing the corresponding tone's address to the Connect Memory Low of the outgoing channel. The address and description of each tone is listed in Table 15.

Outgoing gain control of +3 to -27 dB in steps of 1dB, as well as -∞ dB, is provided for outgoing channels connected to the tone generator output locations. Refer to Section 7.0 for further description of gain control.

All in-band (i.e. 500hz to 3.5khz) harmonics and noise components are at least 35dB below the fundamental frequencies. Total signal to distortion ratio over this band is at least 30dB.

Coefficient Value	Formula Hz	Frequency Range Hz	Resolution Hz
0	Disabled	-	-
1-63	250+(Coef x 3.90625)	253.91-496.09	3.90625
64-127	Coef x 7.8125	500.0 - 992.19	7.8125
128-255	(Coef x 15.625) - 1000	1000.0 - 2984.38	15.625

Table 14 - Programmable Frequencies Available

Addr	Frequency(Hz)	Application	Addr	Frequency(Hz)	Application (Type of cadenced tones generated)
00	697+1209	DTMF digits 1	10	350+440	Dial Tone, Recall Dial Tone, Confirmation Tone
01	697+1336	DTMF digit 2	11	440	Call Waiting, Busy Verification, Executive Override
02	697+1477	DTMF digit 3	12	440+480	Audible Ringback, Special Audible Ringback
03	697+1633	DTMF digit A	13	440+620	Intercept Tone
04	770+1209	DTMF digit 4	14	480+620	Reorder Tone, Busy Tone
05	770+1336	DTMF digit 5	15	400	Busy, Conference Exterior, Call Waiting
06	770+1477	DTMF digit 6	16	400+450	Audible Ring Tone
07	770+1633	DTMF digit B	17	425	Dial Tone
08	852+1209	DTMF digit 7	18	1400	Intrusion Tone
09	852+1336	DTMF digit 8	19	L1+H1	Programmable 1[1]
0A	852+1477	DTMF digit 9	1A	L2+H2	Programmable 2[1]
0B	852+1633	DTMF digit C	1B	L3+H3	Programmable 3
0C	941+1209	DTMF digit *	1C	L4+H4	Programmable 4
0D	941+1336	DTMF digit 0	1D	L5+H5	Programmable 5
0E	941+1477	DTMF digit #	1E	L6+H6	Programmable 6
0F	941+1633	DTMF digit D	1F	L7+H7	Programmable 7[2]

Table 15 - Tone Block Address

Note 1: 1st and 2nd programmable tones can be programmed as dual frequency squarewave Tone Ringer signals
Note 2: 7th programmable tone is replaced with FSK signal when FSK Transmitter is enabled.

16.1 Tone Ringer

Of the 7 programmable tone generators the first two can be used to provide dual frequency squarewave ringing signals. To enable this mode and generate the squarewave ringing signals, the Tone Ringer Enable bits, TRE1 and TRE2, in the Tone Generation and Energy Detect Control Register (TEDC) must be set. TRE1 and TRE2 enable the first and second Tone Ringer circuits, respectively. The digital tone generator uses the values programmed into the low and high Tone Coefficient Registers to generate two different squarewave frequencies. Both coefficients are determined by the following equation:

Coef = [8000/Frequency(Hz)] - 1

where Coef is an integer between 1 and 255. This produces frequencies between 31.25 - 4000 Hz with a non-linear resolution as shown in Table 16. The ringer program switches between these two frequencies at a 5 Hz or 10 Hz rate as selected by the WR bit in the TEDC register.

coef	freq	coef	freq	coef	freq	coef	freq	coef	freq	coef	freq	coef	freq	coef	freq
0	NA	32	242.42	64	123.08	96	82.47	128	62.02	160	49.69	192	41.45	224	35.56
1	4000.00	33	235.29	65	121.21	97	81.63	129	61.54	161	49.38	193	41.24	225	35.40
2	2666.67	34	228.57	66	119.40	98	80.81	130	61.07	162	49.08	194	41.03	226	35.24
3	2000.00	35	222.22	67	117.65	99	80.00	131	60.61	163	48.78	195	40.82	227	35.09
4	1600.00	36	216.22	68	115.94	100	79.21	132	60.15	164	48.48	196	40.61	228	34.93
5	1333.33	37	210.53	69	114.29	101	78.43	133	59.70	165	48.19	197	40.40	229	34.78
6	1142.86	38	205.13	70	112.68	102	77.67	134	59.26	166	47.90	198	40.20	230	34.63
7	1000.00	39	200.00	71	111.11	103	76.92	135	58.82	167	47.62	199	40.00	231	34.48
8	888.89	40	195.12	72	109.59	104	76.19	136	58.39	168	47.34	200	39.80	232	34.33
9	800.00	41	190.48	73	108.11	105	75.47	137	57.97	169	47.06	201	39.60	233	34.19
10	727.27	42	186.05	74	106.67	106	74.77	138	57.55	170	46.78	202	39.41	234	34.04
11	666.67	43	181.82	75	105.26	107	74.07	139	57.14	171	46.51	203	39.22	235	33.90
12	615.38	44	177.78	76	103.90	108	73.39	140	56.74	172	46.24	204	39.02	236	33.76
13	571.43	45	173.91	77	102.56	109	72.73	141	56.34	173	45.98	205	38.83	237	33.61
14	533.33	46	170.21	78	101.27	110	72.07	142	55.94	174	45.71	206	38.65	238	33.47
15	500.00	47	166.67	79	100.00	111	71.43	143	55.56	175	45.45	207	38.46	239	33.33
16	470.59	48	163.27	80	98.77	112	70.80	144	55.17	176	45.20	208	38.28	240	33.20
17	444.44	49	160.00	81	97.56	113	70.18	145	54.79	177	44.94	209	38.10	241	33.06
18	421.05	50	156.86	82	96.39	114	69.57	146	54.42	178	44.69	210	37.91	242	32.92
19	400.00	51	153.85	83	95.24	115	68.97	147	54.05	179	44.44	211	37.74	243	32.79
20	380.95	52	150.94	84	94.12	116	68.38	148	53.69	180	44.20	212	37.56	244	32.65
21	363.64	53	148.15	85	93.02	117	67.80	149	53.33	181	43.96	213	37.38	245	32.52
22	347.83	54	145.45	86	91.95	118	67.23	150	52.98	182	43.72	214	37.21	246	32.39
23	333.33	55	142.86	87	90.91	119	66.67	151	52.63	183	43.48	215	37.04	247	32.26
24	320.00	56	140.35	88	89.89	120	66.12	152	52.29	184	43.24	216	36.87	248	32.13
25	307.69	57	137.93	89	88.89	121	65.57	153	51.95	185	43.01	217	36.70	249	32.00
26	296.30	58	135.59	90	87.91	122	65.04	154	51.61	186	42.78	218	36.53	250	31.87
27	285.71	59	133.33	91	86.96	123	64.52	155	51.28	187	42.55	219	36.36	251	31.75
28	275.86	60	131.15	92	86.02	124	64.00	156	50.96	188	42.33	220	36.20	252	31.62
29	266.67	61	129.03	93	85.11	125	63.49	157	50.63	189	42.11	221	36.04	253	31.50
30	258.06	62	126.98	94	84.21	126	62.99	158	50.31	190	41.88	222	35.87	254	31.37
31	250.00	63	125.00	95	83.33	127	62.50	159	50.00	191	41.67	223	35.71	255	31.25

Table 16 - Tone Ringer Programmable Frequencies

17.0 Frequency Shift Keying (FSK) Transmitter

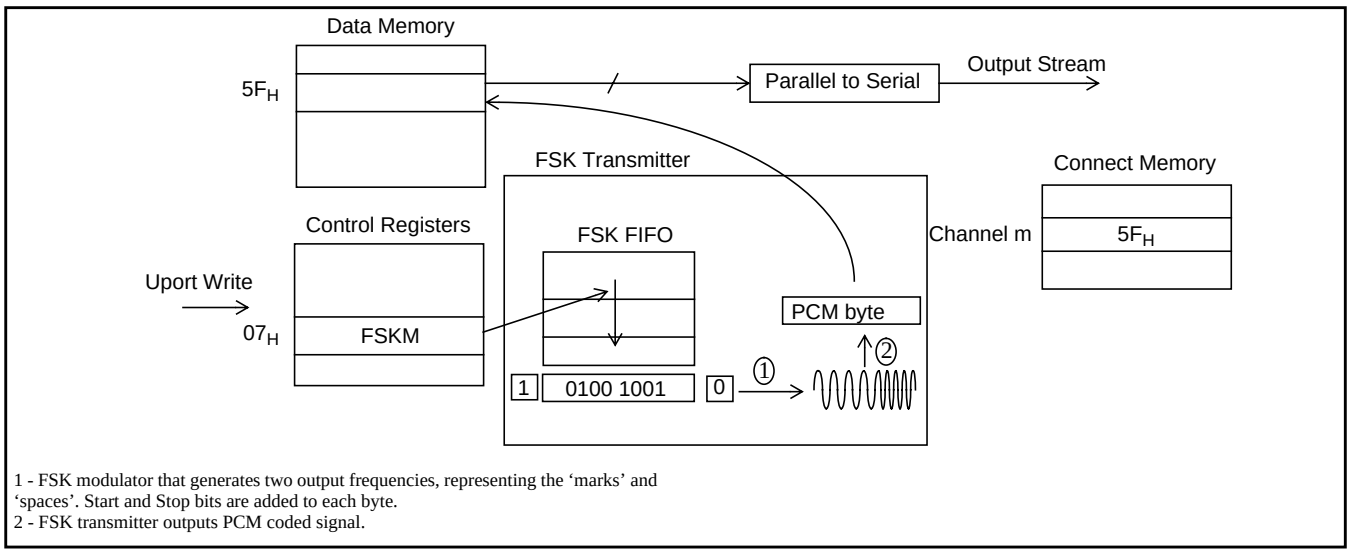
The FSK transmitter is a phase coherent FSK modulator that generates two output frequencies, representing the ‘marks’ and ‘spaces’, of the digital data loaded into the FSK transmit memory. The ‘mark’ and ‘space frequencies are selectable to Bell 202 or CCITT V.23 standards at 1200 baud (refer to Table 17). The FSK transmitter output is a PCM coded signal that can be directed to any outgoing local TDM channel.

	Mark	Space
Bell 202	1200	2200
CCITT V.23	1300	2100

Table 17 - FSK Signalling Frequencies

As with all outgoing channels, a gain from +3 to -27 dB in steps of 1dB, as well as -∞ dB, may be applied to the output of the FSK transmitter. Refer to Section 7.0 for further description of gain control. The signal output level is -6.12dBm0 (μ-Law) and -12.12 dBm0 (A-law), when the programmable gains are set at zero dB.

The FSK transmit memory is a 20-byte FIFO that is accessed at the address 07_H. Refer to Control Register addresses indicated in Table 20 on page 53. The FSK output is memory mapped to address $5F_H$ as shown in Table 3 on page 14. Fig. 26 illustrates the data flow for the FSK transmitter in the MT90812.



1 - FSK modulator that generates two output frequencies, representing the 'marks' and 'spaces'. Start and Stop bits are added to each byte.
2 - FSK transmitter outputs PCM coded signal.

Figure 26 - Data Flow for FSK transmitter

Data is written to the FSK FIFO. Start and Stop bits are added to each byte. The FSK modulator generates two output frequencies, representing the 'marks' and 'spaces'. At 1200 baud, one bit is transmitted every $6^2/_3$ frames. The resulting PCM encoded signal is written to DM where it can be switched to any outgoing channel.

When an interrupt occurs the FTS bit is set in the Interrupt Status Register (INTS). The interrupt may be enabled by setting the FTE bit in Interrupt Enable Register (INTE). An FSK interrupt may occur for two reasons. When the FIS bit, in the Ringer and FSK Control Register (RFC), is Low, an interrupt is generated when the TX FIFO is empty, when the FIS bit is High, an interrupt is generated at the end of transmission.

The FIFO empty interrupt will occur when the last byte has been read and before the byte has been transmitted. FSK transmitter will finish transmitting this last byte 11 bits (73 1/3 frames) later and start the idle state if the FIFO has not been refilled. The 11 bits include the start bit, 8 bits from the FIFO and 2 idle bits.

End of transmission must be confirmed before disabling the FSK transmitter or switching to another output channel. The end of transmission can be selected by setting the FIS bit. End of transmission interrupt will occur after 2 idle state bits have been transmitted. Subsequently end of transmission interrupts occur once every 8 idle state bits.

This interrupt can also be used by the system to count the number of bits sent in the channel seizure and mark preamble before the FSK data. When the FSK transmitter is enabled, by setting the FEN bit in the FSK Control Register, and the FIFO is not written to, the first end of transmission interrupt is after 2 idle state bits (13 1/3 frames). Subsequent interrupts are once every 8 bits (53 1/3 frames).

In addition to selecting the type of interrupt the Ringer and FSK Control Register (RFC) is used to select the idle state of continuous 'mark' or continuous 'space', the 'mark' and 'space' frequency standard, and to turn on or off the transmitter. Also, a 'channel seizure' signal of alternating ones and zero's can be enabled. Refer to the description of the "Ringer and FSK Control Register (RFC)" on page 58.

Programming sequence for on-hook data transmission (channel seizure + mark + data packet):

- Transmit Channel seizure
    1. FEN initially 0 so that FSK transmit is disabled. Select end of transmission interrupt and enable. FSK interrupt. Select channel seizure as idle state.
    2. Enable transmission via FEN=1. Use end of transmission interrupt to count how many bits have been transmitted. The first interrupt occurs after two idle state bits (13 1/3 frames) have been sent.

Subsequently the interrupt occur once every 8 bits (53 1/3 frames). Wait until the desired number of channel seizure bits have been sent.

- Transmit Mark
  3. Switch to mark as the idle state. Again use end of transmission interrupt to count the number of mark bits. When switching the idle state the interrupt bit count is not affected, i.e. the bit count is not restarted but will interrupt 8 bit times after the last interrupt. Wait until the desired number of mark bits have been sent.

- Transmit Data Packet
  4. Select FIFO empty interrupt. End of transmission interrupt is disabled by the selection. Even though the FIFO is empty there will be no interrupt because the empty interrupt occurs only when the FIFO is read to empty, not when it is emptied via FIFO clear. Write to FIFO for up to 20 bytes. The first byte will be sent on the next bit boundary or the one after depending on when the byte is written.
  5. When FIFO empty interrupts, reload FIFO. Repeat as necessary until the entire message has been sent. When the FIFO empty interrupts, there are 11 bit times (73 1/3 frames) before idle state transmission will commence.

- End Transmission
  6. After the FIFO has been loaded for the last time, switch to end of transmission interrupt. Select mark as the idle state.
  7. Wait for end of transmission interrupt which occurs after 2 idle state bits have been sent after the stop bit of the last FIFO byte. If the system does not disable FSK via FEN=0, end of transmission will interrupt again once every 8 bit times.

18.0 Ringing Generator

A Ringing Generator is provided on pins R+ and R-. The output are two square waves 180 degrees out of phase. The frequency is selected with bits F1,F0 in Ringer and FSK Control Register (RFC) and can be 16, 20, 25 or 50 Hz. Setting the bit RE to “0” in the same register tri-states the drivers for both pins R+ and R-.

19.0 Supervisory Signal Detection and Cadence Measurement

Two energy detect blocks, A and B, are provided for monitoring supervisory signalling during trunk calls. Each of energy detect blocks can be assigned to an incoming channel, by programming one of the two Connect Memory Low locations 70_H and 71_H. A low and high threshold level is programmed in the Energy Detect Low and High Threshold Registers (EDLTA/B or EDHTA/B). The Energy Detect blocks are enabled by setting ENA or ENB bits in the Tone Generation and Energy Detect Control Register (TEDC) described on page 61.

The energy detect is implemented using a peak detector with an exponential attack and decay time constant of 2 msec and a 25 msec “leaky” hold time to bridge between the envelope peaks. The peak detector decays exponentially following the hold time limit.

Supervisory signalling cadence measurement is illustrated in Fig. 27. A counter is used to time the cadence of the signal. When the signal envelope crosses the energy detect high threshold at point A, the counter value,t0, is transferred to the SSCR register and the counter is reset and starts counting the next interval. The position of the signal envelope, now above the high threshold, is indicated with bit 7 of SSCR (also labelled the P bit) set to 1. An interrupt is generated and the energy detect bit in the Interrupt Status Register (INTS) is set.

At point B the low threshold limit is crossed, the SSCR register is updated with the new count, t1, and an interrupt is generated. The position of the signal envelope, now below the low threshold, is indicated with the P bit of SSCR set to 0.

For a continuous signal, such as dial tone, where there is no off time, an interrupt occurs when the counter reaches a maximum count of 508 msec. When a maximum count of 508 msec is reached the P bit can be used to determine if the interrupt was a result of a transition or a counter overflow. If the P bit remains unchanged from its previous value then the interrupt is a result of a counter overflow.

Interrupts are generated with a minimum of 4 msec (32 frames) between consecutive IRQs. If a threshold is crossed within 4 msec of the last interrupt, the interrupt will be held off and the SSCR will be updated after the 4 msec time has transpired. Refer to Fig. 27. For example, if the signal envelope crosses the threshold levels at point B and point C, then there will be an interrupt generated at point D 32 frames from point A. The SSCR is updated at the delayed IRQ point D with the last position and count, P=1 and t2, the time between points B to C.

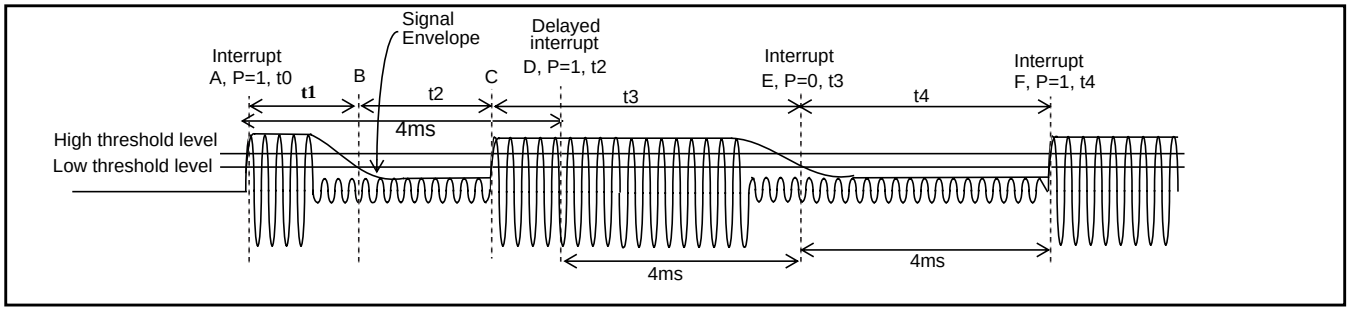


Figure 27 - Time Between Supervisory Signal Detection Interrupts ≥ 4 ms

Table 18 lists the registers which are used for the energy detect blocks.

Register	Description	Page
EDA/B	Energy Detect	page 61
EDALT/EDAHT	Energy Detect A Low and High Threshold	page 62
EDBLT/EDBHT	Energy Detect B Low and High Threshold	page 63
SSCR1/2	Supervisory Signal Cadence Registers	page 62 and page 64

Table 18 - Supervisory Signal Detection Registers

Refer to MSAN-178 note for Implementing an Algorithm for Interpreting The Measured Cadence of a Call Progress Signal by the MT90812.

20.0 Microprocessor Port

The MT90812 provides a parallel microprocessor interface for non-multiplex or multiplexed bus structures. This interface is compatible with Motorola non-multiplexed/multiplexed and Intel/National multiplexed buses.

If the IM input pin is low or not connected, the device assumes its default mode (Motorola Non-multiplexed bus). In non-multiplexed mode, the microprocessor port consists of an 8-bit parallel data bus (AD0-AD7), 10-bit address lines (A0-A9) and four control lines ($\overline{CS}$, DS, R/$\overline{W}$ and $\overline{DTA}$). The parallel microprocessor port provides the access to the control registers and the connection and data memories of the MT90812. Data Memory is read only. **The control register at location 61_H ($3E1_H$ in motorola non-muxed, 061_H in in multiplexed mode) must be initialized to 080_H.**

If the IM pin is high, the microprocessor port provides compatibility to MOTEL interface. In MOTEL interface, Motorola, National, and Intel Multiplexed Bus CPU can be connected to the device. In this mode, the interface pins are: AD<7:0> (data and address), AS/ALE (Address Latch Enable/ Address Strobe), DS/$\overline{RD}$ (Data Strobe/ Read), R/$\overline{W}$ \ $\overline{WR}$ (Read/Write\Write), $\overline{CS}$ (Chip Select) and $\overline{DTA}$ (Data Acknowledgment). The MOTEL circuit automatically identifies the type of CPU Bus connected to the MT90812. This circuit uses the level of the DS/ $\overline{RD}$ input pin at the rising edge of the AS/ALE to identify the appropriate bus timing connected to the MT90812. If DS/$\overline{RD}$ is low at the rising edge of AS/ALE then Motorola bus timing is selected. If DS/$\overline{RD}$ is high at the rising edge of AS/ALE, then Intel bus timing is selected. See Figures 48 to 50 for each CPU interface timing.

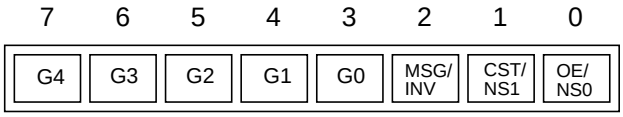
A MT90812 memory address, in multiplexed microport mode, consists of two portions. The higher order bits(3) originate from the Control Register. The lower order bits(8) originate from the address lines directly. The address lines A6-A0, on the Control Interface, give access to the Control Registers directly if A7 is zero, or depending on the contents of Control Register, to the High or Low sections of the Connection Memory, or to the Data Memory. Refer to “Address Memory Map” on page 12.

Interrupts can occur from D-channel Basic Receive Transmit (DBRT), FSK, Energy Detect, Conference, or Timing blocks. Two registers are provided to help the microprocessor deal with interrupts. The Interrupt Enable register (INTE), allows interrupts from each source to be enabled or disabled. The Interrupt Status register (INTS), indicates which interrupt source has generated an interrupt. For further description on the INTS and INTE registers, refer to “Interrupt Status Register (INTS)” on page 56 and “Interrupt Enable Register (INTE)” on page 57, respectively.

21.0 Connection Memory Bits

Locations in the Connection Memory are associated with the local TDM output streams and the Expansion Bus streams. It also determines whether individual output channels are in Message Mode, allows individual output channel to go into a high-impedance state and specifies the gain control for the outgoing channels. Refer to Section 5.2, “Data Memory and Connect Memory” for further description.

21.1 Connection Memory High

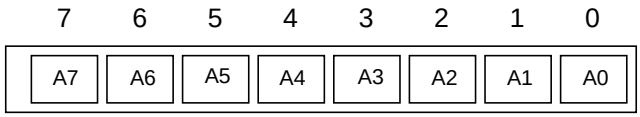


Bit	Name	Description
7-3	Channel Attenuation G4,G3, G2, G1, G0	Defines gain from +3 to -27 dB in steps of 1dB, as well as -∞ dB for the outgoing channel 0000 = +3 dB 0001 = +2 dB 0010 = +1 dB 0011 = 0 dB 0100 = -1 dB 0101 = -2 dB 0110 = -3 dB 0111 = -4 dB 1000 = -5 dB 1001 = -6 dB 1010 = -7 dB 1011 = -8 dB 1100 = -9 dB 1101 = -10 dB 1110 = -11 dB 1111 = -12 dB 10000 = -13dB 10001 = -14dB 10010 = -15dB 10011 = -16dB 10100 = -17dB 10101 = -18 dB 10110 = -19 dB 10111 = -20 dB 11000 = -21 dB 11001 = -22 dB 11010 = -23 dB 11011 = -24 dB 11100 = -25 dB 11101 = -26 dB 11110 = -27 dB 11111 = -∞ dB
2	Message Channel/ Conference Inversion Bit	When 1, the contents of the corresponding location in Connection Memory Low are output on the location’s channel. When 0, the contents of the corresponding location in Connection Memory Low act as an address for the Data Memory and so determine the source of the connection to the location’s channel and stream. Conference Inversion Bit: (For Conference address locations 60-6E) The inversion bit allows for every other channel in a conference to be inverted. This reduces noise due to reflections and line impedance mismatch.
1	CST (address locations other than 60-6E)	This bit is used to select minimum(low) or constant(high) delay, on a per channel basis.
0	Output Enable (address locations other than 60-6E)	If the ODE pin is high and bit 5 of the Control Register is 0, then this bit enables the output driver for the location’s channel and stream. This allows individual channels on individual streams to be made high-impedance, allowing switching matrices to be constructed. A 1 enables the driver and a 0 disables it.
1-0	NS1-NS0 (for Conference address locations 60-6E)	Channel Noise Suppression 00 = no noise suppression 01 = 9/4096 (A-Law), 9/8159 (u-Law) 10 = 16/4096 (A-Law), 16/8159 (u-Law) 11 = 32/4096 (A-Law), 32/8159 (u-Law)

At locations 60 to 6E, Connect Memory High is used to specify the Conference incoming channel attenuation and Noise Suppression. For these locations bits 7-3 are used as incoming channel attenuation, bits 1-0 are used for Noise Suppression bits and bit 2 is not used.

21.2 Connection Memory Low

The CML is defined as follows:



Bit	Name	Description
7-5	Data Memory Block Address Bits	The number expressed in binary notation on these 3 bits is the number of the Data Memory block for the source of the connection. Bit 7 is the most significant bit.
4-0	Channel Address Bits	The number expressed in binary notation on these 5 bits is the number of the channel which is the source of the connection. Bit 4 is the most significant bit. e.g., if bit 4 is 1, bit 3 is 0, bit 2 is 0, bit 1 is 1 and bit 0 is 1, then the source of the connection is channel 19.

Connection Memory Low is used to specify the source for the outgoing channels and connect the Conference, Energy Detect and DBRT blocks to incoming channels. Table 19 lists the Data Memory Block and Channel Address Bits used in Data Memory Addresses.

At locations 60 to 6E, Connect Memory Low is used to identify channels in a conference. At location 6F, Connect Memory Low is used to identify which channel is to be routed to the D-Channel RX FIFO. Locations 70 and 71h are used to identify the channel routed to the Energy Detect A and B blocks, respectively.

Hex Address A7-A5	Hex Address A4-A0	Local/Expansion Data Memory	Description
000	00-1F	Sti0 32 Channels	Sti0 32 Channels
001	00-1F	STi1 32 Channels	STi1 32 Channels
010	00-1F	Tones(32)	Tone Generator output
011	00-0E	CONFout(15),	Conference Output
011	0F	unused	unused(1)
011	10	DCHout(1)	Output from the D-channel TX FIFO buffer. Allows D-channel TX buffer to be directed to any outgoing channel.
011	11-1F	unused(14)	unused(14)
100	00-1F	Ei1 32 Channels	Expansion Bus Block 1
101	00-1F	Ei2 32 Channels	Expansion Bus Block 2
110	00-1F	Ei3 32 Channels	Expansion Bus Block 3
111	00-1F	Ei4 32 Channels	Expansion Bus Block 4

Table 19 - Data Memory Addressing

22.0 Detailed Register Descriptions

The first page of 128 locations of memory contains the control registers. The control registers are accessed independent of the setting of the memory select bits when in multiplexed mode by setting external address bit A7 to 0. In non-multiplexed mode the control registers are accessed with A7,A8 and A9 set to 1 (as described in Section 5.1). The control registers and their addresses are listed in Table 20.

Hex Address A6-A0	Name	Description	Page
00	AMS	Address Memory Select	page 53
01	CTL	Control	page 54
02	TC	Timing Control	page 55
03	OCC	Output Clocking Control	page 56
04	INTS	Interrupt Status	page 56
05	INTE	Interrupt Enable	page 57
06	RFC	Ringer and FSK Control	page 58
07	FSKM	FSK Transmit Memory	page 59
08	CONFO	Conference Overflow Status	page 59
09	CC	Conference Control	page 60
0A-0F	-	Unused (6)	
10	TEDC	Tone Generation and Energy Detect Control	page 61
11	EDALT	Energy Detect A - Low Threshold	page 62
12	EDAHT	Energy Detect A - High Threshold	page 62
13	SSCA	Supervisory Signal Cadence A	page 63
14	EDBLT	Energy Detect B - Low Threshold	page 63
15	EDBHT	Energy Detect B - High Threshold	page 63
16	SSCB	Supervisory Signal Cadence B	page 64
17-1F	-	Unused (9)	
20-26	LTC1-7	Low Tone Coefficient 1-7	page 64
27		unused	
28-2E	HTC1-7	High Tone Coefficient 1-7	page 64
2F		unused	
30-3E	CPC1-15	Conference Party Control 1 - 15	page 65
3F	unused	unused	
40	DRXIT	D-channel Receive Interrupt Threshold	page 66
41	DRXC	D-channel RX Control	page 66
42	DRXS	D-channel BR Status	page 68
43	DRXOUT	D-channel RX FIFO Output	page 68
44	DTXIN	D-channel TX FIFO Input	page 68
45	DTXC	D-channel TX Control	page 69
46-4F	unused	unused(10)	

Hex Address A6-A0	Name	Description	Page
50	HC1	HRA Control 1	page 70
51	HC2	HRA Control 2	page 71
52	HC3	HRA Control 3	page 72
53	HLO1	HRA Lock Out 1	page 72
54	HLO2	HRA Lock Out 2	page 73
55	HS1	HRA Status 1	page 73
56	HS2	HRA Status 2	page 74
57	HS3	HRA Status 3	page 74
58	HS4	HRA Status 4	page 75
59-5F	unused	unused(7)	
60	reserved	reserved	
61	reserved	**must be iniitialized to 80_H**	
62-7F	unused	unused(30)	

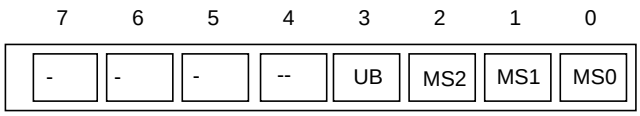
Table 20 - Control Registers

Test Register 1 and 2 are at locations 60_H and 61_H respectively. Location 61_H must be initialized to 80_H.

22.1 Address Memory Select Register (AMS)

The Address Memory Select register (AMS) selects Data/Connect Memory for read/write operations in microport multiplexed mode. The AMS register also allows the microport read of specific Data Memory locations from their lower/upper bytes.

Read/Write Address is: 000_H
Reset Value is: 00_H

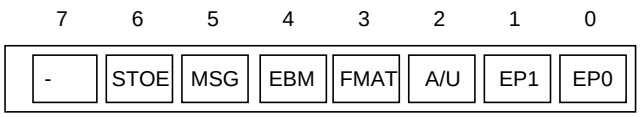


Bit	Name	Description
7-4	(unused)	
3	UB	When 1, the next reads of Data Memory locations associated with tones and conference output are from the upper bytes of these locations. If 0 the reads are from the lower bytes.
2-0	Memory Select	When 000, Local Data Memory is selected for read operation. When 001, Expansion Data Memory is selected for read operation. When 010, Local Connection Memory Low is selected for read or write operations. When 011, Expansion Connection Memory Low is selected for read of write operations. When 100, Local Connection Memory High is selected for read or write operations. When 101, Expansion Connection Memory High is selected for read or write operations. Note: Setting of the memory select bits is required only when operating the microprocessor port in multiplexed mode.

22.2 Control Register (CTL)

The Control register (CTL) selects Data/Connection Memory and defines Expansion bus position.

Read/Write Address is: 001_H
Reset Value is: 00_H



Bit	Name	Description
7	-	**Unused**.
6	Serial Stream Output Enable	**Output enable for the serial outputs**. If this input is low, STo0, STo1, EST0, EST1 are high impedance. If this input is high, each channel may still be put into high impedance state by using per channel control bit in the Connection Memory.
5	Message Mode	When 1, the contents of the Connection Memory Low are output on the Serial Output stream except when the OE bit in CMH for the corresponding channels is low or the ODE pin is low. When 0, the Connection Memory bits for each channel determine what is output.
4	EBM	**EBUS Mode select**. Selects IDX Link Mode if low or TDM Link mode if high.
3	FMAT	**PCM format select**. Selects CCITT PCM coding if high, or SIGN MAGNITUDE PCM if low.
2	Alaw/$\overline{\mu law}$	**Companding Law selection**. A-Law is selected when high. μ-Law is selected when low.
1 - 0	EBUS Position / EBUS Data Rate	When EBUS is in IDX Link Mode, EP0 and EP1 define the sequence of channels on the expansion bus with respect to the frame pulse. (The four positions are shown as A to D in Figure 7 on page 9) 00 selects the output to be the first of every four channels. 01 selects the output to be the second of every four channels. 10 selects the output to be the third of every four channels. 11 selects the output to be the fourth of every four channels. When EBUS is in TDM Link mode, EP0 and EP1 define the data rate of the expansion bus. 00 = 2.048 Mb/s. 01 = 4.096 Mb/s. 10 = 8.192 Mb/s. The clock rate is determined by the Clock mode selected by bits CR1-0 in the Timing Control Register (TC). Refer to description in “Timing and Clock Control” starting on page 24.

22.3 Timing Control Register (TC)

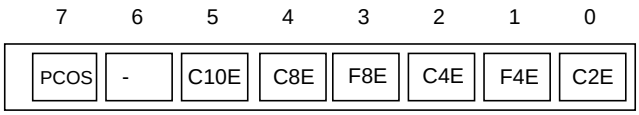
The timing control register is configured as follows:

Read/Write Address is: 002_H Reset Value is: 20_H		
Bit	**Name**	**Description**
7	WDE	**Watchdog Enable**. When 0, disables the Clock Watchdog Circuit. When 1, the Clock Watchdog Circuit will generate an interrupt in the event of the loss of the clock at the C8 input. See “Watchdog Timer” on page 28.
6	FPO	**FPO.** Selects ST-Bus or GCI frame alignment and polarity for outgoing frame pulse generation. When 0, ST-Bus Frame Pulses are generated on F8o and F4o. When 1, GCI frame pulses are generated and the polarities of C4o and C8 are inverted. The outgoing frame pulse mode is independent of the incoming frame pulse mode.
5-4	CR1-0	**Input Clock Reference.** 00 C4 01 C8 10 C8P (default) 11 C16 Selects one of four possible clock references, C4, C8, C8P, or C16. C4 is not valid when the PLL is not enabled. The MT90812 requires at least an 8M clock internally. When the C4 input clock is selected the 8.192 Mhz clock is derived from the PLL. When C8P is selected as the input clock reference no frame pulse is used and the MT90812 generates F4o and F8o when they are enabled. Refer to Table 9, “Clock Modes,” on page 25.
3	HMVIP	**HMVIP Select.** With C16 as Input Clock Reference, when HMVIP=1, enables the HMVIP Frame Alignment interface. Otherwise, the device operates in ST-BUS/GCI mode.
2	PE	**PLL Enable**. When 0, disables the PLL. When 1, enables the PLL. With the PLL off, C10 is disabled and C4 as an input clock reference is not valid.
1	PMS	**PLL Mode Select**. With PE=1, when PMS = 1 the PLL operates in Master Mode. When PMS = 0, the PLL operates in Slave mode. Default Slave Mode.
0	PCS	**PLL Clock Select**. With PE=1, when PCS = 1 selects clocks generated from the PLL for use in STi/o0, STi/o1 and incoming EST0/1 TDM streams, C2o, F4o and C4o. Otherwise the clocks are derived directly from the Input Clock Reference. With C4 as the input clock reference, EST0/1, 4 and 8 Mb/s timing, is generated from the PLL independent of PCS. Refer to Table 9, “Clock Modes,” on page 25 and Section 9.2.5.

22.4 Output Clocking Control Register (OCC)

The register is configured as follows:

Read/Write Address is: 003_H
Reset Value is: 00_H

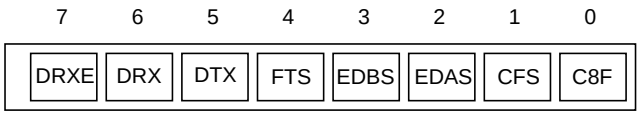


Bit	Name	Description
7	PCOS	**PLL Clock Output Select**. With PE=1, when PCS = 1 selects clocks generated from the PLL for use in outgoing EST1/0 TDM streams, F8o and C8o. Otherwise the clocks are derived directly from the Input Clock Reference. With C4 as the input clock reference, EST0/1, 4 and 8 Mb/s timing, as well as F8o and C8o, are generated from the PLL independent of PCOS. Refer to Table 9, “Clock Modes,” on page 25 and Section 9.2.5
6	-	**Unused**.
5	C10E	**C10 Output Enable**. When 0, C10o is high impedance. When 1 and the PLL is enabled, C10o is enabled.
4	C8E	**C8 Output Enable**. When 0, C8 is high impedance. When 1 and the Input Clock Reference is not C8, then C8 is enabled.
3	F8E	**F8 Output Enable**. When 0, F8 is high impedance. When 1 and the Input Clock Reference is not C8, then F8 is enabled.
2	C4E	**C4 Output Enable**. When 0, C4 is high impedance. When 1, then C4 is enabled.
1	F4E	**F4 Output Enable**. When 0, F4 is high impedance. When 1, then F4o is enabled.
0	C2E	**C2 Output Enable**. When 0, C2 is high impedance. When 1, then C2 is enabled.

22.5 Interrupt Status Register (INTS)

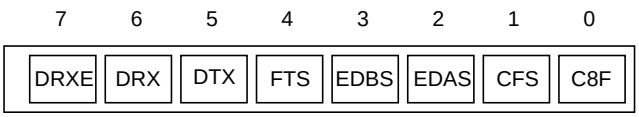
The **INTS** register is configured as follows:

Read Address is: 004_H
Reset Value is: 00_H



Bit	Name	Description
7	DRE	**D-Channel Receive FIFO Error**. Status indicated in “D-Channel BR Status (DRXS)” on page 68.
6	DRX	D-Channel Receiver attained the message length in MLI mode or the RX FIFO interrupt trigger level (number of words) in FLI mode.
5	DTX	D-Channel Transmit FIFO empty or 3/4 empty or transmission complete.
4	FTS	Memory empty status for the FSK transmit memory or end of transmission.
3	EDBS	**Energy Detect Block B interrupt**.
2	EDAS	**Energy Detect Block A interrupt**.

Read Address is: 004_H
Reset Value is: 00_H



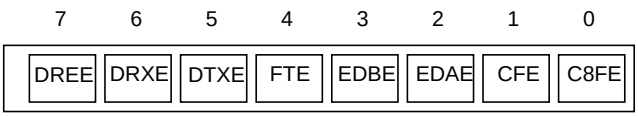
Bit	Name	Description
1	CFS	Overflow status of the conference accumulators.
0	C8F	**C8 input not present**.

This register is a read only register, which would generally be read by the external uP on a regular basis. The contents of this register indicates if an interrupt has occurred. This register is reset when read.

22.6 Interrupt Enable Register (INTE)

The **INTE** register is configured as follows:

Read/Write Address is: 005_H
Reset Value is: 00_H



Bit	Name	Description
7	DREE	**Interrupt enable for D-Channel Receive FIFO Error**. Status indicated in "D-Channel BR Status (DRXS)" on page 68
6	DRXE	**Interrupt enable for D-Channel Receive Message Length or FIFO Level**.
5	DTXE	**Interrupt enable for D-Channel Transmit.** FIFO empty or 3/4 empty and transmission complete.
4	FTE	**Enable FSK transmit memory empty interrupt or end of transmission.**
3	EDBE	**Energy Detect Block B interrupt enable.**
2	EDAE	**Energy Detect Block A interrupt enable.**
1	CFE	**Interrupt enable for conference accumulator overflow.**
0	C8FE	**Enable monitoring for presence of C8.**

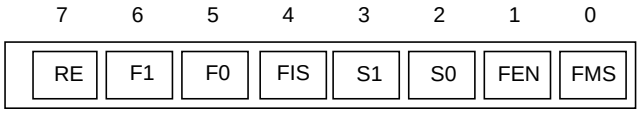
This register enables/disables the interrupts as specified in the Interrupt Status Register (INTS). Setting High the appropriate bits in this register enables the associated interrupt source. If a bit is set LOW in this register the bits in the Interrupt Status Register (INTS) are still valid but they do not cause the $\overline{IRQ}$ output to go LOW.

22.7 Ringer and FSK Control Register (RFC)

The Ringer and FSK Control register (RFC) controls the Ringing Source and FSK Transmitter.

The Ringer and FSK control register is configured as follows:

Read/Write Address is: 006_H
Reset Value is: 00_H



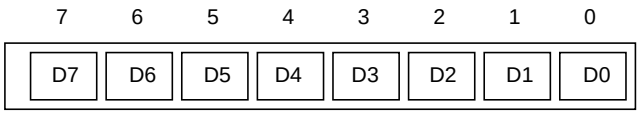
Bit	Name	Description
7	RE	**Ringer Enable bit**.
6-5	F1,F0	**Selects the frequency of the square wave output of the Ringing Generator**. The Ringer outputs are the R+ and R- pins. 00 = 16 Hz square wave 01 = 20 Hz square wave 10 = 25 Hz square wave 11 = 50 Hz square wave
4	FIS	**FSK Interrupt Select**. 0 = interrupt generated when the TX FIFO is empty. 1= interrupt generated at the end of transmission.
2-3	S1, S0	00 = Idle state is continuous ‘space’ (logic zero). 01 = Idle state is continuous ‘mark’ (logic one). 10 = Turn on channel seizure signal. 11 = unused.
1	FEN	**FEN=0 disables the FSK Transmitter and clears the FSK FIFO**. Writing to FSK FIFO while FEN=0 will have no effect. When 1 the FSK transmitter is enabled, and the FSK transmit memory can be written to. When the memory is empty, the idle state set by bits S1-0, is output until the transmit memory is reloaded or the transmitter is turned off.
0	FMS	0 = Mark and Space frequencies of 1200 Hz and 2200 Hz corresponding to Bell 202 standard. 1 = Mark and Space frequencies of 1300 Hz and 2100 Hz corresponding to CCITT V.23 standard.

The Ringer and FSK Control Register (RFC) is used to select the type of interrupt, the idle state, the ‘mark’ and ‘space’ frequency standard, and to turn on or off the transmitter. The idle state of continuous ‘mark’ or continuous ‘space’ or a ‘channel seizure’ signal of alternating ones and zero’s can be selected. Changing S1, S0 bits will change the idle state on the next bit boundary. At 1200 baud, one bit corresponds to $6^2/_3$ frames.

22.8 FSK Transmit Memory (FSKM)

The register is configured as follows:

Write Address is: 007_H
Reset Value is: 00_H



Bit	Name	Description
7-0	D7-D0	**TX FIFO buffer**. D7 is the MSB.

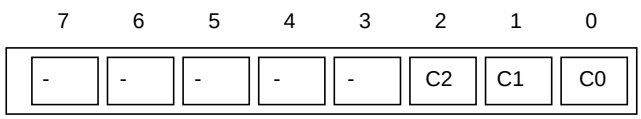
A system write to the TX FIFO buffer is performed by addressing location 07_H of the Control Register page. Up to 20-bytes can be written to the FIFO. The length of the message is determined by the number of bytes written to the FIFO. The FSK output is memory mapped to address $5F_H$ as shown in Table 3 on page 14

Refer to “Frequency Shift Keying (FSK) Transmitter” on page 45.

22.9 Conference Overflow Status Register (CONFO)

The register is configured as follows:

Read Address is: 008_H
Reset Value is: 00_H



Bit	Name	Description
7-3	unused	**Unused**.
2-0	C2-C0	**Conference ID number**. Valid conference ID numbers are: 001 = conference 1 010 = conference 2 011 = conference 3 100 = conference 4 101 = conference 5

This register is a read only register. When a conference overflow occurs the Conference overflow bit in the Interrupt register will be set and the conference ID will be stored in this register. The conference ID will be that of the conference which had an accumulator overflow. The Conference ID corresponds to the Conference ID numbers programmed in the Conference Party Control registers. Refer to Section 22.20.

The Conference ID in this register will not be updated again until it is reset. The register is reset following a read of the register or resetting the conference block or MT90812 device.

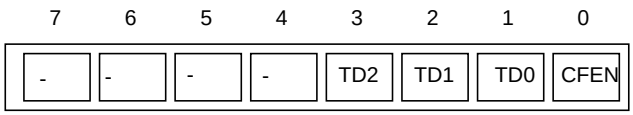
Following an IRQ being asserted by the conference circuit, the INT would generally be read by the external uP. Reading the Interrupt Status Register (INTS) will clear the Conference Overflow bit. Further conference overflows do not trigger an interrupt until the conference overflow bit is cleared. The conference overflow interrupt is maskable using the Interrupt Enable Register (INTE). The conference interrupt mask does not disable updates of the CONFO register.

22.10 Conference Control Register (CC)

The Conference Control register is used in conjunction with the Conference Party Control registers for setting up conferences.

The **CC** register is configured as follows:

Read/Write Address is: 009_H
Reset Value is: 00_H



Bit	Name	Description
7-4	unused	
3-1	TD2-0	**Tone Duration**. Specifies a tone duration from 0.125 seconds to 1.0 seconds in steps of 0.125 seconds. With the addition of a party to a conference, by programming one of the Conference Party Control registers with the appropriate conference ID, the insertion tone will be added to the conference if the IT bit is set. The tone duration is set as follows: 000 = 0.125s 001 = 0.250s 010 = 0.375s 011 = 0.500s 100 = 0.625s 101 = 0.750s 110 = 0.875s 111 = 1.000s
0	CFEN	**0 = Reset for Conference Block**. **1= Enables the conference circuit**.

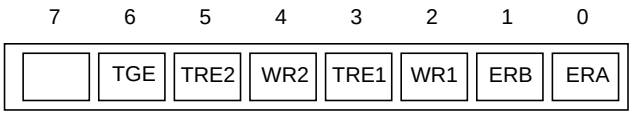
The Conference circuit can be reset with CFEN bit =0. With the Conference circuit reset there is no output generated for all the 15 conference output locations in Data Memory.

22.11 Tone Generation and Energy Detect Control Register (TEDC)

The Tone Generation and Energy Detect register controls the two tone ringers and both A and B energy detect modules.

The **TEDC** register is configured as follows:

Read/Write Address is: 010_H
Reset Value is: 00_H



Bit	Name	Description
7	unused	
6	TGE	**0 = Reset for Tone Generation Circuit**. **1 = Enables Tone Generation**. Tone Generation must be enabled for FSK transmission and Tone Ringer operation.
5	TRE2	**Tone Ringer Enable bit**. For Programmable Tone Generator 2. 1 = The tone ringer generator is enabled using the coefficients for programmable tone generator 2 as well as the WR2 control bit. 0 = The tone ringer generator 2 is disabled. With Tone Ringer 2 disabled the 2nd programmable Coefficients are used to generate DTMF signalling instead of the squarewave ringing tone.
4	WR2	**Warble Rate bit**. For Programmable Tone Generator 2. 1 = The tone ringer circuit will toggle between the two programmed frequencies at a 5 Hz rate. 0 = The tone ringer warble rate is 10 Hz.
3	TRE1	**Tone Ringer Enable bit**. For Programmable Tone Generator 1.
2	WR1	**Warble Rate bit**. For Programmable Tone Generator 1.
1	EDENB	**1 = Enable for Energy Detect B circuit**.
0	EDENA	**1 = Enable for Energy Detect A circuit**.

Of the 7 programmable tone generators the first two can be used to provide dual frequency squarewave ringing signal. TRE1/WR1 and TRE2/WR2 are used to control Tone Ringer generator 1 and 2, respectively. Refer to Tone Ringer description on page 44.

Each energy detect module monitors the signal for the selected incoming channel. Locations 71_H and 72_H of CM are used to specify the incoming channel for EDA and EDB, respectively. An interrupt is generated and the energy detect flag is set when the signal exceeds the threshold set in the Energy Detect A/B Low/High Threshold register. A reset is performed by resetting the EDENA/B bit. During a reset the peak detector value and energy detect flag are set to zero.

The Tone Generation circuit can be enabled with TGE bit set to 1. With the circuit reset there is no output generated for all the 32 tones including the Tone Ringers and FSK transmitter output.

22.12 Energy Detect A - Low Threshold (EDALT)

The **EDALT** register is configured as follows:

Read/Write Address is: 011_H
Reset Value is: 00_H

7	6	5	4	3	2	1	0
-	ET6	ET5	ET4	ET3	ET2	ET1	ET0

Bit	Name	Description
7	Unused	
6-0	Low Threshold	**Energy Detect Low Threshold**. PCM sign-magnitude format with no sign bit. Bit 6 = MSB.

ET0-ET3 encode the PCM step number while ET4-ET6 encode the PCM chord number.

22.13 Energy Detect A - High Threshold (EDAHT)

The **EDAHT** register is configured as follows:

Read/Write Address is: 012_H
Reset Value is: 00_H

7	6	5	4	3	2	1	0
-	ET6	ET5	ET4	ET3	ET2	ET1	ET0

Bit	Name	Description
7	Unused	
6-0	High Threshold	**Energy Detect High Threshold**. PCM sign-magnitude format with no sign bit. Bit 6 = MSB.

ET0-ET3 encode the PCM step number while ET4-ET6 encode the PCM chord number.

22.14 Supervisory Signal Cadence Register A (SSCA)

Read Address is: 013_H
Reset Value is: 00_H

7	6	5	4	3	2	1	0
p	t6	t5	t4	t3	t2	t1	t0

Bit	Name	Description
7	p	Position with respect to high and low thresholds. 1 = above high threshold. 0 = below low threshold.
0-6	t6-t0	Cadence of the supervisory signal ranging from 0 to 508 msec in units of 4 msec.

The SSCA register is used to store the cadence information for Energy Detect block A. Refer to “Supervisory Signal Detection and Cadence Measurement” on page 47.

The counter is used to time the cadence of the signal. When the signal envelope crosses the energy detect threshold the counter starts. When the other threshold limit is crossed the P bit is updated, the counter value is transferred to bits t6-t0, in this SSC register and an interrupt is generated.

The P bit specifies the current envelope position with respect to the high and low thresholds. When P is set this indicates the signal envelope has crossed above the high threshold otherwise it had crossed below the low threshold.

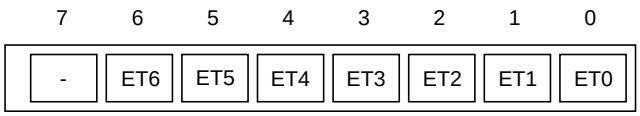
The count is stored in 4 msec intervals and ranges from 0 to 508 msec.

For a continuous signal, such as dial tone, where there is no off time, an interrupt is generated when the counter reaches a maximum count of 508 seconds or $7F_H$. The continuous signal is indicated by the P bit maintaining the same value.

22.15 Energy Detect B - Low Threshold Register (EDBLT)

The **EDBLT** register is configured as follows:

Read/Write Address is: 014_H
Reset Value is: 00_H



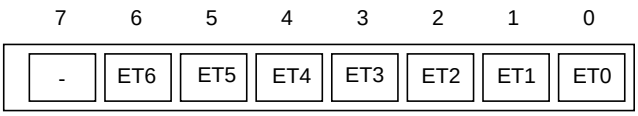
Bit	Name	Description
7	Unused	**Reserved**.
6-0	Low Threshold	**Energy Detect Low Threshold**. PCM sign-magnitude format with no sign bit. Bit 6 = MSB.

ET0-ET3 encode the PCM step number while ET4-ET6 encode the PCM chord number.

22.16 Energy Detect B - High Threshold Register (EDBHT)

The **EDBHT** register is configured as follows:

Read/Write Address is: 015_H
Reset Value is: 00_H

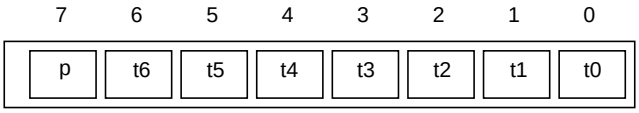


Bit	Name	Description
7	Unused	**Reserved**.
6-0	High Threshold	**Energy Detect High Threshold**. PCM sign-magnitude format with no sign bit. Bit 6 = MSB.

ET0-ET3 encode the PCM step number while ET4-ET6 encode the PCM chord number.

22.17 Supervisory Signal Cadence Register B (SSCB)

Read Address is: 016_H
Reset Value is: 00_H



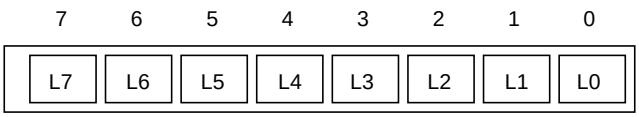
Bit	Name	Description
7	p	**Position with respect to high and low thresholds**. 1 = above high threshold. 0 = below low threshold.
0-6	t6-t0	Cadence of the supervisory signal ranging from 0 to 508 msec in units of 4 msec.

The SSCB register is used to store the cadence information for Energy Detect Block B. Refer to the description of the “Energy Detect B - Low Threshold Register (EDBLT)” on page 63.

22.18 Low Tone Coefficient Registers 1-7 (LTC1-7)

The seven **LTC** registers are configured as follows:

Read/Write Addresses are: $20\text{-}26_H$
Reset Value is: 00_H

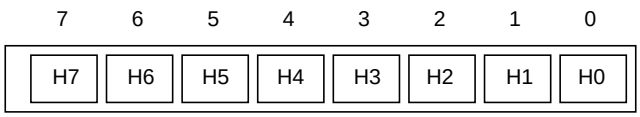


Bit	Name	Description
0-7	L0-L7	**Low Tone Coefficient**.

22.19 High Tone Coefficient Registers 1-7 (HTC1-7)

The seven **HTC** registers are configured as follows:

Read/Write Addresses are: $28\text{-}2E_H$
Reset Value is: 00_H



Bit	Name	Description
0-7	H0-H7	**High Tone Coefficient**.

Each of the seven programmable Tone Generators has a Low and High Tone Coefficient Register used to program the two tone frequencies. Frequencies for the programmable tone generators can be specified according to one of three formula’s, depending on what range the coefficient value is in, as shown in Table 14.

The coefficient is an integer value from 0 to 255. If a single tone is desired then one of the registers is programmed to zero. A tone output is disabled if both low and high coefficient registers are programmed to zero.

Of the 7 programmable tone generators the first two can also be used to provide dual frequency squarewave ringing signals. Tone Ringer enable bits, TRE1 and TRE2, in the TEDC register, enable the generation of the squarewave ringing signals by the two Tone Ringer circuits. The Tone Generator and Tone Ringer functions are described in Section 16.0

22.20 Conference Party Control Register (CPC1-15)

The **Conference Party Control** register contains the conference ID, start bit, insertion tone enable and outgoing channel attenuation.

The register is configured as follows:

Read/Write Address is: 30-3EH
Reset Value is: 00_H

7	6	5	4	3	2	1	0
C2	C1	C0	-	ST*	IT*	GC1	GC0

Bit	Name	Description
7-5	C2-C0	**Conference ID number** 000 = null conference 001 = conference 1 010 = conference 2 101 = conference 3 100 = conference 4 101 = conference 5 111 = clear all conferences
4	unused	
3	ST	**Start Conference Setting**. The **ST** bit for the **first** party programmed for a conference will remove any other parties that may have been previously programmed for that conference. This is implemented at the time the Conference Party Control Register is updated and the state of the ST bit is not actually stored in the register.
2	IT	I**nsertion Tone Enable**.
1-0	GC1-GC0	**Outgoing Gain Control** 00 = 0 dB 01 = -3 dB 10 = -6 dB 11 = -9 dB

The conference block provides conference call capability in the MT90812 and supports a total of 15 parties maximum, distributed over up to 5 conferences, i.e. 1x15 parties, 3x5 parties, 5x3 parties etc. Each of the 15 parties are associated to a conference by programming the corresponding Conference ID number.

As a party is added to a conference, if the insertion tone bit (IT) is set, all channels connected in a conference will have the tone added to the conference output. The DM address of the desired tone must be programmed at location $6F_H$ of CML, ($16F_H$ non-mux mode, EF_H for mux-mode addressing). The PCM data from the specified Data Memory location will be added to the conference output for a specified tone duration.

The IT bit will be set for the duration of the tone added to the conference. Reading any of the CPC registers in a particular conference, will show the IT bit set for that time.

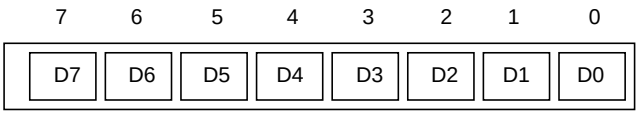
Channel Attenuation is provided on incoming and outgoing channels in a conference. The incoming channel attenuation is set in CMH for the specific conference party. The outgoing gain is applied to the output of the conference block before it is written to the Data Memory output conference location.

Refer to “Conferencing” on page 18.

22.21 D-Channel Receive Interrupt Threshold (DRXIT)

The register is configured as follows:

Read/Write Address is: 40_H
Reset Value is: 00_H



Bit	Name	Description
7-0	D7-D0	**Message Length Interrupt Mode**. D-Channel Receive Message Length 1-256 bits. FIFO Level Interrupt Mode: D5-D0 used to specify FIFO Level of 1-32.

The D-Channel Receiver Interrupt Threshold is specified in two ways depending on whether Message Length Interrupt Mode or FIFO Level Interrupt Mode is used.

22.21.1 Message Length Interrupt Mode

An interrupt is generated when a message of N bits is received, where N is the message Length in bits specified by D7-D0. D7 is the MSB. For example, 00_H corresponds to a bit length of 1 and FF_H corresponds to a bit length of 256.

The message length count is the number of bits between the start bit and the parity bit or stop bit.

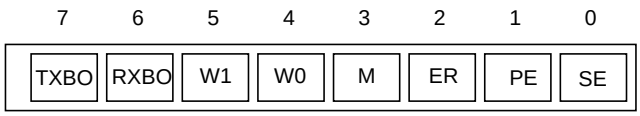
22.21.2 FIFO Level Interrupt Mode

An interrupt is generated when there are N bytes in the FIFO, where N is specified by D5-D0. D5 is the MSB. For example, 01_H corresponds to an interrupt level of 1 byte in the FIFO and 20_H corresponds to an interrupt level of 32 bytes in the FIFO.

22.22 D-Channel RX Control (DRXC)

The register is configured as follows:

Read/Write Address is: 41H
Reset Value is: 00_H



Bit	Name	Description
7	TXBO	**Transmitter Bit Order**. When '0' the first bit transmitted on the TDM channel is the LSB read on the microport data bus (D0). When '1' The RX-FIFO will maintain the same bit ordering as an access to DM. That is first bit transmitted in the TDM channel is the MSB read on the D7 of the microport data bus.
6	RXBO	**Receiver Bit Order**. When '0' the first bit Received on the TDM channel is the LSB read on the microport data bus (D0) When '1' the RX-FIFO will maintain the same bit ordering as an access to DM. That is first bit received on the TDM channel is the MSB read on the D7 of the microport data bus.
5-4	W1-W0	**Data Rate** 00 = 1 bit per frame 01 = 2 bits per frame 10= 8 bits per frame
3	M	**1 = Message Length Interrupt Mode**, i.e. Message oriented, or Message oriented with parity. **0 = FIFO Level Interrupt Mode**, i.e. Unframed, Byte oriented, or Byte oriented with parity.
2	ER	**Enable Receiver**. If 0, clears RX FIFO and resets counter. When ER=0, data is undefined when a RX FIFO read is performed. ER= 1, the Receiver is enabled.
1	PE	**Parity Enable**. In MLIM, if 0 the receiver does not expect the Parity bit. If 1 the receiver expects the Parity bit following the message bits and before the stop bit. In FLIM, when SE=1 and PE = 1 the receiver expects a parity bit per message byte. Otherwise no parity bit is expected. If parity is enabled then an even number of logic 1's is expected in the data words and parity bit.
0	SE	**Start and Stop bit Enable**. In FLI mode, if SE=0 then no start and stop bits are expected. If SE=1 then start and stop bits are expected in each message byte. In MLI mode Start and Stop bits are always expected.

The Enable bit for the RX FIFO is used to disable all the DBR circuitry including the transfer of data from DM to the RX. If there is a read of the RX FIFO while it is disabled then the data is undefined.

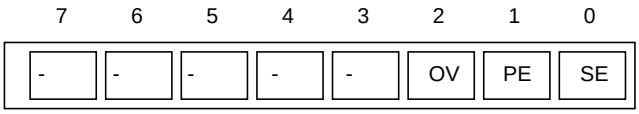
In MLI mode, when the DBR is enabled the receiver identifies the first low bit as the start bit and then collects bits as specified by the data rate, 1,2 or 8 bits per frame.

In FLI Mode when the ER bit is set the receiver transfers either 1,2 or 8 bits to the RX from Data Memory. If S=1 then the Start and Stop bits are expected on a per byte basis. If S=0 reception starts immediately after ER is set.

22.23 D-Channel BR Status (DRXS)

The register is configured as follows:

Read Address is: 42_H
Reset Value is: 00_H

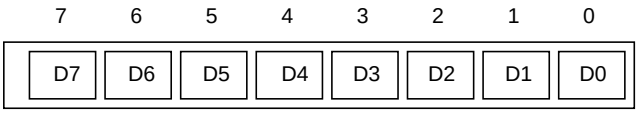


Bit	Name	Description
7-3	-	**Unused**.
2	OE	**RX Overrun Error**. Gets set when writing to a full FIFO.
1	PE	**RX Parity Error**.
0	SE	**RX Stop bit Error**.

22.24 D-Channel RX FIFO Output (DRXOUT)

The register is configured as follows:

Read Address is: 43_H



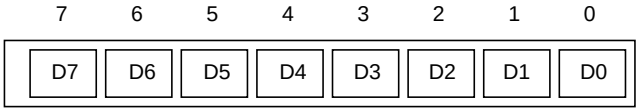
Bit	Name	Description
7-0	D7-D0	**Next data byte in the RX FIFO buffer**. D7 is the MSB.

The receiver transfers incoming data for a specified channel to the RX FIFO. The D-Channel RX channel is identified in address 70_{HEX} of Connect Memory Low (refer to Section 5.3). The data in this channel is transferred to the RX FIFO buffer. A read of control register D-Channel RX FIFO Output (DRXOUT) at 43_{HEX} accesses the next data byte in the RX FIFO buffer.

22.25 D-Channel TX FIFO Input (DTXIN)

The register is configured as follows:

Write Address is: 44_H



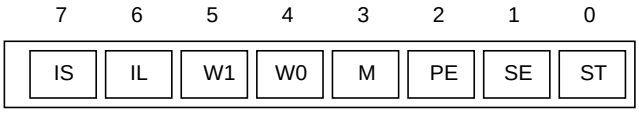
Bit	Name	Description
7-0	D7-D0	**TX FIFO buffer**. D7 is the MSB.

A system write to the TX FIFO buffer is performed by addressing location 44_{HEX} of the Control Register page. Up to 32 bytes can be written to the FIFO. The length of the message is determined by the number of bytes written to the FIFO. If N-bytes are written to this location and the ST bit in the D-Channel Receive Interrupt Threshold (DRXIT)is set, the message transmitted will be N-bytes long. Refer to “Transmitter Operation” on page 33.

22.26 D-Channel TX Control (DTXC)

The register is configured as follows:

Read/Write Address is: 45_H
Reset Value is: 00_H



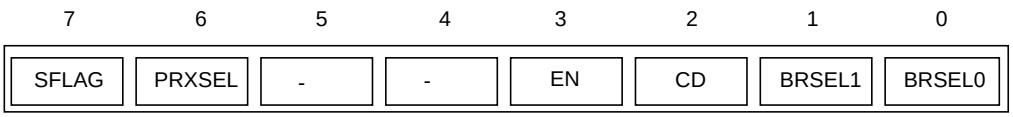
Bit	Name	Description
7	IS	**TX FIFO Interrupt Select**. When DTXE=1 and IS=0 then when the TX FIFO is empty or 3/4 empty (as selected by IL bit) an interrupt is generated.When DTXE=1 and IS=1 then an interrupt is generated when the transmission has ended.
6	IL	I**nterrupt Level**. 0 = interrupt generated when the TX FIFO is empty. 1= interrupt generated when the TX FIFO is 3/4 empty, when there are 8 bytes remaining.
5-4	W1-W0	**TX Data Rate** 00 = 1 bit per frame 01 = 2 bits per frame 10= 8 bits per frame
3	M	**1 = Message Length Interrupt Mode**, i.e. Message oriented, or Message oriented with parity. **0 = FIFO Level Interrupt Mode**, i.e. Unframed, Byte oriented, or Byte oriented with parity.
2	PE	**Parity Enable**. If 0 disable Parity bit. if PE =1 then enable Parity Bit. In FLI mode parity can be enabled only if the start and stop bits are used, i.e. S=1.
1	SE	**Start and Stop bit Enable**. In FLI mode, if 0 transmit message without including start, parity and stop bits. If 1 transmit message with start and stop bits; also transmit parity according to PE bit. In MLI mode start and stop bits are always used.
0	ST	**Start Transmitter**. ST=1 starts transmission of the message following a write to the TX FIFO. ST=0 clears the FIFO and resets its pointers.

The Transmitter Bit Order (TXBO) bit resides in the DRXC register described in Section 22.21.

22.27 HRA CTRL Register 1(HC1)

The register is configured as follows:

Read/Write Address is: 50_H
Reset Value is: 01_H

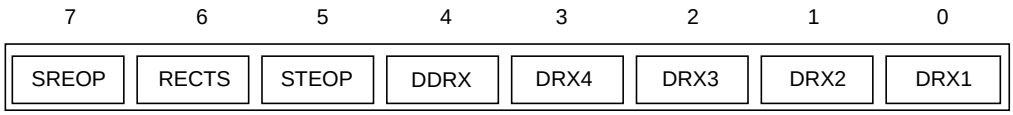


Bit	Name	Description
7	SFLAG	**Software Controlled Flag Detect (SFLAG)**. SFLAG is used to allow the system to inject a flag (indicating that a peripheral request-to-send has been detected). This bit can be written asynchronously, has exactly the same effect as the normal flag generated by the Auto-hunt circuitry, and is cleared automatically by the RX circuitry when it has been used. On reset, this bit is cleared.
6	PRXSEL	**Present Receive Channel Select (PRXSEL)**. Normally low. This bit is set high if the receive channel is to be selected via DRXi; unlike DDRX, however, CTS is not disabled and RXCHNL and RXACT are not held high. Instead, the receiver can be exercised by manipulating SREOP and SFLAG in a manner similar to normal multiplexed operation. Primarily intended as a test mode. On reset, this bit is cleared.
5-4	-	**Unused**.
3	EN	**ENABLE HRA**. If 0, disables HRA block. If 1 the HRA block is enabled.
2	CD	0 = D before C-Channel. The D-channel is transferred before the C-channel following the Frame Pulse. The D-channels are located in the first 16 of the 32 channels of STi/o1 stream. 1 = C before D-Channel. The C-channel is transferred before the D-channel following the Frame Pulse. The D-channels are located in channels 16-31 of STi/o1 stream.
1-0	BRSEL1-0	**Baud Rate Select**. The Baud Rate Select field controls the number of bit times actually used for D-channel activity within a selected transmit or receive channel time. It also controls the rate at which the Auto-hunt circuitry monitors peripherals for request-to-sends. During inactive bit times within an active channel, idles are generated and output. One active bit gives a baud rate of 8K, while eight active bits gives a baud rate of 64K. 00 8K 01 16K 10 64K 11 Unused. On reset, 16K baud rate will be selected.

22.28 HRA CTRL Register 2 (HC2)

The register is configured as follows:

Read/Write Address is: 51_H
Reset Value is: 00_H

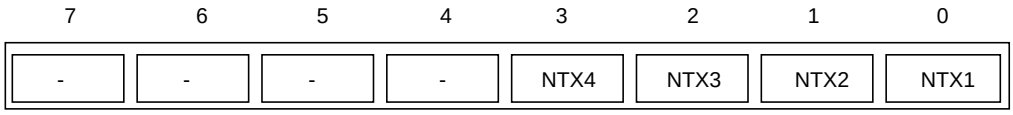


Bit	Name	Description
7	SREOP	**Software Controlled RX End Of Packet (SREOP).** The system can at any time inject a receive end-of-packet by setting this bit. When RX circuitry uses this bit, SREOP will be automatically cleared. SREOP has exactly the same effect and internal timing as REOP. On reset, this bit is cleared.
6	RECTS	**Re-initiate Clear To Send (RECTS)**. By setting this bit, the system can initiate another “go-ahead” flag to the peripheral currently enabled for transmission to the system. This is used when the CTS, which is automatically generated upon receive channel selection, is not detected at the peripheral. RECTS is used with the same internal timing as the normal source of CTS initiation. When RECTS has been used by the RX circuitry it is automatically cleared. A RECTS request will be accepted only if the receiver is active; the request will be ignored, and the RECTS bit cleared, if the receiver is inactive. On reset, this bit is cleared.
5	STEOP	**Software Controlled TX End Of Packet (STEOP)**. The system can at any time inject a transmit end-of-packet by setting this bit. When the TX circuitry uses this bit, STEOP will be automatically cleared. STEOP has exactly the same effect and internal timing as TEOP. On reset, this bit is cleared.
4	DDRX	**Dedicated RX Control**. This bit when high enables dedicated reception from the channel selected by the DRXi bits. At the same time, the generation of CTS is disabled, and flags generated by the Auto-hunt circuitry are ignored. RXCHNL and RXACT are held high in dedicated receive mode. If this bit is low, normal RX operation is enabled. On reset, this bit is cleared.
3-0	DRX4-1	**Dedicated RX Channel Number**. If the DDRX bit or the PRXSEL bit is high, then these bits control the selection of the current receive channel, overriding the output of the Auto-hunt circuitry. The RX Channel Number selects one of the first 16 timeslots of STi1, with HC1 register bit CD=0, or the last 16 timeslots with bit CD=1. DRX4 is the MSB and DRX1 is the LSB. On reset, these bits are cleared.

22.29 HRA CTRL Register 3 (HC3)

The register is configured as follows:

Read/Write Address is: 52_H
Reset Value is: 00_H

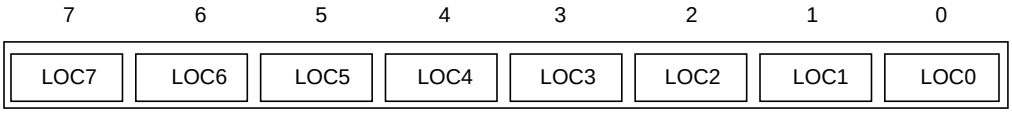


Bit	Name	Description
7-4	unused	**Unused**.
3-0	NTX4-1	**Next TX Channel Number**. These bits represent the channel number for the next packet to be transmitted and selects one of the first 16 timeslots of STo1, with HC1 register bit CD=0, or the last 16 timeslots with bit CD=1. NTX4 is the MSB and NTX1 is the LSB. On reset, this register is cleared. A write to this register causes the status bit TXCHNL, readable from the HRA Status 2 register, to be reset to low.

22.30 HRA Lock Out Register 1 (HLO1)

The register is configured as follows:

Read/Write Address is: 53_H
Reset Value is: FF_H

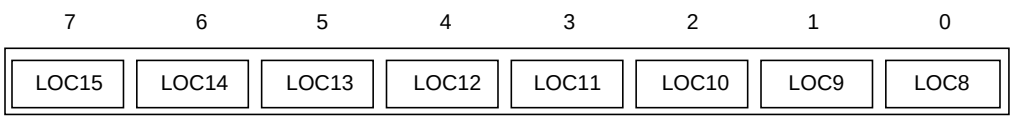


Bit	Name	Description
7-0	LOC7-0	Setting any bit in this register disables reception from the corresponding channel number. LOC0-7 correspond to channels 0 to 7 on stream STi1, with HC1 register bit CD=0, or channels 16 to 23 with bit CD=1. On reset, this register is set, so that all channels are disabled. Example: LOC2 is channel 2 on STi1

22.31 HRA Lock Out Register 2 (HLO2)

The register is configured as follows:

Read/Write Address is: 54_H
Reset Value is: FF_H

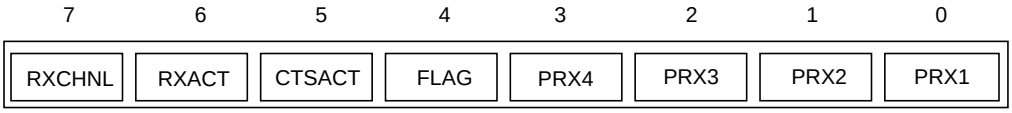


Bit	Name	Description
7-0	LOC15-8	Setting any bit in this register disables reception from the corresponding channel number. LOC8-15 correspond to channels 8 to 15 on stream STi1, with HC1 register bit CD=0, or channels 24 to 31 with bit CD=1. On reset, this register is set, so that all channels are disabled.

22.32 HRA Status 1 (HS1)

The register is configured as follows:

Read Address is: 55_H
Reset Value is: 00_H

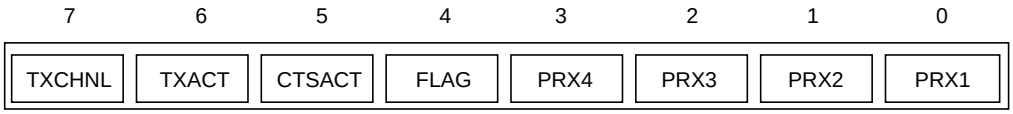


Bit	Name	Description
7	RXCHNL	**Receive Channel Latched (RXCHNL)**. When this bit is high it indicates that a new receive channel number has been latched internally, and is as shown in the currently read byte. A system read of HRA Status register 3 will automatically clear this status bit. In dedicated receive mode, this bit will be held high. On reset, this bit will be low.
6	RXACT	**Receiver Active (RXACT)**. When high, this status bit indicates that the receiver is currently active. On reset, this bit will be low, and $\overline{\text{RxCEN}}$ will be disabled. In dedicated receive mode, this bit will be held high.
5	CTSACT	**Clear-to-Send Active (CTSACT)**. If high, this status bit indicates that the receiver is currently transmitting a clear-to-send go-ahead pattern to the peripheral on the transmit channel denoted by PRXi. In dedicated receive mode, this bit will be held low, disabling CTS generation and transmission. On reset, this bit will be low.
4	FLAG	**Flag Detect (FLAG)**. When high, FLAG indicates that the Auto-hunt circuitry has detected a request-to-send from a peripheral, but has not yet acted upon it. FLAG will also go high if the system injects an SFLAG via the micro interface. As soon as the RX circuitry selects the corresponding peripheral for system receive, this status bit is cleared. On reset, this bit will be low. This bit is primarily used for test purposes.
3-0	PRX4-1	**Present Receive Channel (PRX)**. The current receive channel number is contained in these five bits. Reading the channel number via HRA Status register 3 clears the status bit RXCHNL. PRX4-1 represent channels 0-15 on STi1 stream, with HC1 register bit CD=0, or channels 16 to 31 with bit CD=1. On reset, channel 0 will be selected, but will be inactive.

22.33 HRA Status 2 (HS2)

The register is configured as follows:

Read Address is: 56_H
Reset Value is: 80_H

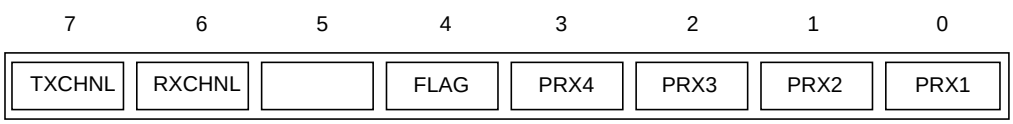


Bit	Name	Description
7	TXCHNL	**TX Channel Number Latched (TXCHNL)**. The next TX channel number in write register 3 has been latched by the TX control circuitry and may be rewritten when this bit is high. The bit is automatically reset when a write to register 3 occurs. On reset, this bit will be high, although the transmitter will be inactive.
6	TXACT	**Transmitter Active (TXACT)**. When high, this status bit indicates that the transmitter is currently active. On reset, this bit will be low, and $\overline{\text{TxCEN}}$ will be disabled.
5	CTSACT	**Clear-to-Send Active (CTSACT)**. See description in HS1 register.
4	FLAG	**Flag Detect (FLAG)**. See description in HS1 register.
3-0	PRX4-1	**Present Receive Channel (PRX)**. See description in HS1 register.

22.34 HRA Status 3 (HS3)

The register is configured as follows:

Read Address is: 57_H
Reset Value is: 80_H



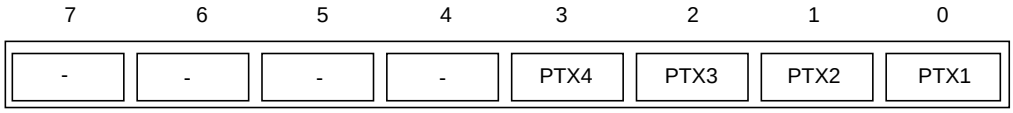
Bit	Name	Description
7	TXCHNL	**TX Channel Number Latched (TXCHNL)**.
6	RXCHNL	**Receive Channel Latched (RXCHNL)**. See description in HS1 register.
5	unused	**Unused**.
4	FLAG	**Flag Detect (FLAG)**. See description in HS1 register.
3-0	PRX4-1	**Present Receive Channel (PRX)**. See description in HS1 register.

Reading the channel number via this register clears the status bit RXCHNL.

22.35 HRA Status 4 (HS4)

The register is configured as follows:

Read Address is: 58_H
Reset Value is: 00_H



Bit	Name	Description
7-4	-	**Unused**.
3-0	PTX4-1	**Present Transmit Channel (PTX)**. The current transmit channel number is contained in these four bits. Reading the channel number via this register does not clear the status bit TXCHNL.PTX4-1 represent channels 0-15 on STo1 stream, with HC1 register bit CD=0, or channels 16 to 31 with bit CD=1. On reset, channel 0 will be selected, but will be inactive.

23.0 Applications

23.1 Local TDM Channel Assignment

Fig. 28 shows the channel assignment for the local TDM streams used to support the stations, trunks and analog ports for a typical configuration. There are 8 stations supported by MT9171/72 DNIC transceivers, 8 analog ports supported by 8 Codecs and 4 trunks supported by another 4 Codecs.

In this example, the B-channel information is on the STi/o0 streams. The C- and D-channel information is placed on the STi/o1 streams (Dual Port mode).

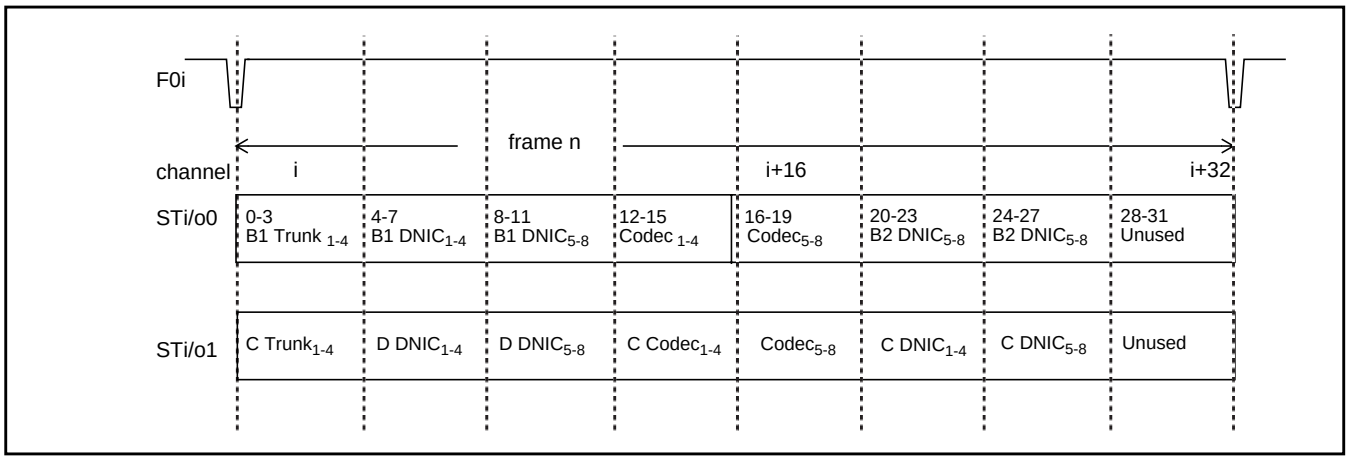


Figure 28 - MT90812 Local TDM Channel Assignment for Typical Configuration

The local STi/o0 and STi/o1 channel assignment is summarized in Table 21.

Channel	# of channels	Device	STi/o0	STi/o1
0-3	4	Trunk CODEC 1-4	B1	C
4-11	8	DNIC 1-8	B1	D
12-15	4	CODEC 1-4	B1	C
16-19	4	CODEC 5-8	B1	C
20-27	8	DNIC 1-8	B2	C
28-31	4	Unused.	-	-

Table 21 - TDM Channel Assignment

23.2 DNIC Channel Assignment

The MT90812 supports direct connection to the DNICs placed in Digital Network (DN), Dual Port mode. The DNIC transfers four channels of information via the DV and CD ports. They are B1, B2, C and D-channels. The B1 and B2 channels each have a bandwidth of 64 kbit/s and are used for carrying PCM encoded voice or data.

The C-channel, having a bandwidth of 64kbit/s, provides a means for the system microprocessor to control the DNIC and for the DNIC to pass status information back to the system microprocessor. The D-Channel can be transmitted and received on the line with either 8, 16, or up to 64 kbit/s bandwidth. To support this, the MT90812 provides buffering of 1, 2 or 8 bits per frame to support D-Channel end to end signalling or low speed data transfer.

In DN, Dual Port mode, the DNIC receives a D-Channel on CDSTi while transmitting a D-Channel on CDSTo. Fifteen channel times later (halfway through the frame) a C-Channel is received on CDSTi while a C-Channel is transmitted on CDSTo. The timeslot assignment used by the DNIC is shown in Fig. 29.

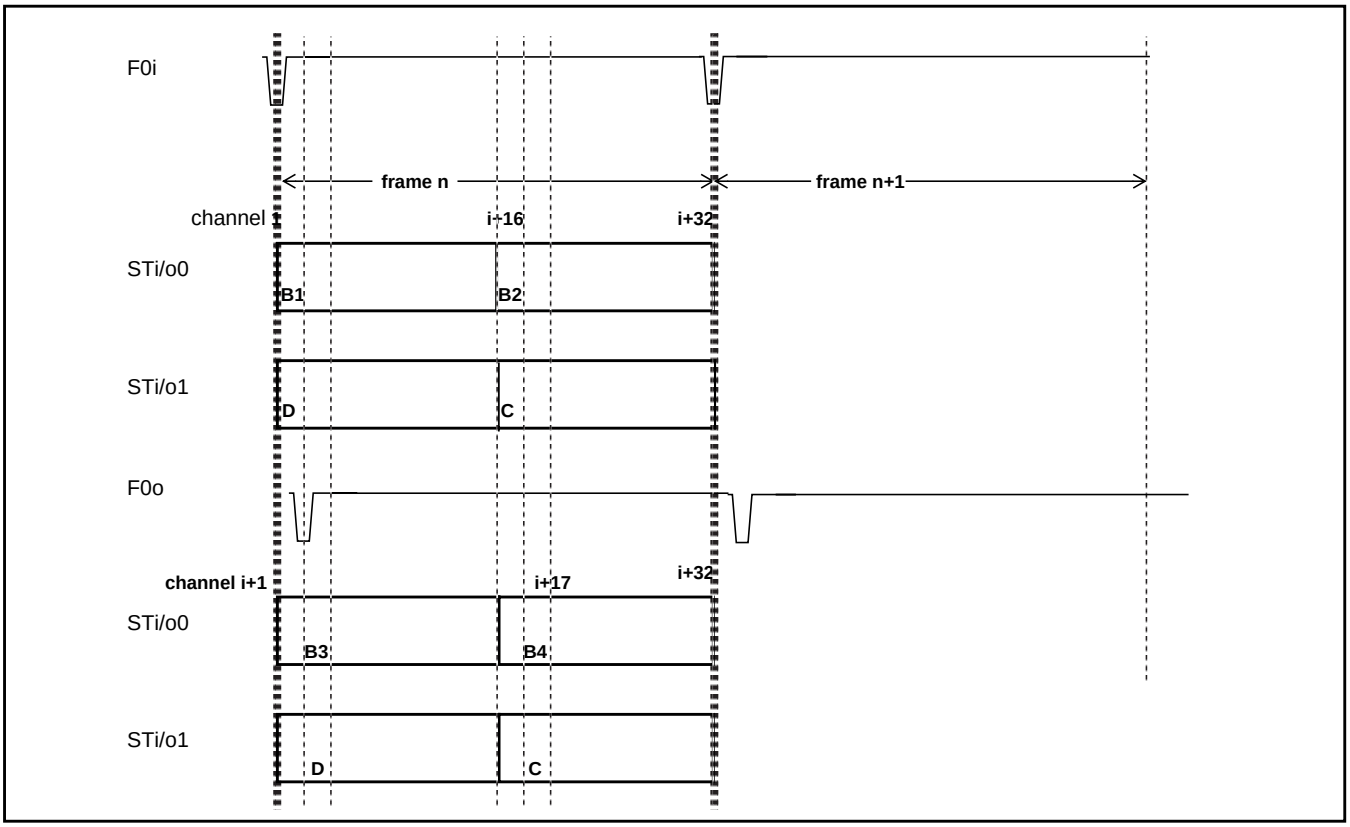


Figure 29 - DNIC Time Slot Assignment for STi/o0 and STi/o1 TDM Streams

In Figure 28, on page 70, timeslots 4-11 and 20-27 are allocated for the 8 DNICs. Timeslots 4-11 contain the B1 channels on STi/o0 and D-channels on STi/o1. Timeslots 20-27 contain the B2 channels on STi/o0 and C-channels on STi/o1.

24.0 AC/DC Electrical Characteristics

Absolute Maximum Ratings* - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	V_{DD} - V_{SS}	V_{DD}	- 0.3	7.0	V
2	Voltage on any pin I/O (other than supply pins)	$V_{I/O}$	V_{SS} - 0.3	V_{DD} + 0.3	V
3	Current at any pin other than supply pins	I_{PIN}		40	mA
4	Package power dissipation	P_D		2	W
5	Storage temperature	T_S	- 65	+ 150	^oC

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	Operating Temperature	T_{OP}	- 40	+ 85	^oC
2	Positive Supply	V_{DD}	4.5	5.5	V
3	Input Voltage	V_I	0	V_{DD}	

DC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Unit	Test Conditions
1		Supply Current	I_{DD}		9	14	mA	PLL Off, Outputs unloaded
			I_{DD}		10	15	mA	PLL On, Outputs unloaded
2		Input High Voltage	V_{IH}	2.0		V_{DD}	V	
3		Input Low Voltage	V_{IL}	0		0.8	V	
4	C8P	Input High Voltage	V_{IH}	3.6		V_{DD}	V	
5		Input Low Voltage	V_{IL}	0		0.8	V	
6		Leakage Current	I_{LK}			10	uA	$0 \le V \le V_{DD}$
7		Pin Capacitance	C_P			10	pF	
8		Output Voltage High (digital outputs)	V_{OH}	2.4			V	I_{OH} = 12mA
9		Output Voltage Low (digital outputs)	V_{OL}			0.4	V	I_{OL} = 10mA
10		Output High Sourcing Current (digital outputs)	I_{OH}	12			mA	V_{OH} = 2.4V
11		Output Low Sinking Current (digital outputs)	I_{OL}	10			mA	V_{OL} = 0.4V
12	RESET	Positive Threshold Voltage Hysteresis Negative Threshold Voltage	V+ V_H V-	3.7	 1.0	 1.3	V V V	

† Characteristics are for clocked operation over the ranges of recommended operating temperature and supply voltage.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics - Timing Parameter Measurement Voltages Levels

Characteristics	Symbol	TTL Pin	CMOS Pin	Units
TTL reference level	V_{TT}	1.5	-	V
CMOS reference level	V_{CT}	-	$0.5*V_{DD}$	V
Input HIGH level	V_H	2.4	$0.9*V_{DD}$	V
Input LOW level	V_L	0.4	$0.1*V_{DD}$	V
Rise/Fall HIGH meas. pt.	V_{HM}	2.0	$0.7*V_{DD}$	V
Rise/Fall LOW meas. pt.	V_{HL}	0.8	$0.3*V_{DD}$	V

AC Electrical Characteristics - Input Clock Parameters

Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
C4i clock period	t_{C4iP}	220	244		ns	
C4i clock width (High)	t_{C4iH}	110	122	140	ns	
C4i clock width (Low)	t_{C4iL}	110	122	140	ns	
C4i clock rise/fall time	$t_{C4iR/F}$			10	ns	
C8 clock period	t_{C8P}	110	122		ns	
C8 clock width (High)	t_{C8H}	50	61.0	70	ns	
C8 clock width (Low)	t_{C8L}	50	61.0	70	ns	
C8 clock rise/fall time	$t_{C8iR/F}$			10	ns	
C16 clock period	t_{C16iP}	50	61.0	70	ns	
C16 clock width (High)	t_{C16iH}	25	30.5	35	ns	
C16 clock width (Low)	t_{C16iL}	25	30.5	35	ns	
C16 clock rise/fall time	$t_{C16iR/F}$			10	ns	

‡ Typical figures are at 25˚C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics - Input Frame Pulse Parameters

Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions†
F4i Setup Time (ST-Bus, GCI)	t_{F4iS}	10		150	ns	17
F4i Hold Time (ST-Bus, GCI)	t_{F4iH}	20		150	ns	17
F4i Width (ST-Bus, GCI)	t_{F4iW}	195	244	295	ns	
F8 Setup Time (ST-Bus, GCI)	t_{F8S}	10			ns	18
F8 Hold Time (ST-Bus, GCI)	t_{F8H}	10			ns	18
F8 Width (ST-Bus, GCI) 8.192 MHz 16.384 Mhz	t_{F8W}	50 50	122 61	145 70	ns	

‡ Typical figures are at 25˚C and are for design aid only: not guaranteed and not subject to production testing.
† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - 8.192 MHZ Master Clock Input

Characteristics	Sym	Min	Max	Units	Conditions/Notes†
Tolerance		-32	+32	ppm	
Duty cycle		40	60	%	

† See "Notes" following AC Electrical Characteristics tables.

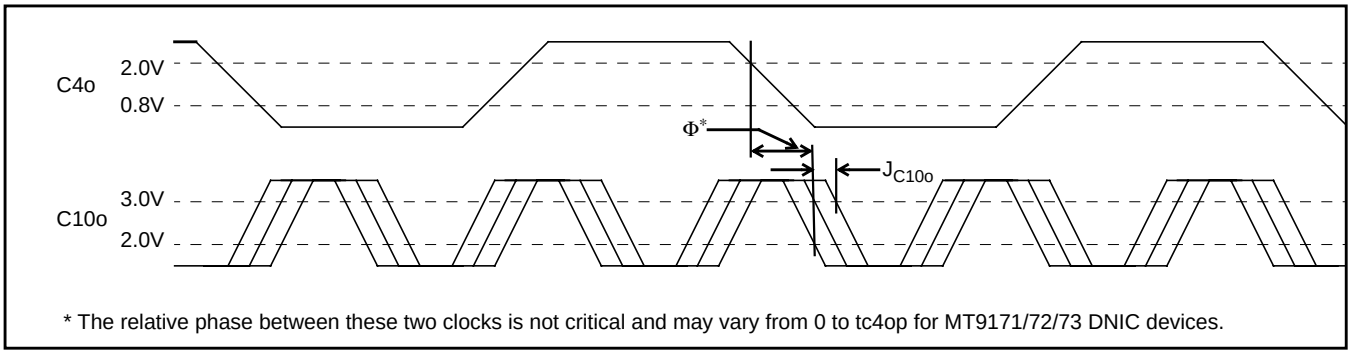


Figure 30 - Frequency Locking for the C4o and C10o Clock

AC Electrical Characteristics - Output Clock Parameters

Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
C10o clock frequency	f_{C10}		10.24		MHz	
C10o output clock period	t_{C10P}		97.65		ns	
C10o clock duty cycle	DC_{C10}	40	50	60	%	refer to table on page 95
C10o clock Jitter (w.r.t. C4o)	J_{C10}	-15		+15	ns	

‡ Typical figures are at 25˚C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics - Output Frame Pulse Parameters

Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
F4o output delay (High to Low) from C4o	t_{F4oL}	0		15	ns	
F4o output delay (Low to High) from C4o	t_{F4oH}	0		15	ns	
F4o Width	t_{F4oW}		244		ns	
F8 output delay (High to Low) from C8 output clock	t_{F8oL}	0		15	ns	
F8 output delay (Low to High) from C8 output clock	t_{F8oH}	0		15	ns	
F8 Width	t_{F8oW}		122		ns	

‡ Typical figures are at 25˚C and are for design aid only: not guaranteed and not subject to production testing.

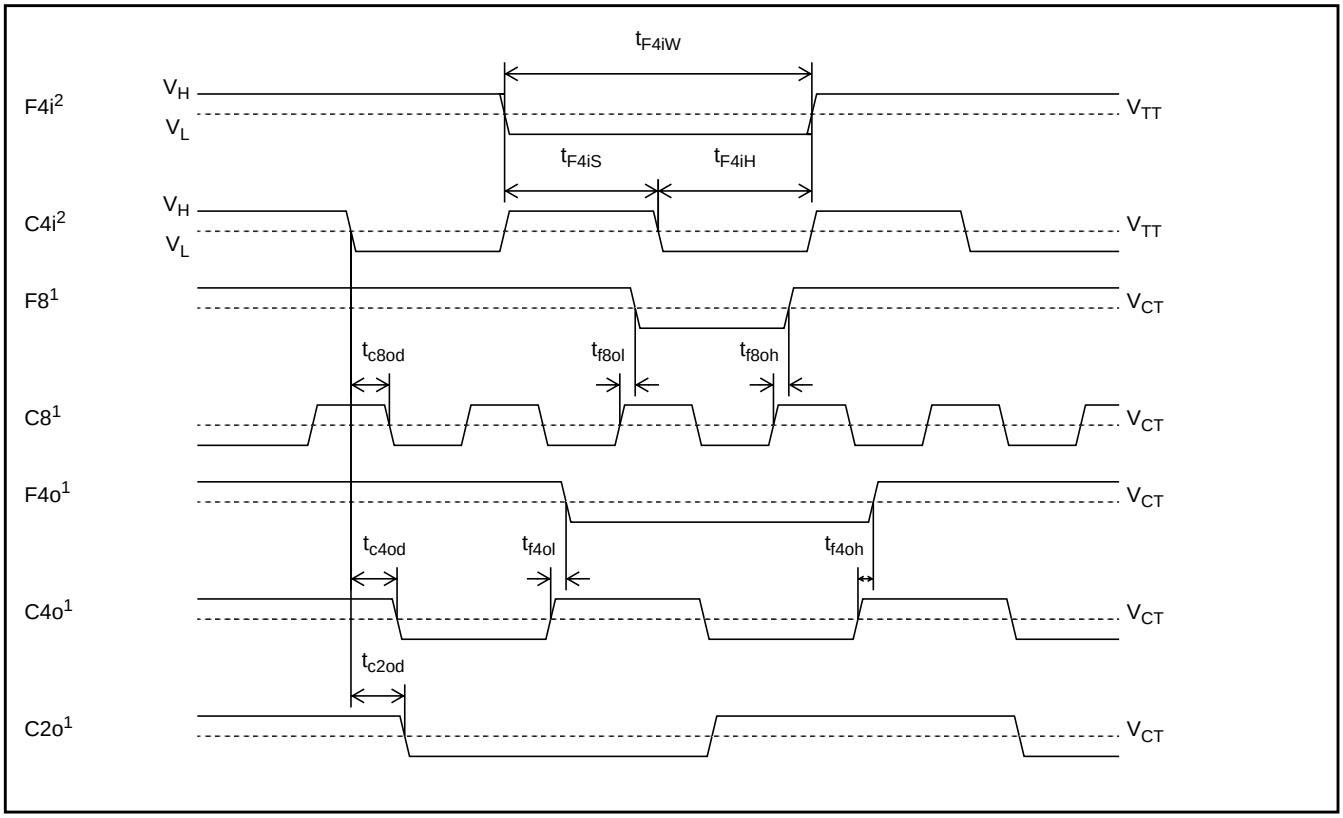


Figure 31 - C4/F4 Input Clock Reference - ST-Bus

Notes: 1. CMOS output 2. TTL input

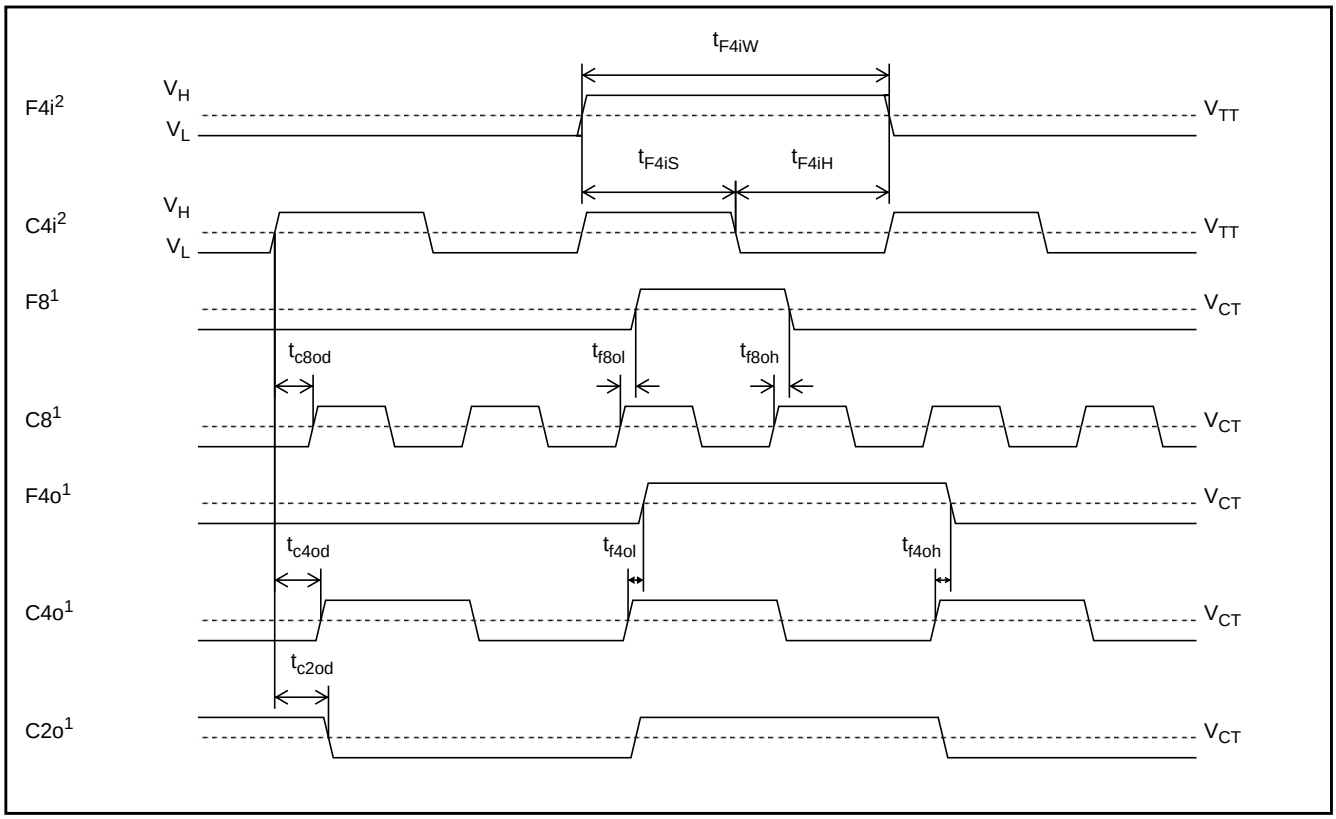


Figure 32 - C4/F4 Input Clock Reference - GCI

Notes: 1. CMOS output 2. TTL input

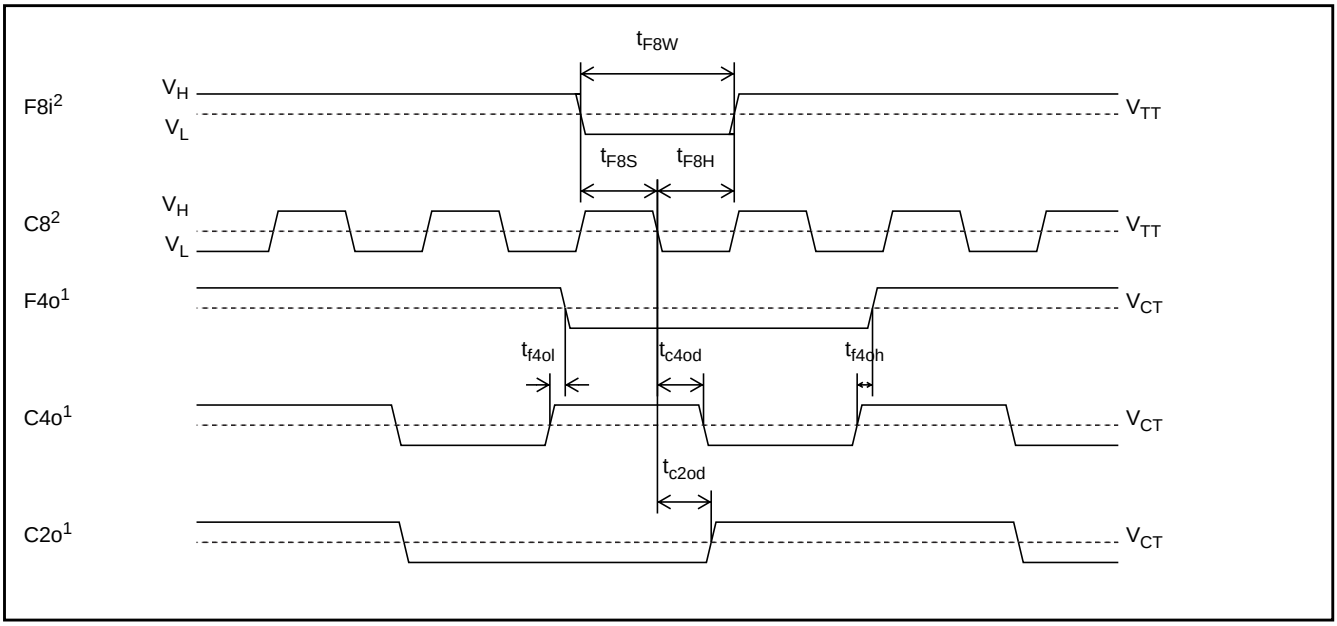


Figure 33 - C8/F8 Input Clock Reference - ST-Bus

Notes: 1. CMOS output 2. TTL input

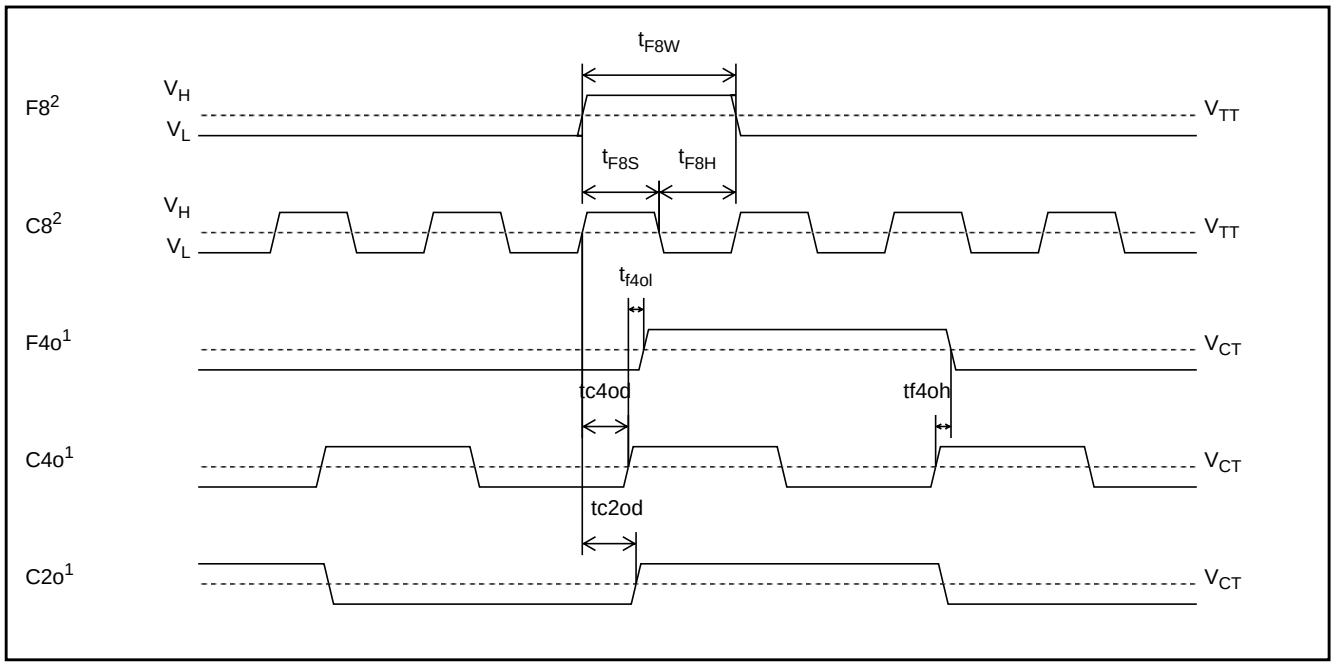


Figure 34 - C8/F8 Input Clock Reference - GCI

Notes: 1. CMOS output 2. TTL input

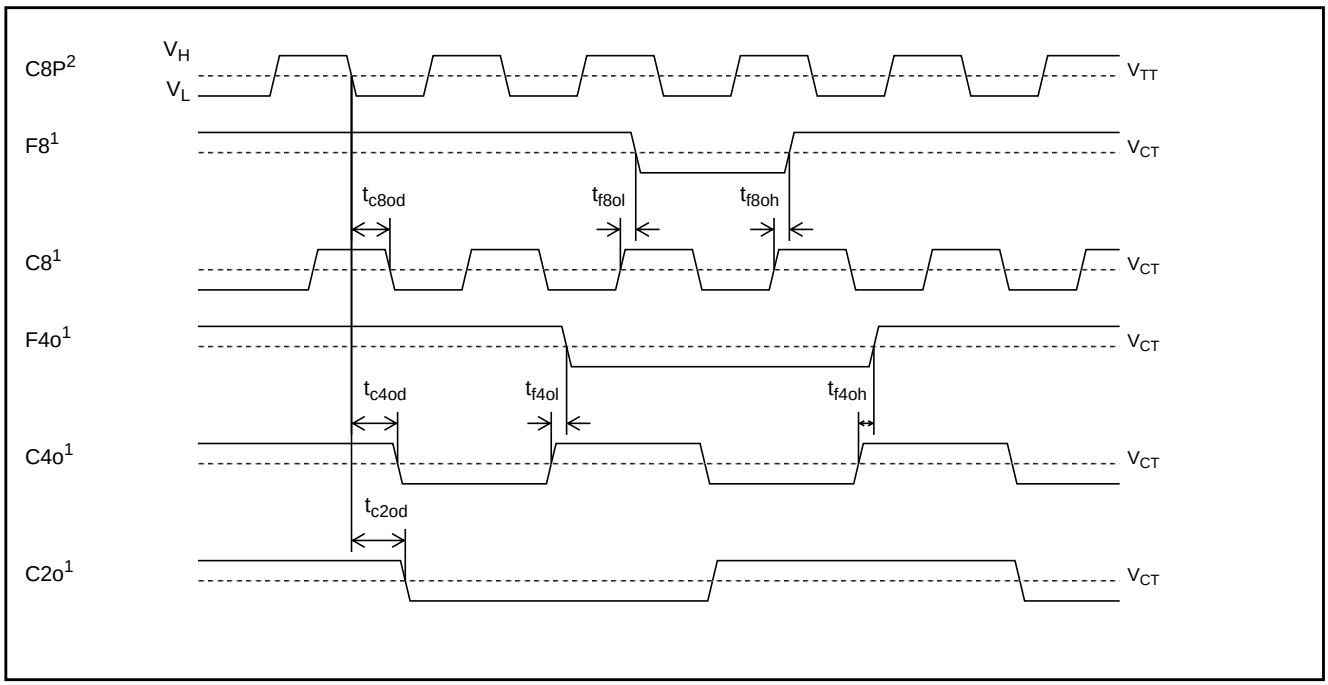


Figure 35 - C8P Input Clock Reference - ST-Bus (Timing Control, FPO bit =0)

Notes: 1. CMOS output 2. TTL input

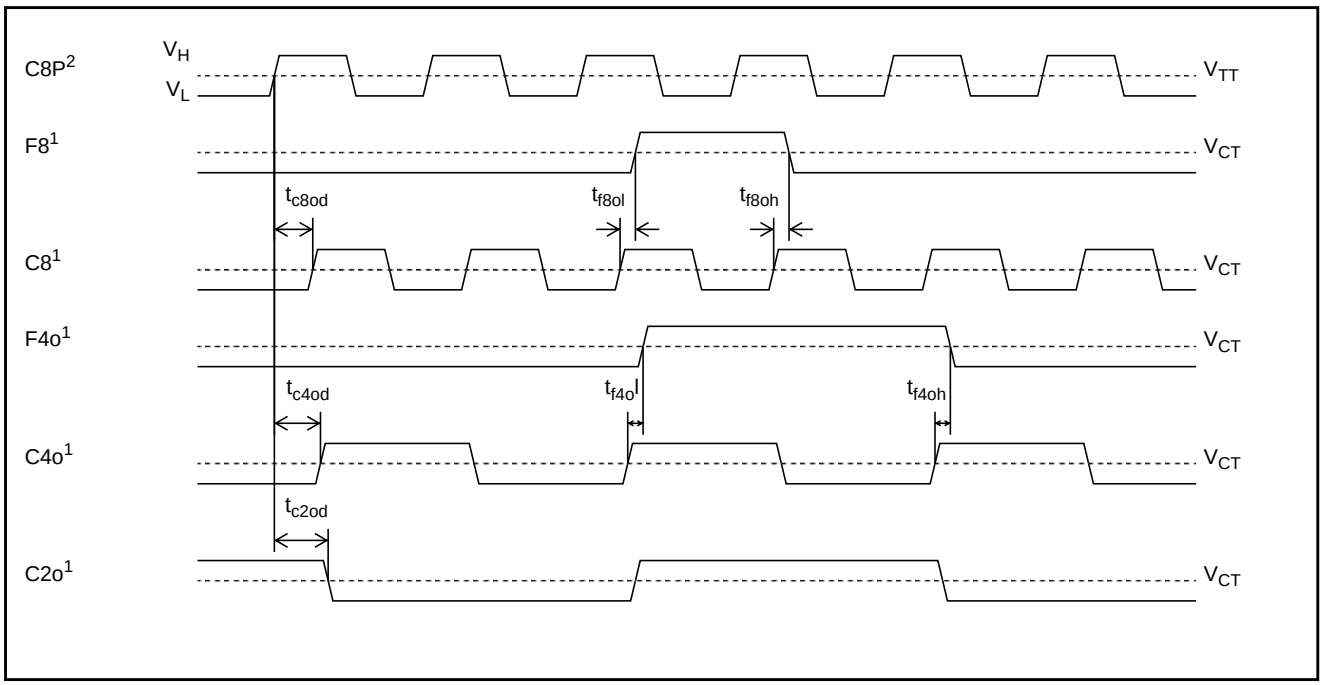


Figure 36 - C8P Input Clock Reference - GCI (Timing Control, FPO bit =1)

Notes: 1. CMOS output 2. TTL input

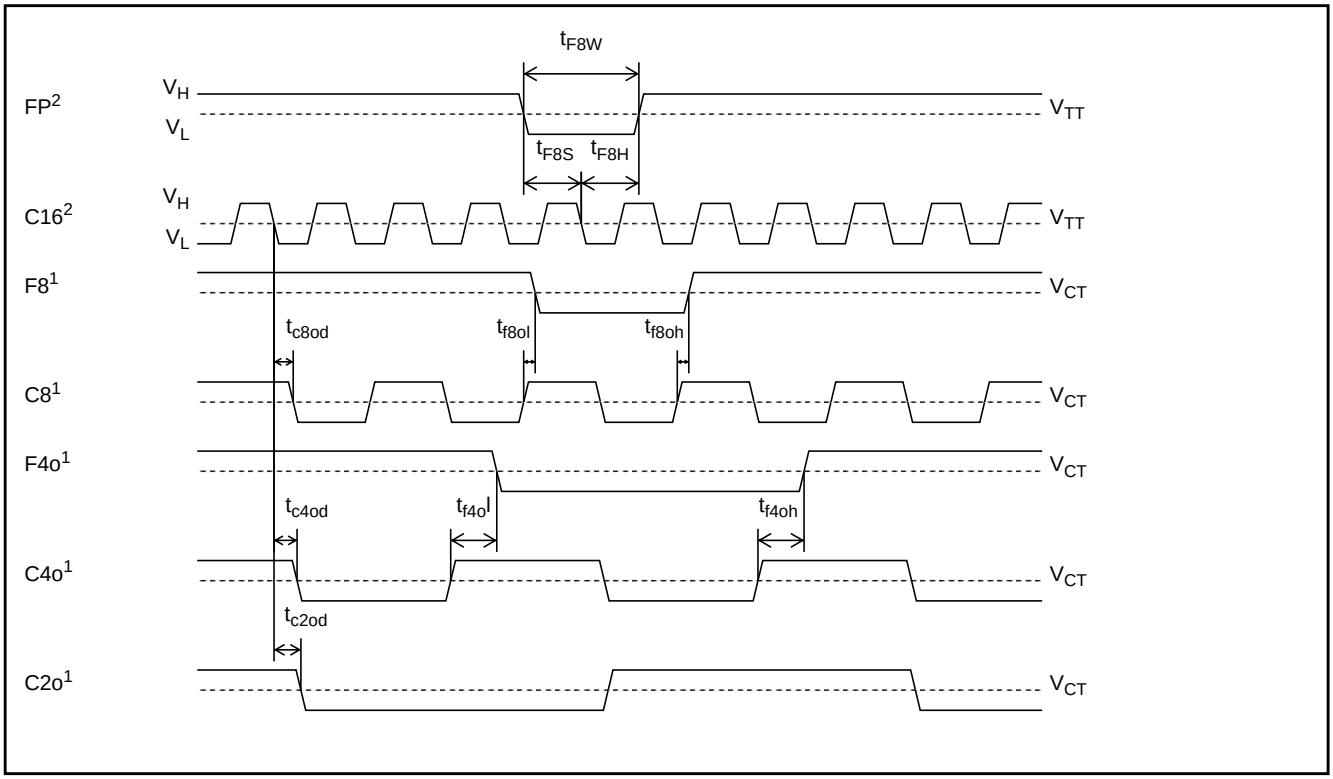


Figure 37 - C16/F8 Input Clock Reference - ST-Bus

Notes: 1. CMOS output 2. TTL input

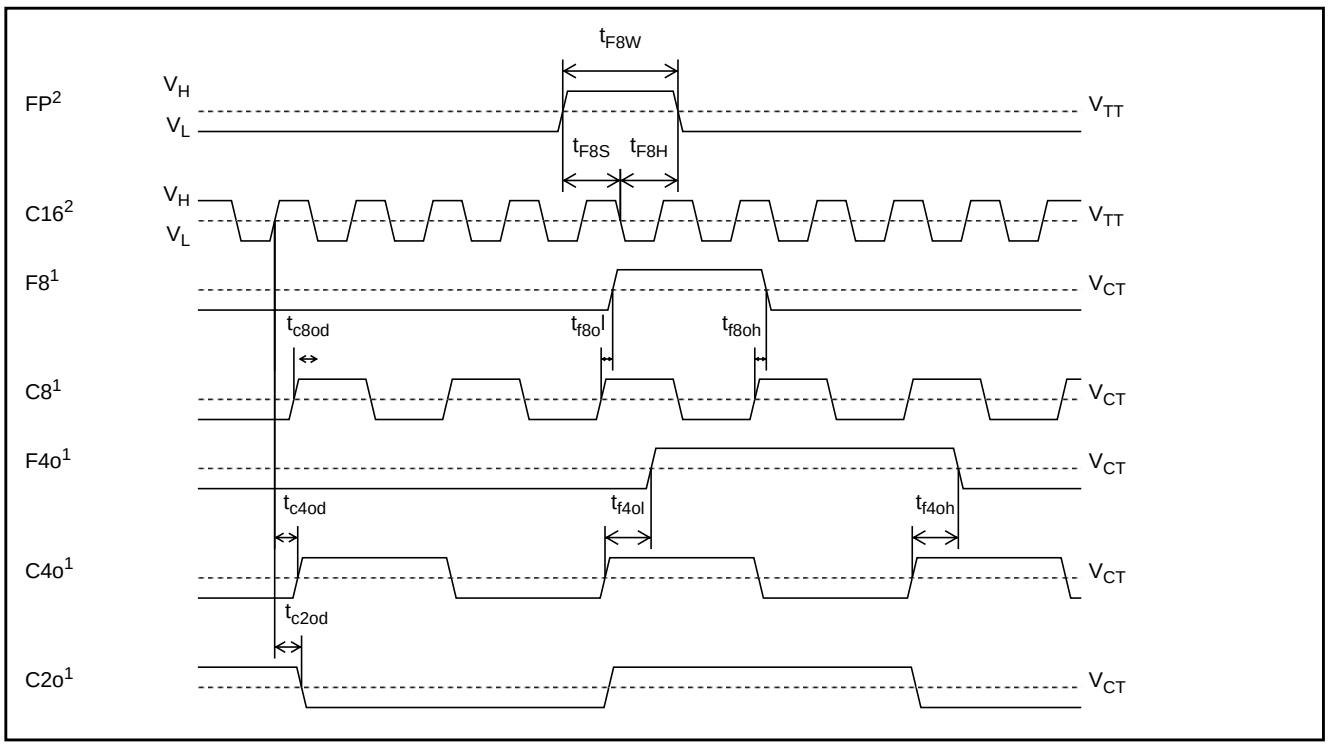


Figure 38 - C16/F8 Input Clock Reference - GCI

Notes: 1. CMOS output 2. TTL input

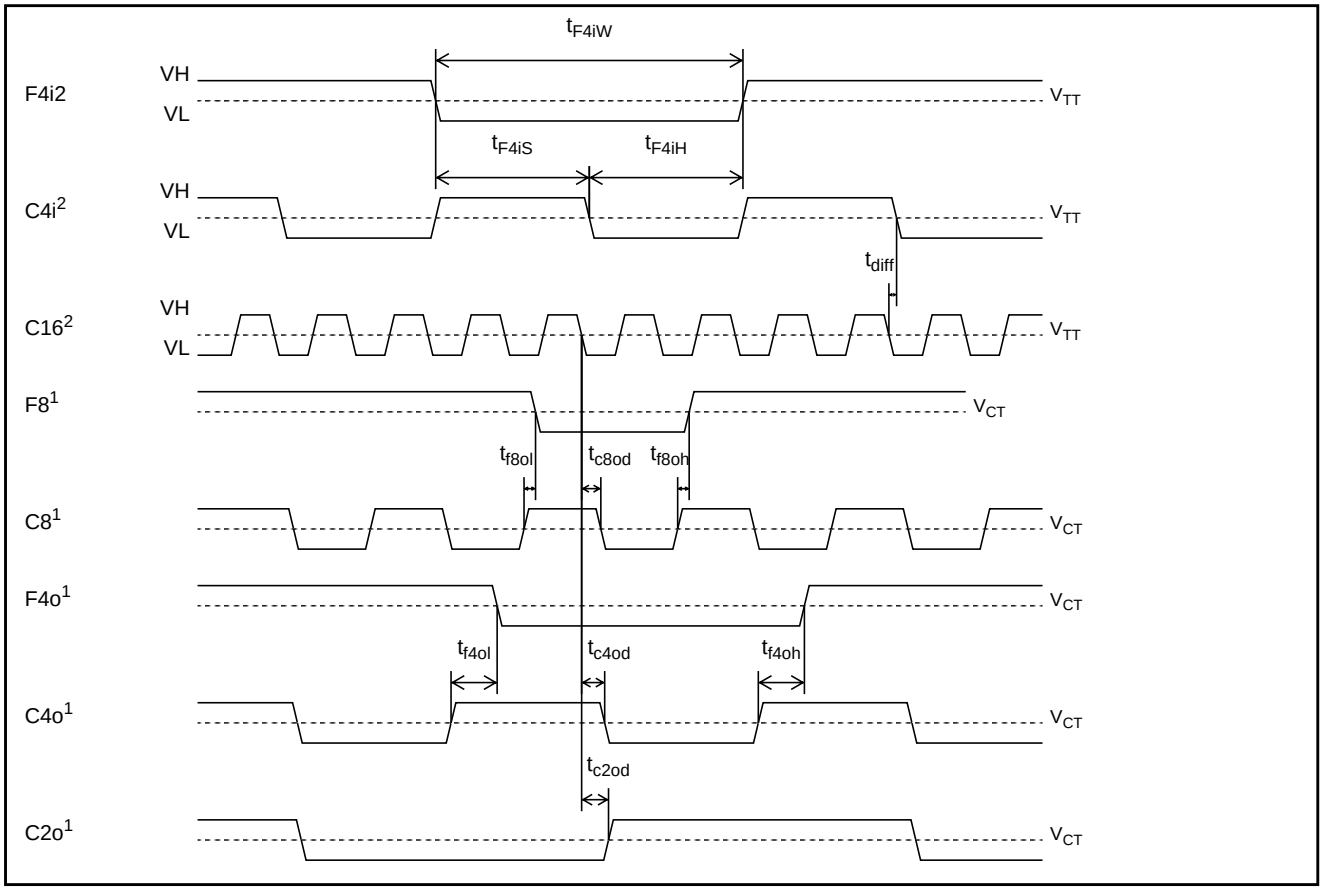


Figure 39 - C16 HMVIP Input Clock Reference

Notes: 1. CMOS output 2. TTL input

24.1 Timing References for TDM Streams

The Expansion Bus operates in two modes; IDX Link and TDM Link modes (refer to Section 3.0). In TDM Link mode there are three data rates supported, 2.048, 4.096, and 8.192 Mb/s. The IDX Link mode supports 8.192 Mb/s data rate. Depending on the Clock Control Mode selected the serial stream AC parameters are specified with respect to a given clock reference. Table 22 lists the timing references used for the TDM streams given the Clock Control Mode, PCS and PCOS settings. The timing diagrams to be used for the given TDM stream and timing mode are listed for both ST-Bus and GCI modes. The clock reference is labelled, CLK, in each diagram and is either C4i, C4o, C8 (as an input or output), or C16, where C16 refers to 16.384 MHz signal applied to C8P_C16 pin. The frame pulse reference is labelled FP in each diagram and is either F4i, F4o, F8(input) or F8(output).

TDM and Data Rate	Clock Control Mode	PCS	PC0S	CLK	FP	CLK Rate/ Data Rate	Timing Diagram
Local 2 Mb/s	all	0	0	C4i	F4i	2	Fig. 40 (ST-Bus) & Fig. 41 (GCI)
Local 2 Mb/s	all	1	1	C4o	F4o	2	Fig. 40 (ST-Bus) & Fig. 41 (GCI)
EBUS 2 Mb/s (TDM Link)	all	0	0	C4i	F4i	2	Fig. 40 (ST-Bus) & Fig. 41 (GCI)
EBUS 2 Mb/s (TDM Link)	all	1	1	C4o	F4o	2	Fig. 40 (ST-Bus) & Fig. 41 (GCI)
EBUS 4Mb/s (TDM Link)	C4/F4	X	X	C8 (Output)	F8 (Output)	2	Fig. 40 (ST-Bus) & Fig. 41 (GCI)

TDM and Data Rate	Clock Control Mode	PCS	PC0S	CLK	FP	CLK Rate/ Data Rate	Timing Diagram
	C8/F8, C8P	0	0	C8 (Input)	F8 (Input)	2	Fig. 40 (ST-Bus) & Fig. 41 (GCI)
	C16	0	0	C16 (Input)	F8 (Input)	4	Fig. 40 (ST-Bus) & Fig. 41 (GCI) CLK shown as C8
	C8/F8, C8P, C16	1	1	C8 (Output)	F8 (Output)	2	Fig. 40 (ST-Bus) & Fig. 41 (GCI)
EBUS 8Mb/s	C4/F4	X	X	C8 (Output)	F8 (Output)	1*	Fig. 42 (ST-Bus) & Fig. 43 (GCI)
	C8/F8, C8P	0	0	C8 (Input)	F8 (Input)	1	Fig. 42 (ST-Bus) & Fig. 43 (GCI)
	C16/F8	0	0	C16 (Input)	F8 (Input)	2	Fig. 40 (ST-Bus) & Fig. 41 (GCI)
	C16/HMVIP	0	0	C16 (Input)	F4 (Input)	2	Fig. 44 (HMVIP)
	C8/F8, C8P, C16	1	1	C8 (Output)	F8 (Output)	1*	Fig. 40 (ST-Bus) & Fig. 41 (GCI)

Table 22 - Timing References for TDM Streams

* Clock Rate/Data Rate=1, however the incoming data is clocked with the PLL generated clock at 3 quarters into the bit cell.

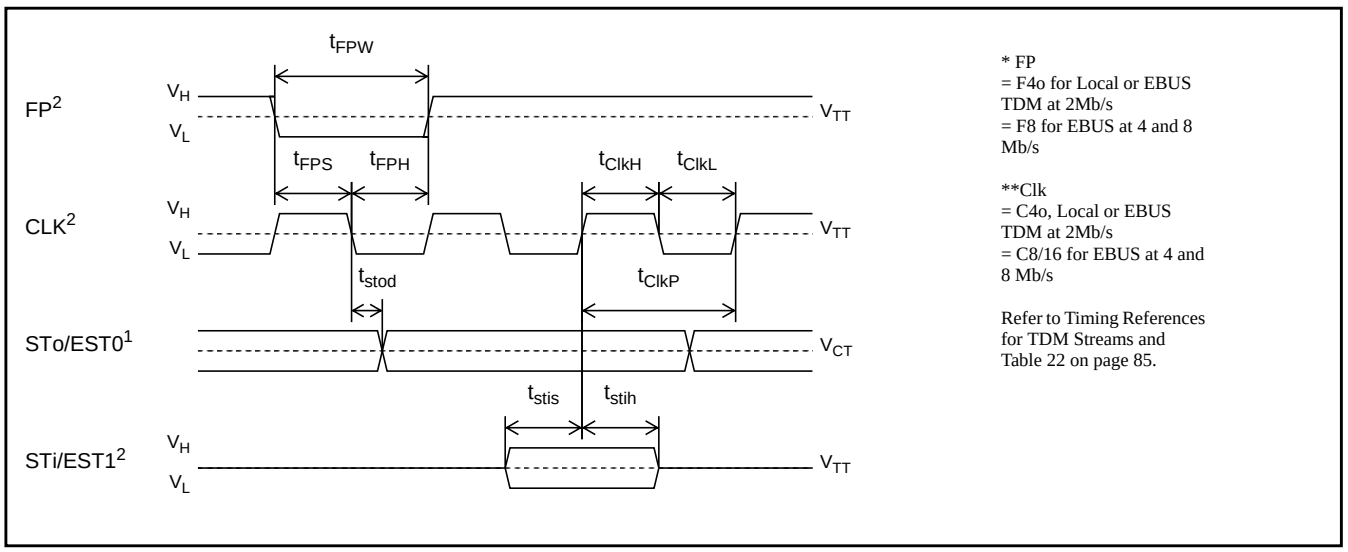


Figure 40 - ST-BUS Timing for Local TDM Bus at 2.048 Mb/s and Expansion Bus Interface at 2.048 Mb/s, 4.096 Mb/s and 8.192 Mb/s (8.192 Mb/s with 16.384 MHz clock)

Notes: 1. CMOS output 2. TTL input

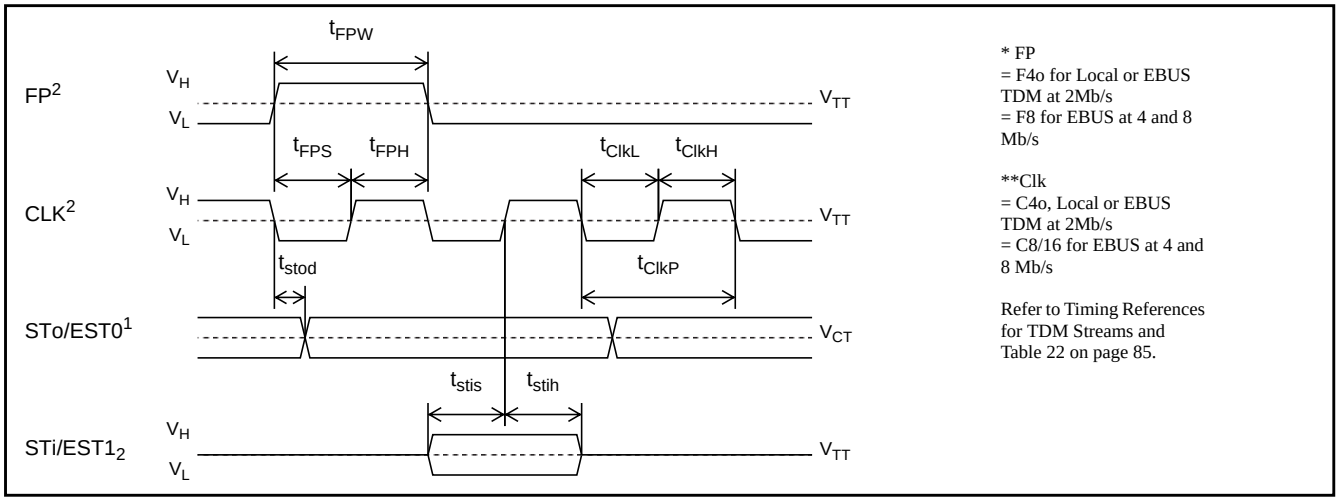


Figure 41 - - GCI Timing for Local TDM Bus at 2.048 Mb/s and Expansion Bus Interface at 2.048 Mb/s, 4.096 Mb/s and 8.192 Mb/s (8.192 Mb/s with 16.384 MHz clock)

Notes: 1. CMOS output 2. TTL input

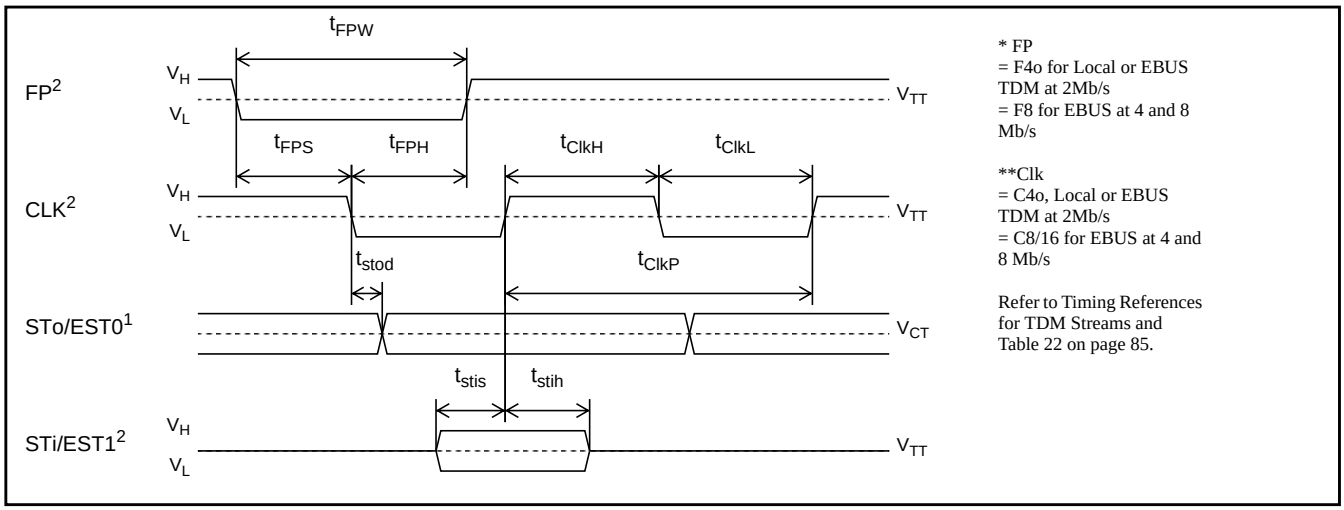


Figure 42 - ST-BUS Timing for Expansion Bus Interface at 8.192 Mb/s with 8.192 MHz clock

Notes: 1. CMOS output 2. TTL input

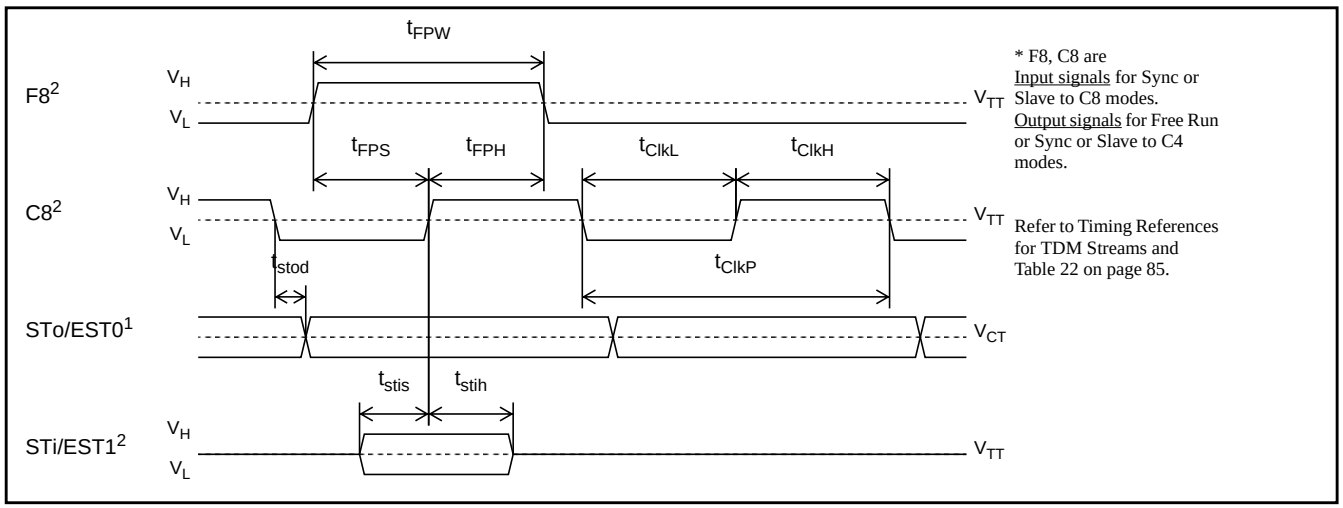


Figure 43 - - GCI Timing for Expansion Bus Interface at 8.192 Mb/s (8.192 MHz clock)

Notes: 1. CMOS output 2. TTL input

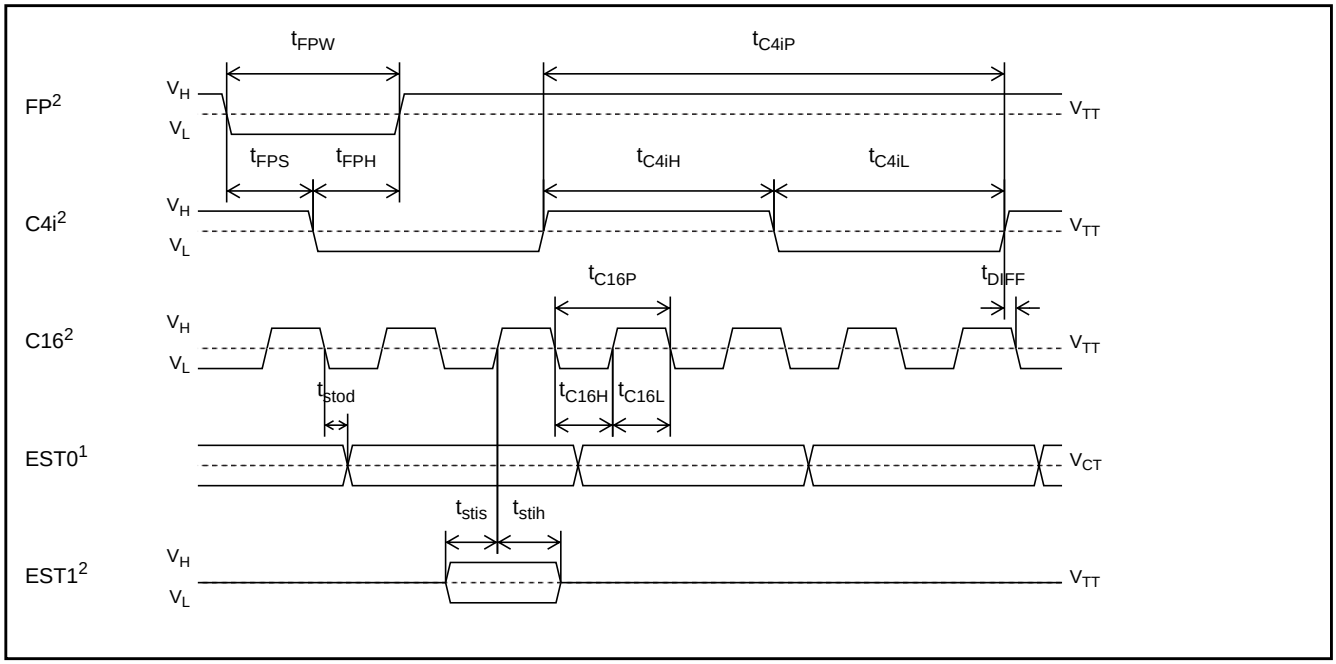


Figure 44 - - HMVIP Bus Timing for Serial Interface (8.192Mb/s)

Notes: 1. CMOS output 2. TTL input

AC Electrical Characteristics - HMVIP Bus Timing

Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
F4i Setup Time	t_{FPS}	10			ns	
F4i Hold Time	t_{FPH}	20			ns	
F4i Width	t_{FPW}		244		ns	
Delay between rising edge of C4i and rising edge C8/16.	t_{diff}	-3		3	ns	

‡ Typical figures are at 25˚C and are for design aid only: not guaranteed and not subject to production testing.

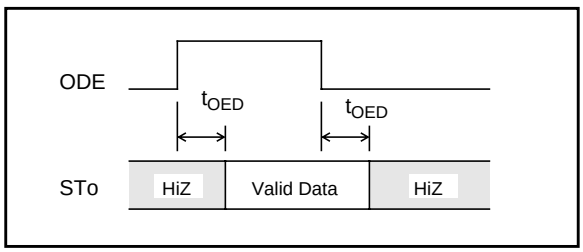


Figure 45 - Output Driver Enable (ODE)

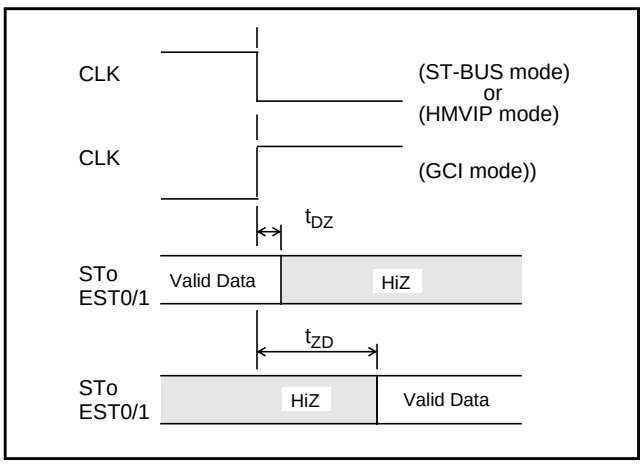


Figure 46 - Serial Output and External Control

24.2 AC Parameters Referenced to Incoming Clock Signals

AC parameters are either measured with respect to incoming or outgoing clock signals. A list of the Clock Control Modes for the Local or Expansion Bus streams where the AC parameters are measured with respect to incoming clock signals are listed in Table 23. The parametric values are listed in the following tables.

TDM and Data Rate	Clock Control Mode	PCS	PC0S	CLK	FP	CLK Rate / Data Rate	Timing Diagram
Local 2 Mb/s	all	0	0	C4i	F4i	2	Fig. 40 (ST-Bus) & Fig. 41 (GCI)
EBUS 2 Mb/s (TDM Link)	all	0	0	C4i	F4i	2	
EBUS 4Mb/s (TDM Link)	C8/F8, C8P	0	0	C8 (Input)	F8 (Input)	2	Fig. 40 (ST-Bus) & Fig. 41 (GCI)
	C16	0	0	C16 (Input)	F8 (Input)	4	Fig. 40 (ST-Bus) & Fig. 41 (GCI) CLK shown as C8
EBUS 8Mb/s	C8/F8, C8P	0	0	C8 (Input)	F8 (Input)	1	Fig. 42 (ST-Bus) & Fig. 43 (GCI)
	C16/F8	0	0	C16 (Input)	F8 (Input)	2	Fig. 40 (ST-Bus) & Fig. 41 (GCI)
	C16/HMVIP	0	0	C16 (Input)	F4 (Input)	2	Fig. 44 (HMVIP)

Table 23 - Timing Referenced to Input Clock Signals for TDM Streams

AC Electrical Characteristics - Output Delay Parameters Referenced to Input Clock Signals

Characteristics	Sym	Min	Max	Units	Test Conditions†
Output Driver Enable Delay (2.048, 4.096, 8.192 Mb/s)	t_{OED}		55	ns	3
STo delay, active to active, High-Z to active, active to High-Z	t_{SToD}, t_{ZD}, t_{DZ}				Non-PLL Clock 3, 9, 10.
2.048 Mb/s			65	ns	
4.096 Mb/s			55	ns	
8.192 Mb/s			55	ns	
Sto delay, active to active, High-Z to active, active to High-Z	t_{SToD}, t_{ZD}, t_{DZ}				PLL Output Clock
2.048 Mb/s - Sto0,Sto1			45	ns	3, 11, 14, 15
2.048 Mb/s - EST0			45	ns	3, 11, 14, 16
4.096 Mb/s			45	ns	3, 11, 14, 16
8.192 Mb/s			45	ns	3, 11, 14, 16
Clock Output Delays					Non-PLL Clock. 3, 9,10
C2o	t_{c2od}		50	ns	
C4ob	t_{c4od}		50	ns	
C8o	t_{c8od}		40	ns	
Clock Output Delays					PLL Output Clock
C2o	t_{c2od}		35	ns	3, 11, 14, 15
C4ob	t_{c4od}		35	ns	3, 11, 14, 15
C8o	t_{c8od}		30	ns	3, 11, 14, 16
C10o	t_{c10od}		35	ns	3, 11, 14

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - Input Set and Hold Parameters Referenced to Input Clock Signals

Characteristics	Sym	Min	Max	Units	Test Conditions†
Sti Set-up Time before CLK rising (ST-Bus mode) before CLK falling (GCI mode)	t_{STiS}				Non-PLL Clock 3, 9, 10
2.048 Mb/s - Sto0,Sto1,EST1		5		ns	
4.096 Mb/s		5		ns	
8.192 Mb/s		5		ns	
Sti Set-up Time before CLK rising (ST-Bus mode) before CLK falling (GCI mode)	t_{STiS}				PLL Clock
2.048 Mb/s - Sto0,Sto1,EST1		10		ns	3, 11, 14, 15
4.096 Mb/s		10		ns	1, 3, 11, 14, 16
8.192 Mb/s		5		ns	2, 3, 11, 14, 16
Sti Hold Time before CLK rising (ST-Bus mode) before CLK falling (GCI mode)	t_{STiH}				Non-PLL Clock. 3, 9, 10 PLL Clock. 3, 11, 14, 15
2.048 Mb/s - Sto0,Sto1,EST1		20		ns	
4.096 Mb/s		20		ns	
8.192 Mb/s		20		ns	

† See "Notes" following AC Electrical Characteristics tables.

24.3 AC Parameters Referenced to Outgoing C4 or C8 Clock Signals

AC parameters are either measured with respect to incoming or outgoing clock signals. A list of the Clock Control Modes for the Local or Expansion Bus streams where the AC parameters are measured with respect to the outgoing clock signals are listed in Table 24. The parametric values are listed in the following tables.

TDM and Data Rate	Clock Control Mode	PCS	PC0S	CLK	FP	CLK Rate/ Data Rate	Timing Diagram
Local 2 Mb/s	all	1	1	C4o	F4o	2	Fig. 40 (ST-Bus) & Fig. 41 (GCI)
EBUS 2 Mb/s	all	1	1	C4o	F4o	2	
EBUS 4Mb/s	C4/F4	X	X	C8 (Output)	F8	2	
	C8/F8, C8P, C16	1	1	C8 (Output)	F8	2	
EBUS 8Mb/s	C4/F4	X	X	C8 (Output)	F8	1*	Fig. 42 (ST-Bus) & Fig. 43 (GCI)
	C8/F8, C8P, C16	1	1	C8 (Output)	F8	1*	Fig. 40 (ST-Bus) & Fig. 41 (GCI)

Table 24 - Timing Referenced to Output Clock Signals for TDM Streams

* Clock Rate/Data Rate=1, however the incoming data is clocked with the PLL generated clock at 3 quarters into the bit cell.

AC Electrical Characteristics - Output Delay Parameters Referenced to Output C4/C8 Signals

Characteristics	Sym	Min	Max	Units	Test Conditions†
Output Driver Enable Delay (2.048, 4.096, 8.192 Mb/s)	t_{OED}		55	ns	3
STo delay from active to High-Z, active to High-Z	t_{DZ},t_{ZD}				
2.048 Mb/s - Sto0,Sto1, EST0			35	ns	3, 11, 14, 15, 19
4.096 Mb/s			40	ns	3, 11, 14, 16, 20
8.192 Mb/s			40	ns	3, 11, 14, 16, 20
Sto Delay (high and low) from CLK falling (ST-Bus mode) from CLK rising (GCI mode)	t_{SToD}				
2.048 Mb/s - Sto0,Sto1,EST0			35	ns	3, 11, 14, 15, 19
4.096 Mb/s			40	ns	3, 11, 14, 16, 20
8.192 Mb/s			40	ns	3, 11, 14, 16, 20

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - Input Set and Hold Parameters Referenced to Output C4/ C8 Signals

Characteristics	Sym	Min	Max	Units	Test Conditions†
Sti Set-up Time before CLK rising (ST-Bus mode) before CLK falling (GCI mode)	t_{STiS}				
2.048 Mb/s - Sto0,Sto1,EST1		20		ns	3, 11, 14, 15, 19
4.096 Mb/s		15		ns	3, 11, 14, 15, 20
8.192 Mb/s		10		ns	3, 11, 14, 15, 20
Sti Hold Time before CLK rising (ST-Bus mode) before CLK falling (GCI mode)	t_{STiH}				
2.048 Mb/s - Sto0,Sto1,EST1		30		ns	3, 11, 14, 15, 19
4.096 Mb/s		25		ns	3, 11, 14, 15, 20
8.192 Mb/s		25		ns	3, 11, 14, 15, 20

† See "Notes" following AC Electrical Characteristics tables.

24.4 HRA Timing

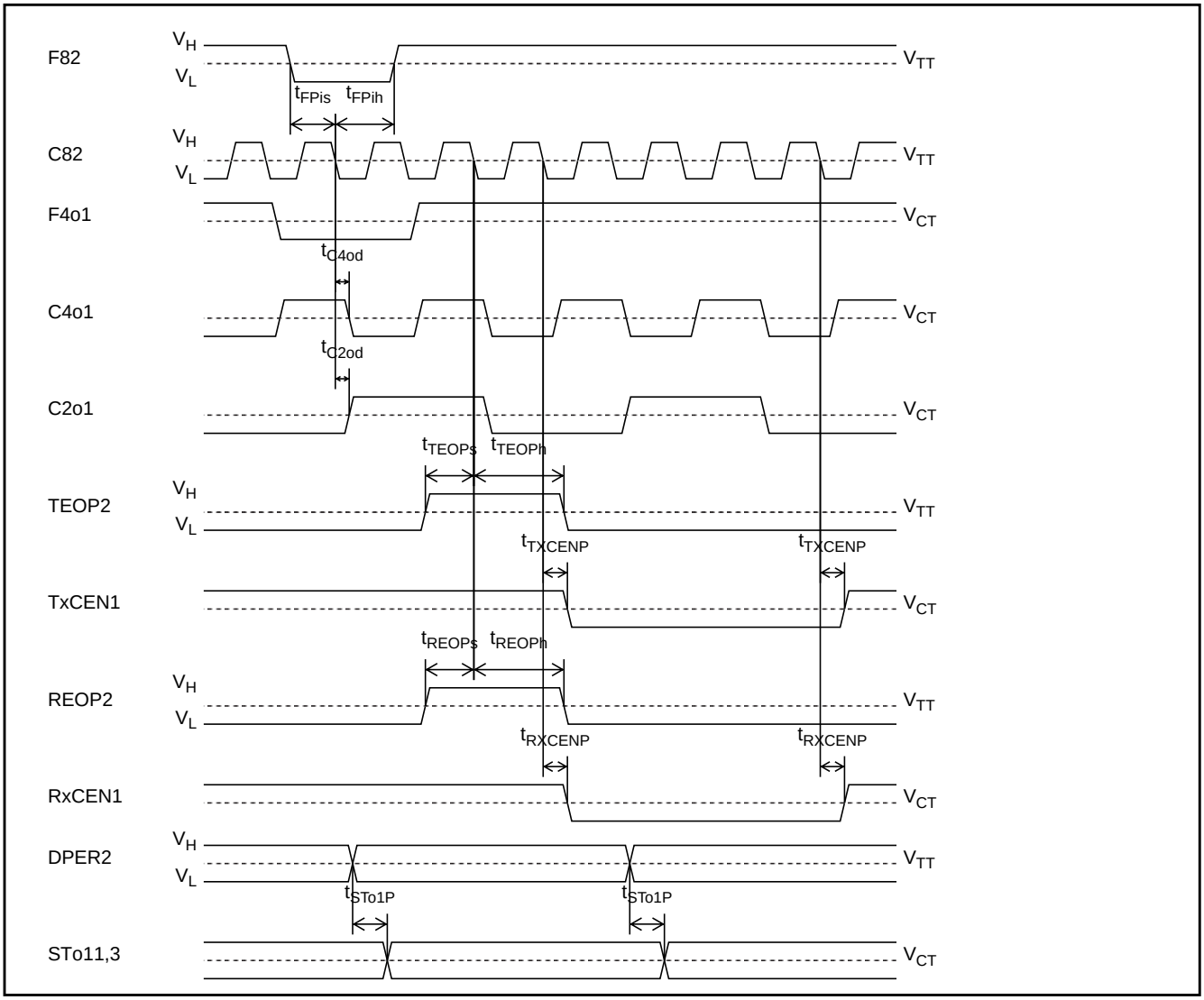


Figure 47 - The HDLC Controller Related Signals

Notes: 1. CMOS output 2. TTL input 3. Refer to STo1 output delay parameters.

AC Electrical Characteristics - HRA Timing

Characteristics	Sym	Min	Max	Units	Test Conditions†
TEOP Setup time	t_{TEOPS}	0	450	ns	9
TEOP Hold time	t_{TEOPH}	20	450	ns	9
TxCEN Propagation delay	t_{TxCENP}		70	ns	3, 9
REOP Setup time	t_{REOPS}	0	450	ns	9
REOP Hold time	t_{REOPH}	20	450	ns	9
RxCEN propagation delay	t_{RxCENP}		70	ns	3, 9
DPER to STo1 Propagation delay	t_{STo1P}		65	ns	3

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - PLL Typical Intrinsic Jitter‡

Characteristics	Master	Slave	Conditions/Notes†
	UIpp	UIpp	
Intrinsic jitter at C2o (2.048 MHz)	0.015	0.008	12,14-16,21,25,27-32
Intrinsic jitter at C4o (4.096 MHz)	0.029	0016	12,14-16,22,25,27-32
Intrinsic jitter at C8 (8.192 MHz)	0.057	0.033	12,14-16,23,25,27-32
Intrinsic jitter at C10o (10.24 MHz)	0.072	0.041	12,14-16,24,25,27-32

‡ Typical figures are at 25˚C and are for design aid only: not guaranteed and not subject to production testing.
† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - PLL Typical Input to Output Jitter Transfer for Master Mode‡

Characteristics	Input Jitter Frequency kHz	Output Jitter UIpp	Conditions/Notes†
Jitter at output for Input Jitter Frequency at 0.10UIpp	0.100	0.187	12,14-16,22,25,27-32,33
	4	0.187	
	5	0.191	
	6	0.194	
	8	0.200	
	10	0.207	
	15	0.228	
	20	0.247	
	25	0.261	
	28	0.257	
	30	0.241	
	34	0.224	
	36	0.210	
	40	0.180	
	45	0.165	
	50	0.150	
	60	0.130	
	70	0.119	
	80	0.109	
	90	0.105	
	100	0.101	
	200	0.088	

‡ Typical figures are at 25˚C and are for design aid only: not guaranteed and not subject to production testing.
† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - PLL Typical Input to Output Jitter Transfer for Slave Mode‡

Characteristics	Input Jitter Frequency kHz	Output Jitter UIpp	Conditions/Notes†
Jitter at output for Input Jitter Frequency at 0.09UIpp	0.001	0.077	12,14-16,22,25,27-32,34
	0.002	0.125	
	0.003	0.147	
	0.005	0.150	
	0.010	0.156	
	30	0.158	
	40	0.164	
	60	0.172	
	80	0.193	
	100	0.213	
	120	0.240	
	140	0.290	
	160	0.326	
	170	0.315	
	180	0.285	
	190	0.250	
	200	0.221	
	220	0.178	
	240	0.150	
	260	0.133	
	300	0.112	
	350	0.100	

‡ Typical figures are at 25˚C and are for design aid only: not guaranteed and not subject to production testing.
† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - PLL Typical Input Jitter Tolerance for C10o 40/60 Duty Cycle‡

Characteristics	Input Jitter Frequency kHz	Input Jitter Ulpp		Conditions/Notes†
		Master	Slave	
Input Jitter Tolerance for C10o 40/60 Duty Cycle	1	20.0	20.0	5,12,14-16,22,25,27-32,34
	3	8.0	8.0	
	5	5.0	3.0	
	10	1.0	0.9	
	20	1.0	0.5	
	40	0.7	0.4	
	60	0.4	0.5	
	80	0.2	0.3	
	100	0.1	0.2	
	120	0.07	0.2	
	140	0.07	0.2	
	160	0.04	0.2	
	180	0.04	0.2	

‡ Typical figures are at 25˚C and are for design aid only: not guaranteed and not subject to production testing.
† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - Intel/National - HPC Multiplexed Bus Mode

	Characteristics	Sym	Min	Max	Unit	Test Conditions†
1	ALE pulse width	t_{ALW}	20		ns	
2	Address setup from ALE falling	t_{ADS}	5		ns	
3	Address hold from ALE falling	t_{ADH}	10		ns	
4	$\overline{RD}$ active after ALE falling	t_{ALRD}	10		ns	
5	Data setup from $\overline{DTA}$ Low on Read	t_{DDR}	5		ns	5
6	$\overline{CS}$ hold after $\overline{RD}/\overline{WR}$	t_{CSRW}	0		ns	
7	$\overline{CS}$ setup from $\overline{RD}$	t_{CSR}	0		ns	
8	Data hold after $\overline{RD}$	t_{DHR}	5	30	ns	3, 4
9	$\overline{WR}$ delay after ALE falling	t_{ALWR}	10		ns	
10	$\overline{CS}$ setup from $\overline{WR}$	t_{CSW}	0		ns	
11	Valid Data Delay on write	t_{SWD}	0		ns	
12	Data hold after write	t_{DHW}	10		ns	
11	Acknowledgment Delay: Register Data Memory or Connect Memory Data Memory A6=1 DBR, DBT and FSK FIFO Read DBR, DBT and FSK FIFO Write	t_{AKD}		 95 135 200 + 1/2 C8P 2xC8p + 95 1.5xC8p + 85	 ns ns ns ns ns	 5 5 5,7 5 5
14	Acknowledgment Hold Time	t_{AKH}		15	ns	3, 4

† See "Notes" following AC Electrical Characteristics tables.

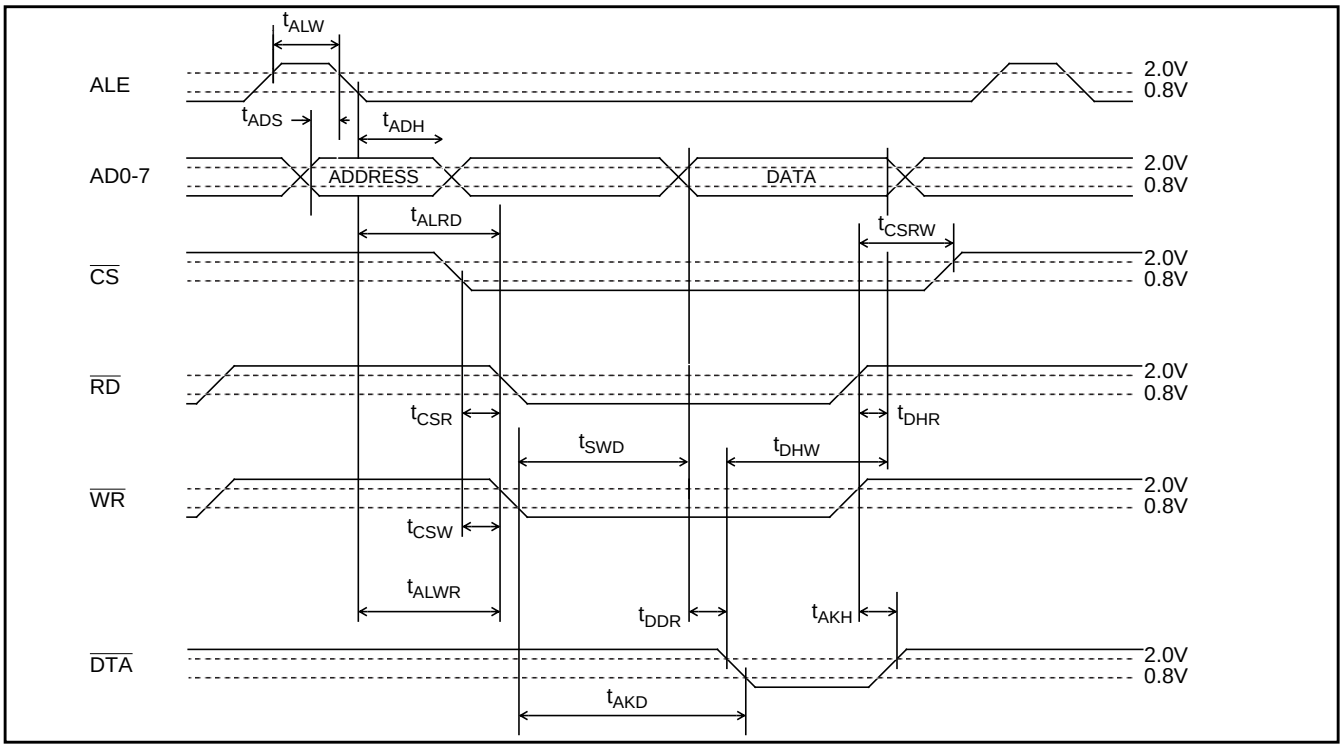


Figure 48 - Intel/National Multiplexed Bus Timing

AC Electrical Characteristics - Motorola Multiplexed Bus Mode

	Characteristics	Sym	Min	Max	Units	Test Conditions†
1	AS pulse width	t_{ASW}	20		ns	
2	Address setup from AS falling	t_{ADS}	5		ns	
3	Address hold from AS falling	t_{ADH}	10		ns	
4	Data setup from $\overline{DTA}$ Low on Read	t_{DDR}	0		ns	5
5	$\overline{CS}$ hold after DS falling	t_{CSH}	0		ns	
6	$\overline{CS}$ setup from DS rising	t_{CSS}	0		ns	
7	Data hold after write	t_{DHW}	10		ns	
8	Valid Data Delay on write	t_{SWD}	0		ns	
9	R/$\overline{W}$ setup from DS rising	t_{RWS}	0		ns	
10	R/$\overline{W}$ hold after DS falling	t_{RWH}	0		ns	
11	Data hold after read	t_{DHR}	5	30	ns	3, 4
12	DS delay after AS falling	t_{DSH}	10		ns	
13	Acknowledgment Delay: Register Data Memory or Connect Memory Data Memory A6=1 DBR, DBT and FSK FIFO Read DBR, DBT and FSK FIFO Write	t_{AKD}		 95 135 200 + 1/2 C8P 2xC8p + 95 1.5xC8p + 85	 ns ns ns ns ns	 5 5 5,7 5 5
14	Acknowledgment Hold Time	t_{AKH}		15	ns	3, 4

† See "Notes" following AC Electrical Characteristics tables.

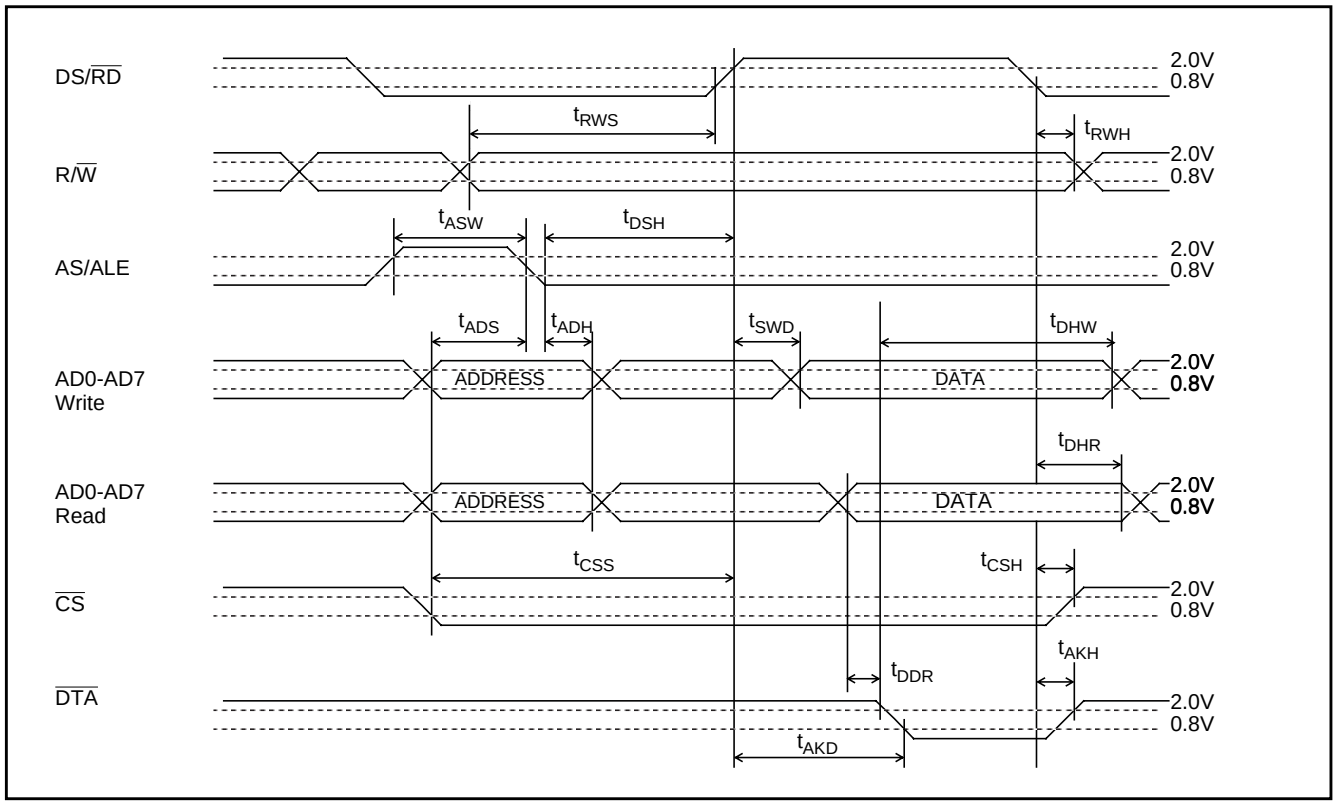


Figure 49 - Motorola Multiplexed Bus Timing

AC Electrical Characteristics - Motorola Non-Multiplexed Bus Mode

	Characteristics	Sym	Min	Max	unit	Test Conditions†
1	$\overline{CS}$ setup from $\overline{DS}$[1] falling	t_{CSS}	0		ns	
2	R/$\overline{W}$ setup from $\overline{DS}$[1] falling	t_{RWS}	0			
3	Address setup from $\overline{DS}$[1] falling	t_{ADS}	5		ns	
4	Address hold after $\overline{DS}$[1] falling	t_{ADH}	10		ns	
5	$\overline{CS}$ hold after $\overline{DS}$[1] rising	t_{CSH}	0			
6	R/$\overline{W}$ hold after $\overline{DS}$[1] rising	t_{RWH}	0			
7	Data setup from $\overline{DTA}$ Low on Read	t_{DDR}	5		ns	5
8	Data hold on read	t_{DHR}	5	30	ns	3, 4
9	Valid Data Delay on write	t_{SWD}	0		ns	
10	Data hold on write	t_{DHW}	10		ns	
11	Acknowledgment Delay: Register Data Memory or Connect Memory Data Memory A6=1 DBR, DBT and FSK FIFO Read DBR, DBT and FSK FIFO Write	t_{AKD}		 95 135 200 + 1/2 C8P 2xC8p + 95 1.5xC8p + 85	 ns ns ns ns ns	 5 5 5,7 5 5
12	Acknowledgment Hold Time	t_{AKH}		15	ns	3, 4

Note: 1. DS pin is used as $\overline{DS}$ in Motorola Non-Multiplexed Mode.
† See "Notes" following AC Electrical Characteristics tables.

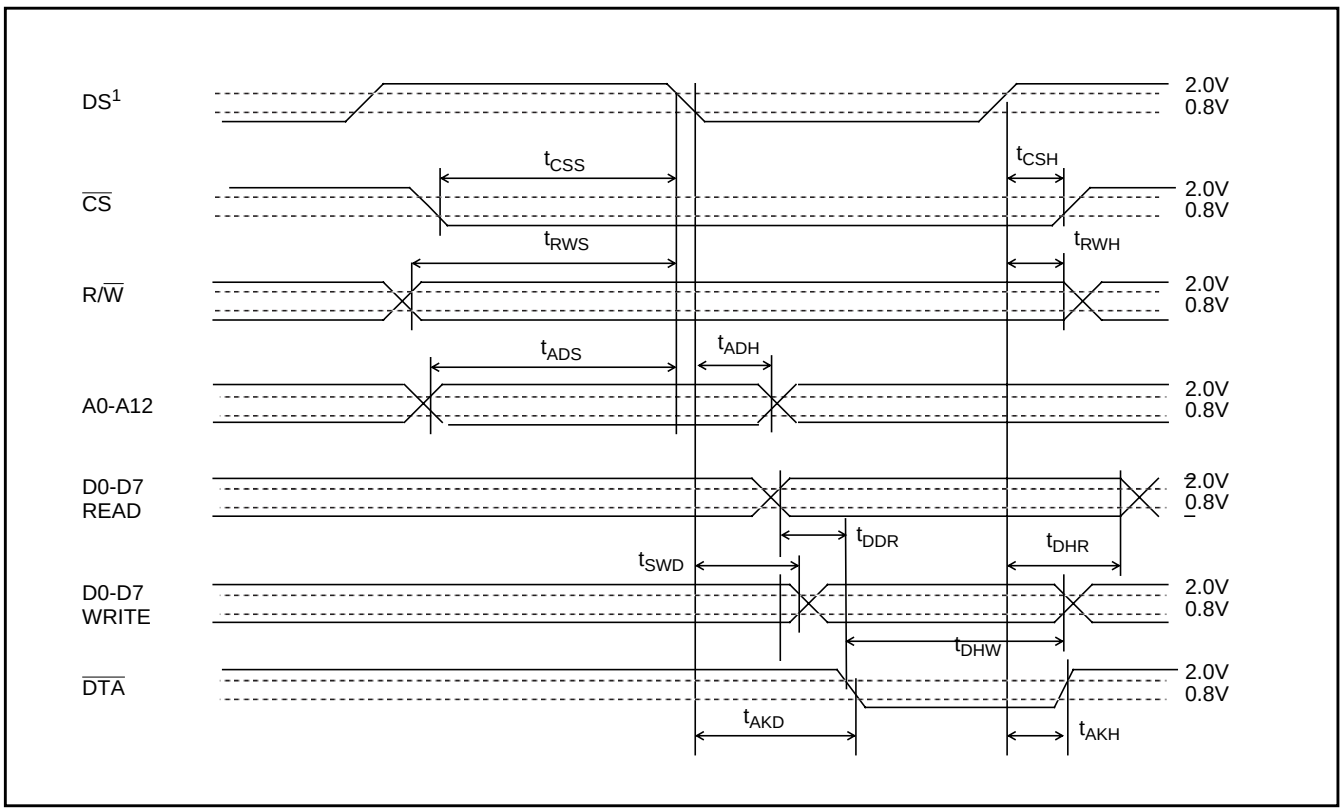


Figure 50 - Motorola Non-Multiplexed Bus Timing.

Note: 1. DS pin is used as $\overline{DS}$ in Motorola Non-Multiplexed Mode.

Notes:

Voltages are with respect to ground (Vss) unless otherwise stated.
Supply Voltage and operating temperature are as per Recommended Operating Conditions.
Timing parameters are as per AC Electrical Characteristics - Timing Parameter Measurement Voltage Levels

1: Measured with respect to 3/4 bittime, which for 4.096 Mb/s is 244ns x 3/4 = 183ns from beginning of bit cell
2: Measured with respect to 3/4 bittime, which for 8.192 Mb/s is 122ns x 3/4 = 91.5ns from beginning of bit cell
3: CL= 150pF, RL=1 K Ω load.
4: High Impedance is measured by pulling to the appropriate rail with RL with timing corrected to cancel time to discharge CL.
5: CL= 150pF capacitive load.
6: DS pin is used as DS in Motorola Non-Multiplexed Mode.
7: Acknowledgment may be held off for read of DM page a6=1.

8: PLL Disabled.
9: Timing Control Register bit PCS = 0.
10: Output Clock Control Register bit PCOS = 0.

11: Jitter on reference input is less than 1ns pp.
12: Applied jitter is sinusoidal.
13: Applied jitter is a squarewave of 8kHz of 32ns pp.

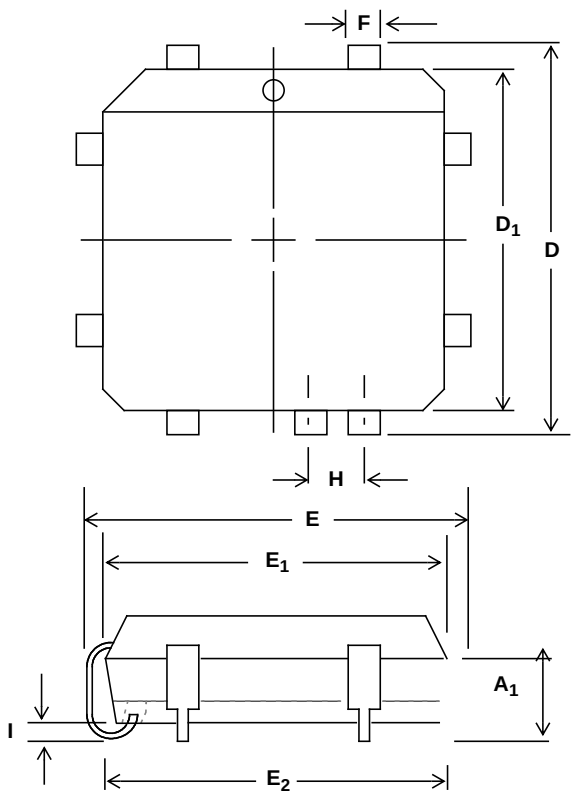
14: PLL Enabled.
15: Timing Control Register bit PCS = 1.
16: Output Clock Control Register bit PCOS = 1.

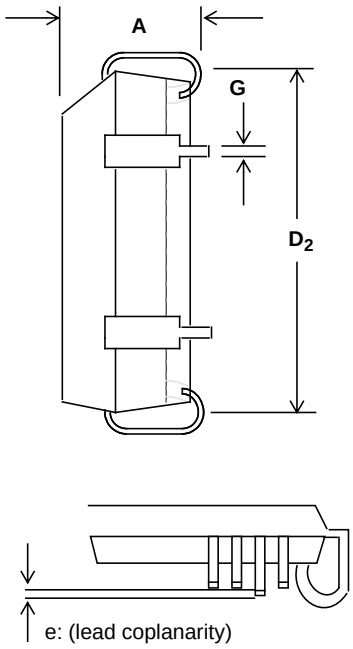
17: Measured w.r.t. to C4i.
18: Measured w.r.t. to C8 Input Clock.
19: Measured w.r.t. to C4ob.
20: Measured w.r.t. to C8 Output Clock.

21: 1 UIpp = 488ns for 2.048MHz signals.
22: 1 UIpp = 244ns for 4.096MHz signals.
23: 1 UIpp = 122ns for 8.192MHz signals.
24: 1 UIpp = 97.65ns for 10.24MHz signals.

25: No filter
26: Input clock reference selected is not C4F4.
27: C4F4 Input clock reference selected.
28: C8P Input clock reference selected.
29: C8F8 Input clock reference selected.
30: C16F8 Input clock reference selected.
31: C16 Input clock reference and HMVIP selected.
32: Jitter on reference input is 0.008 UIpp. 1UI=244ns.
33: PLL is in Master Mode.
34: PLL is in Slave Mode.

Package Outlines





Notes:
1) Not to scale
2) Dimensions in inches
3) (Dimensions in millimeters)
4) For D & E add for allowable Mold Protrusion 0.010"

Dim	20-Pin		28-Pin		44-Pin		68-Pin		84-Pin	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.200 (5.08)	0.165 (4.20)	0.200 (5.08)
A_1	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.130 (3.30)	0.090 (2.29)	0.130 (3.30)
D/E	0.385 (9.78)	0.395 (10.03)	0.485 (12.32)	0.495 (12.57)	0.685 (17.40)	0.695 (17.65)	0.985 (25.02)	0.995 (25.27)	1.185 (30.10)	1.195 (30.35)
D_1/E_1	0.350 (8.890)	0.356 (9.042)	0.450 (11.430)	0.456 (11.582)	0.650 (16.510)	0.656 (16.662)	0.950 (24.130)	0.958 (24.333)	1.150 (29.210)	1.158 (29.413)
D_2/E_2	0.290 (7.37)	0.330 (8.38)	0.390 (9.91)	0.430 (10.92)	0.590 (14.99)	0.630 (16.00)	0.890 (22.61)	0.930 (23.62)	1.090 (27.69)	1.130 (28.70)
e	0	0.004	0	0.004	0	0.004	0	0.004	0	0.004
F	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)
G	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)
H	0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)	
I	0.020 (0.51)		0.020 (0.51)		0.020 (0.51)		0.020 (0.51)		0.020 (0.51)	

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