MT9700FCLE/AG

FHD LCD Controller

Data Sheet

Version:	0.1
Release date:	2021-02-19

Document Revision History

Revision	Date	Author	Description
0.1	2021-02-19	DCC	Initial release

Table of Contents

1 Features

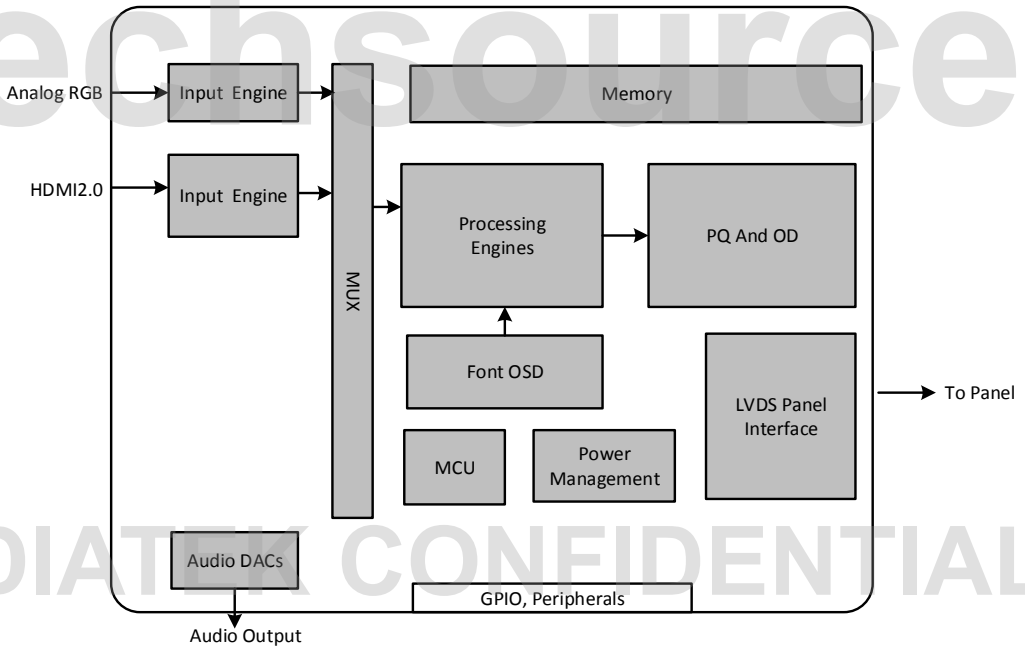
MT9700FCLE/AG key features include:

1. *High-quality scaling engine supports up to FHD @75 Hz (1920x1080@ 75 Hz) Panel*
2. *Multi-function digital interface engines*
3. *Integrated HDMI2.0 compliant receiver*
4. *10-bit data processing*
5. *Built-in LVDS Interface*
6. *Supports Response Time Enhancement*
7. *QFP 128 package*

- Input Ports
  - RGB analog input port supports up to 205 MHz
  - Full SOG supports up to 1080P
  - Composite sync supports copy protected signals
  - One digital input port
  - HDMI 2.0 and DVI 1.0 compliant receiver with HDCP 1.4/2.2
  - Supports HDMI 2.0 8/10/12-bit deep color mode (up to 225 MHz @ 1080P 60Hz with 12-bit deep color resolution)
  - Supports FreeSync
- Display Processing Engine
  - Variable sharpness control
  - Interlaced to progressive conversion
  - Media Window Enhancement (MWE)
    -Dynamic Luma Curve (DLC) with 32 segments
    -6 axis adjustments
  - Peaking & coring functions for sharpness enhancement and noise reduction
  - Brightness and contrast control
  - Programmable 10-bit gamma correction
  - sRGB support
  - Supports xvYCC
- Auto-Detection / Auto-Tune Support
  - Auto input signal format (SOG, Composite, Separated HSYNC, VSYNC, and DE)
  - Input mode detection support analyzes input video signal (H/V polarity, H/V frequency, interlace/field detect) – extensive status registers support robust detection of all VESA & IBM modes
  - Auto-tuning function including support for phase selection, image position, offset & gain and jitter detection
  - Smart screen-fitting
- On-screen Display Controller (OSD)
  - Built-in OSD generator with 2048 character fonts programmable RAM
  - OSD programmable font height
  - Internal OSD rotation degree of 90 and 270
  - Supports 2/4/8 multi-color fonts
  - Supports 256 color palette
  - Supports 6K code attributes
  - Gradient color function
  - Pattern generator for production test
  - Supports OSD MUX and alpha blending capability
  - Supports OSD gradient engine
- DPMS Support
  - Full Green Mode DPMS support
  - Low standby current
  - Ultra-low off mode
- Response Time Enhancement
  - Programmable look-up table with various word-length selections
  - Proprietary algorithm for memory size reduction
  - Programmable RTE strength
- Output Display Interface
  - Supports up to 2-ch LVDS FHD @90 Hz (1920x1080 @ 90Hz) panel interface
  - Spread spectrum output frequency for EMI suppression
  - PWM backlight intensity control
- Analog Audio Interface
  - Stereo L/R line input & output
  - Built-in audio output DAC
  - Separates analog PGA control for L/R channel
  - 60 steps analog PGA control range from -60dB to 6dB with mute
  - Digital PGA control range from -112dB to +12dB with fading and mute function
  - Supports headphone drive (20mW@32 Ohm, 40mW@16 Ohm)

- Digital Audio Interface
  - Supports master I²S and S/PDIF output interface
  - Supports volume control (-0.75dB/step)
  - Supports mute and fading function
- Embedded MCU
  - 32-bit micro controller
  - ISP interface
  - UART interface
  - GPIO & PWM for system control
- External Connection/Component
  - Built-in DDC circuit
  - DDC2B/2Bi/2B+/CI support
  - Supports External Serial Flash
- Misc.
  - Advanced power management controller
  - 128-pin QFP package

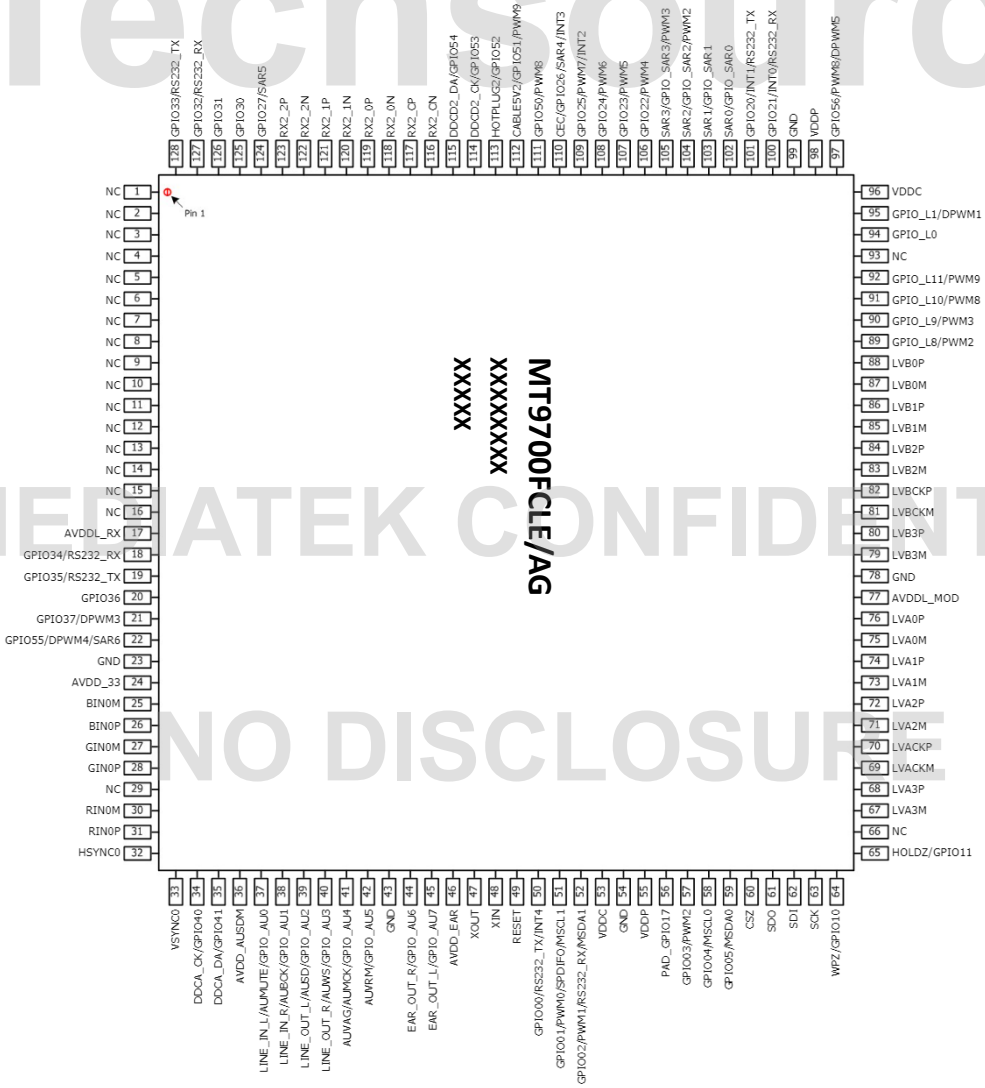
2 Block Diagram



3 General Description

The MT9700FCLE/AG is total solution graphics processing IC for LCD monitors with panel resolutions up to FHD. It is configured with a high-speed integrated triple-ADC/PLL, an integrated DVI / HDMI2.0 receiver, a high quality 10-bit display processing engine, an integrated micro-controller and output display interface that can support 2-ch LVDS panel interface format. MT9700FCLE/AG supports three flexible and configurable digital input interfaces to meet all state-of-the-art monitor design. To further reduce system costs, the MT9700FCLE/AG also integrates external LDO and power management control capability for green-mode requirements and spread-spectrum support for EMI management.

4 Pin Diagram (MT9700FCLE/AG)



5 Pin Description

5.1 Analog Interface

Pin Name	Pin Type	Function	Pin
BIN0M	Analog Input	Reference Ground for Analog Blue Input	25
BIN0P	Analog Input	Analog Blue Input	26
GIN0M	Analog Input	Reference Ground for Analog Green Input	27
GIN0P	Analog Input	Analog Green Input	28
RIN0M	Analog Input	Reference Ground for Analog Red Input	30
RIN0P	Analog Input	Analog Red Input	31
HSYNC0	Schmitt Trigger Input w/5V-tol.	Analog HSYNC Input	32
VSYNC0	Schmitt Trigger Input w/5V-tol.	Analog VSYNC Input	33

5.2 Combo Interface

Pin Name	Pin Type	Function	Pin
RX2_CN	DVI/HDMI Input	Negative DVI/HDMI Input for Link 2 Clock Channel	116
RX2_CP	DVI/HDMI Input	Positive DVI/HDMI Input for Link 2 Clock Channel	117
RX2_0N	DVI/HDMI Input	Negative DVI/HDMI Input for Link 2 Data Channel 0	118
RX2_0P	DVI/HDMI Input	Positive DVI/HDMI Input for Link 2 Data Channel 0	119
RX2_1N	DVI/HDMI Input	Negative DVI/HDMI Input for Link 2 Data Channel 1	120
RX2_1P	DVI/HDMI Input	Positive DVI/HDMI Input for Link 2 Data Channel 1	121
RX2_2N	DVI/HDMI Input	Negative DVI/HDMI Input for Link 2 Data Channel 2	122
RX2_2P	DVI/HDMI Input	Positive DVI/HDMI Input for Link 2 Data Channel 2	123

5.3 Audio Interface

Pin Name	Pin Type	Function	Pin
LINEIN_L/ AMUTE/ GPIO_AU0	Analog Input/ Output/ I/O	Main Audio Line Input Left Channel/ Audio Output Mute Control/ General Purpose Input/Output; 4mA driving strength	37
LINEIN_R/ AUBCK/ GPIO_AU1	Analog Input/ Output/ I/O	Main Audio Line Input Right Channel/ Audio Serial Clock Output/ General Purpose Input/Output; 4mA driving strength	38
LINEOUT_L/ AUSD/ GPIO_AU2	Analog Output/ Output/ I/O	Main Audio Line Output Left Channel/ Audio Serial Data Output/ General Purpose Input/Output; 4mA driving strength	39
LINEOUT_R/ AUWS/ GPIO_AU3	Analog Output/ Output/ I/O	Main Audio Line Output Right Channel / Audio Serial Word Select Output/ General Purpose Input/Output; 4mA driving strength	40
AUVAG/ AUMCK/ GPIO_AU4	Analog Output/ Output/ I/O	Reference Voltage for Audio Common Mode/ Audio Master Clock Output/ General Purpose Input/Output; 4mA driving strength	41
AUVRM/ GPIO_AU5	Analog Output/ I/O	Negative Reference Voltage for Audio ADC/ General Purpose Input/Output; 4mA driving strength	42
EAROUT_R/ GPIO_AU6	Analog Output/ I/O	Audio Right Channel Headphone Output/ General Purpose Input/Output; 4mA driving strength	44
EAROUT_L/ GPIO_AU7	Analog Output/ I/O	Audio Left Channel Headphone Output/ General Purpose Input/Output; 4mA driving strength	45

5.4 LVDS Interface

Pin Name	Pin Type	Function	Pin
LVA0M	Output	LVDS A-Link Channel 0 Negative Data Output	75
LVA0P	Output	LVDS A-Link Channel 0 Positive Data Output	76
LVA1M	Output	LVDS A-Link Channel 1 Negative Data Output	73
LVA1P	Output	LVDS A-Link Channel 1 Positive Data Output	74
LVA2M	Output	LVDS A-Link Channel 2 Negative Data Output	71
LVA2P	Output	LVDS A-Link Channel 2 Positive Data Output	72
LVA3M	Output	LVDS A-Link Channel 3 Negative Data Output	67
LVA3P	Output	LVDS A-Link Channel 3 Positive Data Output	68
LVACKM	Output	LVDS A-Link Negative Clock Output	69

Pin Name	Pin Type	Function	Pin
LVACKP	Output	LVDS A-Link Positive Clock Output	70
LVB0M	Output	LVDS B-Link Channel 0 Negative Data Output	87
LVB0P	Output	LVDS B-Link Channel 0 Positive Data Output	88
LVB1M	Output	LVDS B-Link Channel 1 Negative Data Output	85
LVB1P	Output	LVDS B-Link Channel 1 Positive Data Output	86
LVB2M	Output	LVDS B-Link Channel 2 Negative Data Output	83
LVB2P	Output	LVDS B-Link Channel 2 Positive Data Output	84
LVB3M	Output	LVDS B-Link Channel 3 Negative Data Output	79
LVB3P	Output	LVDS B-Link Channel 3 Positive Data Output	80
LVBCKM	Output	LVDS B-Link Negative Clock Output	81
LVBCKP	Output	LVDS B-Link Positive Clock Output	82

5.5 Serial Flash Interface

Pin Name	Pin Type	Function	Pin
CSZ	Output	SPI Flash Chip Select	60
SDO	Input	SPI Flash Serial Data Output	61
SDI	Output	SPI Flash Serial Data Input	62
SCK	Output	SPI Flash Serial Clock	63
WPZ/ GPIO10	I/O w/ 5V-tolerant	SPI Flash Write Protect/ General Purpose Input/Output; 4mA driving strength	64
HOLDZ/ GPIO11	I/O w/ 5V-tolerant	SPI Flash Hold/ General Purpose Input/Output; 4mA driving strength	65

5.6 GPIO Interface

Pin Name	Pin Type	Function	Pin
GPIO00/ RS232_TX/ INT4	I/O w/5V-tolerant	General Purpose Input/Output; 4mA driving strength/ UART Transmitter/ External interrupt 4	50
GPIO01/ PWM0/ SPDIFO/ MSCL1	I/O w/5V-tolerant/ Output/ Output/ I/O w/5V-tolerant	General Purpose Input/Output; 4mA driving strength/ Pulse Width Modulation Output/ Audio S/PDIF Output / Master I2C Clock 1	51

Pin Name	Pin Type	Function	Pin
GPIO02/ PWM1/ RS232_RX/ MSDA1	I/O w/5V-tolerant/ Output/ I/O w/5V-tolerant/ I/O w/5V-tolerant	General Purpose Input/Output; 4mA driving strength/ Pulse Width Modulation Output/ UART Receiver/ Master I2C Data 1	52
GPIO03/ PWM2	I/O w/5V-tolerant/ Output	General Purpose Input/Output; 4mA driving strength/ Pulse Width Modulation Output	57
GPIO04/ MSCL0	I/O w/5V-tolerant	General Purpose Input/Output; 4mA driving strength/ Master I2C Clock 0	58
GPIO05/ MSDA0	I/O w/5V-tolerant	General Purpose Input/Output; 4mA driving strength/ Master I2C Data 0	59
GPIO17	I/O w/5V-tolerant	General Purpose Input/Output; 4mA driving strength	56
GPIO20/ INT1/ RS232_TX/ PM0W_PWR	I/O w/5V-tolerant	General Purpose Input/Output; 4mA driving strength/ External interrupt 1/ UART Transmitter/ Ultra-low Off mode Power Control	101
GPIO21/ INT0/ RS232_RX/ PM0W_WK	I/O w/5V-tolerant	General Purpose Input/Output; 4mA driving strength / External interrupt 0/ UART Receiver/ Ultra-low Off Mode Wakeup	100
GPIO22/ PWM4	I/O w/5V-tolerant/ Output	General Purpose Input/Output; 8/16mA driving strength/ Pulse Width Modulation Output	106
GPIO23/ PWM5	I/O w/5V-tolerant/ Output	General Purpose Input/Output; 8/16mA driving strength/ Pulse Width Modulation Output	107
GPIO24/ PWM6	I/O w/5V-tolerant/ Output	General Purpose Input/Output; 4mA driving strength/ Pulse Width Modulation Output	108
GPIO25/ PWM7/ INT2	I/O w/5V-tolerant/ Output/ -	General Purpose Input/Output; 4mA driving strength/ Pulse Width Modulation Output/ External Interrupt 2	109
CEC/ GPIO26/ SAR4/ INT3	I/O / I/O w/5V-tolerant/ Input/ -	HDMI Consumer Electrics Control(CEC) Bus IO with 27Kohm pull high/ General Purpose Input/Output; 4mA driving strength/ SAR ADC Input/ External Interrupt 3	110
GPIO27/ SAR5	I/O w/5V-tolerant/ Input	General Purpose Input/Output; 4mA driving strength/ SAR ADC Input	124
GPIO30	I/O w/ 5V-tolerant	General Purpose Input/Output ; 4mA driving strength	125
GPIO31	I/O w/ 5V-tolerant	General Purpose Input/Output ; 4mA driving strength	126

Pin Name	Pin Type	Function	Pin
GPIO32/ RS232_RX	I/O w/ 5V-tolerant/	General Purpose Input/Output ; 4mA driving strength/ UART Receiver	127
GPIO33/ RS232_TX	I/O w/ 5V-tolerant/	General Purpose Input/Output ; 4mA driving strength/ UART Transmitter	128
GPIO34/ RS232_RX	I/O w/ 5V-tolerant/	General Purpose Input/Output ; 4mA driving strength/ UART Receiver	18
GPIO35/ RS232_TX	I/O w/ 5V-tolerant/	General Purpose Input/Output ; 4mA driving strength/ UART Transmitter	19
GPIO36	I/O w/ 5V-tolerant	General Purpose Input/Output ; 4mA driving strength	20
GPIO37/ DPWM3	I/O w/ 5V-tolerant/ Output	General Purpose Input/Output ; 4mA driving strength/ Display Pulse Width Modulation Output	21
GPIO50/ PWM8	I/O w/5V-tolerant/ Output	General Purpose Input/Output; 4mA driving strength/ Pulse Width Modulation Output	111
GPIO55/ DPWM4/ SAR6	I/O w/5V-tolerant/ Output/ Input	General Purpose Input/Output; 4mA driving strength/ Display Pulse Width Modulation Output SAR ADC Input/	22
GPIO56/ PWM8/ DPWM5	I/O w/5V-tolerant/ Output/ Output	General Purpose Input/Output; 4mA driving strength/ Pulse Width Modulation Output/ Display Pulse Width Modulation Output	97
GPIO_L0	I/O w/ 5V-tolerant	General Purpose Input/Output; 4mA driving strength	94
GPIO_L1/ DPWM1	I/O w/ 5V-tolerant/ Output	General Purpose Input/Output; 4mA driving strength/ Display Pulse Width Modulation Output	95
GPIO_L8/ PWM2	I/O w/ 5V-tolerant/ Output	General Purpose Input/Output ; 4mA driving strength/ Pulse Width Modulation Output	89
GPIO_L9/ PWM3	I/O w/ 5V-tolerant/ Output	General Purpose Input/Output ; 4mA driving strength/ Pulse Width Modulation Output	90
GPIO_L10/ PWM8	I/O w/ 5V-tolerant/ Output	General Purpose Input/Output ; 4mA driving strength/ Pulse Width Modulation Output	91
GPIO_L11/ PWM9	I/O w/ 5V-tolerant/ Output	General Purpose Input/Output ; 4mA driving strength/ Pulse Width Modulation Output	92
SAR0/ GPIO_SAR0	Input/ I/O w/5V-tolerant	SAR ADC Input/ General Purpose Input/Output; 4mA driving strength	102
SAR1/ GPIO_SAR1	Input/ I/O w/5V-tolerant	SAR ADC Input/ General Purpose Input/Output; 4mA driving strength	103
SAR2/ GPIO_SAR2/ PWM2	Input/ I/O w/5V-tolerant/ Output	SAR ADC Input/ General Purpose Input/Output; 4mA driving strength/ Pulse Width Modulation Output	104

Pin Name	Pin Type	Function	Pin
SAR3/ GPIO_SAR3/ PWM3	Input/ I/O w/5V-tolerant/ Output	SAR ADC Input/ General Purpose Input/Output; 4mA driving strength/ Pulse Width Modulation Output	105

5.7 Misc. Interface

Pin Name	Pin Type	Function	Pin
DDCD2_CK/ GPIO53	I/O w/ 5V-tolerant	DDC Clock and HDCP Slave Serial Port Clock for DVI/HDMI Interface Main Link 2/ General Purpose Input/Output ; 4mA driving strength	114
DDCD2_DA/ GPIO54	I/O w/ 5V-tolerant	DDC Data and HDCP Slave Serial Port Data for DVI/HDMI Interface Main Link 2/ General Purpose Input/Output ; 4mA driving strength	115
HOTPLUG2/ GPIO52	I/O w/ 5V-tolerant	HOTPLUG for DVI/HDMI Interface Link2/ General Purpose Input/Output ; 4mA driving strength	113
CABLE5V2/ GPIO51/ PWM9/ DPWM0	I/O w/ 5V-tolerant/ I/O w/ 5V-tolerant/ Output/ Output	Cable 5V for HPD/ General Purpose Input/Output ; 4mA driving strength/ Pulse Width Modulation Output/ Display Pulse Width Modulation Output	112
DDCA_CK/ GPIO40	I/O w/ 5V-tolerant	DDC Clock for Analog Input/ General Purpose Input/Output ; 4mA driving strength	34
DDCA_DA/ GPIO41	I/O w/ 5V-tolerant	DDC Data for Analog Input/ General Purpose Input/Output ; 4mA driving strength	35
RESET	Input w/5V-tolerant	Chip Reset; High Reset	49
XIN	Analog Input	Crystal Oscillator Input	48
XOUT	Analog Output	Crystal Oscillator Output	47

5.8 Power Pin Interface

Pin Name	Pin Type	Function	Pin
AVDD_33	3.3V Power	Analog Power	24
AVDDL_RX	0.95V Power	Analog Power	17
AVDDL_MOD	0.95V Power	Digital Power for Panel Interface	77
AVDD_EAR	3.3V Power	Analog Power for Earphone	46

Pin Name	Pin Type	Function	Pin
AVDD_AUSDM	3.3V Power	Analog Power for Audio	36
VDDP	3.3V Power	Digital Output Power	55, 98
VDDC	0.95V Power	Digital Core Power	53, 96
GND	Ground	Ground	23, 43, 54, 78, 99

5.9 No Connection

Pin Name	Pin Type	Function	Pin
NC	-	No connect. Leave this pin floating.	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 29, 66, 93

6 Electrical Specifications

6.1 Analog Interface Characteristics

Parameter	Min	Typ	Max	Unit
VIDEO ADC Resolution		8		Bits
DC ACCURACY				
Differential Nonlinearity		±0.5		LSB
Integral Nonlinearity		±1		LSB
VIDEO ANALOG INPUT				
Input Voltage Range	0.5		1.0	V p-p
Input Full-Scale Matching		1.5		%FS
Brightness Level Adjustment		50		%FS
Sync-On-Green Amplitude		0.3		V p-p
SWITCHING PERFORMANCE				
Maximum Conversion Rate	202.5			MSPS
Minimum Conversion Rate			12	MSPS
HSYNC Input Frequency	15		200	kHz
VSYNC Input Frequency	10		200	Hz
PLL Clock Rate	12		220	MHz
PLL Jitter		500		ps p-p
Sampling Phase Tempco		15		ps/°C
DIGITAL INPUTS				
Input Voltage, High (V_{IH})	2.5			V
Input Voltage, Low (V_{IL})			0.8	V
Input Current, High (I_{IH})			-1.0	uA
Input Current, Low (I_{IL})			1.0	uA
Input Capacitance		5		pF
DIGITAL OUTPUTS				
Output Voltage, High (V_{OH})	VDDP-0.1			V
Output Voltage, Low (V_{OL})			0.1	V
AUDIO				
ADC Input		3.3		V p-p
DAC Output		2.828		V p-p
SAR ADC Input	0		VDDP	V

Parameter	Min	Typ	Max	Unit
GPIO Interface				
Input Voltage, High (VIH)			2.0	V
Input Voltage, Low (VIL)	0.8			V

Specifications subject to change without notice.
Note: Input full scale is 1.0V, but input range is 0 ~ 3.3V.
VDDP is 3.3V supply voltages

6.2 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
3.3V Supply Voltages	V_{VDD_33}	3.14	3.3	3.46	V
0.95V Supply Voltages	V_{VDDC}	0.92	0.95	0.98	V
Ambient Operating Temperature	T_A	0		70	°C
Junction Temperature	T_J			125	°C

6.3 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
3.3V Supply Voltages	V_{VDD_33}		3.63	V
0.95V Supply Voltages	V_{VDDC}		1.05	V
Input Voltage (5V tolerant inputs)	$V_{IN5Vtol}$		5.3	V
Input Voltage (non 5V tolerant inputs)	V_{IN}		V_{VDD_33}	V
Storage Temperature	T_{STG}	-40	150	°C

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

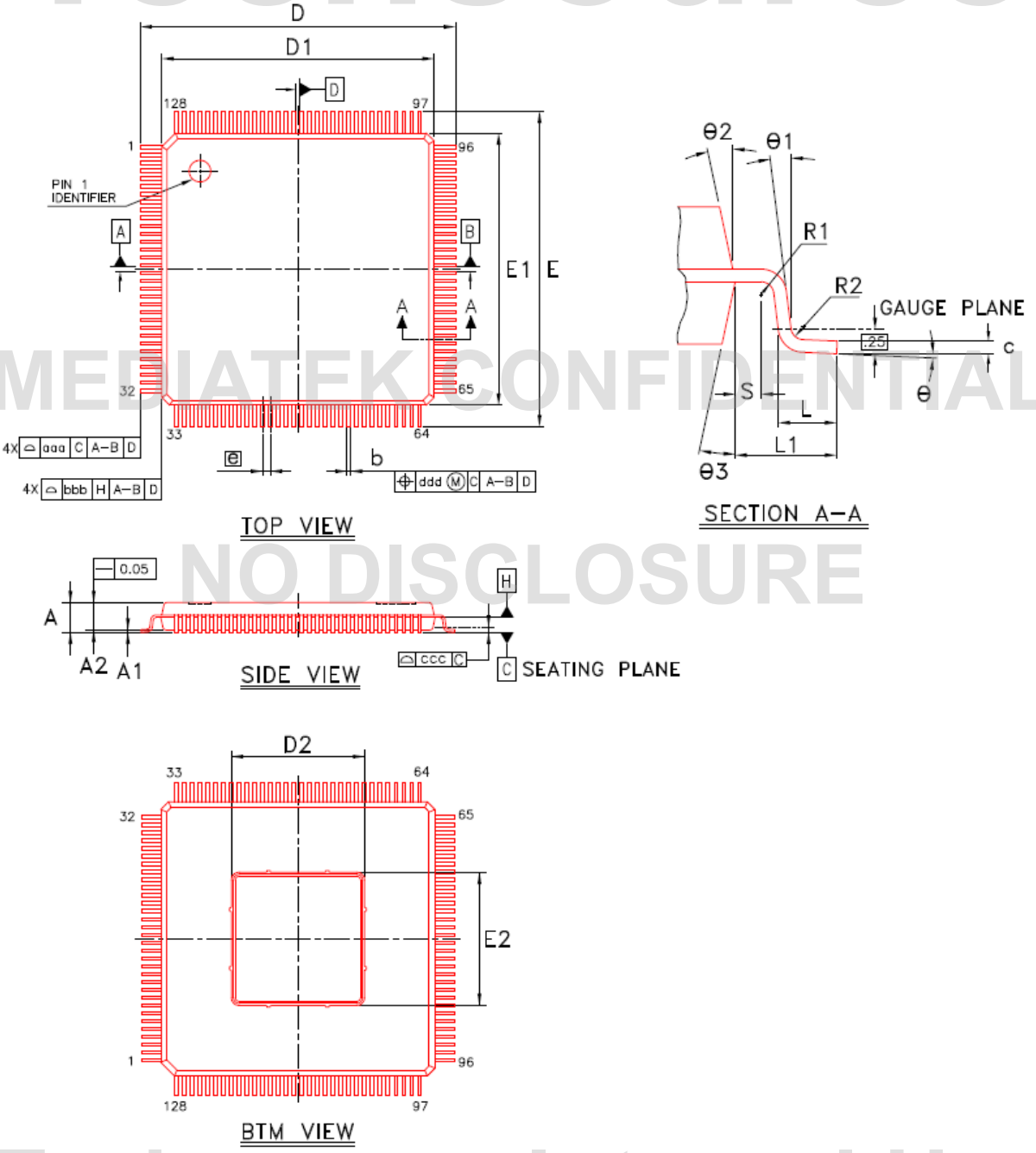
7 Ordering Guide

Part Number	Temperature Range	Package Description	Package Option
MT9700FCLE/AG	0°C to +70°C	QFP	128-pin

8 Top Marking

Line	Content	Description
1	MEDIATEK	Logo
2	MT9700FCLE/AG	Part Name
3	DDDD	Date Code
	H	Green Package

9 Mechanical Dimensions



ITEM		SYMBOL	MIN.	NOM.	MAX.
Total height		A	--	--	1.60
Stand off		A1	0.025	--	0.127
Mold thickness		A2	1.35	1.40	1.45
Lead width		b	0.13	0.18	0.23
Outer Lead Distance	X	D	16.00 BSC.		
	Y	E	16.00 BSC.		
Package size	X	D1	14.00 BSC.		
	Y	E1	14.00 BSC.		
E-pad size	X	D2	6.70	6.80	6.90
	Y	E2	6.70	6.80	6.90
Lead pitch		e	0.40 BSC.		
Lead ARC		R1	0.08	--	--
Lead ARC		R2	0.08	--	0.20
Angle		θ	0°	3.5°	7°
Angle 1		θ1	0°	--	--
Angle 2		θ2	11°	12°	13°
Angle 3		θ3	11°	12°	13°
L/F thickness		c	0.09	--	0.20
L		L	0.45	0.60	0.75
Lead length		L1	1.00 REF.		
S		S	0.20	--	--
Package profile of a surface		aaa	0.20		
Package profile of a surface		bbb	0.20		
Lead profile of a surface		ccc	0.08		
Lead position		ddd	0.07		

TITLE: PACKAGE OUTLINE EP-LQFP 128L 14 X 14 X 1.6 mm			
DWG. NO.	REV.	SHEET	UNIT
MT-SP01211	A	1 OF 2	MM

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