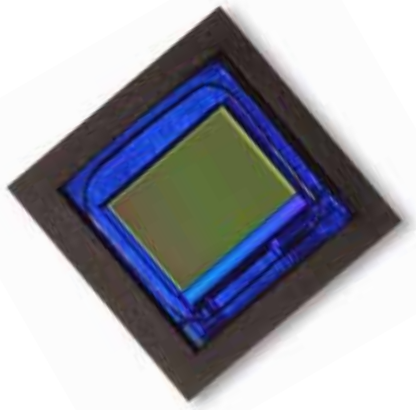
1/3-Inch, Wide-VGA CMOS Digital Image Sensor

Rugged Specs and High Quality for Scene-Understanding and Smart Imaging Applications Micron's MT9V022 has specifically been designed to support the demanding interior and exterior needs of automotive imaging, which makes it ideal for a wide variety of scene understanding and smart imaging applications in real-world environments. This wide-VGA CMOS image sensor features DigitalClarity™, Micron's breakthrough, low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.



Applications

- Automotive
- Unattended surveillance
- Stereo vision
- Security
- Smart vision
- Automation
- Video as input
- Machine vision

Features

- Micron's DigitalClarity™ CMOS imaging technology
- Double-buffered global shutter photodiode pixels
- Simultaneous integration and readout
- Enhanced Near-IR performance (NIR QE >35%)
- Progressive or interlaced readout modes
- Linear or high dynamic range pixel response
- >99% global shutter efficiency
- Register lock capability
- User-Programmable window size within frame
- 2 x 2 and 4 x 4 pixel averaging of the full resolution
- ADC On-Chip (10-bit linear or 12-bit to 10-bit companding mode)
- Auto exposure control (AEC)
- Auto gain control (AGC)
- Black level calibration (BLC)
- User-Programmable regional gain and exposure weighting (25 regions)
- Support for 4 unique serial control register IDs to control multiple imagers on the same bus
- Master/Slave dual sensor operation for stereoscopic, foveal, or hyperspectral operation
- On-Chip digital thermometer
- Data output formats:
  - Single sensor mode: 10-bit parallel/stand-alone or 8-bit or 10-bit serial LVDS
  - Dual sensor mode: Interspersed 8-bit serial LVDS

Key Parameters	
Optical format	1/3-inch
Active imager size	4.51mm(H) x 2.88mm(V) 5.35mm Diagonal
Active pixels	752H x 480V
Pixel size	6.0µm x 6.0µm
Color filter array	Monochrome or color RGB Bayer pattern
Shutter type	Double-Buffered global shutter TrueSNAP™
Maximum data rate Master clock	26.6 Mp/s 26.6 MHz
Full resolution	752 x 480
Frame rate	60 fps (at full resolution)
ADC resolution	10-bit
Responsivity	4.8 V/lux-sec (550nm)
Dynamic range	>55dB linear; >80dB–100dB in HiDy Mode
Supply voltage	3.3V ±0.3V (all supplies)
Power consumption	<320mW at maximum data rate; 100µW standby current
Operating temperature	–40°C to +85°C
Packaging	52-ball IBGA, automotive-qualified; wafer or die

General Description

The MT9V022 active imaging pixel array is 752H x 480V. It incorporates sophisticated camera functions on-chip, such as averaging 2 x 2 and 4 x 4, to improve SNR when operating in smaller resolutions, as well as windowing and column and row mirroring. It is programmable through a simple two-wire serial interface. The MT9V022 pixel response can be configured for either linear light response with >55dB of dynamic range or for high dynamic range response with as much as 100dB of dynamic range.

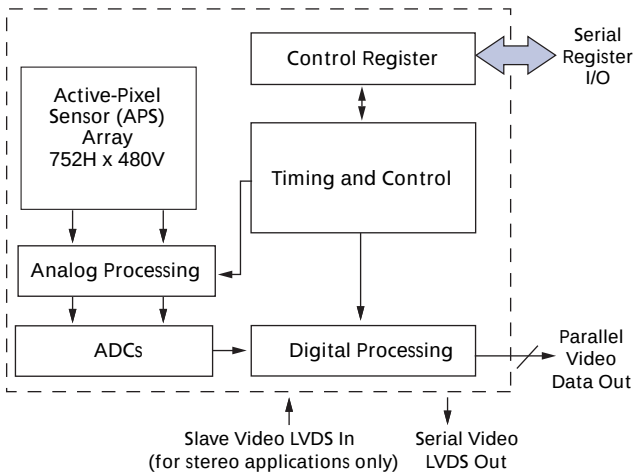
The MT9V022 can be operated in its default mode or be programmed by the user for frame size, exposure, gain setting, and other parameters. The default mode outputs a wide-VGA-sized image at 60 frames per second (fps). An on-chip analog-to-digital converter (ADC) provides 10 bits per pixel. The user can alternatively enable 12-bit resolution companded to 10 bits for small signals, enabling more accurate digitization for darker areas in the image.

In addition to a traditional, parallel logic output, the MT9V022 also features a serial low-voltage differential signaling (LVDS) output.

The sensor can be operated in stereo-camera mode, where the sensor, designated as a stereo-master, is able to merge the data from itself and the stereo-slave sensor into one serial LVDS stream.

The sensor is designed to operate in a wide temperature range (–40°C to +85°C). A built-in digital thermometer allows the host to read the temperature through the two-wire serial interface.

Figure 1: Block Diagram



Operational Modes

The MT9V022 works in master, snapshot, or slave mode. In master mode, the sensor generates the readout timing. There are two possible operation methods for master mode: simultaneous and sequential. In simultaneous master mode, the exposure period occurs during readout. The exposure and readout occur in parallel rather than sequentially, making this the fastest mode of operation.

In sequential master mode, the exposure period is followed by readout, and the frame rate changes as the integration time changes.

In snapshot mode, the start of the integration period is determined by the externally-applied EXPOSURE pulse that the user inputs to the MT9V022. The sensor in snapshot mode can capture a single image or a sequence of images.

In slave mode, the sensor accepts both external integration and readout controls.

The integration time is programmed through the two-wire serial interface during master or snapshot modes, or controlled via an externally generated control signal during slave mode.

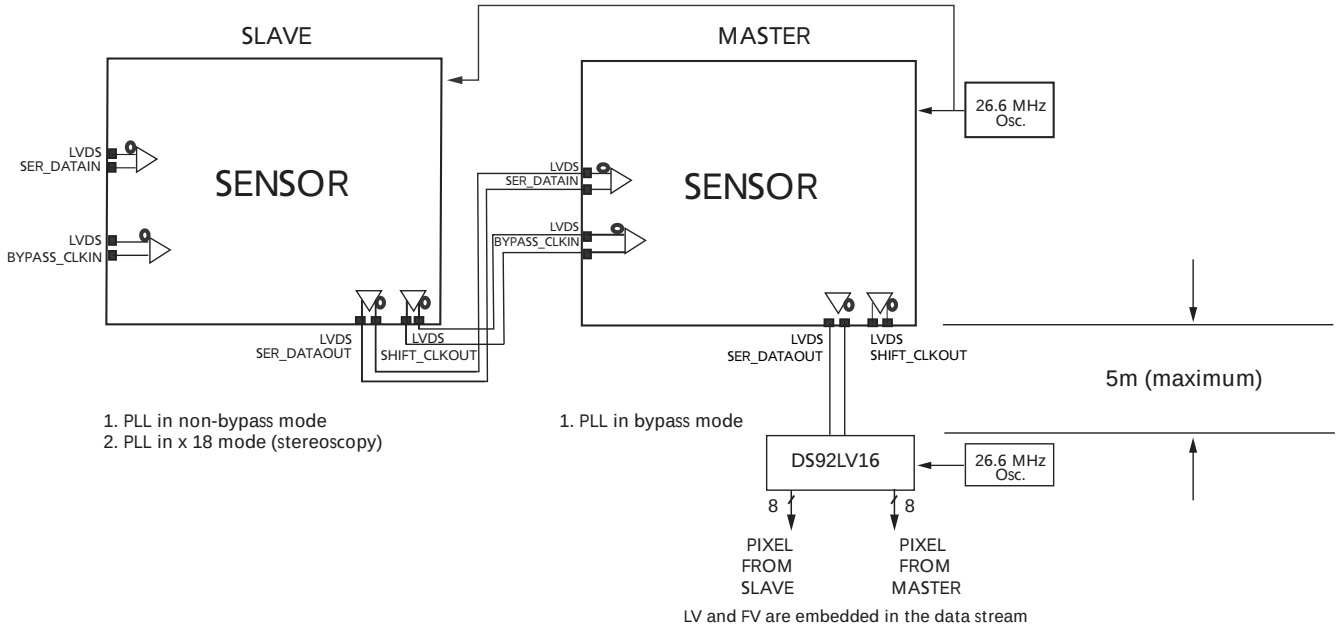
LVDS Serial Output (Stand-Alone and Stereoscopic Operation)

The LVDS interface allows for the streaming of sensor data serially to a standard off-the shelf deserializer up to 8 meters away from the sensor. The LVDS serial output could either be data from a single sensor (stand-alone) or stream-merged data from a pair (master and slave) of synchronized MT9V022 devices.

The pixels (and controls) are packeted—12-bit packets for stand-alone mode and 18-bit packets (2 frame bits and 8 data bits from each sensor) for stereoscopic mode. All serial signals (clock and data) is LVDS.

An LVDS connection overview for a single MT9V022 and for stereoscopic pair of MT9V022 devices is shown in Figure 2.

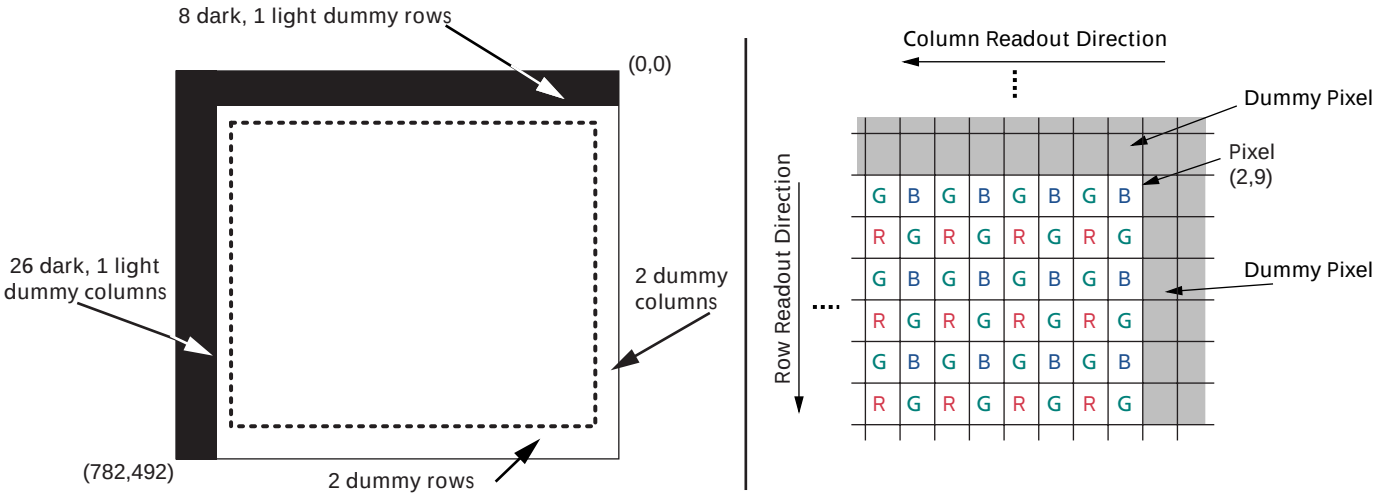
Figure 2: LVDS Stereoscopic Topology



Pixel Data Format and Pixel Array Structure

The MT9V022 pixel array is configured of 782 columns by 492 rows, as shown in Figure 3. The left 26 columns and the top 8 rows of pixels are optically black and can be used to monitor the black level. The black row data is used internally for the automatic black level adjustment.

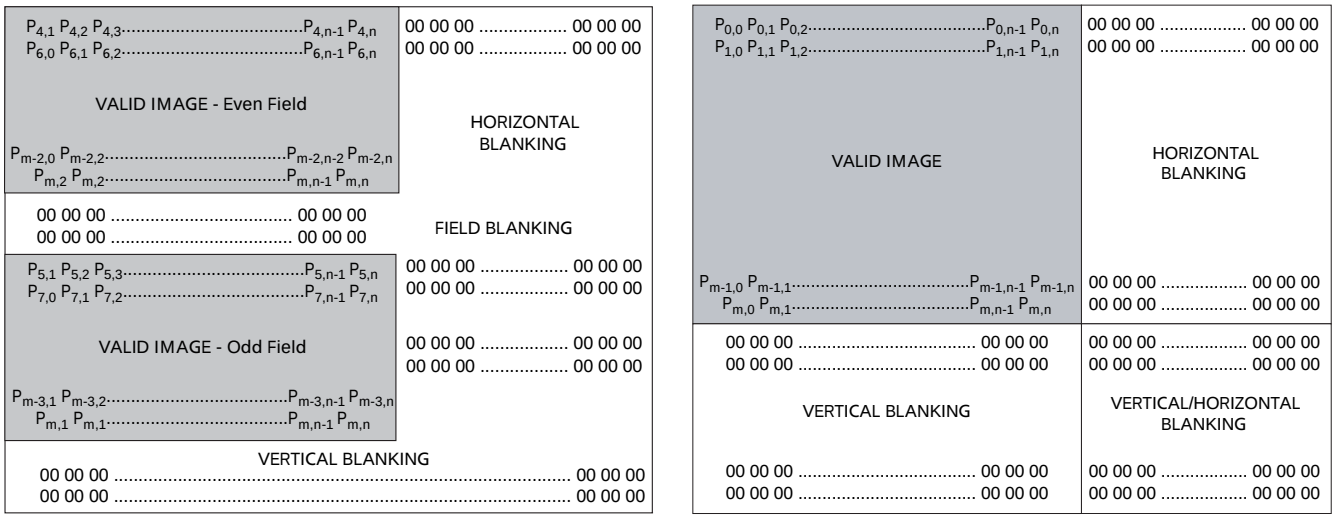
Figure 3: Pixel Array Description and Color Pattern Detail



Output Data Format

The MT9V022 image data can be read out in a progressive scan or in interlaced scan mode. Valid image data is surrounded by horizontal and vertical blanking, as shown in Figure 4.

Figure 4: Spatial Illustration of Image Readout: Interlaced Scan (left) and Progressive Scan (right)



Output Data Timing

The data output of the MT9V022 is synchronized with the PIXCLK output. When LINE_VALID is HIGH, one 10-bit pixel datum is output every PIXCLK period.

Figure 5: Row Timing and FRAME_VALID/LINE_VALID Signals

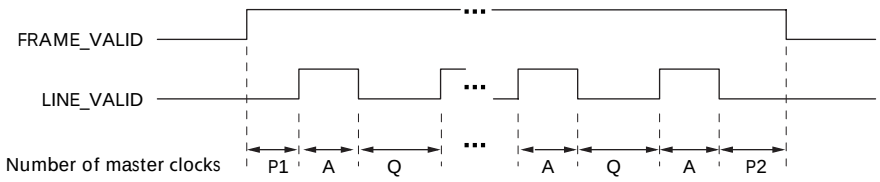
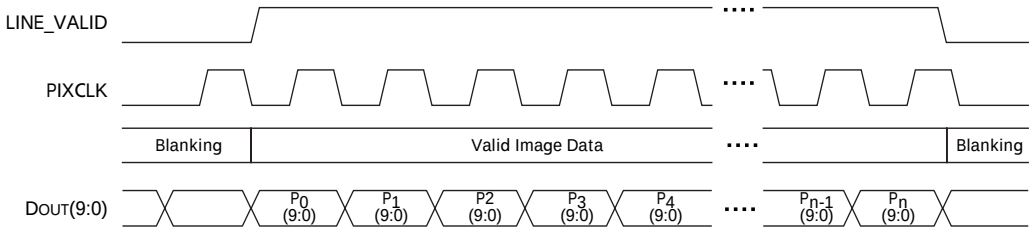


Figure 6: Timing Example of Pixel Data



Note: The parameters P1, A, Q, and P2 are defined in Table 1 on page 5.

Table 1: Frame Time

Parameter	Description	Pixel Clock	Master Clocks	Time	Units
A	Active data time	752	752	28.02	µs
P1	Frame start blanking	71	71	2.66	µs
P2	Frame end blanking	23	23	0.86	µs
Q	Horizontal blanking	94	94	3.52	µs
A + Q	Row time	846	846	31.72	µs
V	Vertical blanking	38,074	38,074	1.43	ms
Nrows	Frame valid time	406,080	406,080	15.23	ms
F	Total frame time	444,154	444,154	16.66	ms

Serial Bus Description

The MT9V022 control registers are written to and read from the two-wire serial interface bus. The MT9V022 is a serial interface slave with four possible IDs (0x90, 0x98, 0xB0, and 0xB8) determined by S_CTRL_ADR0 and S_CTRL_ADR1 inputs.

Data is transferred into the MT9V022 and out through the serial data (SDATA) line. The SDATA line is pulled up to VDD off-chip by a 1. 5kΩ resistor. Either the slave or master device can pull the SDATA line down. The serial interface protocol determines which device is allowed to pull the SDATA line down at any given time.

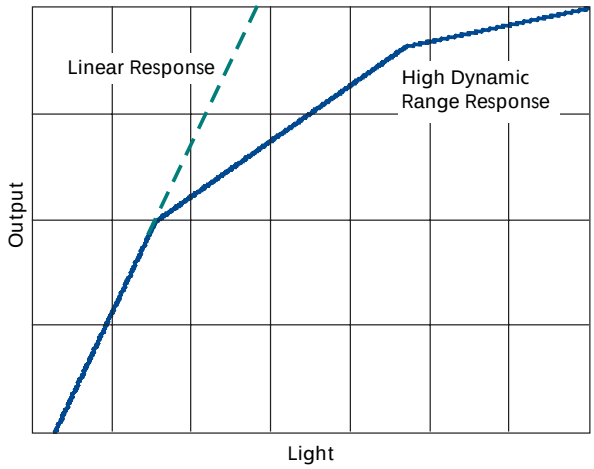
Register Lock

A register lock feature is included in the MT9V022 to help reduce the probability of an inadvertent, noise-triggered two-wire serial interface WRITE to the sensor. The user may lock all registers or only the read mode register. The read mode register controls the image orientation, and an unintended flip to the image can cause serious results.

High Dynamic Range

The MT9V022 pixel light response can be optionally configured to achieve intra-scene dynamic range as high as 100dB. High dynamic range is achieved by controlling the slopes of a three-segment, piecewise, linear pixel response, as illustrated in Figure 7. The slope of the three segments can be programmed via the serial interface.

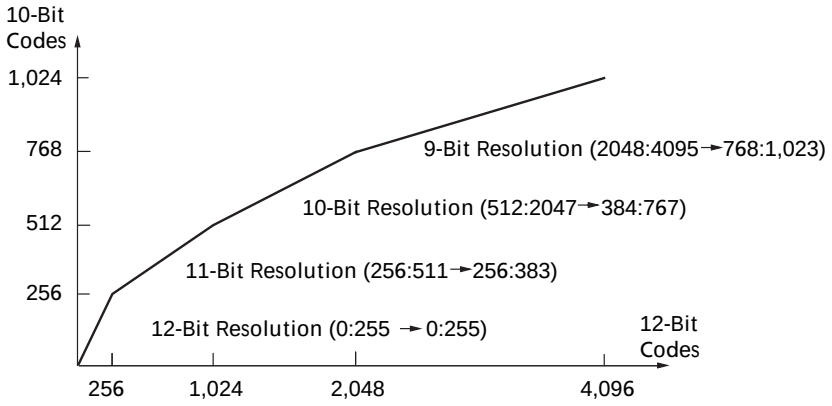
Figure 7: High Dynamic Range



Variable ADC Resolution

By default, the MT9V022 ADC has a linear response with 10-bit resolution. The ADC can also be configured to have a 12- to 10-bit companding response, as illustrated in Figure 7. This mode allows higher ADC resolution (12 bits) for low-level signals (shadow details) and lower ADC resolution (9 bits) for high-level signals (highlight details.)

Figure 8: 12- to 10-Bit ADC Companding Chart



Automatic Gain Control (AGC) and Automatic Exposure Control (AEC)

The integrated AEC/AGC unit is responsible for ensuring that optimal auto settings of exposure and (analog) gain are computed and updated every frame.

When the AGC or AEC are enabled, the MT9V022 measures current scene luminosity and desired output luminosity by accumulating a histogram of pixel values while reading out a frame. The desired exposure and gain are then calculated and applied for the subsequent frame.

Pixel Clock Speed

The pixel clock speed is same as the master clock of 26.66 MHz by default. However, when column binning 2 or 4 is enabled, the pixel clock speed will be reduced by half or one-fourth of the master clock speed, respectively.

Gain Settings

Analog Gain

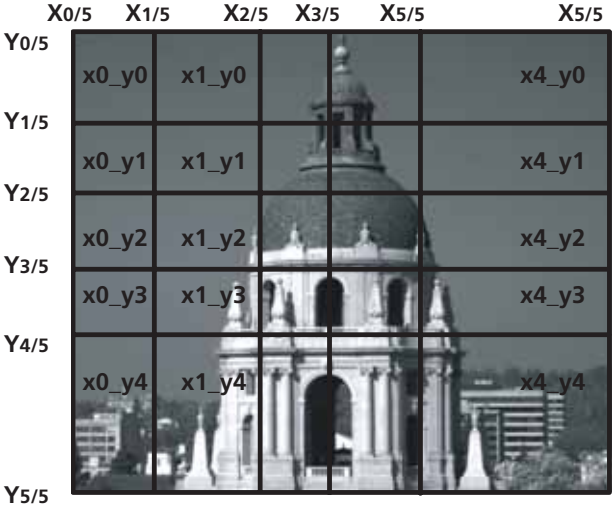
The analog gain range supported in the MT9V022 is 1X–4X with a step size of 6.25 percent.

Digital Gain

In the MT9V022, the user either may apply a single gain value for the entire array or they may divide the image into 25 tiles (Figure 9) through the two-wire serial interface and apply digital gain individually to each tile.

The coordinates and digital gain (0.25 - 3.75X) of each tile may be individually programmed via the two-wire serial interface. This feature should help improve pulling detail out of regions of an image that are either dark, or lighter than the rest of the scene without affecting the rest of the scene.

Figure 9: Digital Gain Tiled Sample



Read Mode Options

Column and Row Flip

To ease mounting orientation issues, the MT9V022 column and row readout order can be independently reversed via the two-wire serial interface. The image will then be represented correctly regardless of camera orientation.

Pixel Binning

In addition to windowing mode— in which smaller resolution (CIF, QCIF, user-selected size frame) is obtained by selecting a small window from the sensor array—the MT9V022 provides the ability to show the entire image captured by the pixel array with smaller resolution by pixel binning. Pixel binning is performed by combining signals from adjacent pixels by averaging. There are two options: binning 2 and binning 4.

When binning 2 is on, 4 pixel signals from 2 adjacent rows and columns are combined. In the case of binning 4 mode, 16 pixels are combined from 4 adjacent rows and columns. Binning may be used in conjunction with image flip. The binning operation increases SNR but decreases resolution. Enabling row bin2 and row bin4 improves frame rate by 2x and 4x, respectively. Column binning does not increase the frame rate.

Power Reduction Modes

Standby Control

The user may set the sensor in standby mode by setting STANDBY HIGH. Once the MT9V022 detects that STANDBY is asserted, it completes the current frame before disabling the digital logic, internal clocks, and analog power enable signal. To release the sensor out from the standby mode, reset STANDBY back to LOW.

Monitor Mode Control

In this mode, the MT9V022 first captures a programmable number of frames and then goes into a sleep period for five minutes. During the sleep period, all of the analog circuitry of the MT9V022 is powered-down and only a small portion of the digital circuitry remains powered.

Thermometer

The MT9V022 thermometer circuit provides a digital output vs. temperature that is accessible via the serial interface. The resolution of the thermometer is approximately 1 LSB per degree Celsius.

Electrical Specifications

Table 2: DC Electrical Characteristics

V_{PWR} = 3.3V ±0.3V; T_A = Ambient = 25°C

Symbol	Definition	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage		V_{PWR} -0.5	–	V_{PWR} +0.3	V
V_{IL}	Input low voltage		-0.3	–	0.8	V
I_{IN}	Input leakage current	No pull-up resistor; V_{IN} = V_{PWR} or V_{GND}	-15.0	–	15.0	µA
V_{OH}	Output high voltage	I_{OH} = -4.0mA	V_{PWR} -0.7	–	–	V
V_{OL}	Output low voltage	I_{OL} = 4.0mA	–	–	0.3	V
I_{OH}	Output high current	V_{OH} = V_{DD} - 0.7	-9.0	–	–	mA
I_{OL}	Output low current	V_{OL} = 0.7	–	–	9.0	mA
V_{AA}	Analog power supply	Default settings	3.0	3.3	3.6	V
I_{PWRA}	Analog supply current	Default settings	–	35.0	60.0	mA
V_{DD}	Digital power supply	Default settings	3.0	3.3	3.6	V
I_{PWRD}	Digital supply current	Default settings, C_{LOAD}= 10pF	—	35.0	60	mA
VAAPIX	Pixel array power supply	Default settings	3.0	3.3	3.6	V
I_{PIX}	Pixel supply current	Default settings	0.5	1.4	3.0	mA

Table 2: DC Electrical Characteristics (continued)
V_{PWR} = 3.3V ±0.3V; T_A = Ambient = 25°C

Symbol	Definition	Condition	Min	Typ	Max	Unit
V_{LVDS}	LVDS power supply	Default settings	3.0	3.3	3.6	V
I_{LVDS}	LVDS supply current	Default settings	11.0	13.0	15.0	mA
I_{PWRA} Standby	Analog standby supply current	STDBY = V_{DD}	2	3	4	µA
I_{PWRD} Standby Clock Off	Digital standby supply current with clock off	STDBY = V_{DD}, CLKIN = 0 MHz	1	2	4	µA
I_{PWRD} Standby Clock On	Digital standby supply current with clock on	STDBY= V_{DD}, CLKIN = 27 MHz	–	1.05	–	mA
LVDS Driver DC Specifications						
|V_{OD}|	Output differential voltage	R_{LOAD} = 100 Ω ±1%	250	–	400	mV
|DV_{OD}|	Change in V_{OD} between complementary output states		–	–	50	mV
V_{OS}	Output offset voltage		1.0	1.2	1.4	mV
DV_{OS}	Change in V_{OS} between complementary output states		–	–	35	mV
I_{OS}	Output current when driver shorted to ground			±10	±12	mA
I_{OZ}	Output current when driver is tri-state			±1	±10	µA
LVDS Receiver DC Specifications						
V_{IDTH+}	Input differential	| V_{GPD}| <925mV	-100	–	100	mV
Iin	Input current		–	–	±20	µA

Table 3: AC Electrical Characteristics
V_{PWR} = 3.3V ±0.3V; T_A = Ambient = 25°C; Output Load = 10pF

Symbol	Definition	Condition	Min	Typ	Max	Unit
	Clock duty cycle		45.0	50.0	55.0	%
^tR	Input clock rise time		1	2	5	ns
^tF	Input clock fall time		1	2	5	ns
$^tPLH_P$	SYSCLK to PIXCLK propagation delay	C_{LOAD} = 10pF	3	7	11	ns
^tPD	PIXCLK to valid D_{OUT}(9:0) propagation delay	C_{LOAD} = 10pF	-2	0	2	ns
^tSD	Data setup time		14	16	–	ns
^tHD	Data hold time		14	16	–	
^tPFLR	PIXCLK to LINE_VALID propagation delay	C_{LOAD} = 10pF	-2	0	2	ns
^tPFLF	PIXCLK to FRAME_VALID propagation delay	C_{LOAD} = 10pF	-2	0	2	ns

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{SUPPLY}	Power supply voltage (all supplies)	-0.3	4.5	V
I_{SUPPLY}	Total power supply current	–	200	mA
I_{GND}	Total ground current	–	200	mA
V_{IN}	DC input voltage	-0.3	V_{DDQ} + 0.3	V
V_{OUT}	DC output voltage	-0.3	V_{DDQ} + 0.3	V
T_{STG} Note:	Storage temperature	-40	+125	°C

Note: Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Figure 10: Propagation Delays for PIXCLK and Data Out Signals

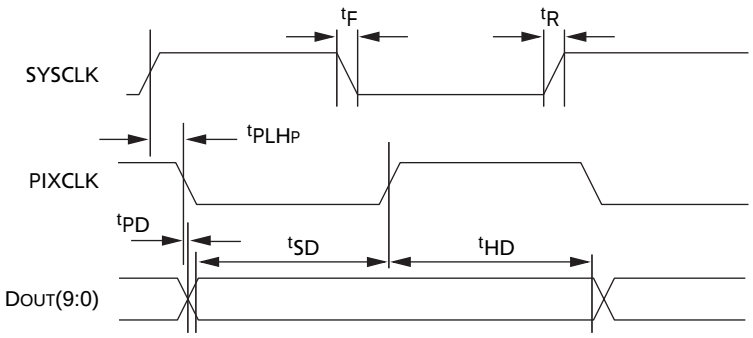


Figure 11: Propagation Delays for FRAME_VALID and LINE_VALID Signals

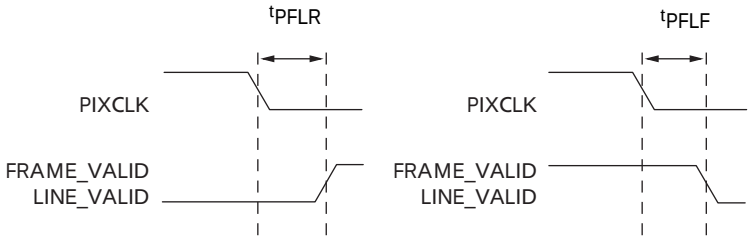


Figure 12: Quantum Efficiency – Color and Monochrome

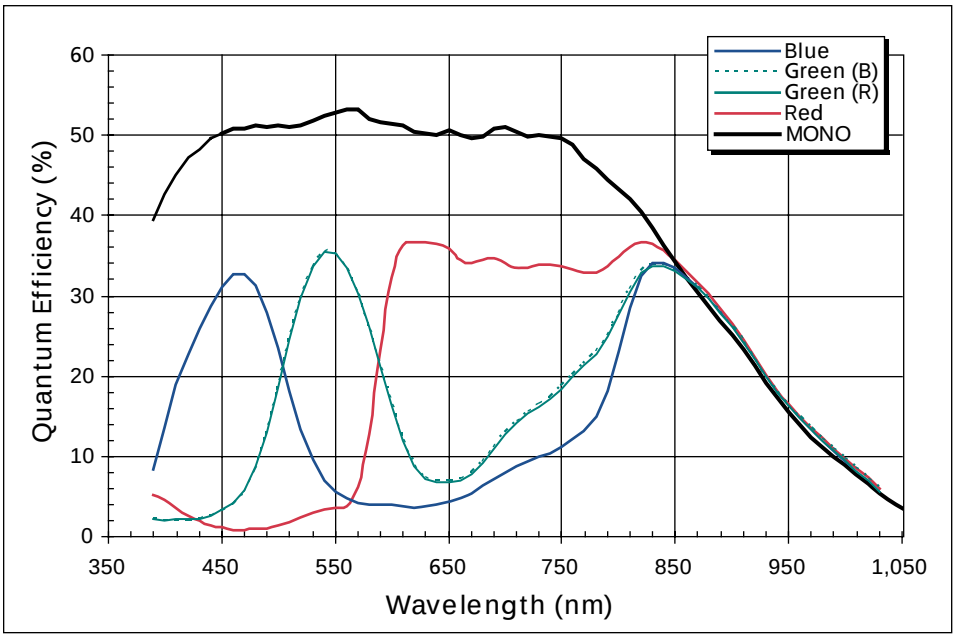
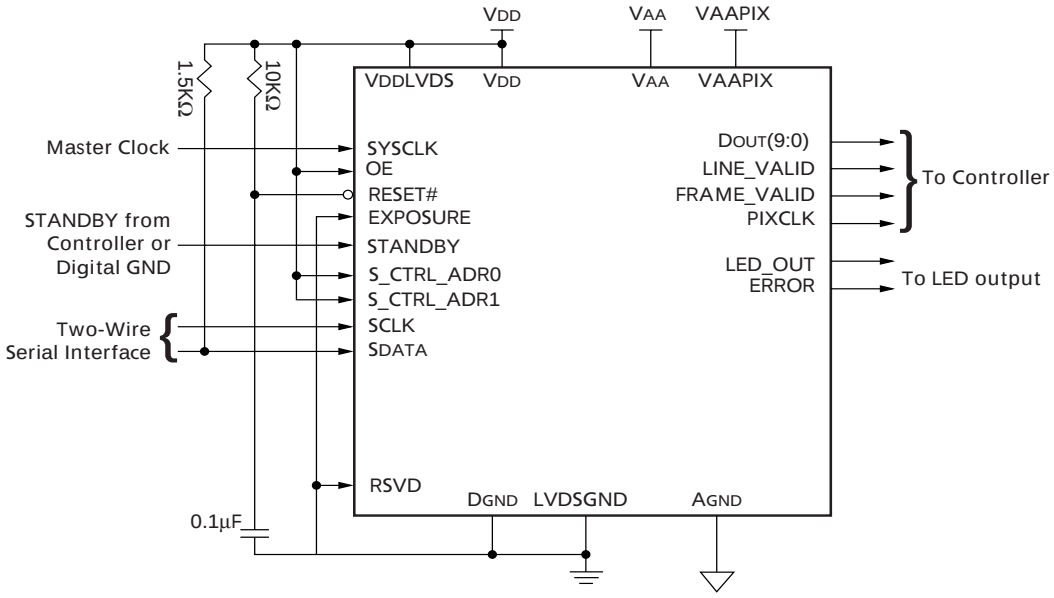
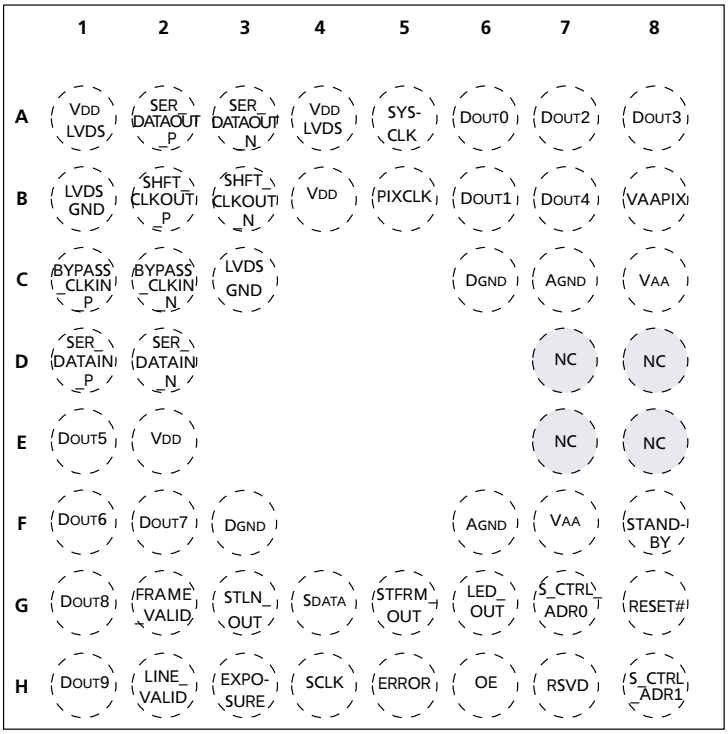


Figure 13: Typical Configuration (Connection) – Parallel Output Mode



Note: LVDS signals are to be left floating.

Figure 14: 52-Ball IBGA Package



Top View
(Ball Down)

Table 5: Ball Descriptions

Only pins DOUT0 through DOUT9 may be tri-stated.

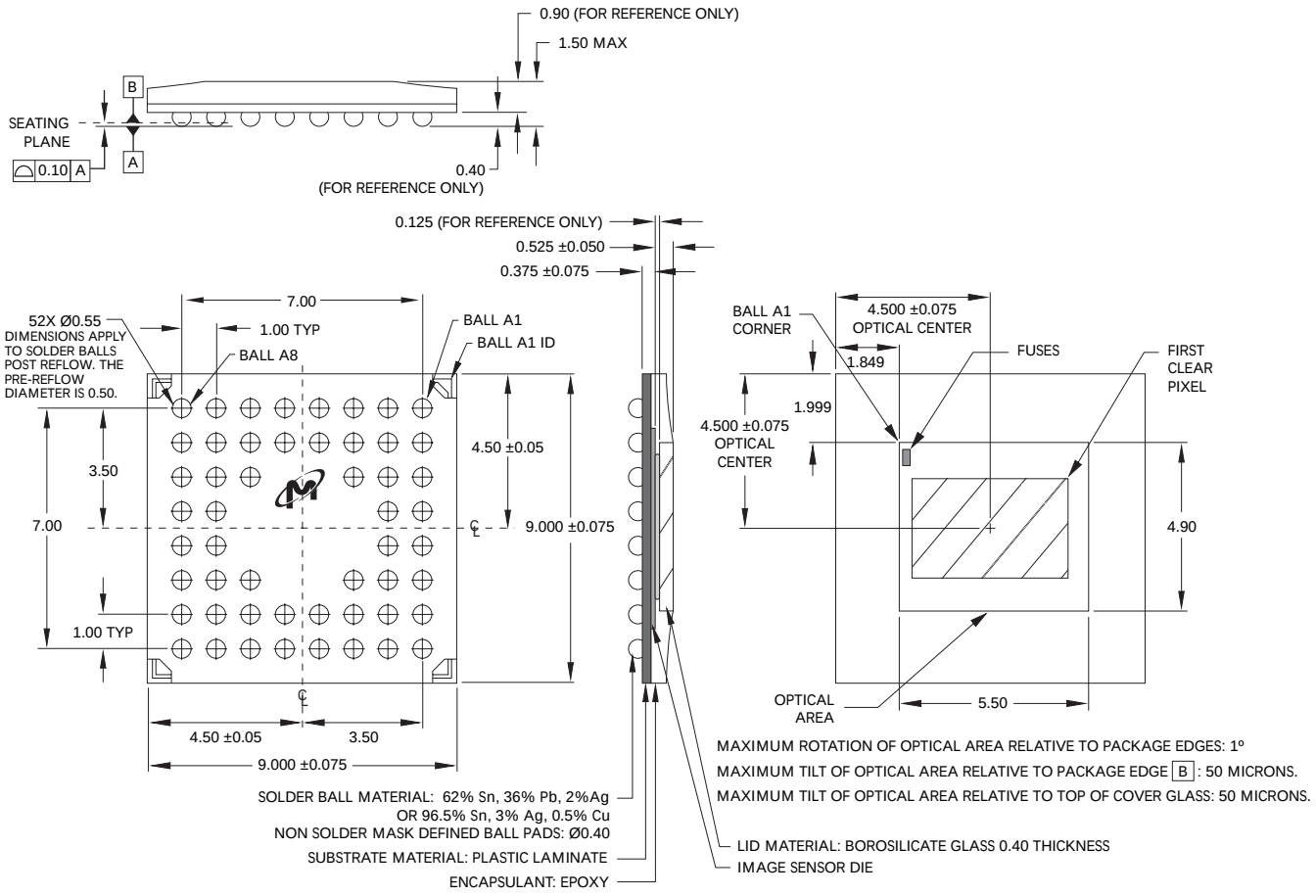
52-Ball IBGA Numbers	Symbol	Type	Description	Notes
H7	RSVD	Input	Connect to DGND.	1
D2	SER_DATAIN_N	Input	Serial data in for stereoscopy (differential negative). Tie to 1KΩ pull-up (to 3.3V) in non-stereoscopy mode.	
D1	SER_DATAIN_P	Input	Serial data in for stereoscopy (differential positive). Tie to DGND in non-stereoscopy mode.	
C2	BYPASS_CLKIN_N	Input	Input bypass shift-CLK (differential negative). Tie to 1KΩ pull-up (to 3.3V) in non-stereoscopy mode.	
C1	BYPASS_CLKIN_P	Input	Input bypass shift-CLK (differential positive). Tie to DGND in non-stereoscopy mode.	
H3	EXPOSURE	Input	Rising edge starts exposure in slave mode.	
H4	SCLK	Input	Two-wire serial interface clock. Connect to VDD with 1.5K resistor even when no other two-wire serial interface peripheral is attached.	
H6	OE	Input	DOUT enable pad, active HIGH.	2
G7	S_CTRL_ADR0	Input	Two-wire serial interface slave address bit 3.	
H8	S_CTRL_ADR1	Input	Two-wire serial interface slave address bit 5.	
G8	RESET#	Input	Asynchronous reset. All registers assume defaults.	
F8	STANDBY	Input	Shut down sensor operation for power saving.	

Table 5: Ball Descriptions (continued)
Only pins DOUT0 through DOUT9 may be tri-stated.

52-Ball IBGA Numbers	Symbol	Type	Description	Notes
A5	SYSCLK	Input	Master clock (26.6 MHz).	
G4	SDATA	I/O	Two-wire serial interface data. Connect to VDD with 1.5K resistor even when no other two-wire serial interface peripheral is attached.	
G3	STLN_OUT	I/O	Output in master mode—start line sync to drive slave chip in-phase; input in slave mode.	
G5	STFRM_OUT	I/O	Output in master mode—start frame sync to drive a slave chip in-phase; input in slave mode.	
H2	LINE_VALID	Output	Asserted when DOUT data is valid.	
G2	FRAME_VALID	Output	Asserted when DOUT data is valid.	
E1	DOUT5	Output	Parallel pixel data output 5.	
F1	DOUT6	Output	Parallel pixel data output 6.	
F2	DOUT7	Output	Parallel pixel data output 7.	
G1	DOUT8	Output	Parallel pixel data output 8	
H1	DOUT9	Output	Parallel pixel data output 9.	
H5	ERROR	Output	Error detected. Directly OR with STEREO ERROR FLAG and PIXEL ERROR FLAG.	
G6	LED_OUT	Output	LED strobe output.	
B7	DOUT4	Output	Parallel pixel data output 4.	
A8	DOUT3	Output	Parallel pixel data output 3.	
A7	DOUT2	Output	Parallel pixel data output 2.	
B6	DOUT1	Output	Parallel pixel data output 1.	
A6	DOUT0	Output	Parallel pixel data output 0.	
B5	PIXCLK	Output	Pixel clock out. DOUT is valid on rising edge of this clock.	
B3	SHFT_CLKOUT_N	Output	Output shift CLK (differential negative).	
B2	SHFT_CLKOUT_P	Output	Output shift CLK (differential positive).	
A3	SER_DATAOUT_N	Output	Serial data out (differential negative).	
A2	SER_DATAOUT_P	Output	Serial data out (differential positive).	
B4, E2	VDD	Supply	Digital power 3.3V.	
C8, F7	VAA	Supply	Analog power 3.3V.	
B8	VAAPIX	Supply	Pixel power 3.3V.	
A1, A4	VDDLVDS	Supply	Dedicated power for LVDS pads.	
B1, C3	LVDSGND	Ground	Dedicated GND for LVDS pads.	
C6, F3	DGND	Ground	Digital GND.	
C7, F6	AGND	Ground	Analog GND.	
E7, E8, D7, D8	NC	NC	No connect.	3

Notes: 1. Pin H7 (RSVD) must be tied to GND.
2. Output Enable (OE) tri-states signals DOUT0-DOUT9. No other signals are tri-stated with OE.
3. No connect. These pins must be left floating for proper operation.

Figure 15: 52-Ball IBGA Package Outline Drawing



Note: All dimensions in millimeters.

Ordering Information

Production Parts

MT9V022I77ATM	Monochrome Pb packaged parts
MT9V022IA7ATM	Monochrome Pb-Free packaged parts
MT9V022I77ATC	Color Pb packaged parts
MT9V022IA7ATC	Color Pb-Free packaged parts

Demo Kits

A demonstration kit is also available for evaluation purposes and consists of:

- Micron Imaging Demo2 Camera Board
- Micron Sensor Head with lens
- USB2.0 Cable
- Software CD
- Demo User Manual picture from Demo Kit

MT9V022I77ATMD ES	Monochrome Demo Kit
MT9V022I77ATCD ES	Color Demo Kit

Headboards

MT9V022I77ATMH ES	Monochrome Headboard
MT9V022I77ATCH ES	Color Headboard

Note: For customers who already have a demo kit with the demo 2 camera board (USB2.0), only order the head board.

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