

P-Channel Enhancement Mode Power MOSFET

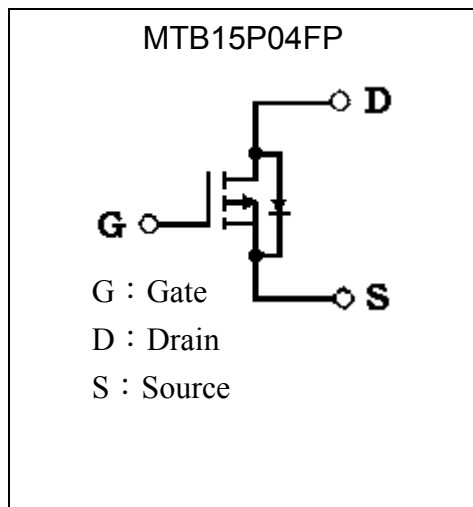
MTB15P04FP

BV_{DSS}	-40V
I_D	-56A
R_{DS(ON)}@ V_{GS}=-10V, I_D=-25A	9.7mΩ (typ)
R_{DS(ON)}@ V_{GS}=-4.5V, I_D=-15A	12.7mΩ (typ)

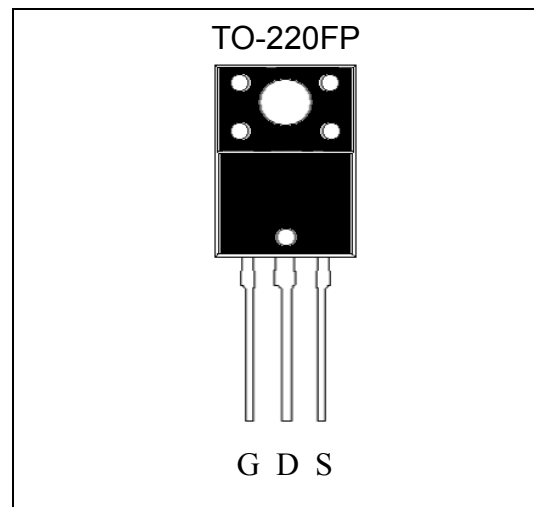
Features

- Single Drive Requirement
- Low On-resistance
- Fast switching Characteristic
- Pb-free lead plating package

Symbol

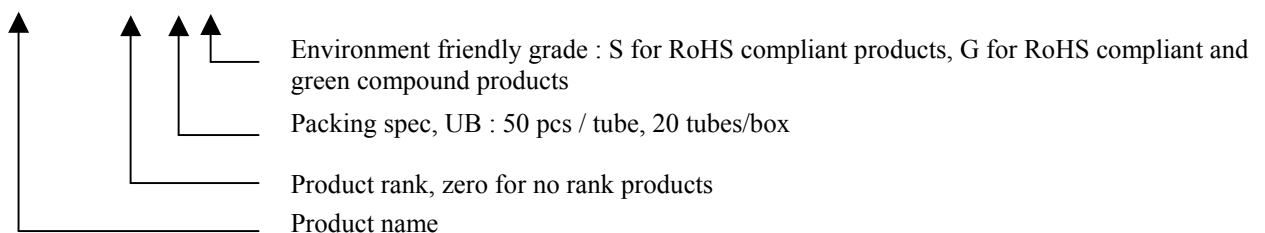


Outline



Ordering Information

Device	Package	Shipping
MTB15P04FP-0-UB-S	TO-220FP (Pb-free lead plating package)	50 pcs/tube, 20 tubes/box, 4 boxes / carton



**Absolute Maximum Ratings** ($T_a=25^{\circ}\text{C}$)

Parameter		Symbol	Limits	Unit
Drain-Source Voltage		V_{DS}	-40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current @ $V_{GS}=-10\text{V}$, $T_C=25^{\circ}\text{C}$ (Package limited)		I_D	-56	A
Continuous Drain Current @ $V_{GS}=-10\text{V}$, $T_C=25^{\circ}\text{C}$ (Silicon limited)			-62.5	
Continuous Drain Current @ $V_{GS}=-10\text{V}$, $T_C=100^{\circ}\text{C}$			-39.5	
Continuous Drain Current @ $V_{GS}=-10\text{V}$, $T_A=25^{\circ}\text{C}$ (Note 2)		I_{DSM}	-10	
Continuous Drain Current @ $V_{GS}=-10\text{V}$, $T_A=70^{\circ}\text{C}$ (Note 2)			-8	
Pulsed Drain Current (Note 4)		I_{DM}	-250	
Power Dissipation	$T_C=25^{\circ}\text{C}$ (Note 1)	P_D	78	W
	$T_C=100^{\circ}\text{C}$ (Note 1)		31.2	
	$T_A=25^{\circ}\text{C}$ (Note 2)	P_{DSM}	2	
	$T_A=70^{\circ}\text{C}$ (Note 2)		1.3	
Single Pulse Avalanche Energy @ $L=1\text{mH}$, $I_{AS}=-20\text{A}$ (Note 3)		E_{AS}	200	mJ
Single Pulse Avalanche Current (Note 3)		I_{AS}	-20	A
Operating Junction and Storage Temperature		T_j, T_{stg}	-55~+150	$^{\circ}\text{C}$

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{th,j-c}$	1.6	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-ambient, max, $t \leq 10\text{s}$ (Note 1)	$R_{th,j-a}$	15	
Thermal Resistance, Junction-to-ambient, max (Note 1)		62.5	

- Note : 1. The power dissipation P_D is based on $T_{J(MAX)}=150^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
2. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2 oz. copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design.
3. Pulse width limited by junction temperature $T_{J(MAX)}=150^{\circ}\text{C}$.
4. Pulse width $\leq 300\mu\text{s}$ pulses and duty cycle $\leq 0.5\%$.
5. The $R_{\theta JA}$ is the sum of thermal resistance from junction to case $R_{\theta JC}$ and case to ambient.



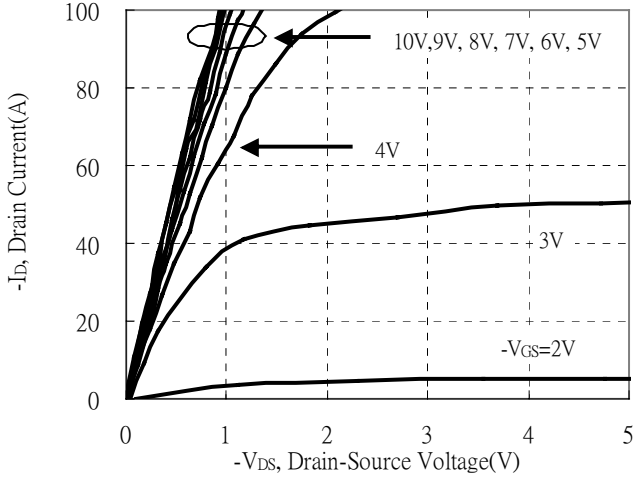
Characteristics (Tj=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	-40	-	-	V	V _{GS} =0V, I _D =-250μA
V _{GS(th)}	-1.0	-	-2.5	V	V _{DS} = V _{GS} , I _D =-250μA
G _{FS}	-	42	-	S	V _{DS} = -5V, I _D =-25A
I _{GSS}	-	-	±100	nA	V _{GS} =±20V
I _{DSS}	-	-	-1	μA	V _{DS} = -32V, V _{GS} = 0V
I _{DSS}	-	-	-25		V _{DS} = -32V, V _{GS} = 0V, Tj=70°C
*R _{DS(ON)}	-	9.7	13	mΩ	V _{GS} = -10V, I _D =-25A
*R _{DS(ON)}	-	12.7	18		V _{GS} = -4.5V, I _D =-15A
Dynamic					
*Q _g	-	40	-	nC	I _D =-25A, V _{DS} =-20V, V _{GS} =-10V
*Q _{gs}	-	13	-		
*Q _{gd}	-	16	-		
*t _{d(ON)}	-	24	-	ns	V _{DS} =-20V, V _{GS} =-10V, R _G =6Ω, I _D =-25A
*t _r	-	15	-		
*t _{d(OFF)}	-	120	-		
*t _f	-	40	-		
C _{iss}	-	3987	-	pF	V _{GS} =0V, V _{DS} =-20V, f=1MHz
C _{oss}	-	325	-		
C _{rss}	-	263	-		
Source-Drain Diode					
*I _S	-	-	-56	A	
*V _{SD}	-	-0.9	-1.2	V	I _S =-25A, V _{GS} =0V
*t _{rr}	-	36	-	ns	I _F =-25A, V _{GS} =0V, dI _F /dt=100A/μs
*Q _{rr}	-	32	-	nC	

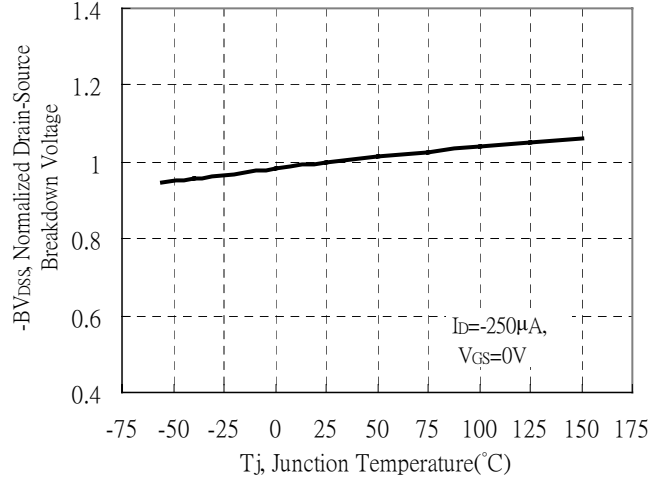
*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Typical Characteristics

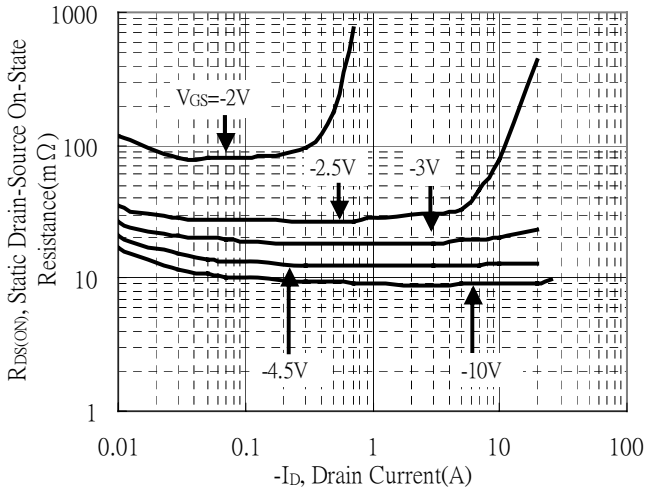
Typical Output Characteristics



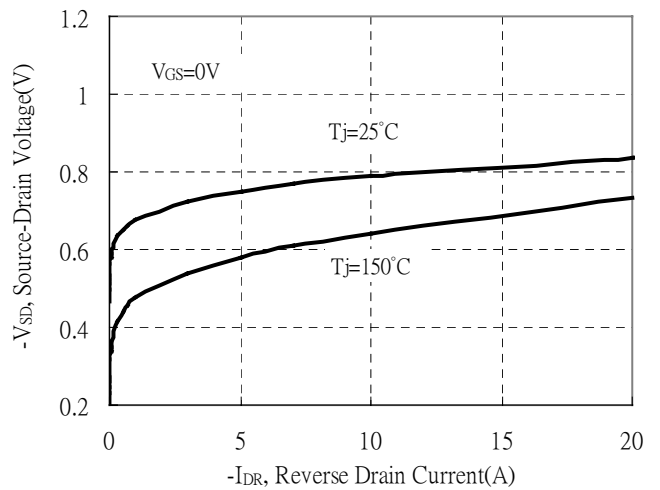
Breakdown Voltage vs Ambient Temperature



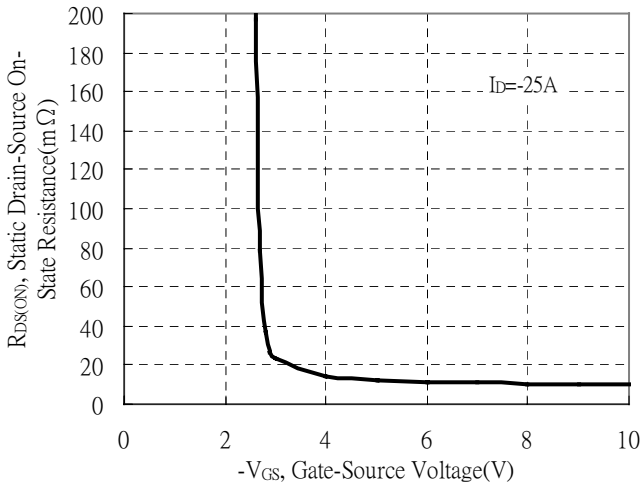
Static Drain-Source On-State resistance vs Drain Current



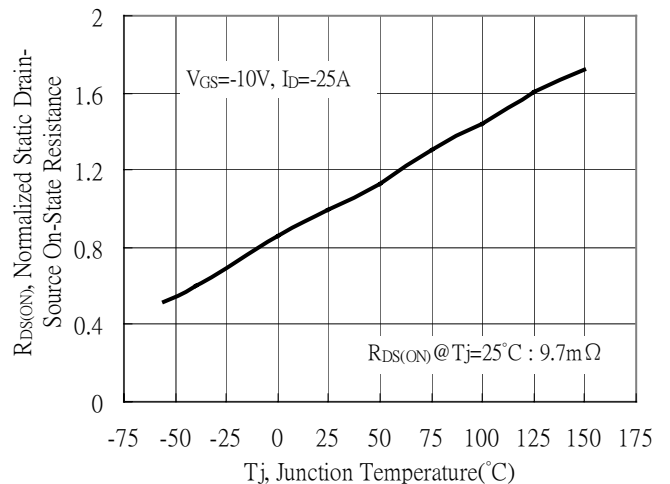
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

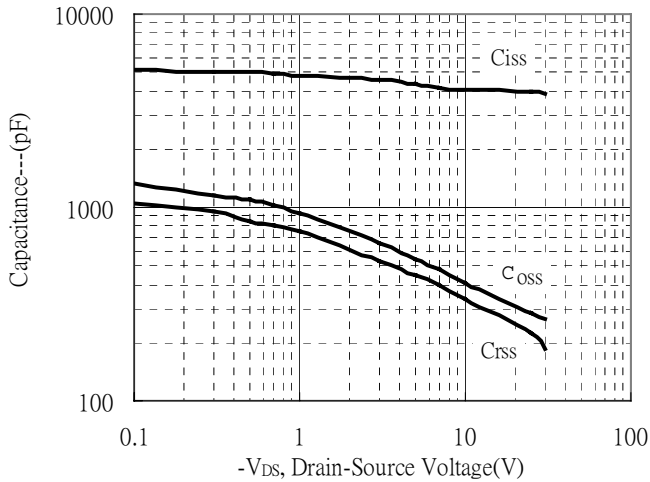


Drain-Source On-State Resistance vs Junction Temperature

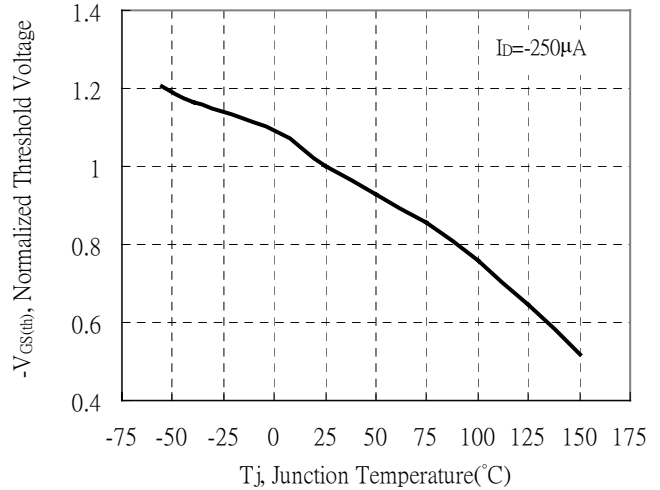


Typical Characteristics(Cont.)

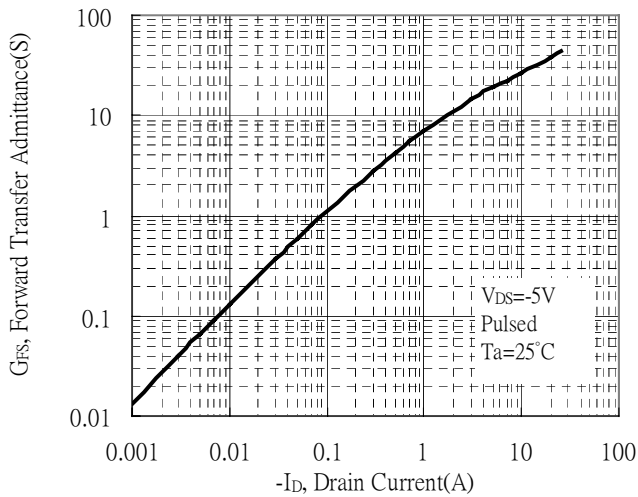
Capacitance vs Drain-to-Source Voltage



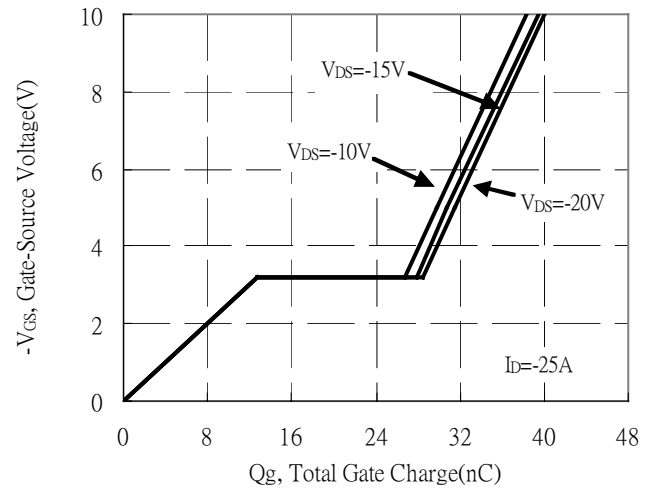
Threshold Voltage vs Junction Temperature



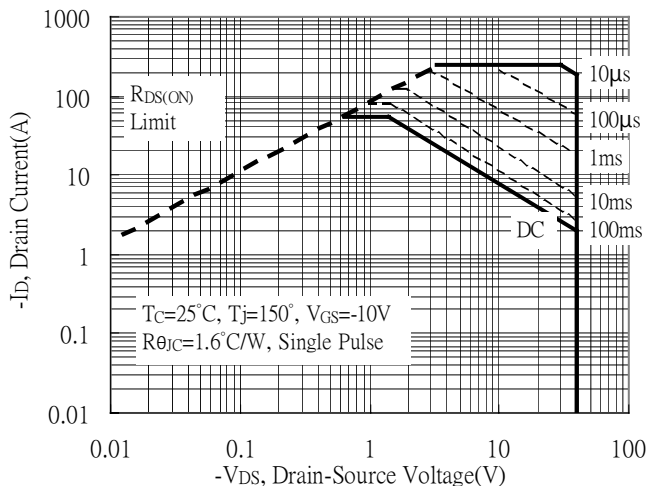
Forward Transfer Admittance vs Drain Current



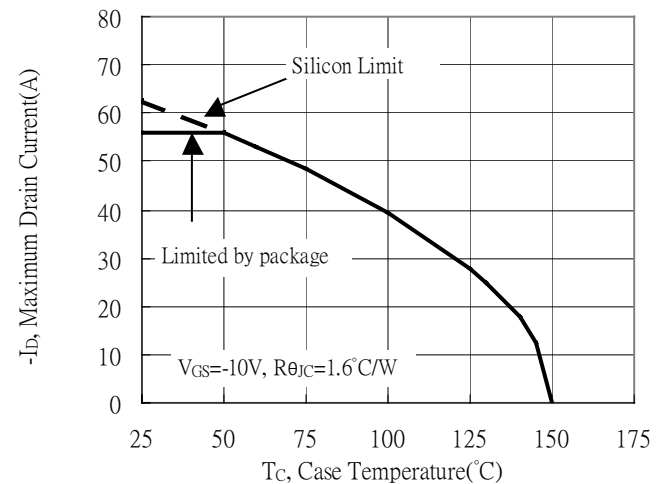
Gate Charge Characteristics



Maximum Safe Operating Area



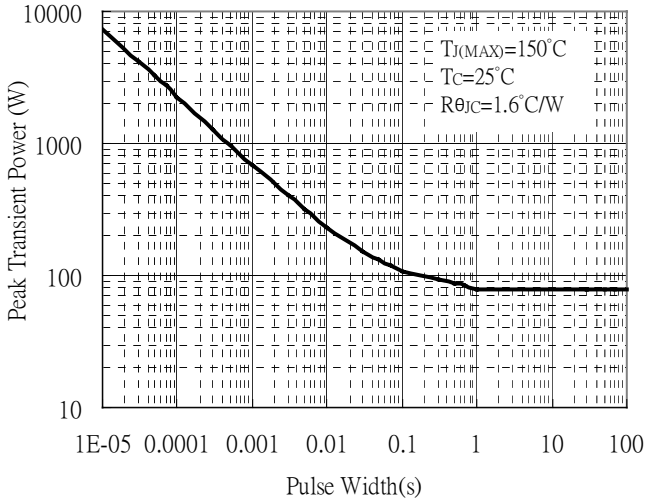
Maximum Drain Current vs Case Temperature



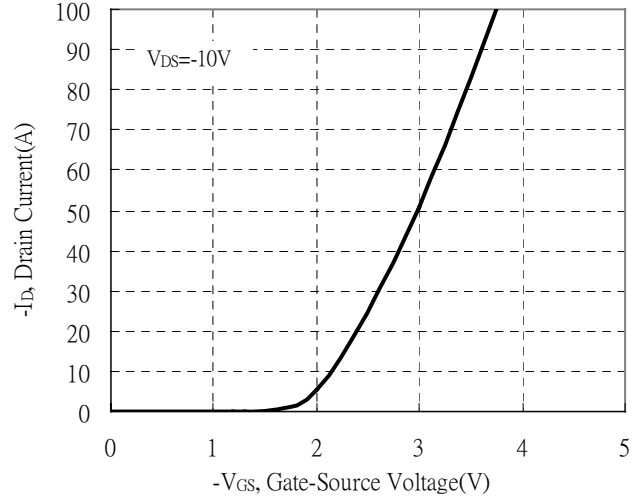


Typical Characteristics(Cont.)

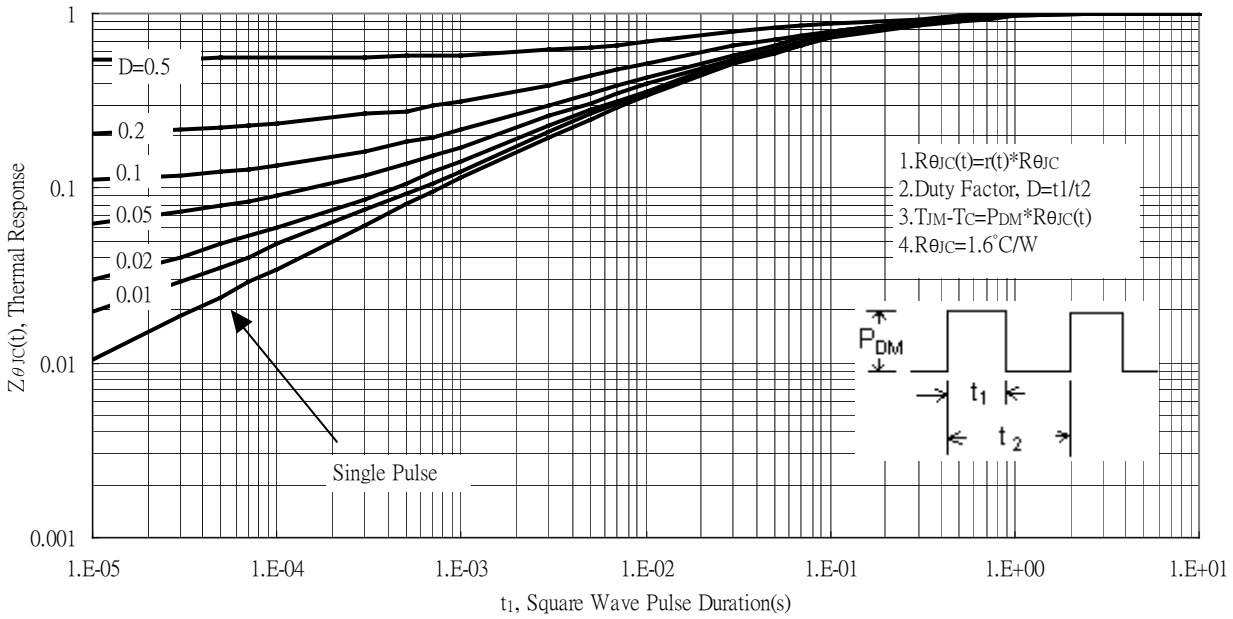
Single Pulse Maximum Power Dissipation



Typical Transfer Characteristics



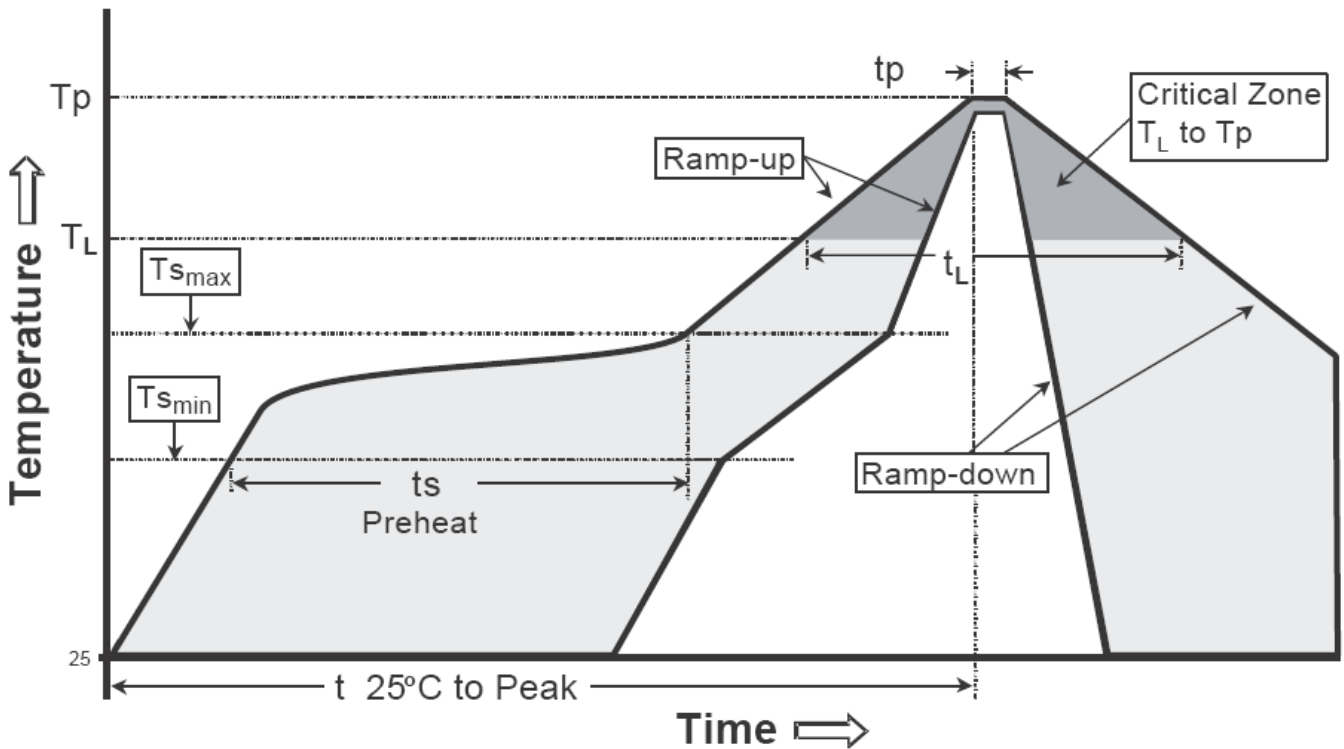
Transient Thermal Response Curves



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

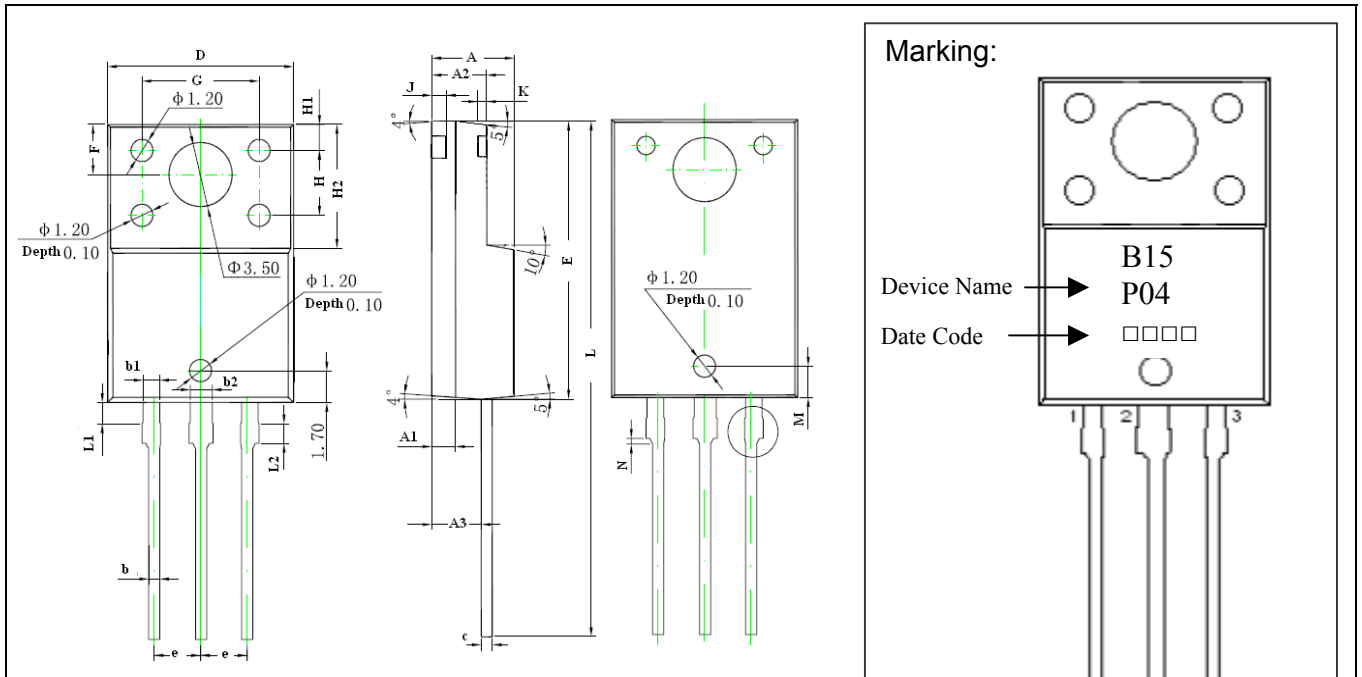
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-220FP Dimension



3-Lead TO-220FP Plastic Package
 CYStek Package Code: FP

Marking:

Device Name → B15
 P04
 Date Code → □□□□

Style: Pin 1.Gate 2.Drain 3.Source

*Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.171	0.183	4.35	4.65	G	0.246	0.258	6.25	6.55
A1	0.051 REF		1.300 REF		H	0.138 REF		3.50 REF	
A2	0.112	0.124	2.85	3.15	H1	0.055 REF		1.40 REF	
A3	0.102	0.110	2.60	2.80	H2	0.256	0.272	6.50	6.90
b	0.020	0.030	0.50	0.75	J	0.031 REF		0.80 REF	
b1	0.031	0.041	0.80	1.05	K	0.020		0.50 REF	
b2	0.047 REF		1.20 REF		L	1.102	1.118	28.00	28.40
c	0.020	0.030	0.500	0.750	L1	0.043	0.051	1.10	1.30
D	0.396	0.404	10.06	10.26	L2	0.036	0.043	0.92	1.08
E	0.583	0.598	14.80	15.20	M	0.067 REF		1.70 REF	
e	0.100 *		2.54*		N	0.012 REF		0.30 REF	
F	0.106 REF		2.70 REF						

- Notes:**
- Controlling dimension: millimeters.
 - Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 - If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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