

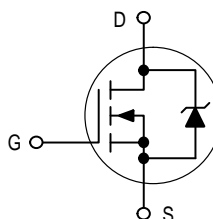
Product Preview

TMOS E-FET™
High Energy Power FET

D2PAK for Surface Mount
N-Channel Enhancement-Mode Silicon Gate

This advanced high voltage TMOS E-FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain-to-source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Low Stored Gate Charge for Efficient Switching
- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
- Source-to-Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode



MTB3N60E
Motorola Preferred Device

TMOS POWER FET
3.0 AMPERES
600 VOLTS
RDS(on) = 2.2 OHMS

CASE 418B-03, Style 2
D2PAK

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	600	Vdc
Drain-Gate Voltage ($R_{GS} = 1.0\text{ M}\Omega$)	V_{DGR}	600	Vdc
Gate-Source Voltage — Continuous — Non-repetitive	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Pulsed	I_D I_D I_{DM}	3.0 2.4 14	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (1)	P_D	75 0.6 2.5	Watts W/ $^\circ\text{C}$ Watts
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

UNCLAMPED DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS ($T_J < 150^\circ\text{C}$)

Single Pulse Drain-to-Source Avalanche Energy — $T_J = 25^\circ\text{C}$ — $T_J = 100^\circ\text{C}$	$W_{DSR}^{(2)}$	290 46	mJ
Repetitive Pulse Drain-to-Source Avalanche Energy	$W_{DSR}^{(3)}$	7.5	

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient(1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.67 62.5 50	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

(1) When surface mounted to an FR-4 board using the minimum recommended pad size

(2) $V_{DD} = 50\text{ V}$, $I_D = 3.0\text{ A}$

(3) Pulse Width and frequency is limited by $T_J(\text{max})$ and thermal response

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Preferred devices are Motorola recommended choices for future use and best overall value

MTB3N60E

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-to-Source Breakdown Voltage (V _{GS} = 0, I _D = 250 μAdc)	V _{(BR)DSS}	600	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 600 V, V _{GS} = 0) (V _{DS} = 480 V, V _{GS} = 0, T _J = 125°C)	I _{DSS}	—	—	10 100	μAdc
Gate-Body Leakage Current — Forward (V _{GSF} = 20 Vdc, V _{DS} = 0)	I _{GSSF}	—	—	100	nAdc
Gate-Body Leakage Current — Reverse (V _{GSR} = 20 Vdc, V _{DS} = 0)	I _{GSSR}	—	—	100	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250 μAdc) (T _J = 125°C)	V _{GS(th)}	2.0 1.5	—	4.0 3.5	Vdc
Static Drain-to-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 1.5 A)	R _{DS(on)}	—	2.1	2.2	Ohms
Drain-to-Source On-Voltage (V _{GS} = 10 Vdc) (I _D = 3.0 A) (I _D = 1.5 A, T _J = 100°C)	V _{DS(on)}	—	—	9.0 7.5	Vdc
Forward Transconductance (V _{DS} = 15 Vdc, I _D = 1.5 A)	g _{FS}	1.5	—	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0, f = 1.0 MHz)	C _{iss}	—	770	—	pF
Output Capacitance		C _{oss}	—	105	—	
Transfer Capacitance		C _{rss}	—	19	—	

SWITCHING CHARACTERISTICS*

Turn-On Delay Time	(V _{DD} = 300 V, I _D ≈ 3.0 A, R _L = 100 Ω, R _G = 12 Ω, V _{GS(on)} = 10 V)	t _{d(on)}	—	23	—	ns
Rise Time		t _r	—	34	—	
Turn-Off Delay Time		t _{d(off)}	—	58	—	
Fall Time		t _f	—	35	—	
Total Gate Charge	(V _{DS} = 420 V, I _D = 3.0 A, V _{GS} = 10 V)	Q _g	—	28	31	nC
Gate-Source Charge		Q _{gs}	—	5.0	—	
Gate-Drain Charge		Q _{gd}	—	17	—	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I _S = 3.0 A, di/dt = 100 A/μs)	V _{SD}	—	—	1.4	Vdc
Forward Turn-On Time		t _{on}	—	**	—	ns
Reverse Recovery Time		t _{rr}	—	400	—	

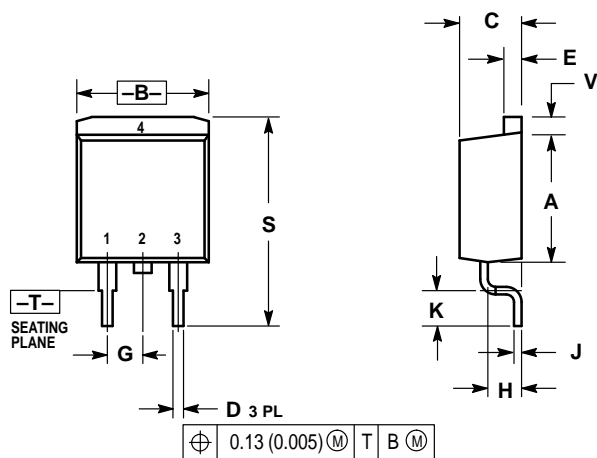
INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L _d	—	—	3.5 4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L _s	—	—	7.5	—	

* Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

** Limited by circuit inductance.

PACKAGE DIMENSIONS




- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 2:
 PIN 1. GATE
 2. DRAIN
 3. SOURCE
 4. DRAIN

CASE 418B-03
 ISSUE C

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How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 1-303-675-2140 or 1-800-441-2447

JAPAN: Nippon Motorola Ltd.: SPD, Strategic Planning Office, 4-32-1,
Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan. 81-3-5487-8488

Customer Focus Center: 1-800-521-6274

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 1-602-244-6609
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ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

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