

N -Channel Logic Level Enhancement Mode Power MOSFET

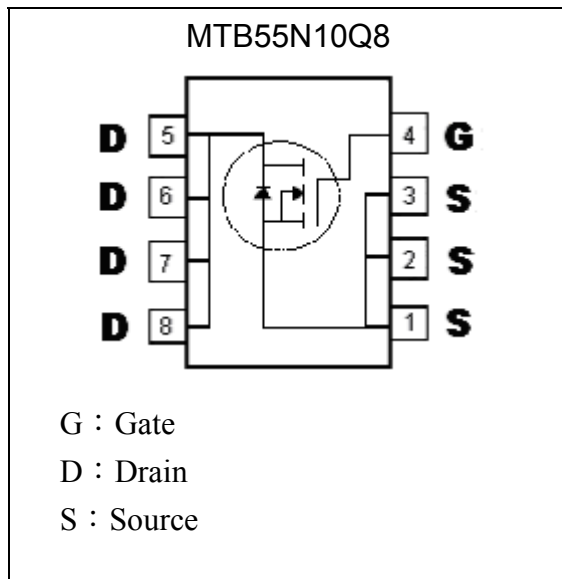
MTB55N10Q8

BV_{DSS}	100V	
$I_D@V_{GS}=10V, T_A=25^\circ C$	4.5A	
$R_{DS(on)(TYP)}$	$V_{GS}=10V, I_D=4.5A$	55mΩ
	$V_{GS}=4.5V, I_D=3A$	58mΩ

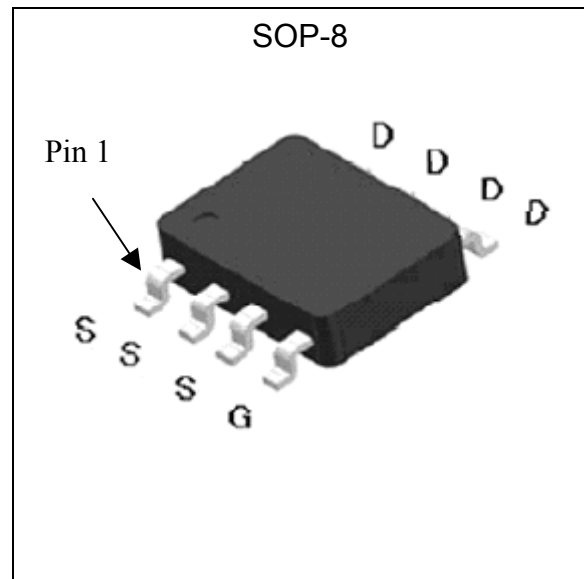
Features

- Low Gate Charge
- Simple Drive Requirement
- Pb-free lead plating package

Symbol

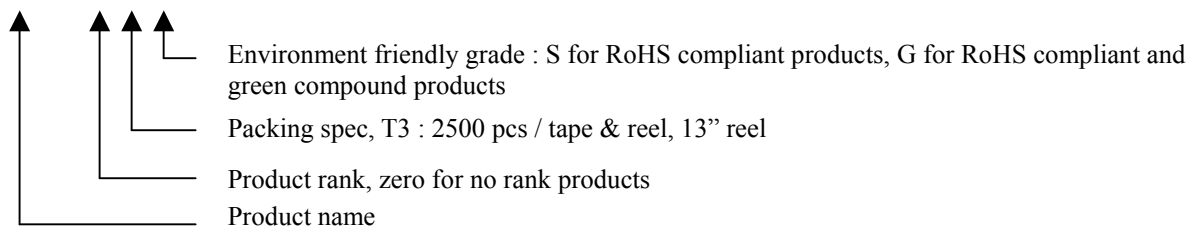


Outline



Ordering Information

Device	Package	Shipping
MTB55N10Q8-0-T3-G	SOP-8 (Pb-free lead plating and halogen-free package)	2500 pcs / tape & reel





Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit	
Drain-Source Voltage	V _{DS}	100	V	
Gate-Source Voltage	V _{GS}	±20		
Continuous Drain Current @V _{GS} =10V, T _A =25°C	I _D	4.5	A	
Continuous Drain Current @V _{GS} =10V, T _A =70°C		3.6		
Pulsed Drain Current	I _{DM}	32 *1		
Avalanche Current	I _{AS}	4.5		
Avalanche Energy @ L=10mH, I _D =4.5A, V _{GS} =20V, V _{DD} =25V	E _{AS}	101	mJ	
Repetitive Avalanche Energy @ L=0.05mH	E _{AR}	0.5 *2		
Total Power Dissipation *3	P _D	T _A =25°C	3.1	W
		T _A =70°C	2	
Operating Junction and Storage Temperature Range	T _j , T _{stg}	-55~+150	°C	

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	R _{th,j-c}	20	°C/W
Thermal Resistance, Junction-to-ambient, max	R _{th,j-a}	40 *3	

- Note : 1. Pulse width limited by maximum junction temperature.
 2. Duty cycle ≤ 1%.
 3. Surface mounted on 1 in² copper pad of FR-4 board, t ≤ 10s ; 125°C/W when mounted on minimum copper pad.
 The value in any given application depends on the user's specific board design.

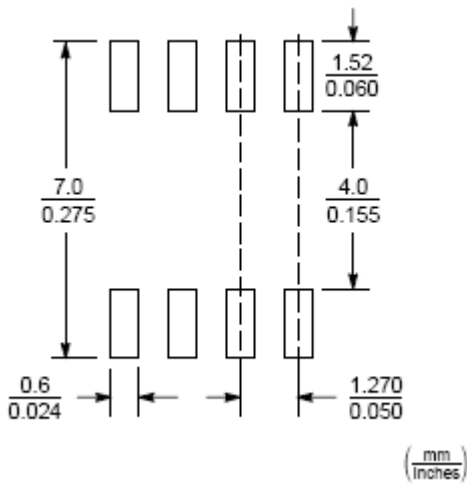
Characteristics (Tc=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	100	-	-	V	V _{GS} =0V, I _D =250μA
V _{GS(th)}	1	1.4	2.5		V _{DS} =V _{GS} , I _D =250μA
I _{GS}	-	-	±100	nA	V _{GS} =±20V, V _{DS} =0V
I _{DSS}	-	-	1	μA	V _{DS} =80V, V _{GS} =0V
	-	-	25		V _{DS} =80V, V _{GS} =0V, T _J =125°C
R _{DS(ON)} *1	-	55	75	mΩ	V _{GS} =10V, I _D =4.5A
	-	58	80		V _{GS} =4.5V, I _D =3A
G _{FS} *1	-	15	-	S	V _{DS} =5V, I _D =3A
Dynamic					
Q _g *1, 2	-	16	21	nC	I _D =4.5A, V _{DS} =80V, V _{GS} =10V
Q _{gs} *1, 2	-	1.9	2.5		
Q _{gd} *1, 2	-	6.7	9		
t _{d(ON)} *1, 2	-	7	15	ns	V _{DS} =50V, I _D =4.5A, V _{GS} =10V, R _G =6Ω
t _r *1, 2	-	4	10		
t _{d(OFF)} *1, 2	-	20	40		
t _f *1, 2	-	11	25		

Ciss	-	662	860	pF	V _{GS} =0V, V _{DS} =25V, f=1MHz
Coss	-	71	93		
Crss	-	32	42		
Rg	-	3.5	-	Ω	f=1MHz
Source-Drain Diode					
I _S *1	-	-	3.5	A	
I _{SM} *3	-	-	14		
V _{SD} *1	-	0.72	1	V	I _S =1A, V _{GS} =0V
trr	-	30	-	ns	I _F =3A, dI _F /dt=100A/μs
Qrr	-	90	-	nC	

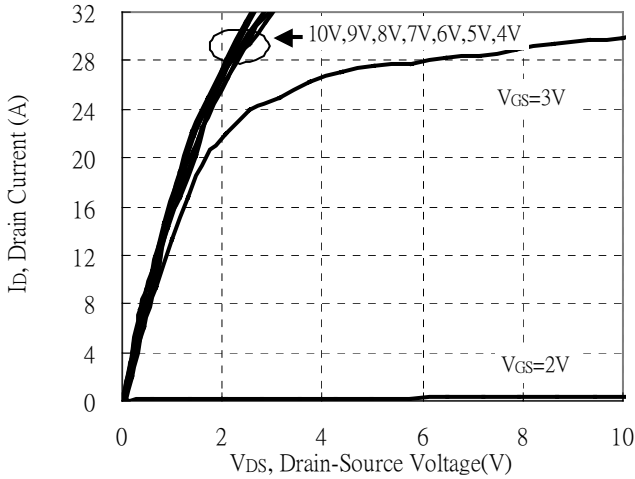
Note : *1.Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%
 *2.Independent of operating temperature
 *3.Pulse width limited by maximum junction temperature.

Recommended Soldering Footprint

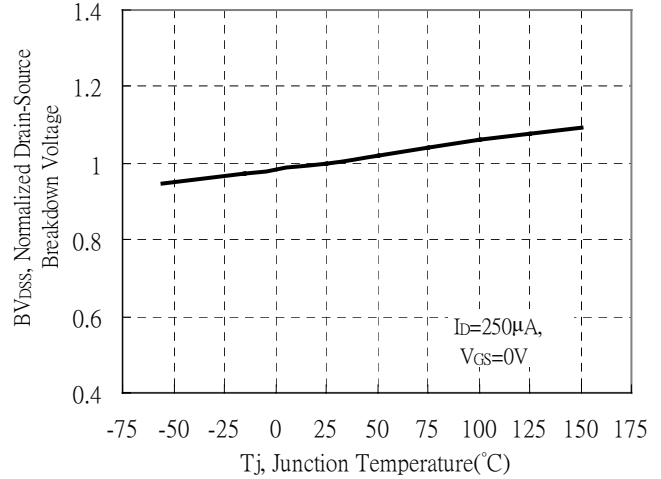


Typical Characteristics

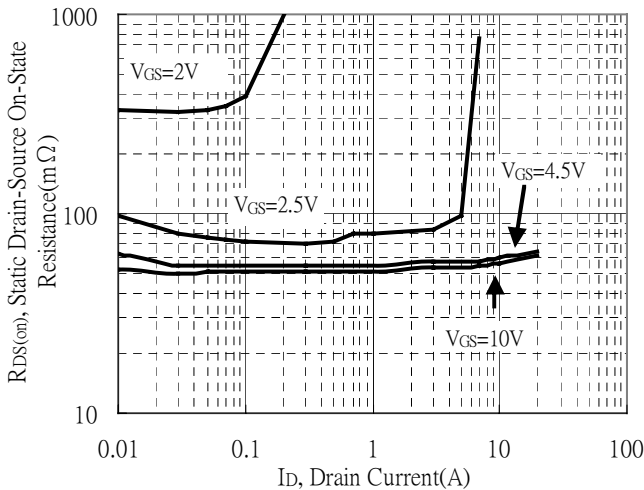
Typical Output Characteristics



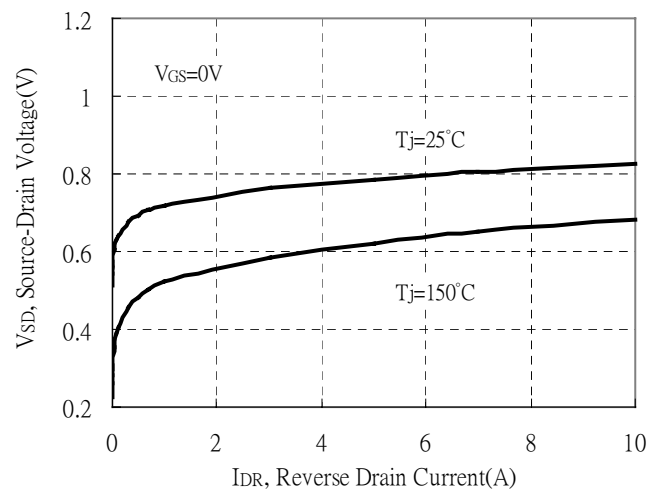
Brekdown Voltage vs Ambient Temperature



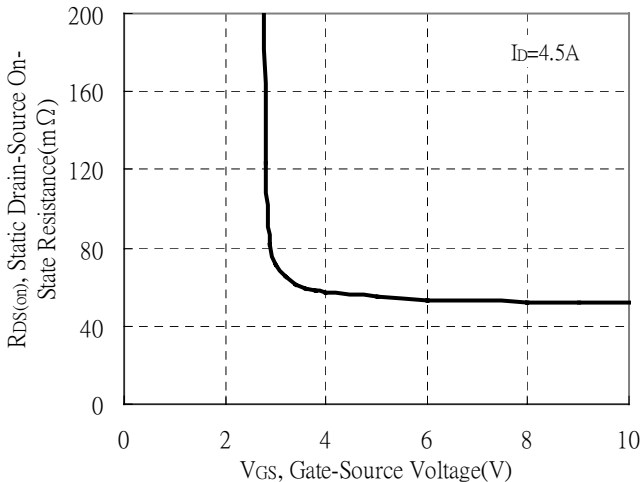
Static Drain-Source On-State resistance vs Drain Current



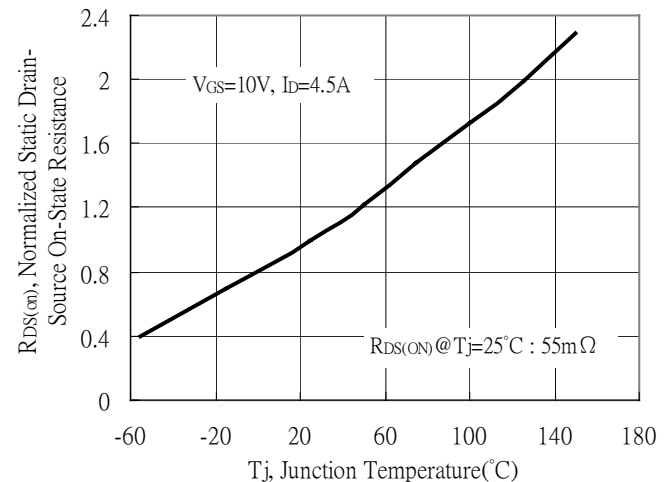
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage



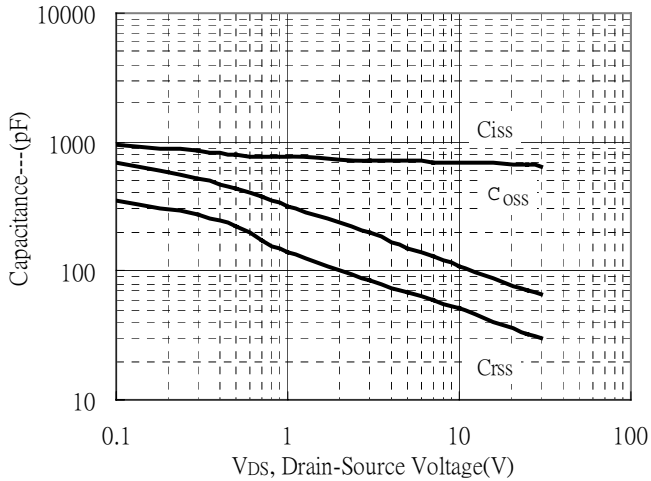
Drain-Source On-State Resistance vs Junction Temperature



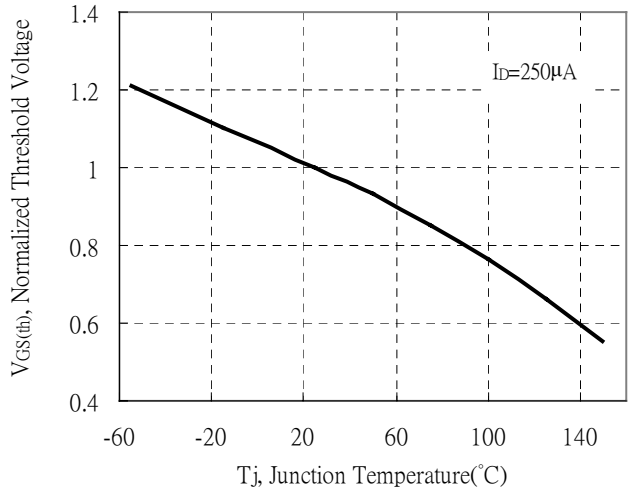


Typical Characteristics(Cont.)

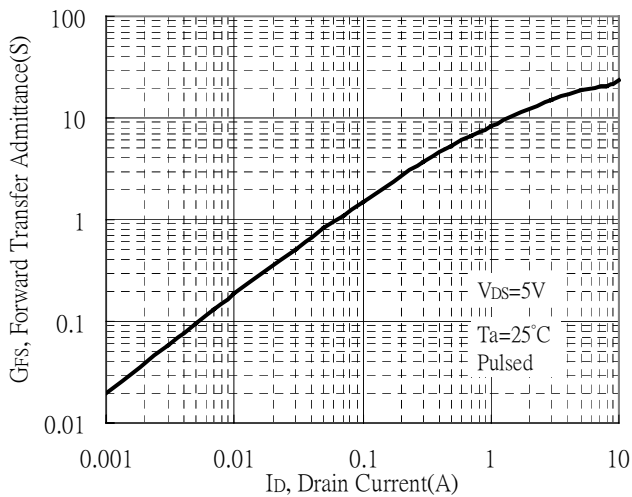
Capacitance vs Drain-to-Source Voltage



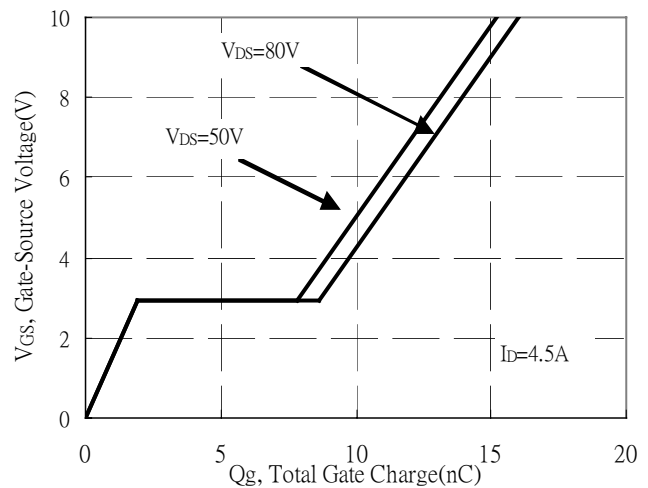
Threshold Voltage vs Junction Temperature



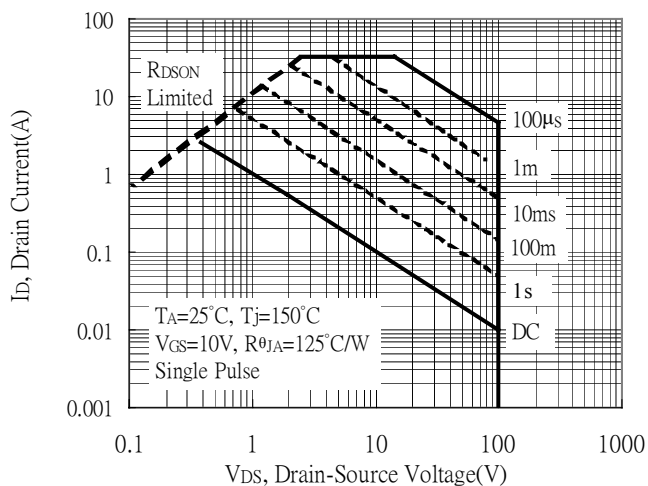
Forward Transfer Admittance vs Drain Current



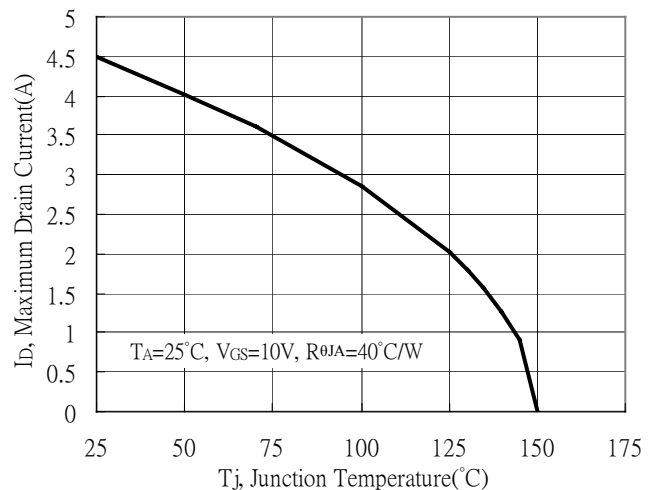
Gate Charge Characteristics



Maximum Safe Operating Area

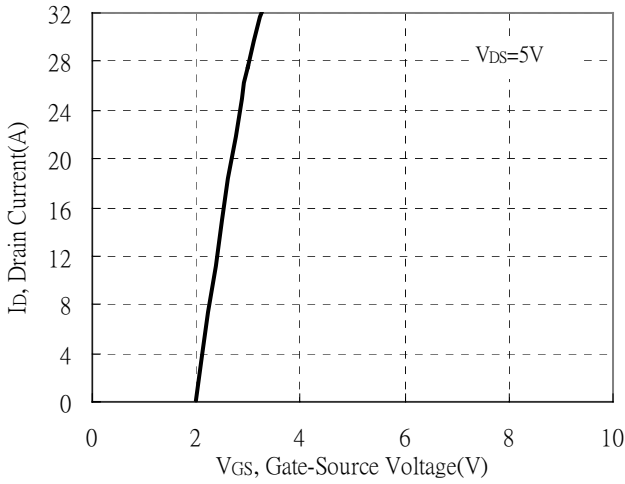


Maximum Drain Current vs Junction Temperature

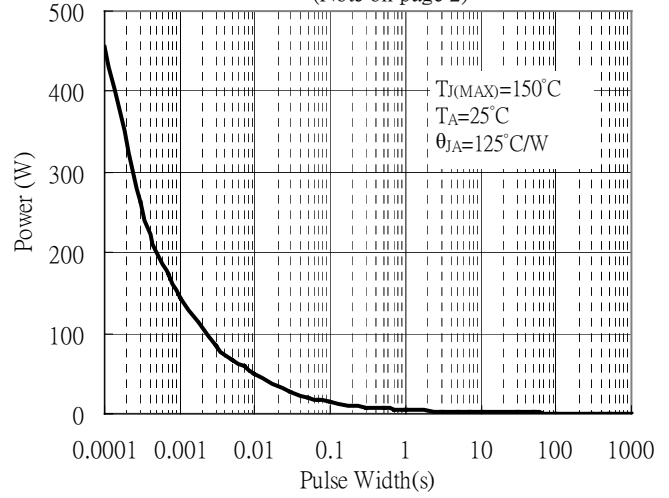


Typical Characteristics(Cont.)

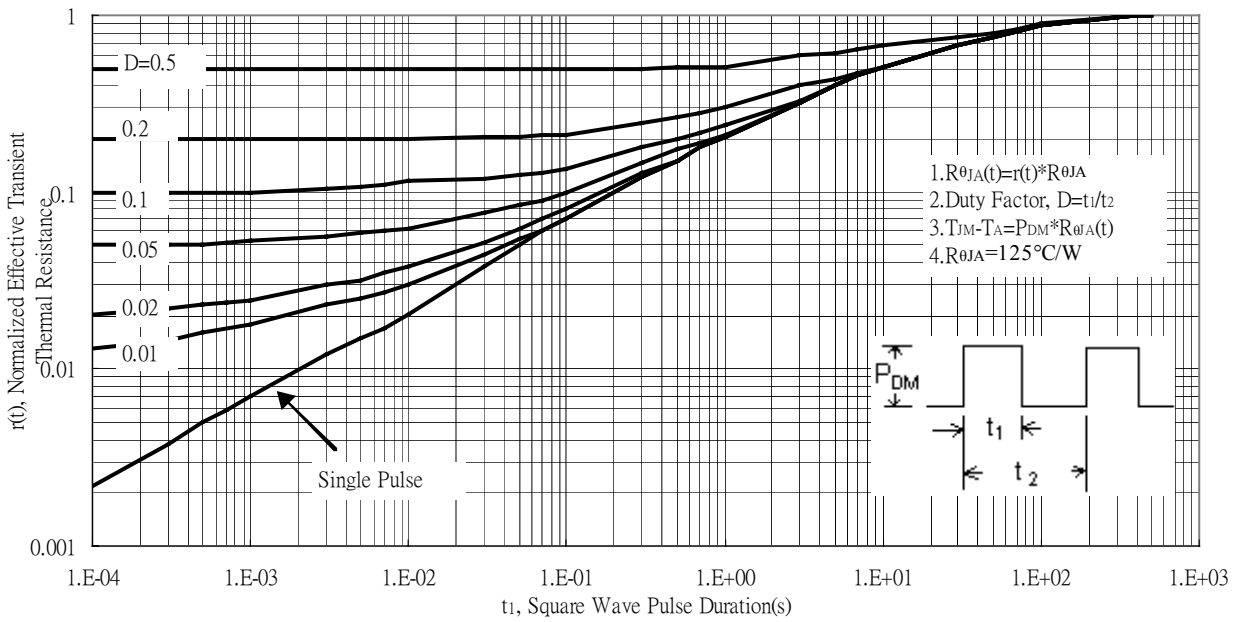
Typical Transfer Characteristics



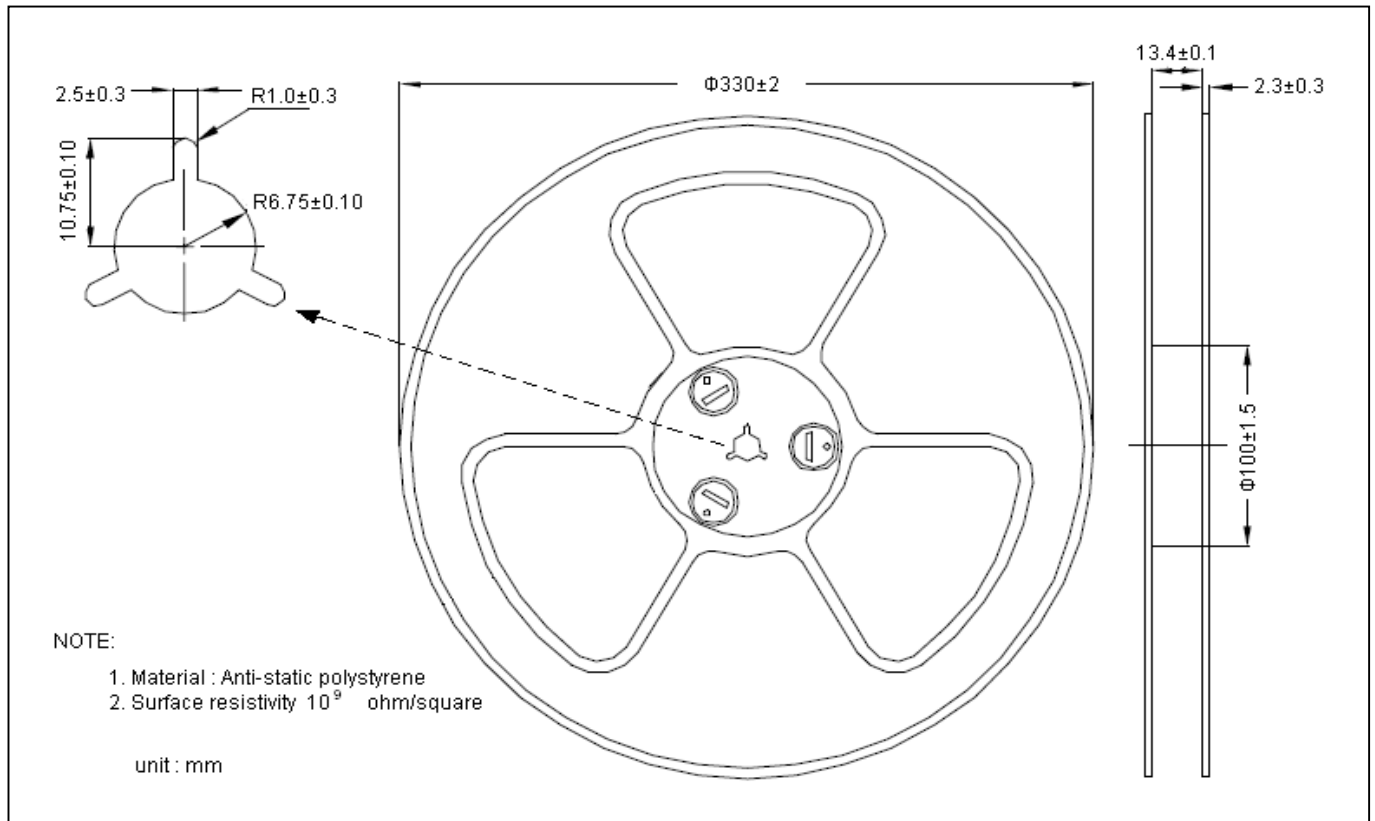
Single Pulse Power Rating, Junction to Ambient
 (Note on page 2)



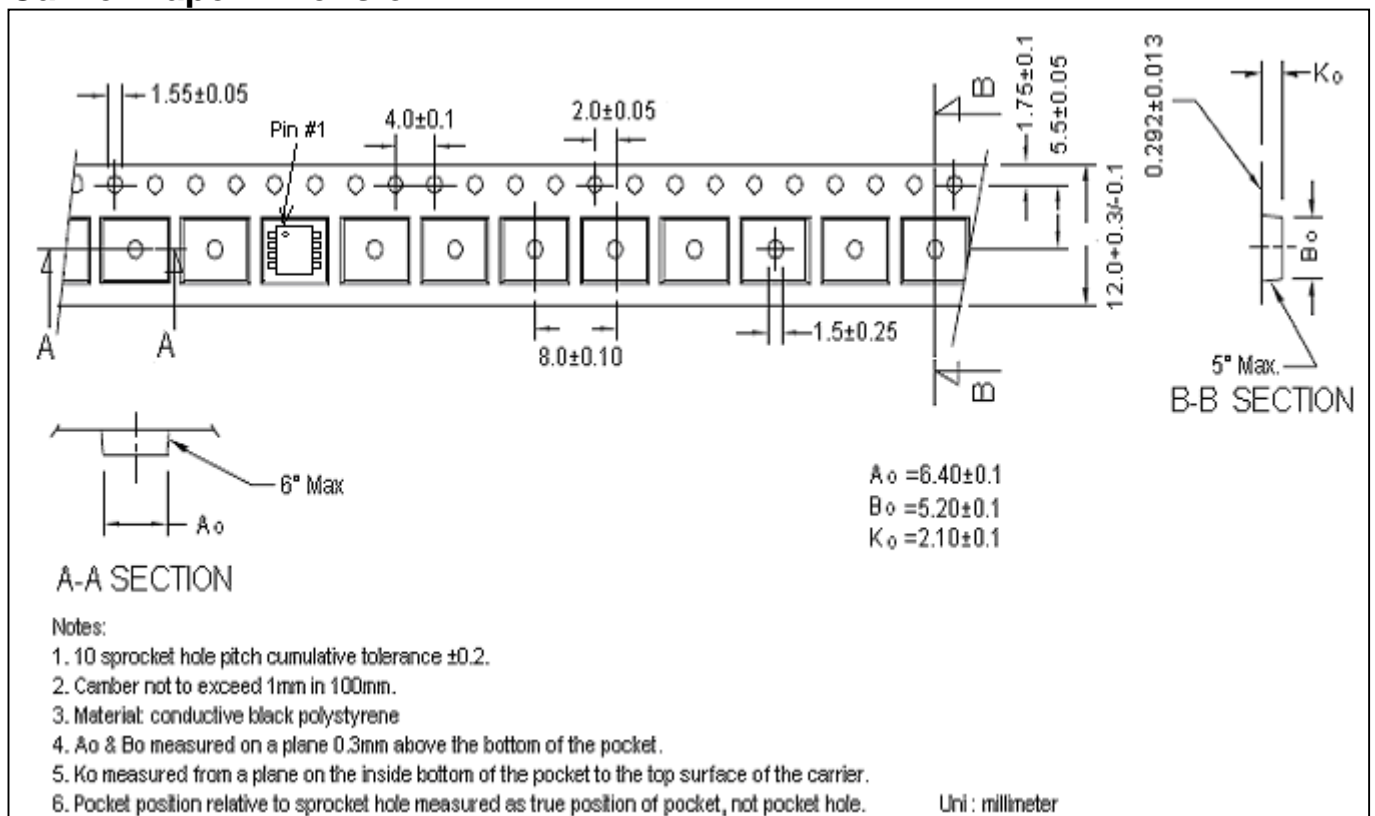
Transient Thermal Response Curves



Reel Dimension



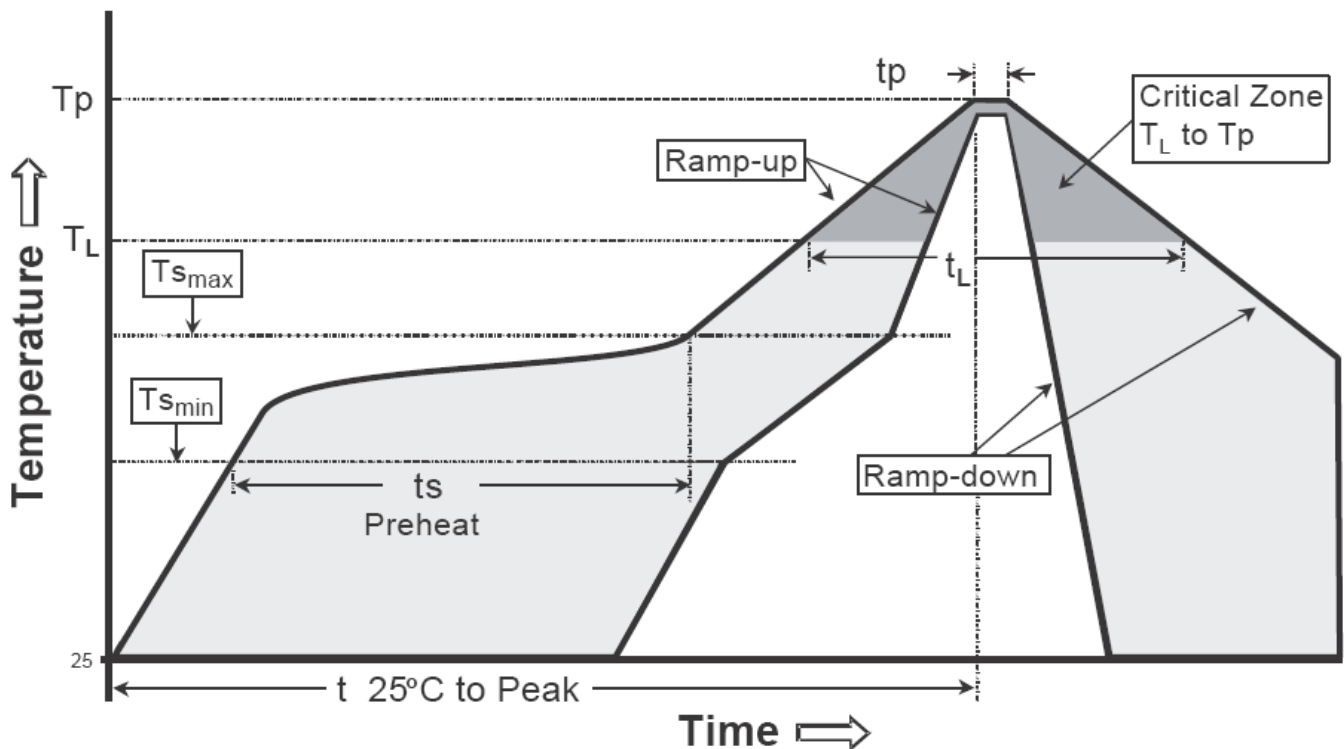
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

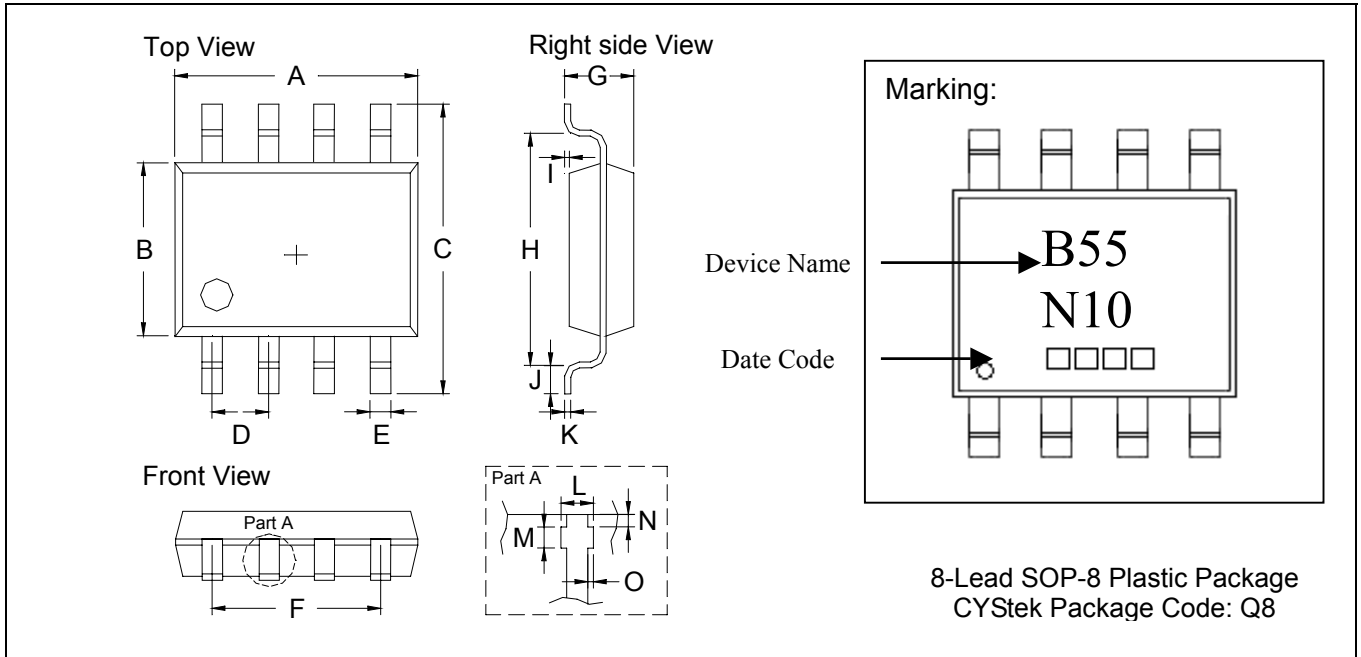
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

SOP-8 Dimension



*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1850	0.2007	4.70	5.10	I	0.0031	0.0110	0.08	0.28
B	0.1457	0.1614	3.70	4.10	J	0.0157	0.0323	0.40	0.83
C	0.2283	0.2441	5.80	6.20	K	0.0074	0.0102	0.19	0.26
D	0.0500*		1.27*		L	0.0145	0.0204	0.37	0.52
E	0.0130	0.0201	0.33	0.51	M	0.0118	0.0197	0.30	0.50
F	0.1472	0.1527	3.74	3.88	N	0.0031	0.0051	0.08	0.13
G	0.0472	0.0638	1.20	1.62	O	0.0000	0.0059	0.00	0.15
H	0.1889	0.2007	4.80	5.10					

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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