MTC-2010 CMOS 2µ

Standard Cell Library

Services

CMOS Family

Features

- **Technology:**
  CMOS 2 µ channel length, silicon gate, low or high ohmic double poly, double metal
- **Typical Gate Delay:**
  LS TTL compatible, 2.0 ns loaded typical on-chip gate delay
- **Speed:**
  Up to 25 MHz operation (Commercial Temp. Range)
- **Power Consumption:**
  2µW/gate/MHz
- **Operating Temperature Range: -55 to 125°C**
- **Power Supply (operation):**
  3 - 7 V digital
  3 - 12 V analog
- **I/O Characteristics:**
  - **TTL or CMOS levels**
  - **Full electrostatic protection**
  - **High latch-up immunity**
  - **Inverting or non-inverting; push-pull, open-drain or 3-state; unidirectional or bidirectional**
  - **Drive: 2 to 4 TTL loads**
- **Analog Possibilities:**
  - **Offset < 5 mV**
  - **Bandwidth > 2 MHz**
  - **Reference voltage ± 5%**
  - **Resistor matching ± 1%**
- **Computer-Aided Design:**
  Fully-integrated MADE™System
- **Compilers:**
  RAM, PLA, ROM and Switched-Capacitor Filter

Product Description

Alcatel Mietec's standard cell family reduces costs for custom LSI circuits. Due to smaller die sizes, standard cell parts can be more economical than gate arrays at as few as 10K to 20K units. The availibility of a wide range of packaging styles contributes greatly to offering the most cost-effective solutions.
Each pre-developed cell is optimized for area, speed, and electrical characteristics, resulting in a reduction in unit costs over gate arrays while maintaining comparatively low development costs and a relatively short development schedule. This methodology combines the dense layout characteristics of CMOS with the convenience of a highly-automated and comprehensive CAD package, the MADE system (Mietec Analog and Digital Engineering).

Library

Alcatel Mietec's standard cell family uses a CMOS 2µ process with two levels of polysilicon and two levels of metal interconnects.

The library consists of different levels of core cells, reflecting the levels of complexity of the circuit.

- At the first level, a set of standard digital cells and analog cells is available. These cells are 84.8 µ high (digital cells), and 208 µ high (analog cells), with variable widths placed side-by-side in rows.
- Block cells are part of the second level of cells: optimised functional blocks (e.g. ADC) or submodules, possibly distributed over several rows.
- The third level includes software generated cells (PLA, RAM, ROM, Switched-Capacitor filter).

Input and output cells are then placed at the periphery and the entire circuit is automatically interconnected.

Unlike gate arrays, only those cells and interconnects actually needed are used, so a smaller die size is achieved. In addition, different speed ranges are available in many cells, allowing optimization of speed and die size.

Propagation Delay

For digital cells, delays can be calculated by the equation :

$$t_d = t_{ti} + t_{dl} \times C_L$$

where
t_{di} = intrinsic delay (ns)
t_{dl} = load-dependent delay (ns/pF)
C_L = capacitive load (pF)

The parameters are specified in the individual cell data sheets included in Alcatel Mietec's Standard Cell Design Manual, which contains all the information necessary to design a circuit. C_L will be determined by the input capacitance of the cell as well as by interconnect capacitance. The equation yields nominal delay values for worst case processing conditions.

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Worst case delays can then be obtained by multiplying t_d by temperature of voltage derating factors which are also obtained from the design manual.

The MADE™ System

The MADE™ (Mietec Analog and Digital Engineering) system is a mixed mode design tool, combining the power of analog capabilities with advanced commercial tools for digital design.

The MADE™ design system provides a complete IC design solution based on an open, flexible design framework architecture and a broad set of high performance integrated tools, including logic synthesis, logic simulation, analog simulation, mixed digital/analog simulation, fault simulation, test interface, compilation, automatic place & route, layout editing, layout verification and mask preparation.

The MADE™ design system reduces design span time, ensures performances specs are met, and fits within current design methodologies. The results to the user are greater productivity and chip reliability, lower cost, and faster time to market.

The MADE™ system is available on SUN (Unix Operating System). To ease the link to different design systems, standards such as EDIF and VHDL are supported.

MADE™ is available for customer design in Alcatel Mietec's design center (Brussels), and may be released for use on customer premises. Training courses are available.

Absolute Maximum Ratings (Referenced to VSS)

Supply Voltage , V_{DD}
digital: - 0.5 V to + 7.0 V
analog: - 0.5 V to + 12.0 V
Input or Output Voltage
- 0.5 V to (V_{DD} + 0.5 V)
Storage Temperature
(Ceramic) - 65°C to 150 °C

Note:
Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions

Operating Supply Voltage, V_{DD}:
5.0 V ± 10 %
Extended Supply Voltage Option :
- digital: 3.0 V to 7.0 V
- analog: 3.0 V to 12.0V
Operating Temperature :
- 55°C to + 125°C

DC Electrical Characteristics

V_{DD} = 5.0 V ± 10% over temperature range unless otherwise specified.

A. Inputs

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{IL}	Low-Level Input Voltage					
	CMOS Interface				30% V_{DD}	V
	TTL Interface				0.8	V
V_{IH}	High-Level Input Voltage					
	CMOS Interface		70% V_{DD}			V
	TTL Interface		2.0			V
C_{IN}	Input Capacitance	Freq= 1 MHz @ 0V			10	pF
I_{IL}	Low-Level Input Current	$V_{IN} = V_{SS}$			±1	µA
I_{IH}	High-Level Input Current	$V_{IN} = V_{DD}$			±1	µA

B. Outputs

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{OL}	Low-Level Output Voltage	I_{OL} = < 1µA			0.05	V
V_{OH}	High-Level Output Voltage	I_{OH} = < 1 µA	V_{DD} - 0.05			V
I_{OL}	Low-Level Output Current	V_{OL} = 0.4 µA				
	2 TTL Drive		3.2			mA
	4 TTL Drive		6.4			mA
I_{OH}	High-Level Output Current	V_{OH} = 0.4 µA				
	2 TTL Drive		-1.6			mA
	4 TTL Drive		-3.2			mA
I_{OL}	3-State Output Leakage	V_O = 0V or V_{DD}			±1	µA
C_{OUT}	Output Capacitance	Freq= 1 MHz @ 0V			10	pF
C_{BID}	Capacitance at Bidirectional Pin	Freq= 1 MHz @ 0V			20	pF

C. Environment Protection

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{ESD}	Electrostatic Discharge Protection	HBM				
		C=100 pF R=1500 Ohms (MIL 883C Standard Method. 3015.7)	±1000	± 2000		V
		EDM				
		C=200 pF R=0 Ohm (EIAJ MM)	±150			V
V_{LU}	Latch-up Immunity	Jedec Std N°17	±100			mA

Cell Selection Guide

Process: worst case conditions
Voltage: V_{DD} = 5 V
Temperature: 25 °C

A. Digital Core Cells

1. LOGIC GATES		Delay (ns) (1)	Gate equiv. (2)	Sizes (µ x µ)
INV	Inverter	3.6	1	16 x 84.8
INV2	Inverter (x 2 drive)	2.7	2	16 x 84.8
INV4	Inverter (x 4 drive)	2.0	4	24 x 84.8
INV8	Inverter (x 8 drive)	1.8	8	40 x 84.8
NAND2	2-Input nand	4.6	1	24 x 84.8
NAND3	3-Input nand	6.1	2	40 x 84.8
NAND4	4-Input nand	7.4	2	48 x 84.8
NAND5	5-Input nand	8.8	3	48 x 84.8
NOR2	2-Input nor	6.0	1	32 x 84.8
NOR3	3-Input nor	9.7	2	40 x 84.8
NOR4	4-Input nor	15.4	2	40 x 84.8
NOR5	5-Input nor	10.4	3	56 x 84.8
AND2	2-Input and	7.0	2	32 x 84.8
AND3	3-Input and	9.1	2	40 x 84.8
AND4	4-Input and	10.7	3	48 x 84.8
AND6	6-Input and	10.3	3	72 x 84.8
AND7	7-Input and	13.3	4	80 x 84.8
AND8	8-Input and	13.5	4	88 x 84.8
OR2	2-Input or	9.1	2	32 x 84.8
OR3	3-Input or	13.0	2	40 x 84.8
OR4	4-Input or	16.6	3	48 x 84.8
OR6	6-Input or	10.6	3	80 x 84.8
OR7	7-Input or	17.7	4	80 x 84.8
OR8	8-Input or	20.0	4	96 x 84.8
BUF2	Buffer (x 2 drive)	4.9	2	32 x 84.8
BUF4	Buffer (x 4 drive)	5.6	4	40 x 84.8
BUF8	Buffer (x 8 drive)	5.2	8	48 x 84.8
BUF13	Buffer (x 13 drive)	4.6	13	104 x 84.8
BUF20	Buffer (x 20 drive)	5.1	20	120 x 84.8
EXOR	2-Input exor	7.6	3	64 x 84.8
EXNOR	2-Input exnor	7.0	3	56 x 84.8
ANDNOR	2x2-Input and-nor	10.7	3	40 x 84.8
ORNAND	2x2-Input or-nand	10.9	3	48 x 84.8
TRIINV1	Tristate inverting buffer	4.0	2	56 x 84.8
TRIBUF	Tristate non-inverting buffer	7.3	2	96 x 84.8
MUX21	2 to 1 Multiplexer with inverting output	4.8	3	64 x 84.8
MUX41S	4 to 1 Multiplexer with inverting output	10.5	7	112 x 84.8
MUX2	2 to 1 Multiplexer with non-inverting output	9.8	3	48 x 84.8
DEC2E	1-line to 2-line decoder with enable	8.1	3	56 x 84.8
DEC4E	2-line to 4-line decoder with enable	17.6	7	168 x 84.8
HALFA	Half adder	10.7	5	64 x 84.8
FULLA	Full adder	20.7	9	128 x 84.8

2. LATCHES AND FLIPFLOPS		Freq (MHz) (3)	Gate equiv. (2)	Sizes (μ x μ)
NANDSR	Nand SR-latch with set and reset both active low	-	4	40 x 84.8
DL	D-latch (active if EN is high)	54	5	64 x 84.8
DLL	D-latch (active if ENB is low)	54	5	64 x 84.8
DLRL	D-latch with reset (active low)	53	5	88 x 84.8
DLRLPU	D-latch with reset (active low) and D-input connected to VDD	53	5	88 x 84.8
DLSL	D-latch with set (active low)	45	6	104 x 84.8
DLSLQ	D-latch with set (active low) and Q-output only	46	5	72 x 84.8
DLSLQB	D-latch with set (active low) and QB-output only	48	5	64 x 84.8
DLSHRL	D-latch with set (active high) and reset (active low) with reset dominant	51	6	88 x 84.8
DFF	Positive-edge triggered D-flipflop (master slave)	56	7	112 x 84.8
DFFP	D-flipflop with preset	50	9	144 x 84.8
DFFRL	Positive-edge triggered D-flipflop with asynchronous reset (active low)	52	9	144 x 84.8
DFFRLPU	Positive-edge triggered D-flipflop with asynchronous reset (active low) and D-input connected to VDD	52	9	136 x 84.8
DFFSRLQ	Positive-edge triggered D-flipflop with synchronous reset (active low) and Q-output only	38	8	96 x 84.8
DFFSRLQB	Positive-edge triggered D-flipflop with synchronous reset (active low) and QB-output only	37	8	96 x 84.8
DFFSL	Positive-edge triggered D-flipflop with asynchronous set (active low)	54	9	144 x 84.8
DFFSLRL	Positive-edge triggered D-flipflop with asynchronous set and reset (both active low)	51	9	152 x 84.8
SCDSRLQ	Positive-edge triggered Scan-D-flipflop with synchronous reset (active low) and Q-output	29	12	168 x 84.8

3. MISCELLANEOUS		Sizes (μ x μ)
VDD	Core cell to allow connection of input pins to VDD	8 x 84.8
VSS	Core cell to allow connection of input pins to VSS	8 x 84.8
PROBE	Core cell to allow probing of internal nets of an unpassivated chip	24 x 84.8

B. Digital I/O Cells

1. INPUT BUFFERS		Delay (ns) (1)	Sizes (µ x µ)
IC	Non-inverting input cell CMOS-compatible	6.9	208 x 416
IIC	Inverting input cell CMOS-compatible	5.0	208 x 416
IICPUH	Inverting input cell CMOS-compatible with high value pull-up resistor	5.3	208 x 416
IICPDH	Inverting input cell CMOS-compatible with high value pull-down resistor	5.3	208 x 416
IICPUC	Inverting input cell CMOS-compatible with high value pull-up resistor and capacitance to be insensitive to signal feedthrough	5.3	208 x 416
IICPDC	Inverting input cell CMOS-compatible with high value pull-down resistor and capacitance to be insensitive to signal feedthrough	5.3	208 x 416
IT	Non-inverting input cell TTL-compatible	12.5	208 x 416
IIT	Inverting input cell TTL-compatible	10.4	208 x 416
ISC	Non-inverting input cell with Schmitt-trigger characteristic CMOS-compatible	14.3	208 x 416
IISC	Inverting input cell with Schmitt-trigger characteristic CMOS-compatible	13.4	208 x 416
IST	Non-inverting input cell with Schmitt-trigger characteristic TTL-compatible	21.2	208 x 416
IIST	Inverting input cell with Schmitt-trigger characteristic TTL-compatible	21.0	208 x 416
2. INPUT LEVEL SHIFTERS			
ITLS	Non-inverting input level shifter TTL-compatible	86.0	208 x 416
ITLSPUH	Non-inverting input level shifter with high value pull-up resistor TTL-compatible	86.0	208 x 416
3. OUTPUT BUFFERS		**Delay (ns) (1)**	**Sizes (µ x µ)**
OI2	Inverting output cell 2-TTL drive	11.4	208 x 416
OI4	Inverting output cell 4-TTL drive	9.8	224 x 416
O2	Non-inverting output cell, 2-TTL drive	9.2	208 x 416
OT2	Tristate non-inverting output cell, 2-TTL drive	13.2	208 x 416
OT2PDH	Tristate non-inverting output cell, 2-TTL drive with high value pull-down resistor	13.8	208 x 416
OT4	Tristate non-inverting output cell, 4-TTL drive	12.2	264 x 416
OIOD2	Inverting output cell with open drain, 2-TTL drive	7.5	208 x 416
OIOD4	Inverting output cell with open drain, 4-TTL drive	6.8	208 x 416
4. OUTPUT LEVEL SHIFTERS			
O1LS	Non-inverting output level shifter 1-TTL drive	58.0	312 x 416

5. BIDIRECTIONAL BUFFERS		Delay I (ns) (1)	Delay O (ns) (1)	Sizes (µ x µ)
BICT2	Bidirectional cell with CMOS-compatible inverting input and tristate non-inverting output with 2-TTLdrive	5.0	13.2	208 x 416
BICT2PUH	Bidirectional cell with CMOS-compatible inverting input and tristate non-inverting output with 2-TTL drive with high value pull-up resistor	5.3	13.2	208 x 416
BICT2PDH	Bidirectional cell with CMOS-compatible inverting input and tristate non-inverting output with 2-TTL drive with high value pull-down resistor	5.3	13.2	208 x 416
BITT2	Bidirectional cell with TTL-compatible inverting input and tristate non-inverting output with 2-TTL drive	10.4	13.2	208 x 416
BISCT2	Bidirectional cell with CMOS-compatible Schmitt trigger inverting input and tristate non-inverting output 2-TTL drive	13.4	13.2	208 x 416
BSCT2	Bidirectional cell with CMOS-compatible Schmitt trigger non-inverting input and tristate non-inverting output 2-TTL drive	14.2	13.2	208 x 416

6. MISCELLANEOUS		Sizes (µ x µ)
IOVDD	Positive supply-voltage pad (VDD)	168 x 416
IOVSS	Ground connection pad (VSS)	168 x 416
BPU	High value pull-up resistor	24 x 416
BPD	High value pull-down resistor	24 x 416

C. Analog Core Cells

1. VOLTAGE REFERENCES		Output voltage	Power supply depend.	Temperat. sensitivity	Sizes (µ x µ)
CLBGP	Bandgap. Low voltage range.	1.17 V	30 dB	300 ppm/°C	464 x 208
CHBGPC	Bandgap with improved power supply rejection. High voltage range.	1.14 V	40 dB	300 ppm/°C	328 x 208

2. CURRENT REFERENCES		Output current	Power supply depend.	Temperat. sensitivity	Sizes (µ x µ)
CFCUR	Current reference. Full voltage range.	2 µA	8 %/V	0.5 %/°C	120 x 208
CHCURC	Current reference with improved power supply rejection. High voltage range.	2 µA	0.5 %/V	0.4 %/°C	96 x 208
CUR1	Current source to be used with CMPNS and CMPPS	1.4 µA/1µA	4%/V		200 x 84.8

3. CURRENT MIRROR		**Mirror factor type N**	**Mirror factor type P**	**Sizes (µ x µ)**
CFCUMA	Current mirror - type A. Full voltage range	1/7	1/9	48 x 208
CFCUMB	Current mirror - type B. Full voltage range	1/1.4	1/1.8	48 x 208
CFCUMC	Current mirror - type C. Full voltage range	1/0.7	1/0.9	48 x 208
CFCUMD	Current mirror - type D. Full voltage range	1/4.8	1/6.8	40 x 208
CFCUME	Current mirror - type E. Full voltage range	1/1.9	1/2.7	48 x 208
CFCUMF	Current mirror - type F. Full voltage range	2.1	1.5	48 x 208
CHCUMCA	Current mirror type A with improved power supply rejection. High voltage range	1/7	1/9	56 x 208
CHCUMCB	Current mirror type B with improved power supply rejection. Full voltage range	1/1.4	1/1.8	40 x 208
CHCUMCC	Current mirror type C with improved power supply rejection. Full voltage range	1/0.7	1/0.9	48 x 208

4. LEVEL SHIFTER		**Maximum delay (ns)**	**Size (µ x µ)**
CHLSH	Level shifter from low voltage range to high voltage range	12.6	32 x 208

5. ANALOG SWITCH		**Resistance (Ω)**	**Size (µ x µ)**
CFASW	Analog switch with low on-resistance. Full voltage range	350 (at 5 V) 200 (at 10 V)	64 x 208

6. OPERATIONAL AMPLIFIERS		**Size (µ x µ)**
CFOAHLN	Dual stage low offset operational amplifier with P-MOS input stage and high output impedance. Full voltage range	328 x 208

Gain (dB)	**Phase margin (°)**	**Slew rate (V/µs)**
80	70	1.5

CFOAHPS	Dual stage operational amplifier with P-MOS input stage and high output impedance Single poly version - Full voltage range	280 x 208

Gain (dB)	**Phase margin (°)**	**Slew rate (V/µs)**
90	45	0.6

CFOAHND Dual stage operational amplifier with N-MOS input stage and high output impedance. ..... 216 x 208
Double poly version - Full voltage range

Biasing Ref.	Mirror	Voltage range (V)	Gain (dB)	Phase margin (°)	Slew rate (V/µs)	Bias current (µA)
CFCUR	CFCUMA	3-12	95	45	0.37	15
CFCUR	CFCUMB	3-12	81	63	1.70	75
CFCUR	CFCUMC	3-12	75	71	3.60	150
CHCURC	CHCUMCA	7-12	95	45	0.37	15
CHCURC	CHCUMCB	7-12	81	63	1.70	75
CHCURC	CHCUMCC	7-12	75	71	3.60	150

Notes 1. All offsets are lower than 10 mV
2. Maximum load capacitor is 20 pF

CFOALAB Dual stage operational amplifier with parallel N-MOS and P-MOS input stages and low output impedance ..... 600 x 208
Double poly version - Full voltage range

Gain (dB)	Phase margin (°)	Slew rate (V/µs)
155	54	0.3

7. COMPARATORS

Size (µ x µ)

CFCMPNS Comparator with N-mos input and single ended output stage ..... 80 x 208
Full voltage range

Biasing Ref.	Mirror	Gain (dB)	Offset mV	Delay rising µs	Delay falling µs	Bias current µA
CFCUR	CFCUME	97	<5	5.6	15.4	4
CFCUR	CFCUMF	89	<5	1.5	5.9	10
CFCUR	CFCUMD	77	<5	0.8	2.4	40

Note : Propagation delays are for Voverdrive = 100 mV and a typical load.

CFCMPPS Comparator with P-mos input and single ended output stage ..... 80 x 208
Full voltage range

Biasing Ref.	Mirror	Gain (dB)	Offset mV	Delay rising µs	Delay falling µs	Bias current µA
CFCUR	CFCUME	100	<5	7.9	1.6	4
CFCUR	CFCUMF	93	<5	4.1	1.0	10
CFCUR	CFCUMD	81	<5	1.7	0.6	40

Note: Propagation delays are for Voverdrive = 100 mV and a typical load.

CMPNS	Comparator with N-MOS input and single ended output stage	216 x 84.8

Gain	Offset	Delay rising	Delay falling	Bias current
dB	mV	µs	µs	µA
77	<5	0.8	2.4	40

Note: Propagation delays are for Voverdrive = 100 mV and a typical load.

CMPPS	Comparator with P-MOS input and single ended output stage	280 x 84.8

Gain	Offset	Delay rising	Delay falling	Bias current
dB	mV	µs	µs	µA
81	<5	1.7	0.6	40

Note: Propagation delays are for Voverdrive = 100 mV and a typical load.

8. MISCELLANEOUS		**Sizes (µ x µ)**
CFPRB	Core cell to allow probing of internal nets of an unpassivated chip.	24 x 208
CFVDD	Core cell to allow connection of input pins to VDDA	8 x 208
CFVSS	Core cell to allow connection of input pins to VSSA	8 x 208

D. Analog I/O Cells

1. RC OSCILLATORS		**Frequency range(Hz)**	**Precision**	**Sizes (µ x µ)**
RC1	RC-oscillator, programmable externally (R and C)	1 K - 400K	+/- 10 %	416 x 416
RC2	Precision RC-oscillator, programmable externally (R and C)	1 K - 1M	+/- 3 %	264 x 416

2. CRYSTAL OSCILLATORS		**Frequency range(Hz)**	**Current max(µA)**	**Sizes (µ x µ)**
XTAL1	Crystal oscillator	100K - 20M	1340 (20 MHz)	416 x 416
XTAL2	Low power crystal oscillator	100K - 10M	250 (10 MHz)	416 x 416
XTAL4	Low power crystal oscillator	32K	25	416 x 416

3. OPERATIONAL AMPLIFIER		**Size (µ x µ)**
PFOAHND	CFOAHND for peripheral use	256 x 208
PFOALAB	CFOALAB for peripheral use	672 x 208

4. MISCELLANEOUS		Size (μ x μ)
ZERO	Zero cross detector, suited for mains triac burst-switching with symmetrical switch pulse around zero cross.	248 x 416
POR1	Power on reset with built-in hysteresis	208 x 416
PPD	Input pad with protection diodes	208 x 416
PPDR	Input pad with protection diodes and polysilicon resistor	208 x 416
PFPTR	Externally programmable current source with P-MOS transistor. Full voltage range	208 x 416
PHPTRC	Externally programmable cascode current source with P-MOS transistor. Full voltage range.	208 x 416
PFRPO	Polysilicon resistor unit for peripheral use (analog core dimensions)	40 x 208
PFPAD	Bond pad	208 x 416
PFPADR	Bond pad with polysilicon resistor	208 x 416
PFPPD	Input pad with protection diodes	208 x 416
PFPPDR	Input pad with protection diodes and polysilicon resistor	208 x 416
PFVDD	Positive analog supply voltage pad (VDDA)	208 x 416
PFVSS	Analog ground connection pad (VSSA)	208 x 416

E. Block cells

1. DIGITAL CELLS		Features	Sizes (μ x μ)
PLA	Programmed Logic Array generated by the PLA module generator	type 1: static type 2: clocked FSM type 3: dynamic single clock PLA type 4: dynamic two-clock PLA	compiled
SRAM	Static RAM generated by the RAM module generator	430 bits/mm²	compiled
ROM	Read Only Memory generated by the ROM module generator	4kbits/mm²	compiled

2. ANALOG CELLS		Features	Sizes (μ x μ)
SCFILTER	Switched-Capacitor Filter generated by the SC module generator. Automatic generation of cascaded biquad topology starting from frequency template	frequency range: 0.1 to 25 kHz	compiled
RESISTOR	Resistor generated by the R module generator		compiled
AD081	8-bit successive approximation A/D convertor	max sampling rate: 45KHz acquisition time: 4μs integral non linearity: 1/3 LSB differential non linearity: 1/2 LSB	1204 x 744
DA081	8-bit voltage output resistor string D/A convertor	settling time: 3 μs integral non linearity: 3/4 LSB differential non linearity: 1/4 LSB	600 x 816

Notes:

(1) Propagation delay for a typical load:
- Core cells: 400 µm interconnection and a fan-out of 3 inverters
- Input cells: 1 mm interconnection and a fan-out of 10 inverters
- Output cells: 30 pF.

(2) 2-input-NAND gate equivalent

(3) Maximum clock frequency

(4) Voltage ranges for analog cells:
- Low voltage range: 3 V to 7 V
- High voltage range: 7 V to 12 V
- Full voltage range: 3 V to 12 V