

N- AND P-CHANNEL ENHANCEMENT MODE POWER MOSFET

MTC3585N6

Description

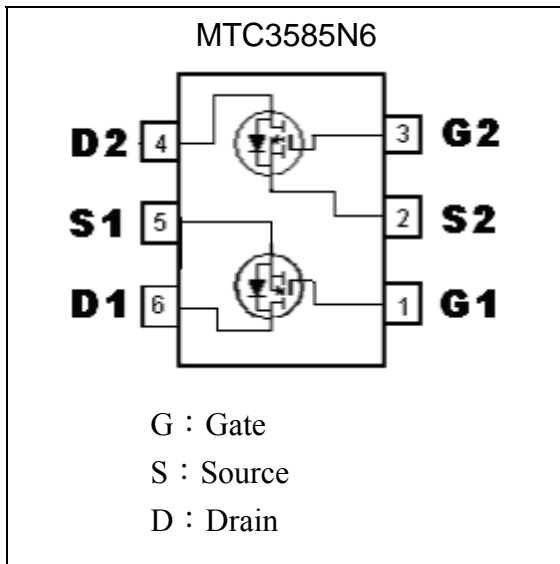
The MTC3585N6 consists of a N-channel and a P-channel enhancement-mode MOSFET in a single SOT-26 package, providing the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-26 package is universally preferred for all commercial-industrial surface mount applications.

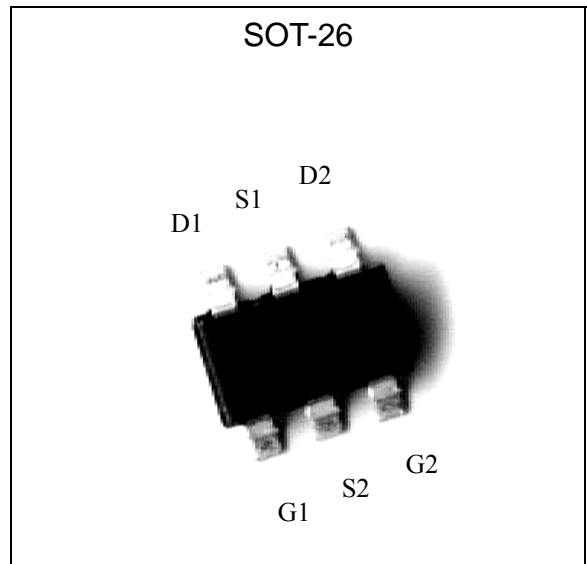
Features

- Simple drive requirement
- Low gate charge
- Low on-resistance
- Fast switching speed
- Pb-free package

Equivalent Circuit



Outline





Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits		Unit
		N-channel	P-channel	
Drain-Source Breakdown Voltage	BV _{DSS}	20	-20	V
Gate-Source Voltage	V _{GS}	±12	±12	V
Continuous Drain Current @T _A =25 °C (Note 1)	I _D	3.5	-2.5	A
Continuous Drain Current @T _A =70 °C (Note 1)	I _D	2.8	-1.97	A
Pulsed Drain Current (Note 2)	I _{DM}	10	-10	A
Total Power Dissipation (Note 1)	P _d	1.14		W
Linear Derating Factor		0.01		W / °C
Operating Junction and Storage Temperature	T _j , T _{stg}	-55~+150		°C
Thermal Resistance, Junction-to-Ambient (Note 1)	R _{th,ja}	110		°C/W

Note : 1.Surface mounted on 1 in² copper pad of FR-4 board, t≤5 sec; 180°C/W when mounted on minimum copper pad
 2.Pulse width limited by maximum junction temperature

N-Channel Electrical Characteristics (Tj=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	20	-	-	V	V _{GS} =0, I _D =250μA
ΔBV _{DSS} /ΔT _j	-	0.02	-	V/°C	Reference to 25°C, I _D =1mA
V _{GS(th)}	0.5	-	1.2	V	V _{DS} =V _{GS} , I _D =250μA
I _{GSS}	-	-	±100	nA	V _{GS} =±12V, V _{DS} =0
I _{DSS}	-	-	1	μA	V _{DS} =20V, V _{GS} =0
I _{DSS}	-	-	10	μA	V _{DS} =16V, V _{GS} =0, T _j =70°C
*R _{DSON}	-	-	75	mΩ	I _D =3.5A, V _{GS} =4.5V
	-	-	125		I _D =1.2A, V _{GS} =2.5V
*G _{FS}	-	7	-	S	V _{DS} =5V, I _D =3A
Dynamic					
C _{iss}	-	230	370	pF	V _{DS} =20V, V _{GS} =0, f=1MHz
C _{oss}	-	55	-		
C _{rss}	-	40	-		
*t _{d(ON)}	-	6	-	ns	V _{DS} =15V, I _D =1A, V _{GS} =5V, R _G =3.3Ω, R _D =15Ω
*t _r	-	8	-		
*t _{d(OFF)}	-	10	-		
*t _f	-	3	-		
*Q _g	-	4	7	nC	V _{DS} =16V, I _D =3A, V _{GS} =4.5V
*Q _{gs}	-	0.7	-		
*Q _{gd}	-	2	-		
R _g	-	1.1	1.7	Ω	f=1MHz
Source-Drain Diode					
*V _{SD}	-	-	1.2	V	V _{GS} =0V, I _S =1.2A
*t _{rr}	-	16	-	ns	I _S =3A, V _{GS} =0V, dI/dt=100A/μs
*Q _{rr}	-	8	-	nC	

*Pulse Test : Pulse Width ≤300μs, Duty Cycle ≤2%



P-Channel Electrical Characteristics (Tj=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	-20	-	-	V	V _{GS} =0, I _D =-250μA
ΔBV _{DSS} /ΔT _j	-	-0.01	-	V/°C	Reference to 25°C, I _D =-1mA
V _{GS(th)}	-	-	-1.2	V	V _{DS} =V _{GS} , I _D =-250μA
I _{GSS}	-	-	±100	nA	V _{GS} =±12V, V _{DS} =0
I _{DSS}	-	-	-1	μA	V _{DS} =-20V, V _{GS} =0
I _{DSS}	-	-	-25	μA	V _{DS} =-16V, V _{GS} =0, T _j =70°C
*R _{DS(ON)}	-	-	120	mΩ	I _D =-2.8A, V _{GS} =-10V
	-	-	160		I _D =-2.5A, V _{GS} =-4.5V
	-	-	300		I _D =-2A, V _{GS} =-2.5V
*G _{FS}	-	4	-	S	V _{DS} =-5V, I _D =-2A
Dynamic					
C _{iss}	-	270	430	pF	V _{DS} =-20V, V _{GS} =0, f=1MHz
C _{oss}	-	70	-		
C _{rss}	-	55	-		
*t _{d(ON)}	-	6	-	ns	V _{DS} =-10V, I _D =-1A, V _{GS} =-10V, R _G =3.3Ω, R _D =10Ω
*t _r	-	17	-		
*t _{d(OFF)}	-	16	-		
*t _f	-	5	-		
*Q _g	-	5	8	nC	V _{DS} =-16V, I _D =-2A, V _{GS} =-4.5V
*Q _{gs}	-	1	-		
*Q _{gd}	-	2	-		
Source-Drain Diode					
*V _{SD}	-	-	-1.2	V	V _{GS} =0V, I _S =-1.2A
*t _{rr}	-	20	-	ns	I _S =-2A, V _{GS} =0V, dI/dt=100A/μs
*Q _{rr}	-	15	-	nC	

*Pulse Test : Pulse Width ≤300μs, Duty Cycle ≤2%

N-channel Characteristic Curves

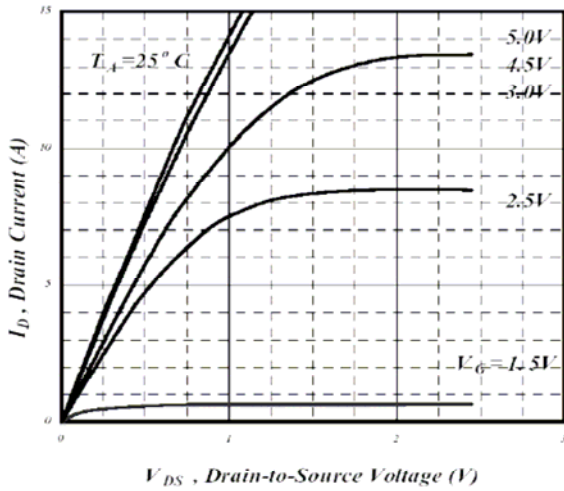


Fig 1. Typical Output Characteristics

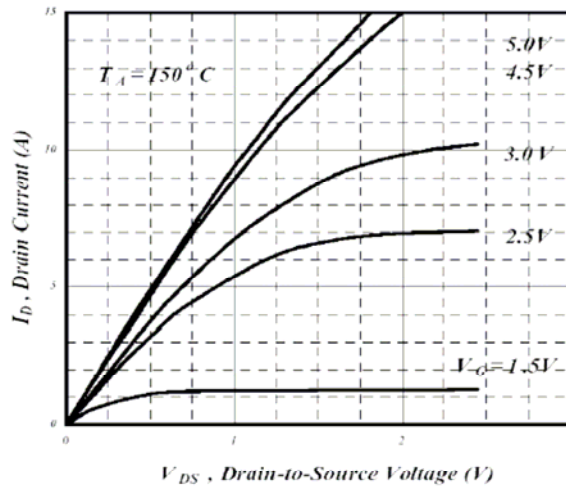


Fig 2. Typical Output Characteristics

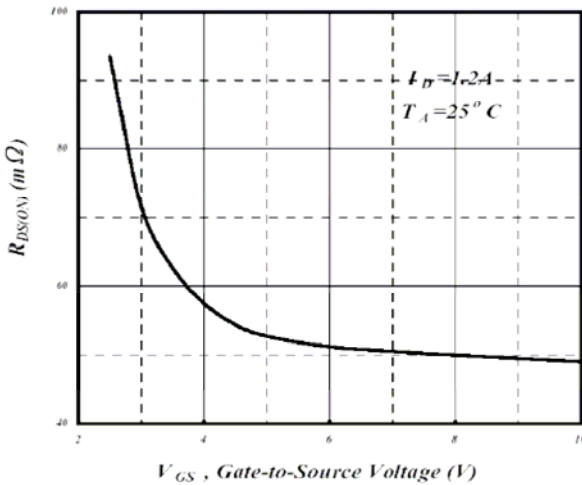


Fig 3. On-Resistance v.s. Gate Voltage

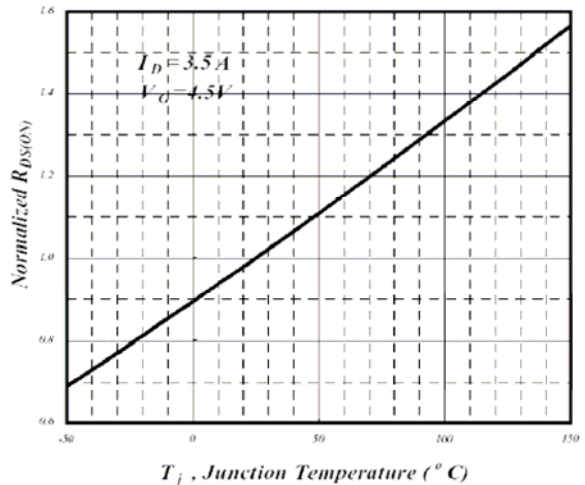


Fig 4. Normalized On-Resistance v.s. Junction Temperature

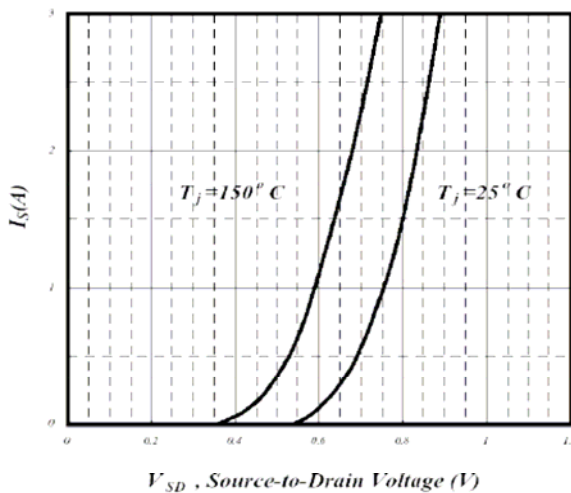


Fig 5. Forward Characteristics of Reverse Diode

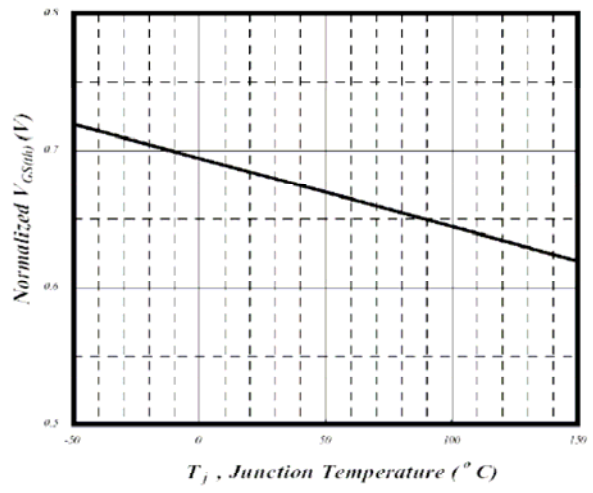


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

N-channel Characteristic Curves(Cont.)

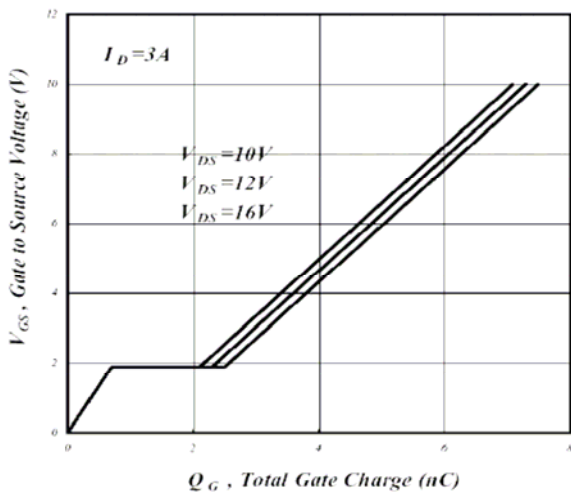


Fig 7. Gate Charge Characteristics

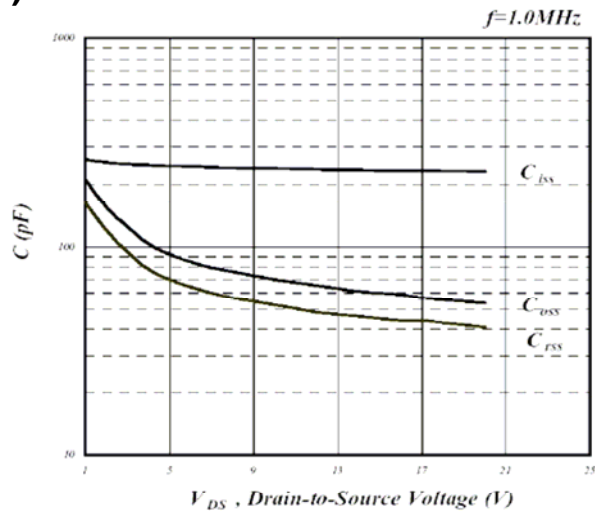


Fig 8. Typical Capacitance Characteristics

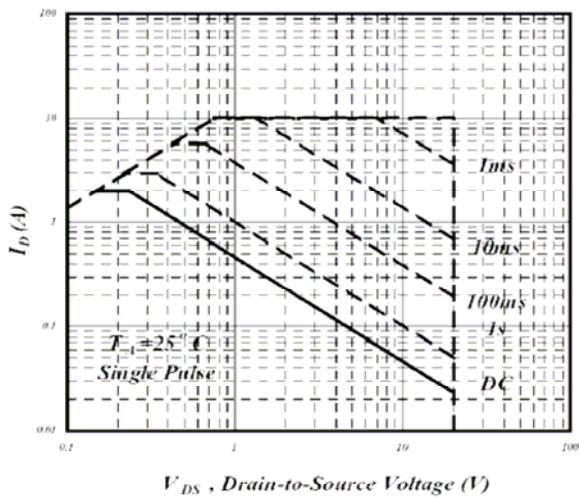


Fig 9. Maximum Safe Operating Area

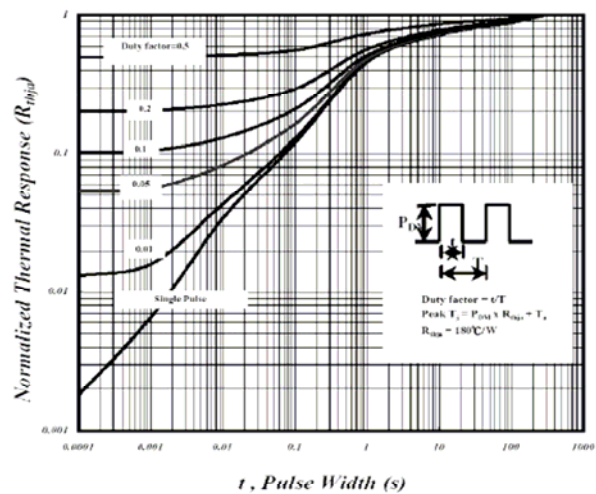


Fig 10. Effective Transient Thermal Impedance

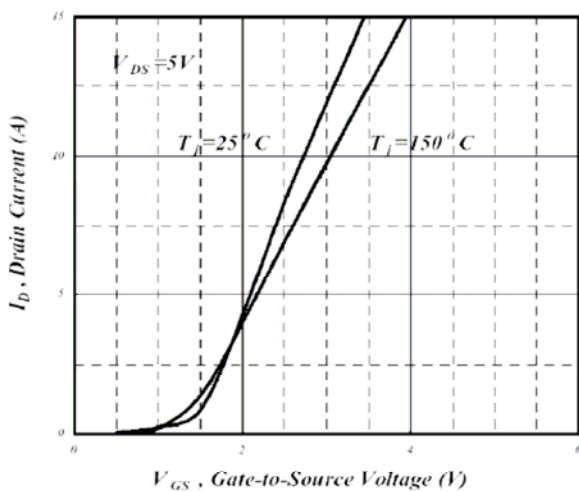


Fig 11. Transfer Characteristics

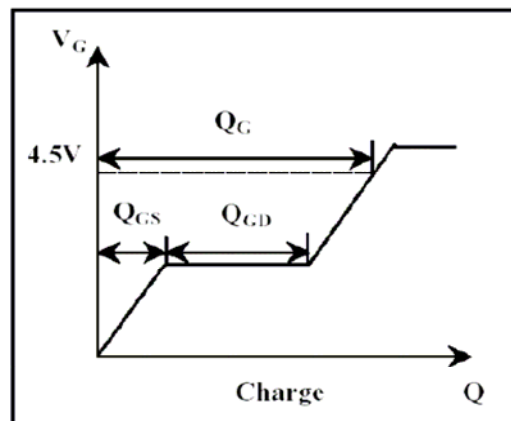


Fig 12. Gate Charge Waveform

P-channel Characteristic Curves

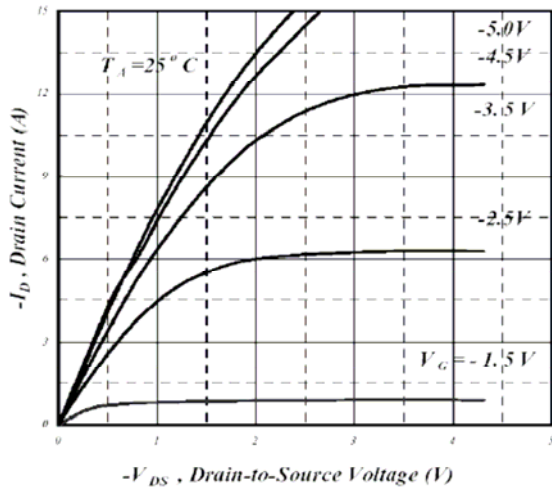


Fig 1. Typical Output Characteristics

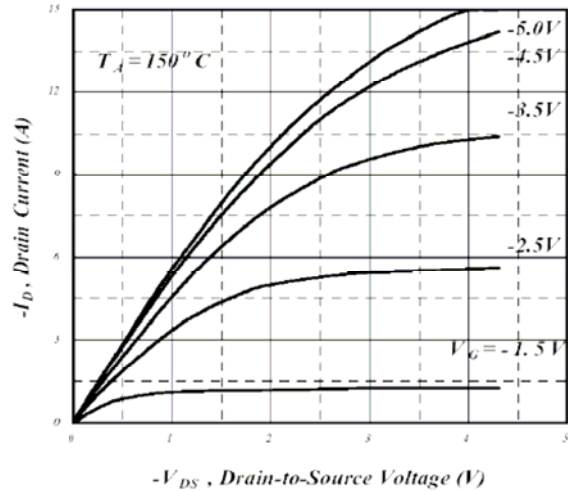


Fig 2. Typical Output Characteristics

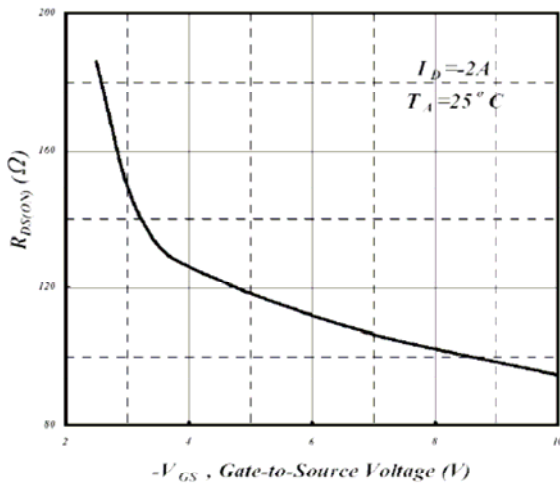


Fig 3. On-Resistance v.s. Gate Voltage

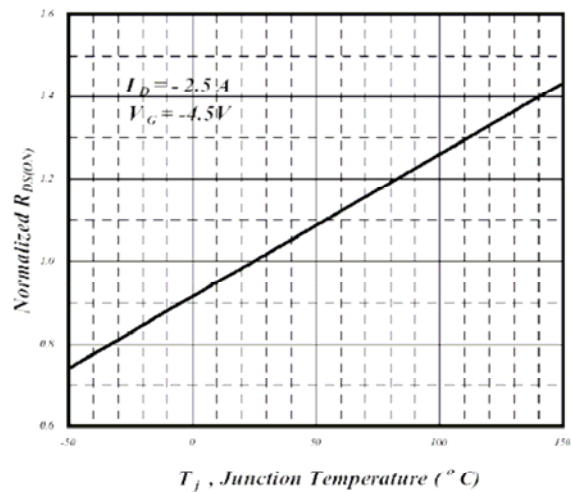


Fig 4. Normalized On-Resistance v.s. Junction Temperature

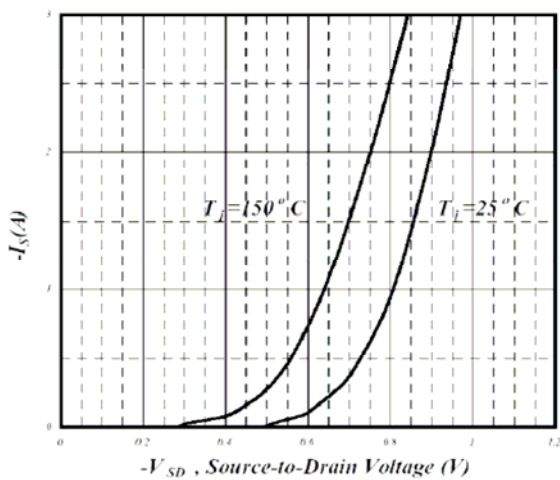


Fig 5. Forward Characteristics of Reverse Diode

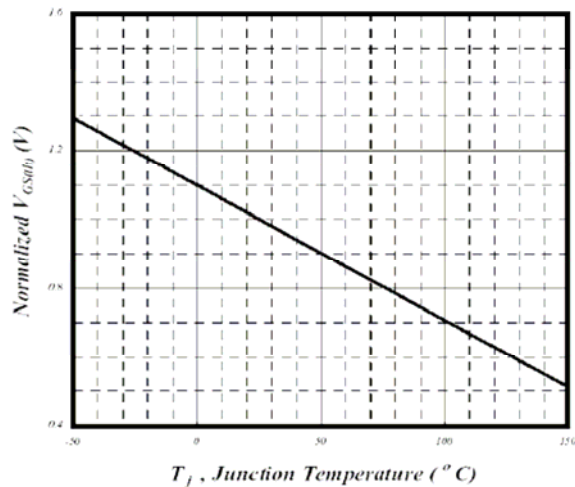


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

P-channel Characteristic Curves(Cont.)

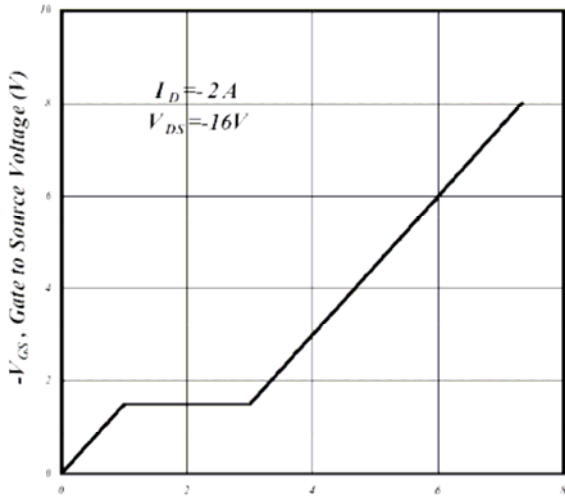


Fig 7. Gate Charge Characteristics

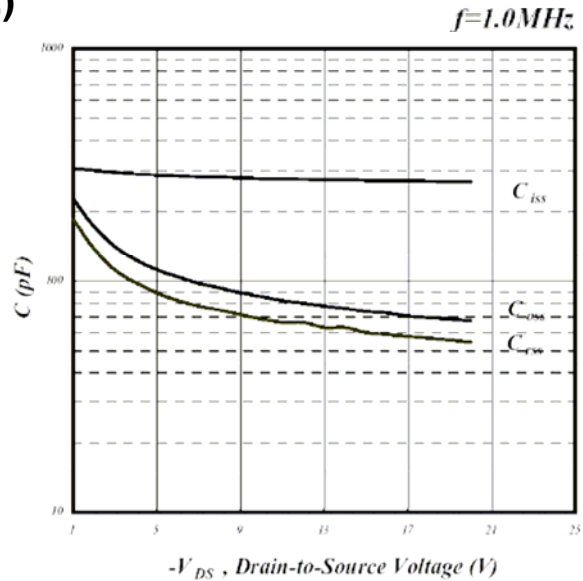


Fig 8. Typical Capacitance Characteristics

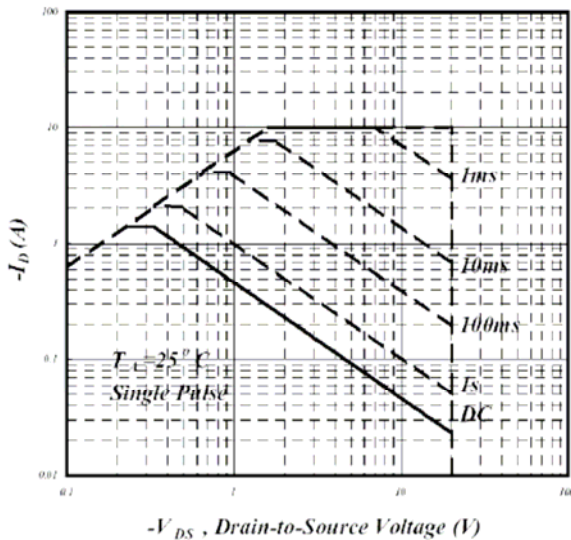


Fig 9. Maximum Safe Operating Area

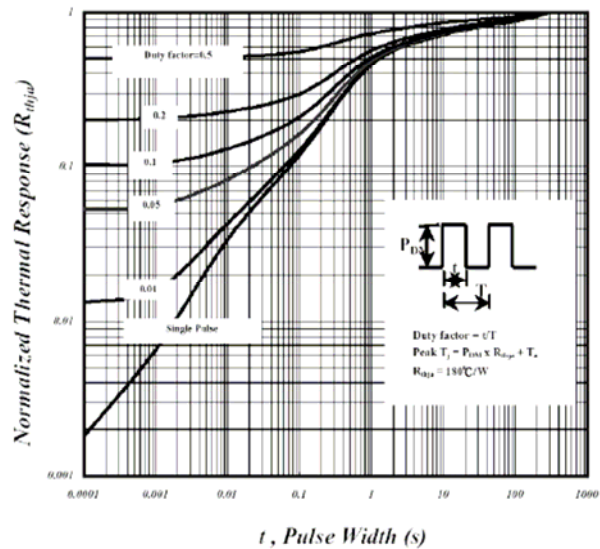


Fig 10. Effective Transient Thermal Impedance

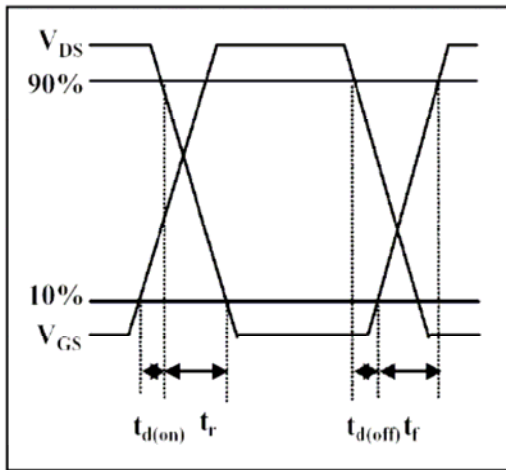


Fig 11. Switching Time Waveform

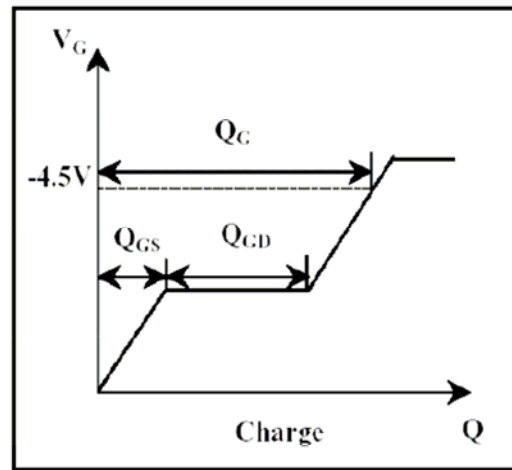
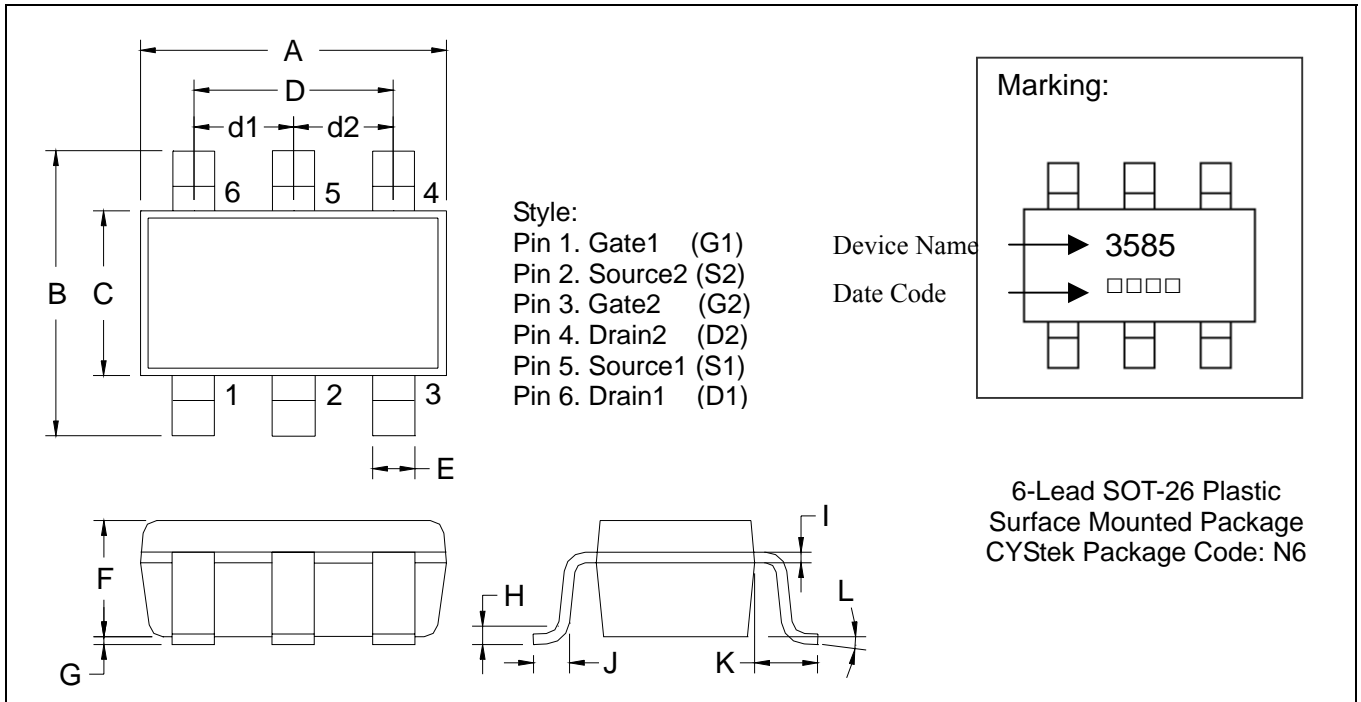


Fig 12. Gate Charge Waveform

SOT-26 Dimension



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1063	0.1220	2.70	3.10	F	0.0472 REF		1.20 REF	
B	0.1024	0.1181	2.60	3.00	G	0	0.0039	0	0.10
C	0.0551	0.0709	1.40	1.80	H	-	0.0079	-	0.20
D	0.0748 REF		1.90 REF		I	0.0047 REF		0.12 REF	
d1	0.0374 REF		0.95 REF		J	0.0146 REF		0.37 REF	
d2	0.0374 REF		0.95 REF		K	0.0236 REF		0.60 REF	
E	0.0118	0.0217	0.30	0.55	L	0°	10°	0°	10°

Notes : 1.Controlling dimension : millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material :

- Lead : 42 Alloy ; solder plating
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.