PHASE CONTROL THYRISTOR-DIODE MODULES

MTT-160, MTTC-160, MTTA-160
MTD-160, MTDC-160, MTDA-160
MDT-160, MDTC-160, MDTA-160

- V_{DRM}/V_{RRM} = **400 - 1600 V**
- $I_{T(AV)}$ = **160 A** (T_C = 85 °C)
- I_{TSM} = **5 kA** (T_{Vj} = 125 °C)

- Heat transfer through AlN ceramic isolated metal baseplate
- Presspack construction
- High reliability at thermal cycles (10^5 at ΔT_C = 70 ºC)
- Case width 34 mm

MAXIMUM RATED VALUES

Parameter and conditions	Symbol	Values			Units
		min.	typ.	max.	
Repetitive peak off-state voltage / Repetitive peak reverse voltage, T_{Vj} = - 60 °C…+ 125 °C	V_{DRM} / V_{RRM}	400 -		1600	V
Non-repetitive peak off-state voltage/Non- repetitive peak reverse voltage, T_{Vj} = - 60 °C…+ 125 °C	V_{DSM} / V_{RSM}	500	-	1700	
Repetitive peak off-state current/ Repetitive peak reverse current, T_{Vj} = 125 °C, V_D / V_R = V_{DRM} / V_{RRM}	I_{DRM} / I_{RRM}	-	-	25	mA
Max. average on-state current, f = 50 Hz, double side cooled, T_C = 85 °C	$I_{T(AV)}$ -		-	160	A
RMS on-state current	I_{RMS}	-	-	250	
Surge non-repetitive current, V_R = 0, T_{Vj} = 125 °C, t_p = 10 ms	I_{TSM}	-	-	5	kA
Safety factor	I^2t	-	-	125	kA^2s
Critical rate of rise of on-state current, V = 0,67V_{DRM} , I_T = 320 A, I_{FG} = 1 A, t_r = 1 µs, f = 50 Hz, T_{Vj} =125 °C	$(di_T/dt)_{crit}$ -		-	320	A/µs
Critical rate of rise of off-state voltage V_D = 0,67V_{DRM}, T_{Vj} = 125 °C	$(dV_D/dt)_{crit}$ 500		-	1000	V/µs
Gate power loss, DC	P_{GM}	-	-	4	W
Operation junction temperature range	T_{Vj}	- 60	-	+ 125	°C
Storage temperature range	T_{stg}	- 60	-	+ 50	

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ELECTRICAL CHARACTERISTICS

Maximum peak on-state voltage, I_T = 502 A, T_{Vj} = 25 °C	V_{TM}	- -		1,50	V
On-state threshold voltage, T_{Vj} = 125 °C, I_T = 200 - 800 A	$V_{(TO)}$	- -		1,00	
On-state slope resistance, T_{Vj} = 125 °C, I_T = 200 - 800 A	r_T	- -		1,05	mΩ
Delay time, $V = 0,67V_{DRM}$, I_T = 160 A, I_{FG} = 1 A, t_r = 1 µs, T_{Vj} = 25 °C	t_d	- -		1,0	µs
Circuit-commutated turn off-time, I_T = 160 A, di_T/dt = - 5 A/µs, $V_R \geq 100$ V, $V_D = 0,67V_{DRM}$, (dV_D/dt) = 50 V/µs, T_{Vj} = 125 °C	t_q	- -		150	
Recovery charge, di_T/dt = - 5 A/µs, T_{Vj} = 125 °C, I_T = 160 A, $V_R \geq 100$ V	Q_{rr}	- -		300	µAs
Holding current, V_D =12 V, T_{Vj} = 25 °C	I_H	- -		200	mA
Gate trigger voltage, V_D = 12 V, T_{Vj} = - 60 °C T_{Vj} = 25 °C T_{Vj} = 125 °C	V_{GT}	- -		4,5 2,5 2,0	V
Gate trigger current, V_D = 12 V, T_{Vj} = - 60 °C T_{Vj} = 25 °C T_{Vj} = 125 °C	I_{GT}	- -		350 200 150	mA
Gate non-trigger voltage, $V_D = 0,67V_{DRM}$, T_{Vj} = 125 °C	V_{GD}	0,25 -		-	V
Gate non-trigger current, $V_D = 0,67V_{DRM}$, T_{Vj} = 125 °C	I_{GD} 10		-	-	mA
Insulation test voltage (RMS), f = 50 Hz, t = 1sec/1min	V_{isol}	- -		3600/3000	V

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THERMAL PARAMETERS					
Thermal resistance junction to case, per thyristor (diode) per module	R_{thjc}	- -		0,170 0,085	°C/W
Thermal resistance case to heatsink, per thyristor (diode) per module	R_{thch} -		-	0,10 0,05	
MECHANICAL PARAMETERS					
Weight w		-	0,5	-	kg
Terminal connection torque	M_t	4 -		6	Nm
Heatsink mounting torque	M_s	4 -		6	Nm
Maximum acceleration (at nominal mounting force)	a -		-	50	m/s^2

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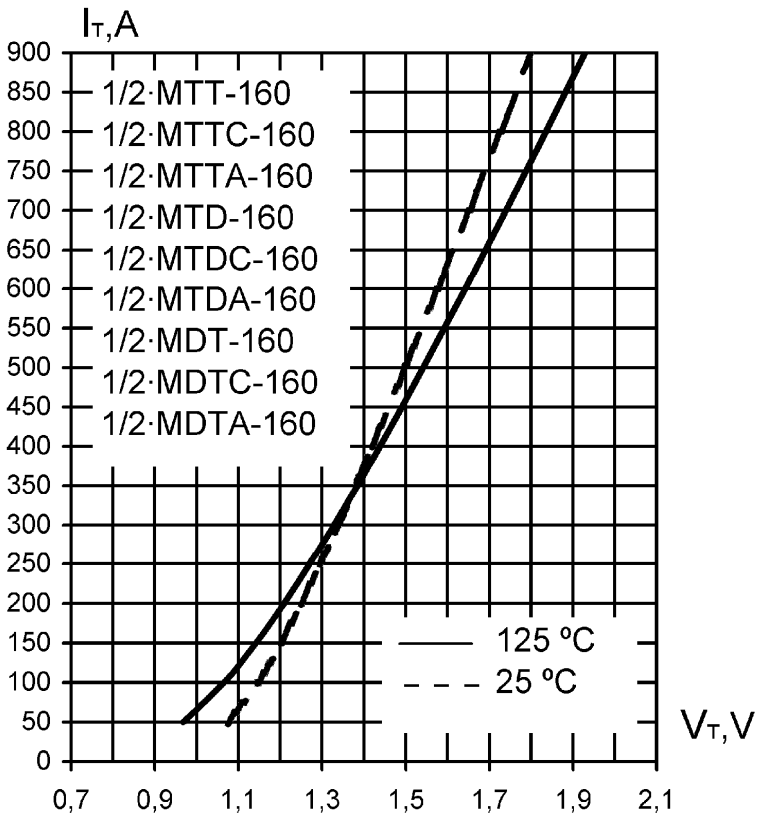

Fig. 1. Maximum on-state characteristics
(Limit device, 10 ms, half sine)

On-state characteristics model

$V_T = A + B \cdot I_T + C \cdot \ln(I_T + 1) + D \cdot \sqrt{I_T}$

Valid for I_T = 50 – 900 A

	T_{Vj} = 125 ºC	T_{Vj} = 25 ºC
A	0.638	0.802
B	0.0007763	0.0007297
C	0.065	0.067
D	0.00499	-0.003767

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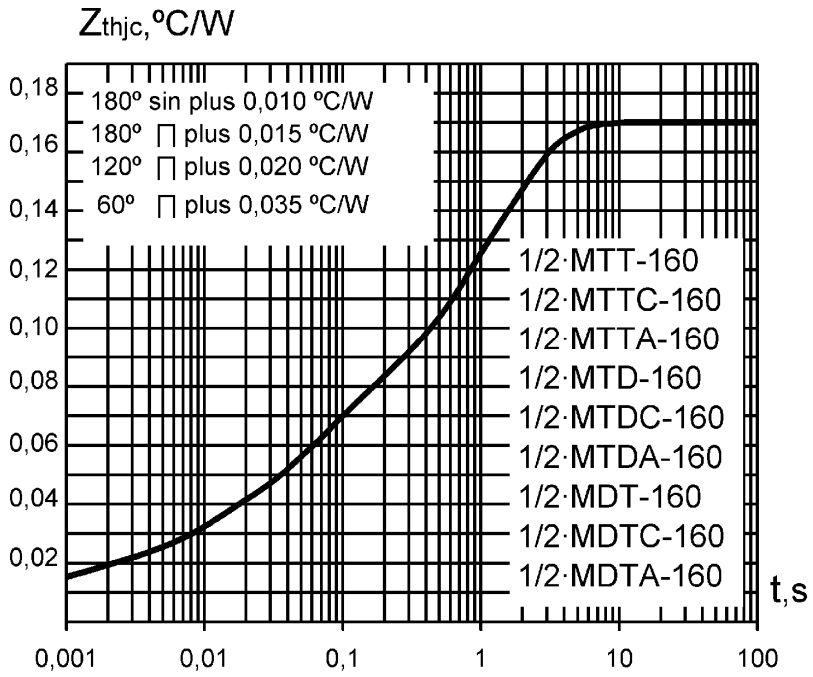

Fig. 2. Transient thermal impedance junction to case (DC)

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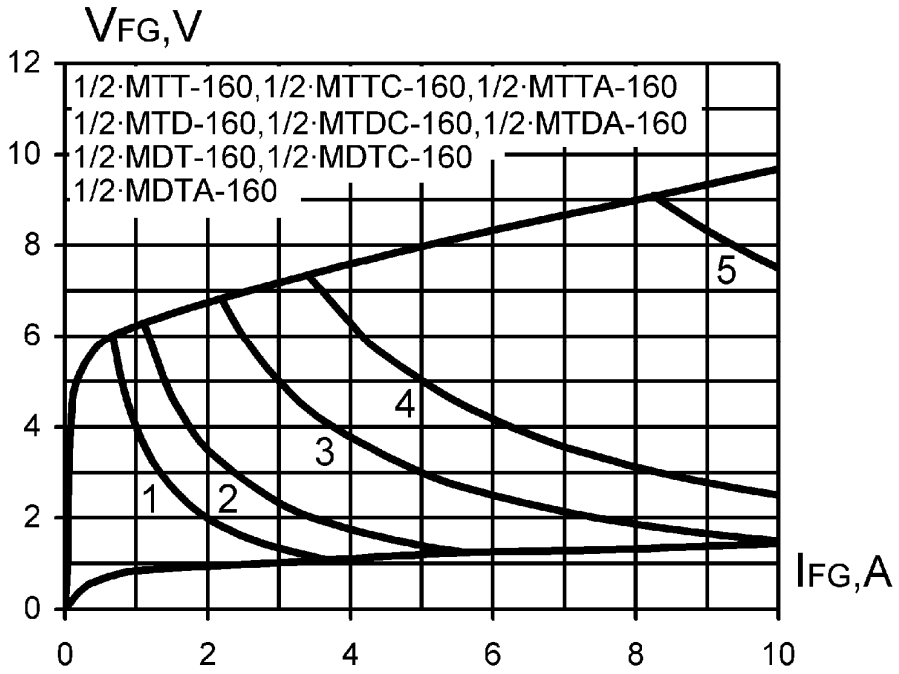

Fig. 3. Maximum peak gate power losses

Position at fig. 3	Duty cycle, $D = f \cdot t_p$	Gate pulse length, t_p, ms	Maximum gate pulse power P_{GM}, W
1 1		DC	4
2 2		10	7
3 20		1,0	15
4 40		0,5	25
5 200		0,1	75

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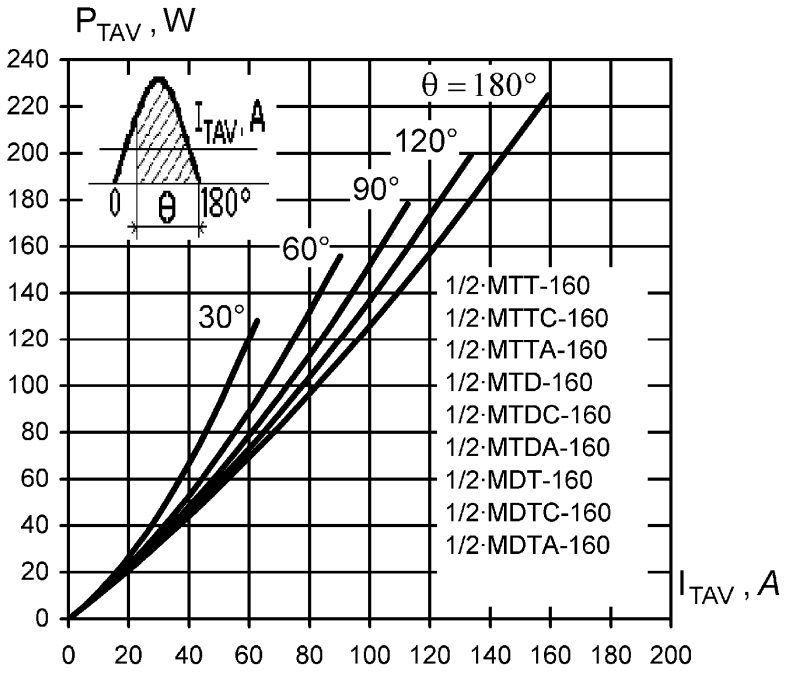

Fig. 4. On-state power loss vs. on-state current
(sine)

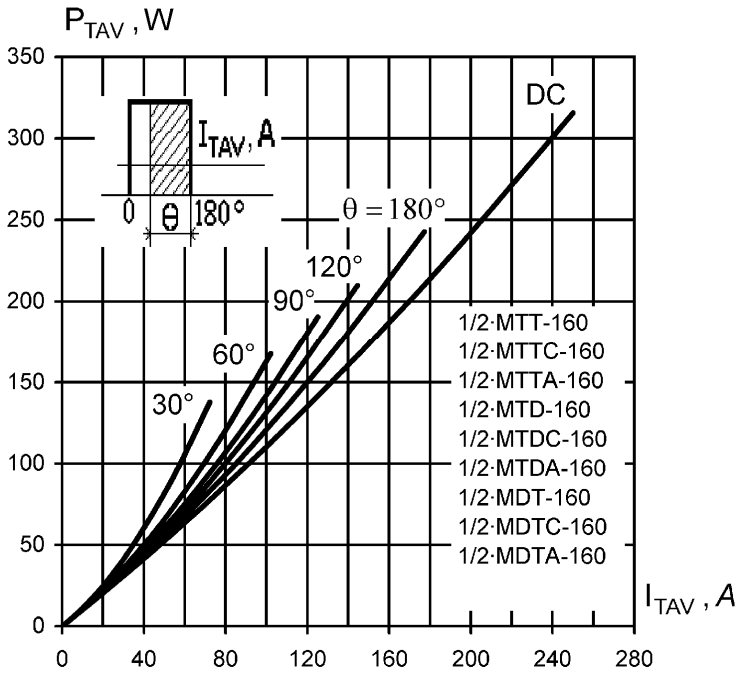

Fig. 5. On-state power loss vs. on-state current
(rectangular)

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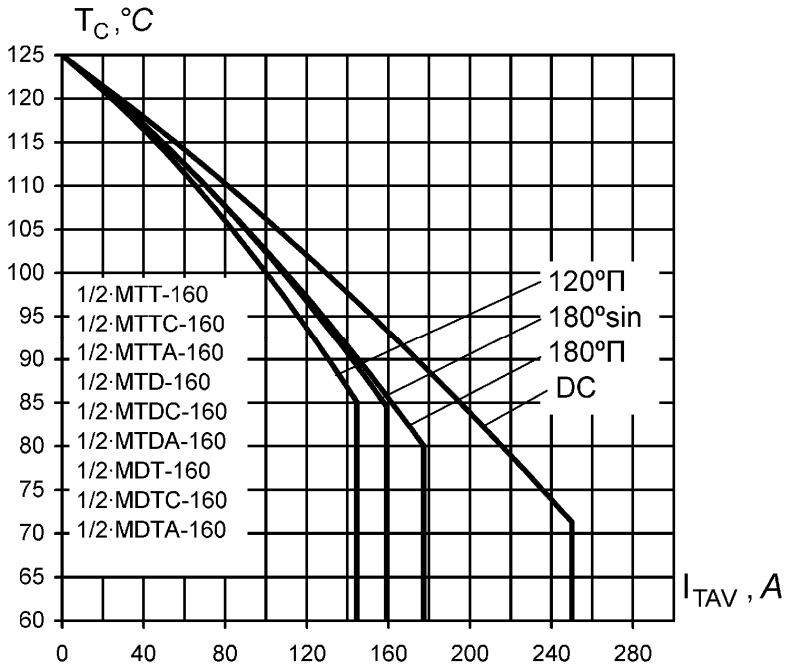

Fig. 6. Max. permissible case temperature vs. mean on-state current

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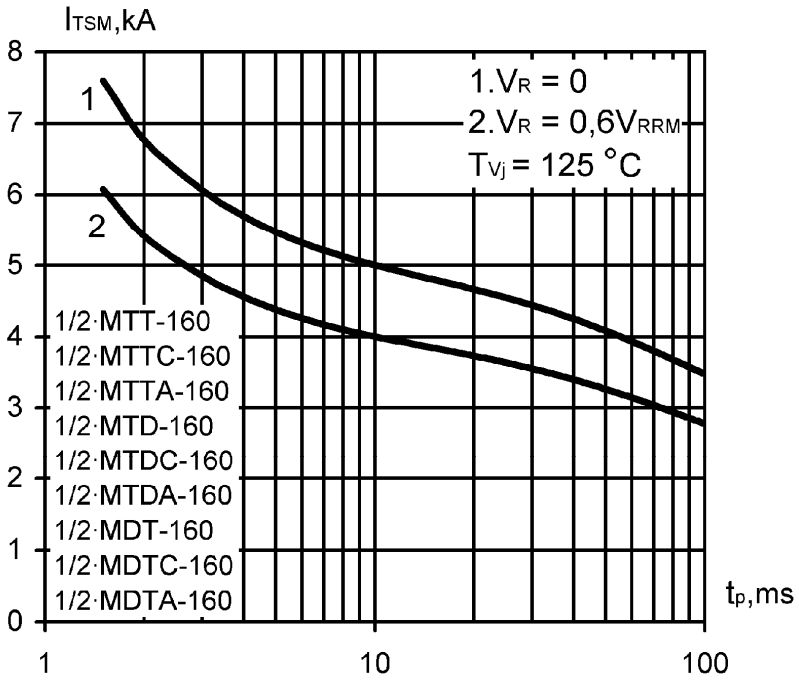

Fig. 7. Surge on-state current vs. pulse length
(half-sine)

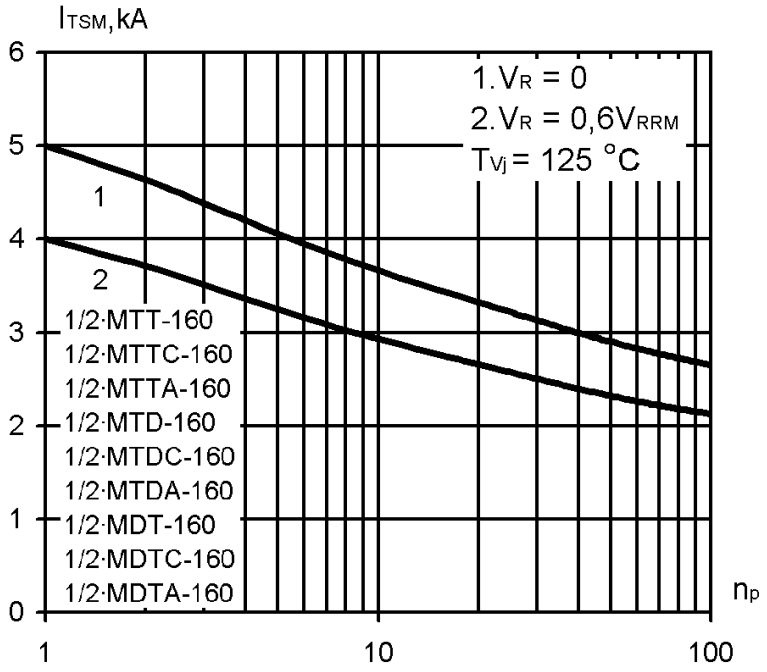

Fig. 8. Surge on-state current vs. number of pulses
(half-sine,10 ms, 50 Hz)

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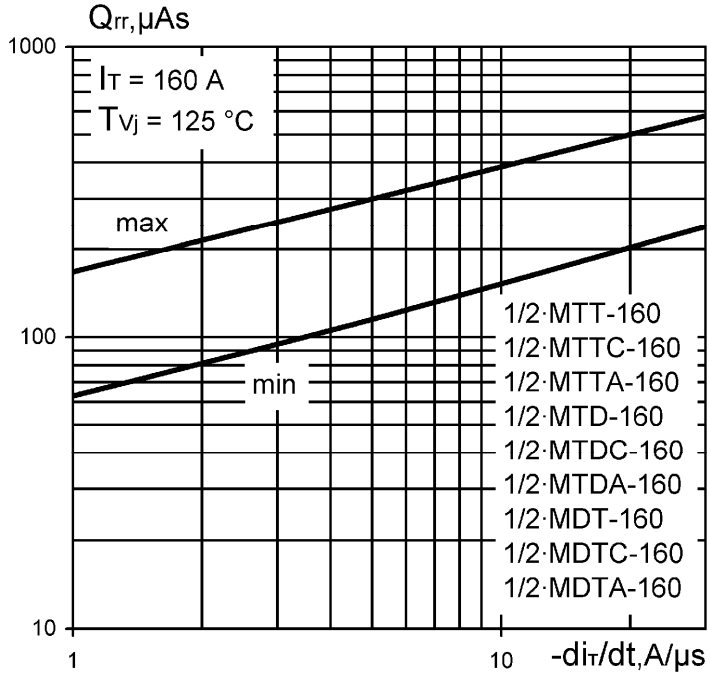

Fig. 9. Recovery charge vs. decay rate of on-state current

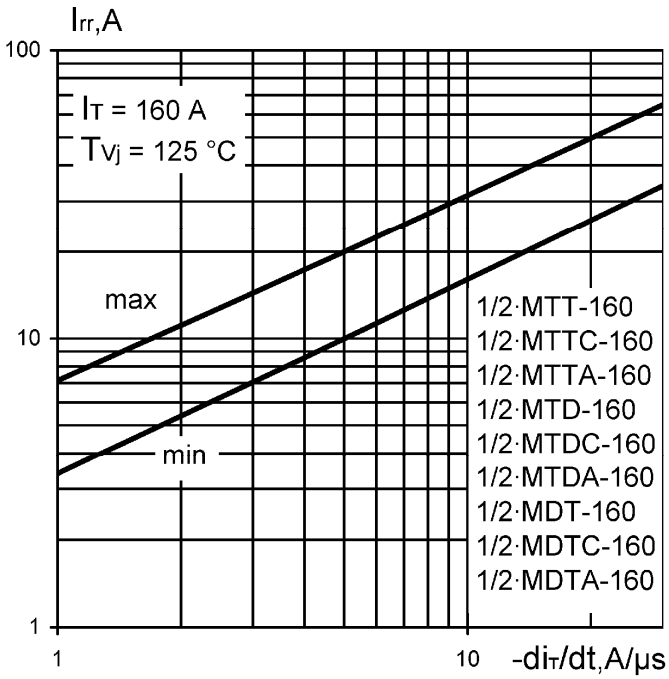

Fig. 10. Peak reverse recovery current vs. decay rate of on-state current

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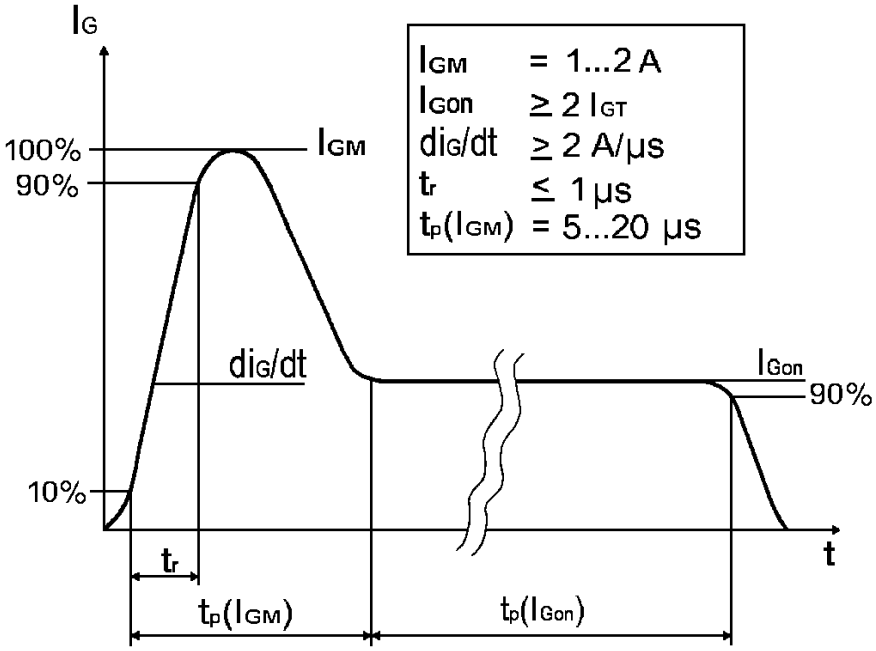

Fig. 11. Recommended gate current waveform

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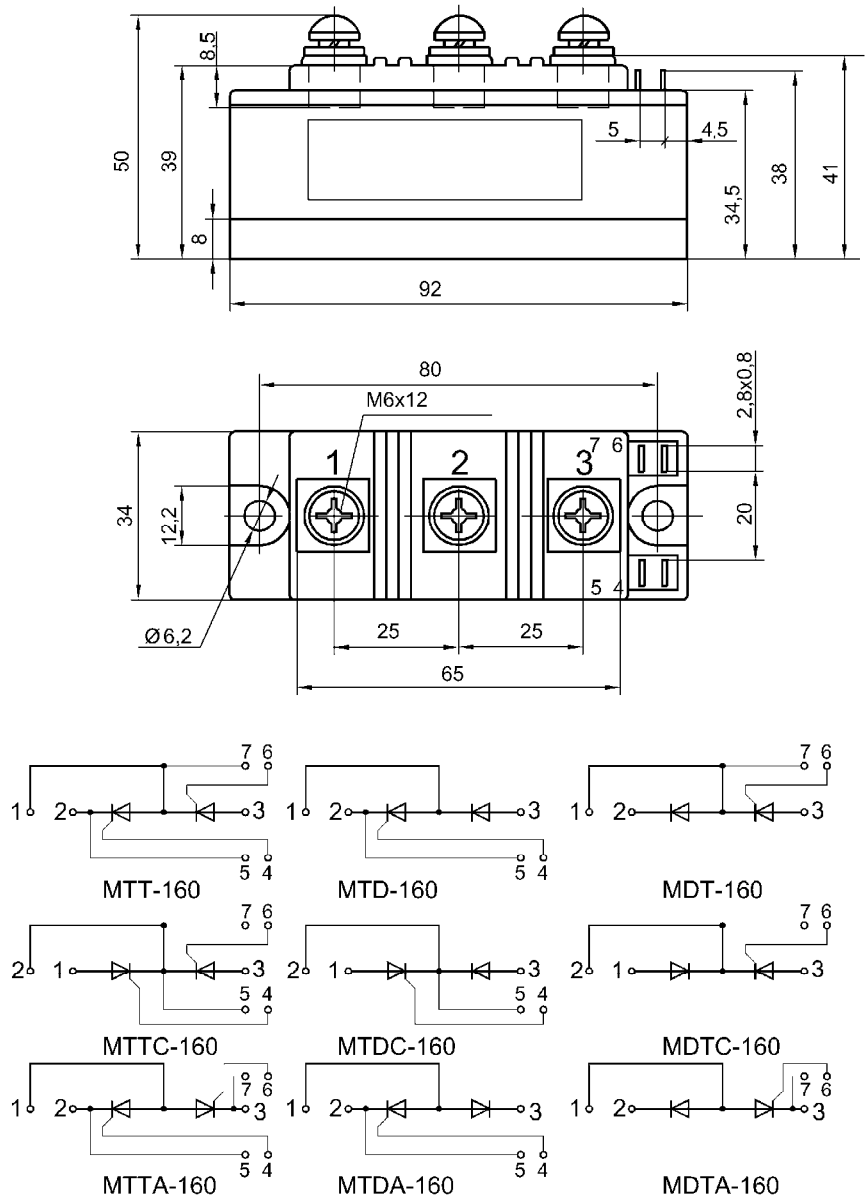

Fig. 12. Device Outline Drawing
(dimensions in mm)

JSC «ELECTROVIPRYAMITEL» reserves the right to change specification without notice.

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