

N-Channel Enhancement Mode Power MOSFET

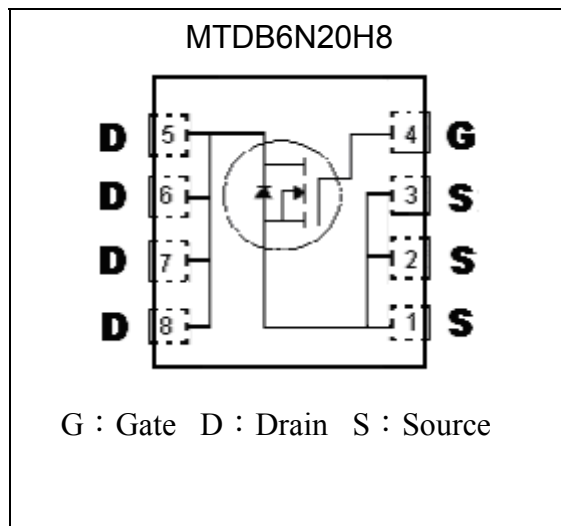
MTDB6N20H8

BV_{DSS}	200 V
$I_D@V_{GS}=10V, T_C=25^{\circ}C$	8 A
$I_D@V_{GS}=10V, T_A=25^{\circ}C$	1.8A
$R_{DS(on)(typ)}@V_{GS}=10V, I_D=3A$	285 m Ω
$R_{DS(on)(typ)}@V_{GS}=4.5V, I_D=2A$	287 m Ω

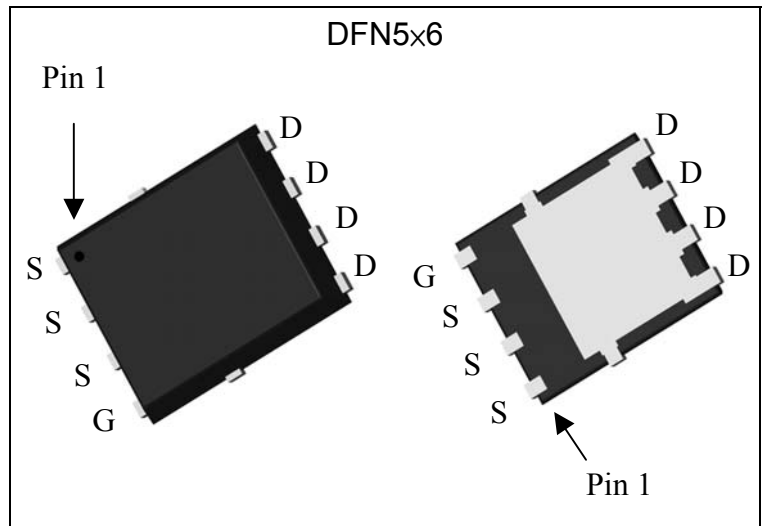
Features

- Single Drive Requirement
- Low On-resistance
- Fast Switching Characteristic
- Pb-free lead plating and Halogen-free package

Symbol

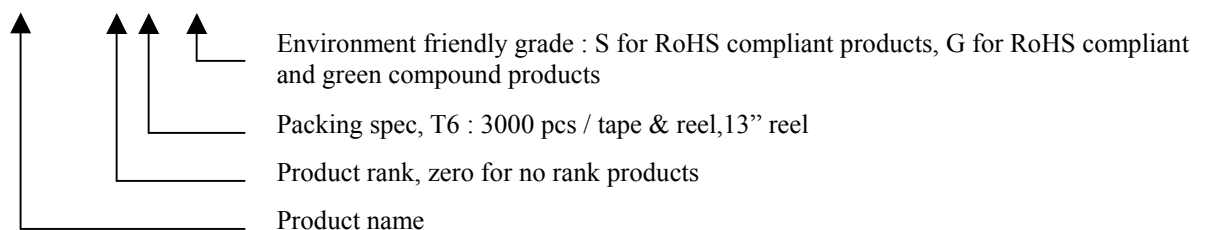


Outline



Ordering Information

Device	Package	Shipping
MTDB6N20H8-0-T6-G	DFN5x6 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel



**Absolute Maximum Ratings** (Ta=25°C)

Parameter		Symbol	Limits	Unit
Drain-Source Voltage		V _{DS}	200	V
Gate-Source Voltage		V _{GS}	±20	
Continuous Drain Current @ T _C =25°C, V _{GS} =10V		I _D	8	A
Continuous Drain Current @ T _C =100°C, V _{GS} =10V			5.1	
Continuous Drain Current @ T _A =25°C, V _{GS} =10V		I _{DSM}	1.8 *3	
Continuous Drain Current @ T _A =70°C, V _{GS} =10V			1.4 *3	
Pulsed Drain Current		I _{DM}	24 *1	
Avalanche Current		I _{AS}	4	mJ
Avalanche Energy @ L=5mH, I _D =3A, V _{DD} =50V		E _{AS}	22.5 *4	
Repetitive Avalanche Energy @ L=0.05mH		E _{AR}	5 *2	
Total Power Dissipation	T _C =25°C	P _D	50	W
	T _C =100°C		20	
	T _A =25°C	P _{DSM}	2.5	
	T _A =70°C		1.6	
Operating Junction and Storage Temperature Range		T _j , T _{stg}	-55~+150	°C

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	R _{θJC}	2.5	°C/W
Thermal Resistance, Junction-to-ambient, max	R _{θJA}	50 *3	

- Note : 1. Pulse width limited by maximum junction temperature
2. Duty cycle ≤ 1%
3. Surface mounted on 1 in² copper pad of FR-4 board, 125°C/W when mounted on minimum copper pad
4. 100% tested by conditions of L=1mH, I_{AS}=3A, V_{GS}=10V, V_{DD}=50V

Characteristics (T_C=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	200	-	-	V	V _{GS} =0V, I _D =250μA
V _{GS(th)}	1.2	-	2.4		V _{DS} = V _{GS} , I _D =250μA
G _F S *1	-	6.6	-	S	V _{DS} =15V, I _D =3A
I _{GSS}	-	-	±100	nA	V _{GS} =±20V
I _{DSS}	-	-	1	μA	V _{DS} =200V, V _{GS} =0V
	-	-	10		V _{DS} =160V, V _{GS} =0V, T _j =85°C
R _{DS(ON)} *1	-	285	360	mΩ	V _{GS} =10V, I _D =3A
	-	287	400		V _{GS} =4.5V, I _D =2A
Dynamic					
C _{iss}	-	498	-	pF	V _{GS} =0V, V _{DS} =25V, f=1MHz
C _{oss}	-	41	-		
C _{rss}	-	26	-		

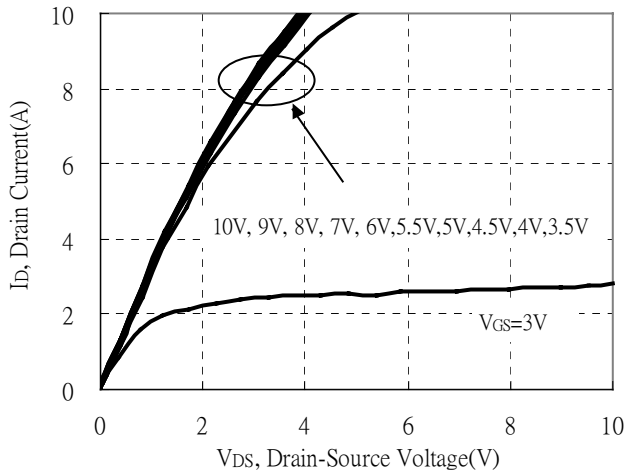


Qg *1, 2	-	14.3	-	nC	V _{DS} =160V, V _{GS} =10V, I _D =3A
Qgs *1, 2	-	1.9	-		
Qgd *1, 2	-	4.3	-		
t _{d(ON)} *1, 2	-	7.6	-	ns	V _{DS} =100V, I _D =3A, V _{GS} =10V, R _{GS} =1 Ω
tr *1, 2	-	17	-		
t _{d(OFF)} *1, 2	-	27.4	-		
t _f *1, 2	-	17.8	-		
R _g	-	3.9	-	Ω	f=1MHz
Source-Drain Diode					
I _S *1	-	-	8	A	
I _{SM} *3	-	-	18		
V _{SD} *1	-	0.78	1.2	V	I _S =2A, V _{GS} =0V
trr	-	51.5	-	ns	I _F =2A, dI _F /dt=100A/μs
Qrr	-	88.8	-	nC	

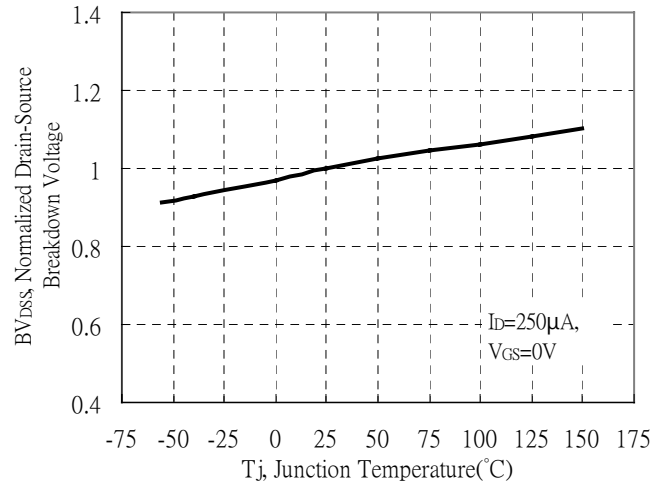
Note : *1.Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%
 *2.Independent of operating temperature
 *3.Pulse width limited by maximum junction temperature.

Typical Characteristics

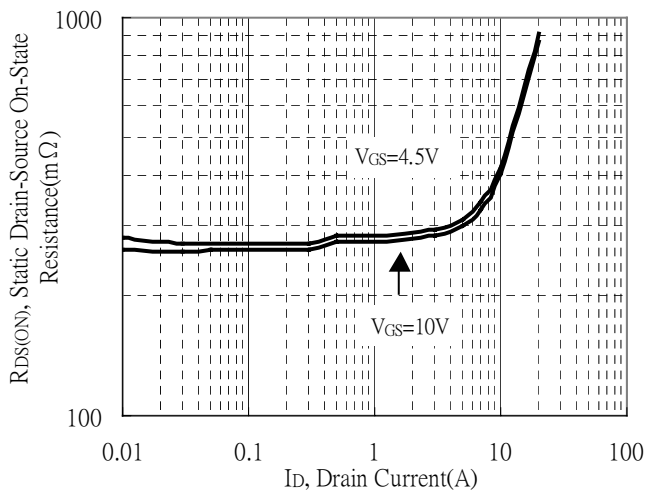
Typical Output Characteristics



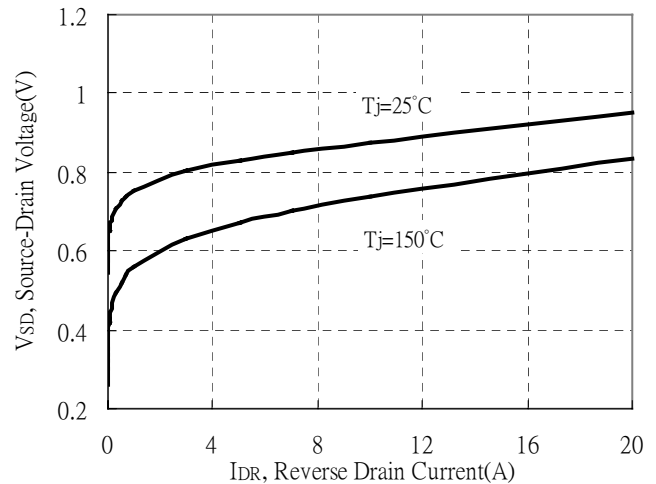
Breakdown Voltage vs Ambient Temperature



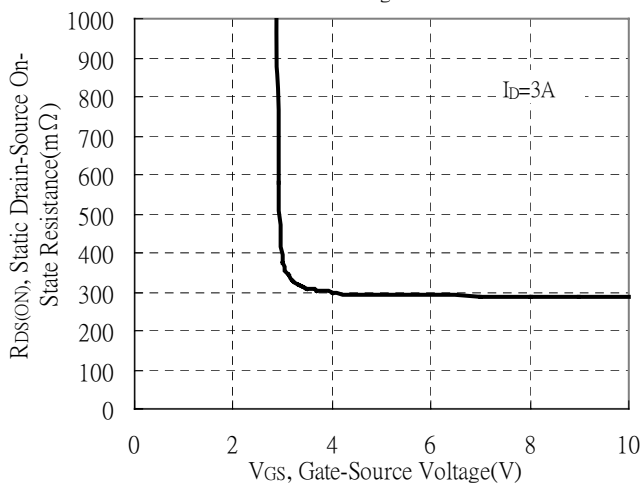
Static Drain-Source On-State resistance vs Drain Current



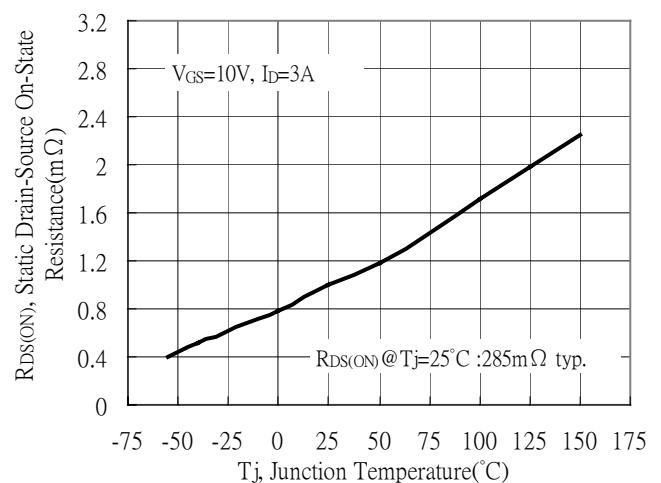
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

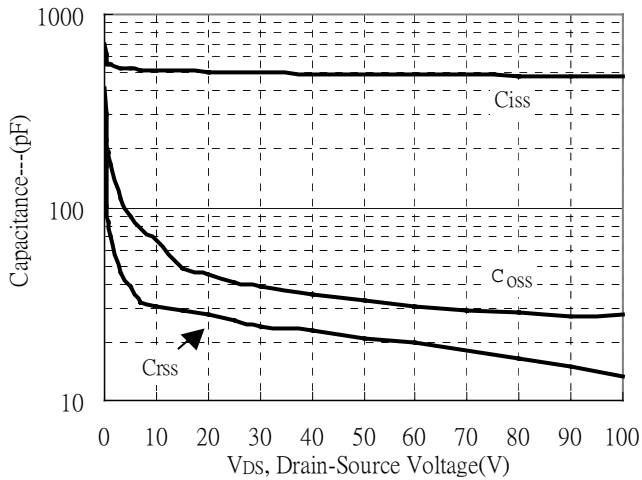


Drain-Source On-State Resistance vs Junction Temperature

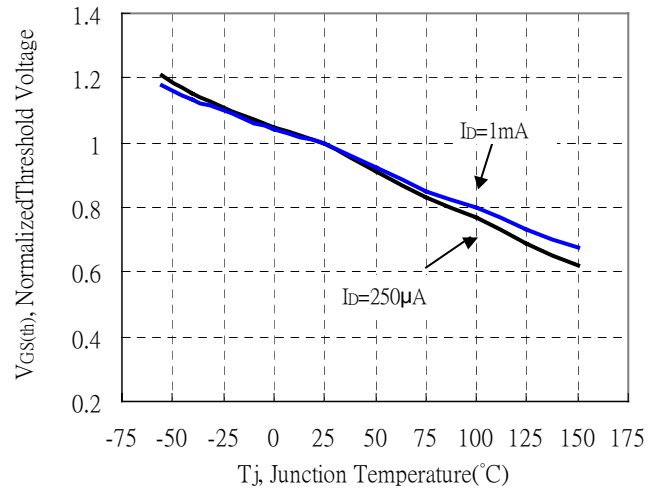


Typical Characteristics(Cont.)

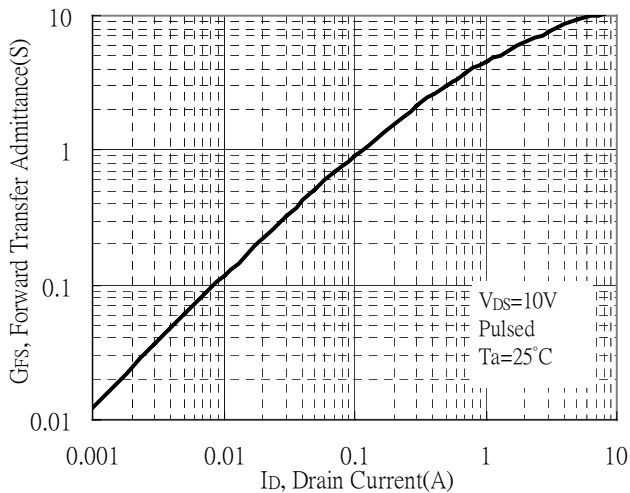
Capacitance vs Drain-to-Source Voltage



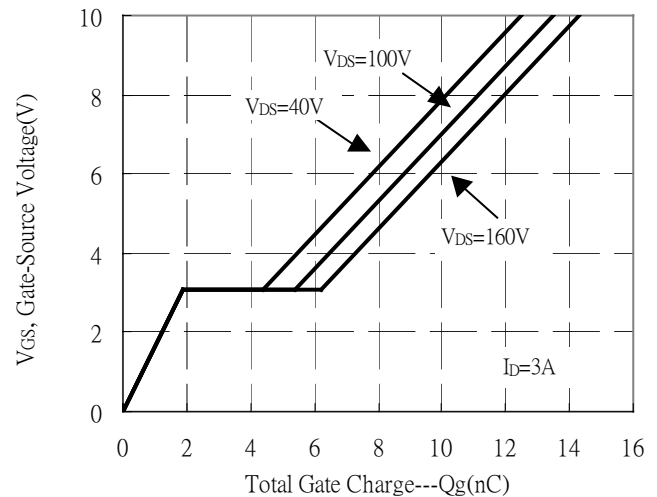
Threshold Voltage vs Junction Temperature



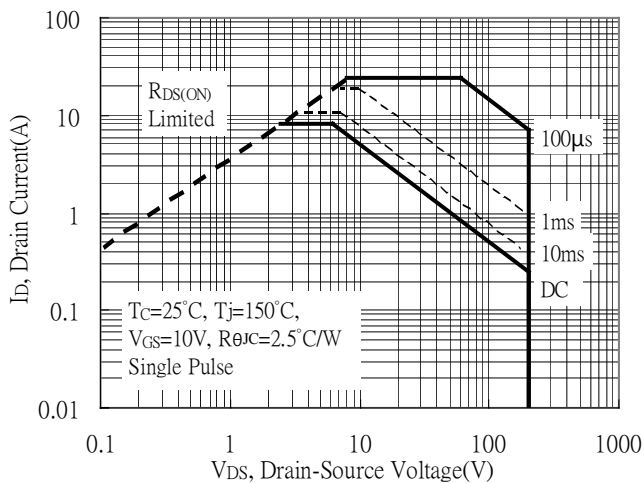
Forward Transfer Admittance vs Drain Current



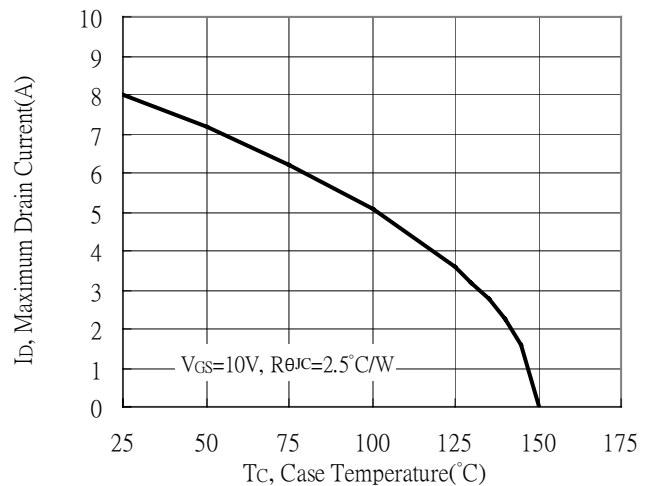
Gate Charge Characteristics



Maximum Safe Operating Area

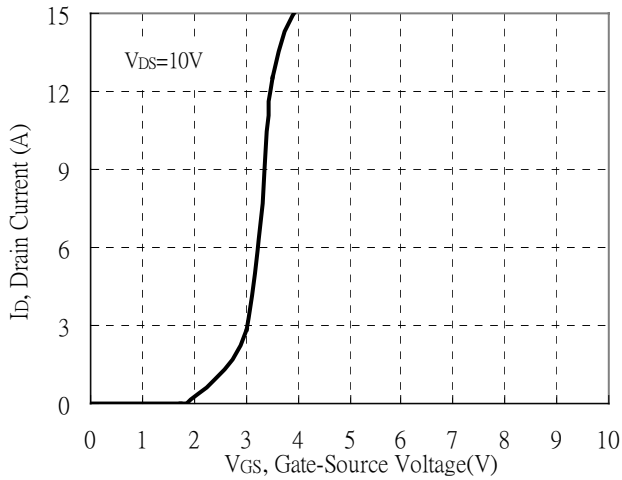


Maximum Drain Current vs Case Temperature

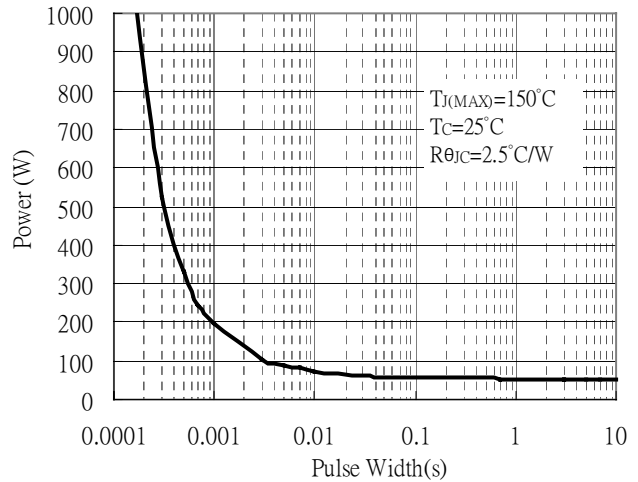


Typical Characteristics(Cont.)

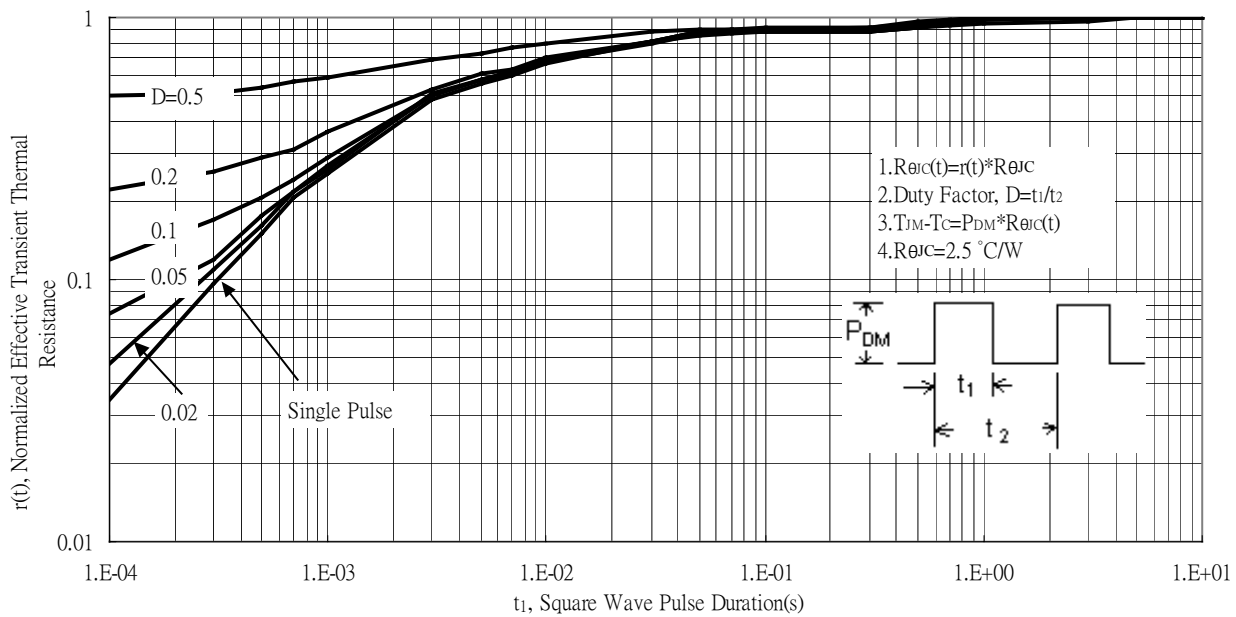
Typical Transfer Characteristics



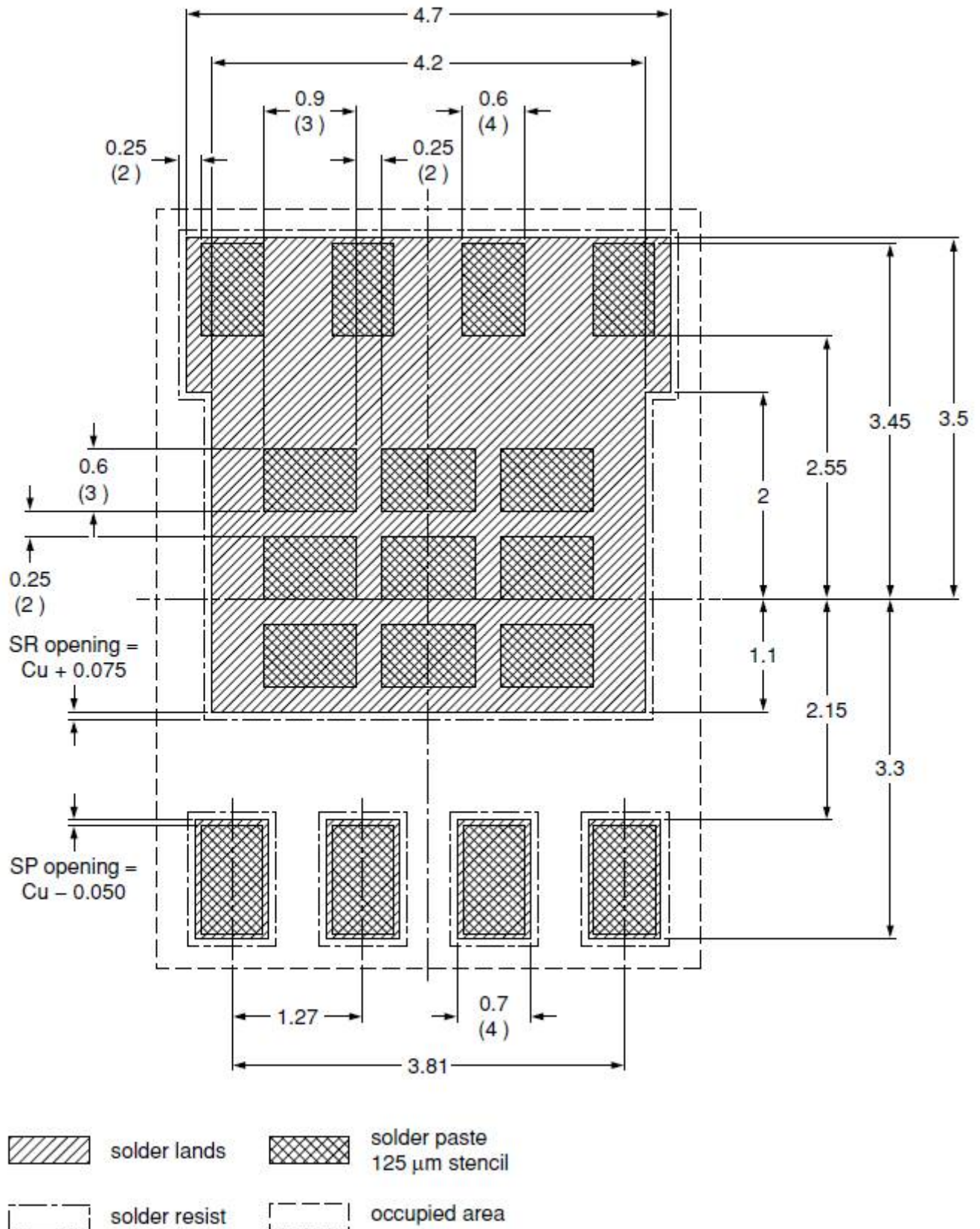
Single Pulse Maximum Power Dissipation



Transient Thermal Response Curves

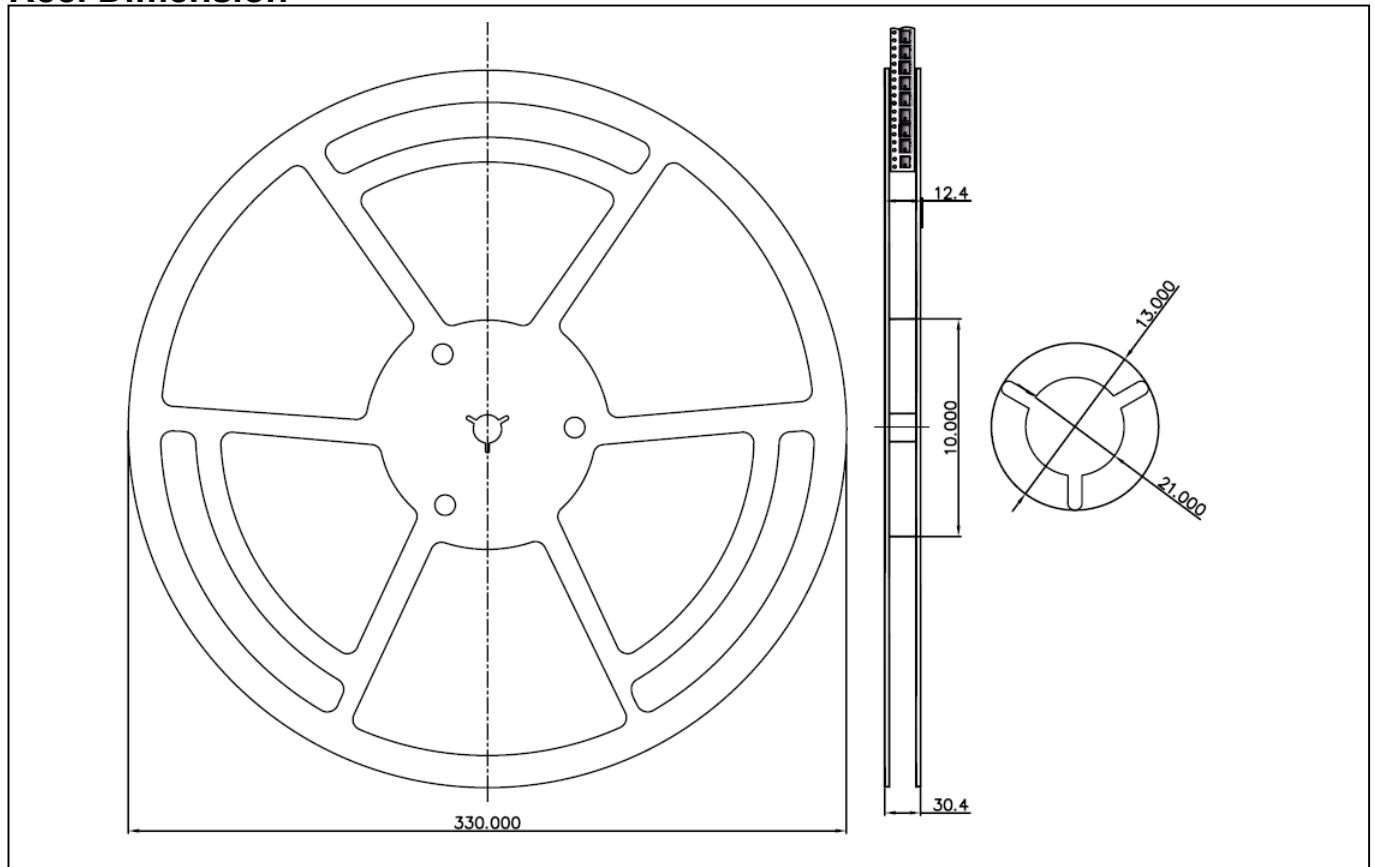


Recommended Soldering Footprint & Stencil Design

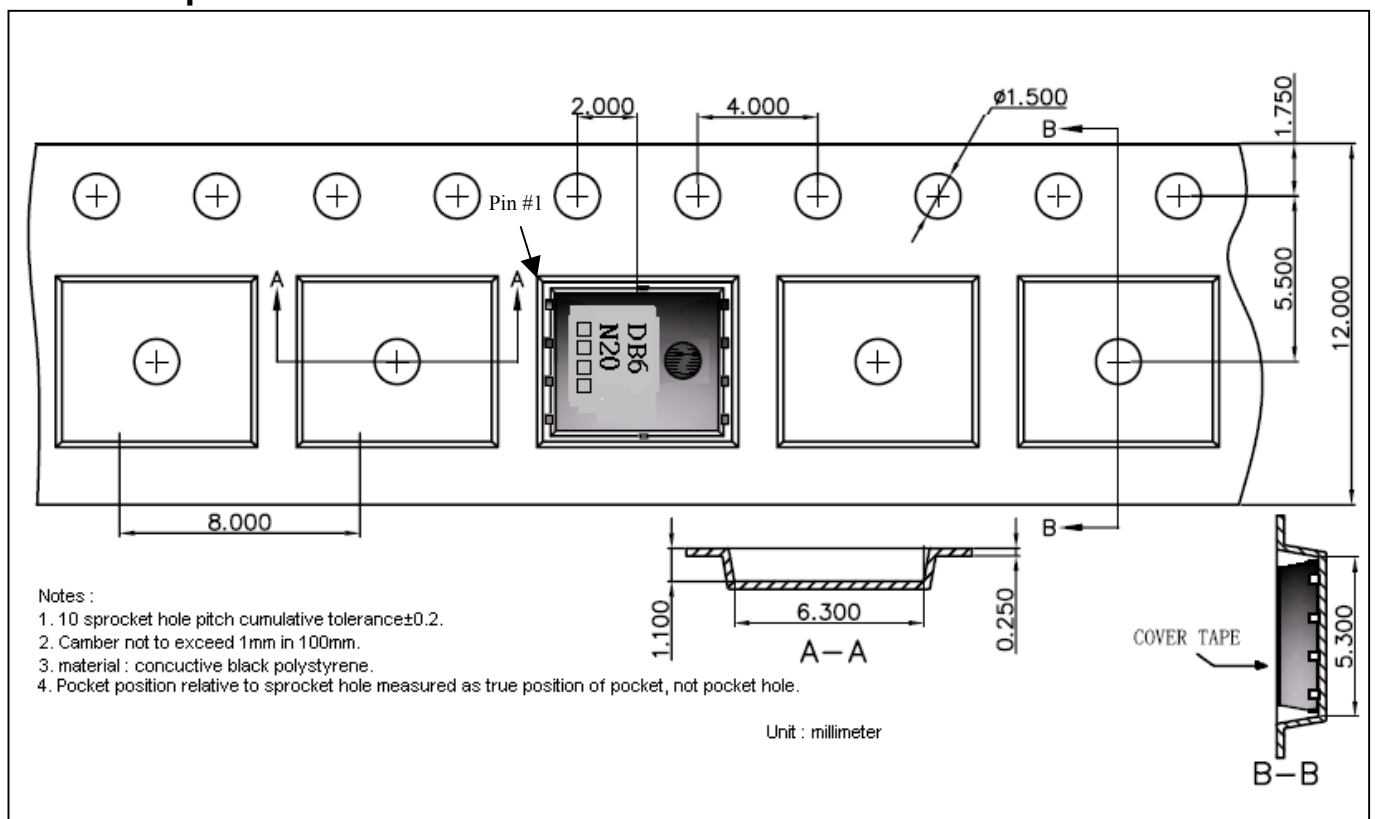


unit : mm

Reel Dimension



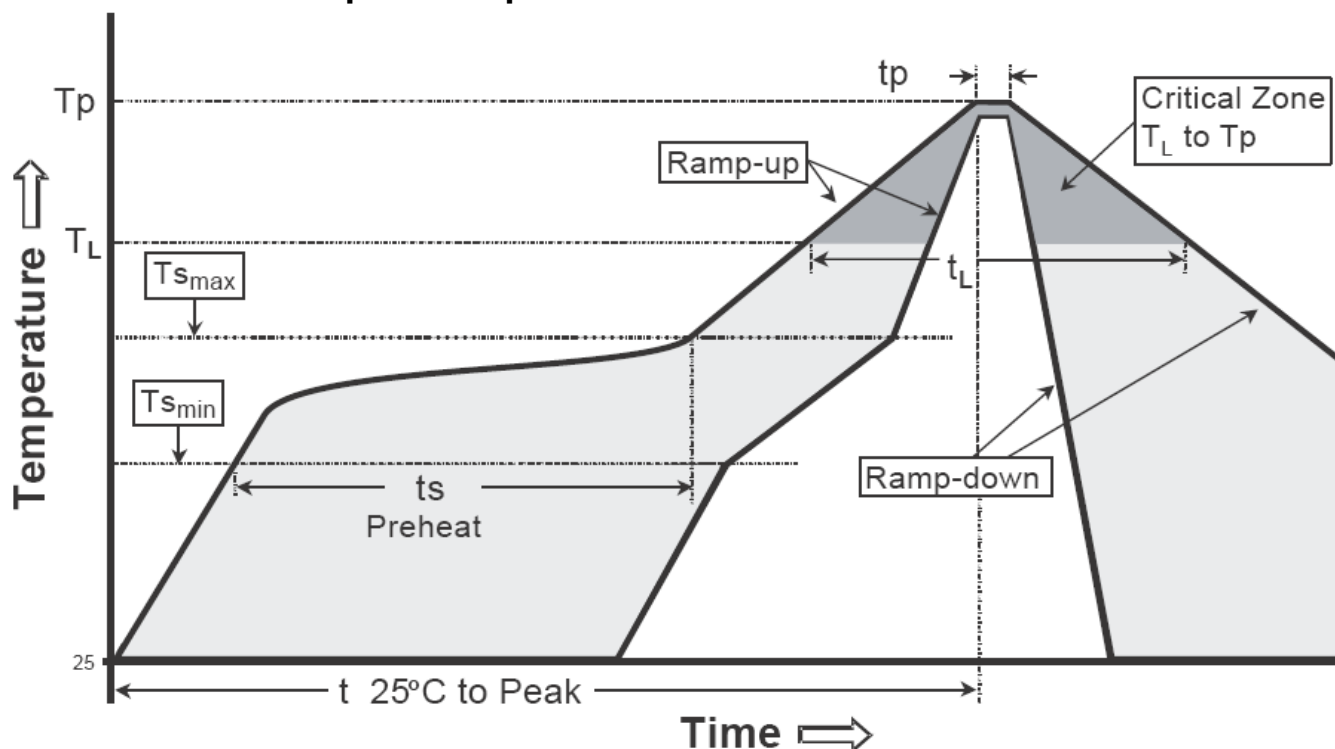
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

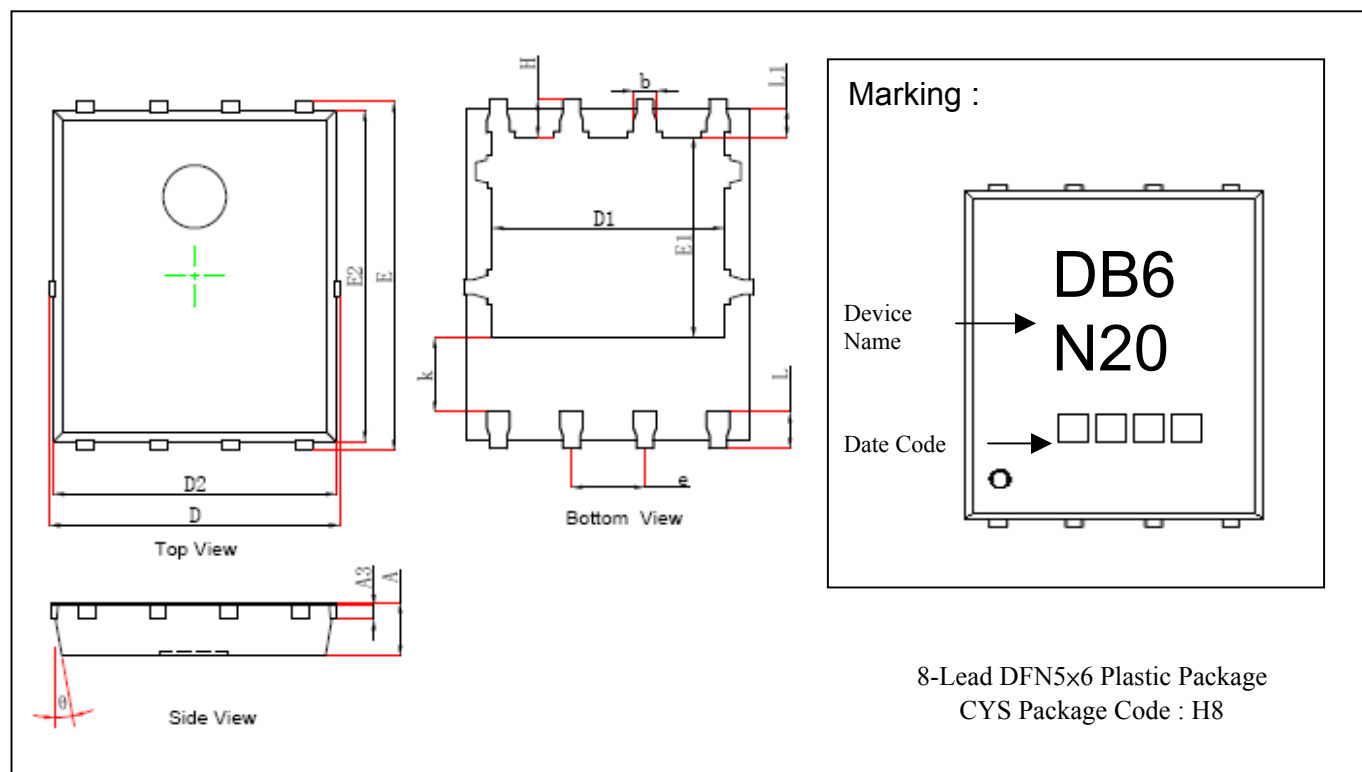
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T_{smax} to T_p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T_{smin})	100°C	150°C
-Temperature Max(T_{smax})	150°C	200°C
-Time(t_{smin} to t_{smax})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T_L)	183°C	217°C
- Time (t_L)	60-150 seconds	60-150 seconds
Peak Temperature(T_p)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(t_p)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

DFN5x6 Dimension



DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039	k	1.190	1.390	0.047	0.055
A3	0.254	REF	0.010	REF	b	0.350	0.450	0.014	0.018
D	4.944	5.096	0.195	0.201	e	1.270	TYP.	0.050	TYP.
E	5.974	6.126	0.235	0.241	L	0.559	0.711	0.022	0.028
D1	3.910	4.110	0.154	0.162	L1	0.424	0.576	0.017	0.023
E1	3.375	3.575	0.133	0.141	H	0.574	0.726	0.023	0.029
D2	4.824	4.976	0.190	0.196	θ	10°	12°	10°	12°
E2	5.674	5.826	0.223	0.229					

Notes: 1. Controlling dimension: millimeters.

2. Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.

3. If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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