

**N-Channel Enhancement Mode Power MOSFET**

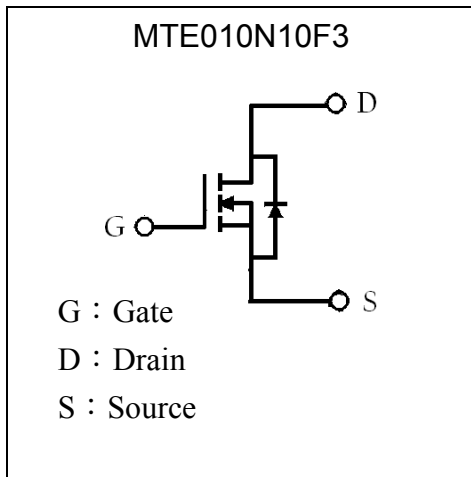
# MTE010N10F3

BV <sub>DSS</sub>	100V
I <sub>D</sub> @ T <sub>C</sub> =25°C, V <sub>GS</sub> =10V (silicon limit)	70A
R <sub>DS(on)(TYP)</sub> @ V <sub>GS</sub> =10V, I <sub>D</sub> =50A	9.6mΩ
R <sub>DS(on)(TYP)</sub> @ V <sub>GS</sub> =7V, I <sub>D</sub> =20A	10.1mΩ

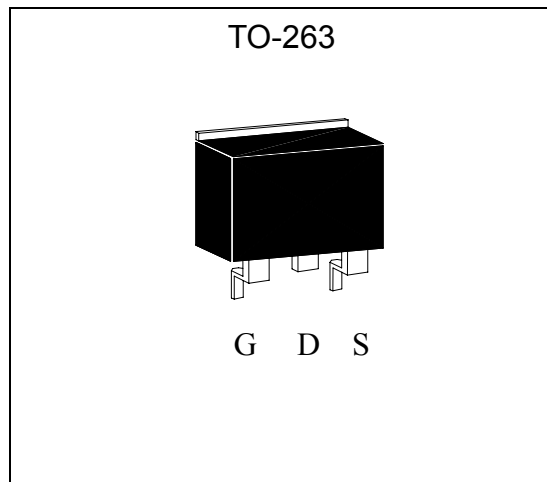
**Features**

- Low Gate Charge
- Simple Drive Requirement
- Repetitive Avalanche Rated
- Fast Switching Characteristic
- RoHS compliant package

**Symbol**

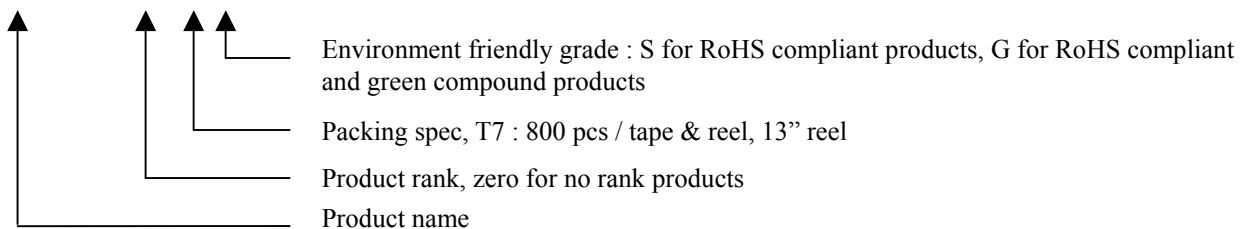


**Outline**



**Ordering Information**

Device	Package	Shipping
MTE010N10F3-0-T7-X	TO-263 (Pb-free lead plating and RoHS compliant package)	800 pcs / Tape & Reel



**Absolute Maximum Ratings** ( $T_C=25^\circ\text{C}$ , unless otherwise noted)

Parameter	Symbol	Limits	Unit	
Drain-Source Voltage	$V_{DS}$	100	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$		
Continuous Drain Current @ $T_C=25^\circ\text{C}$ , $V_{GS}=10\text{V}$ (silicon limit)	$I_D$	70	A	
Continuous Drain Current @ $T_C=100^\circ\text{C}$ , $V_{GS}=10\text{V}$ (silicon limit)		50		
Continuous Drain Current @ $T_C=25^\circ\text{C}$ , $V_{GS}=10\text{V}$ (package limit) (Note 1)		60		
Pulsed Drain Current (Note 3)	$I_{DM}$	300		
Continuous Drain Current @ $T_A=25^\circ\text{C}$ (Note 2)	$I_{DSM}$	8		
Continuous Drain Current @ $T_A=70^\circ\text{C}$ (Note 2)		6.5		
Avalanche Current (Note 3)	$I_{AS}$	80		
Avalanche Energy @ $L=100\mu\text{H}$ , $I_D=80\text{A}$ , $R_G=25\Omega$ (Note 2)	$E_{AS}$	320	mJ	
Repetitive Avalanche Energy @ $L=0.1\text{mH}$ (Note 3)	$E_{AR}$	15		
Power Dissipation	$T_C=25^\circ\text{C}$ (Note 1)	$P_D$	150	W
	$T_C=100^\circ\text{C}$ (Note 1)		75	
Power Dissipation	$T_A=25^\circ\text{C}$ (Note 2)	$P_{DSM}$	2	W
	$T_A=70^\circ\text{C}$ (Note 2)		1.3	
Operating Junction and Storage Temperature	$T_j, T_{stg}$	-55~+175	$^\circ\text{C}$	

**Thermal Data**

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{th,j-c}$	1	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-ambient, max, $t \leq 10\text{s}$ (Note 1)	$R_{th,j-a}$	15	
Thermal Resistance, Junction-to-ambient, max (Note 1)		62.5	

- Note : 1. The power dissipation  $P_D$  is based on  $T_{J(MAX)}=175^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
2. The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2 oz. copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The power dissipation  $P_{DSM}$  is based on  $R_{\theta JA}$  and the maximum allowed junction temperature of  $150^\circ\text{C}$ . The value in any given application depends on the user's specific board design, and the maximum temperature of  $175^\circ\text{C}$  may be used if the PCB allows it.
3. Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=175^\circ\text{C}$ . Ratings are based on low frequency and low duty cycles to keep initial  $T_J=25^\circ\text{C}$ .
4. The maximum current limited by package is 60A.
5. The static characteristics are obtained using  $<300\mu\text{s}$  pulses, duty cycle 0.5% maximum.
6. The  $R_{\theta JA}$  is the sum of thermal resistance from junction to case  $R_{\theta JC}$  and case to ambient.



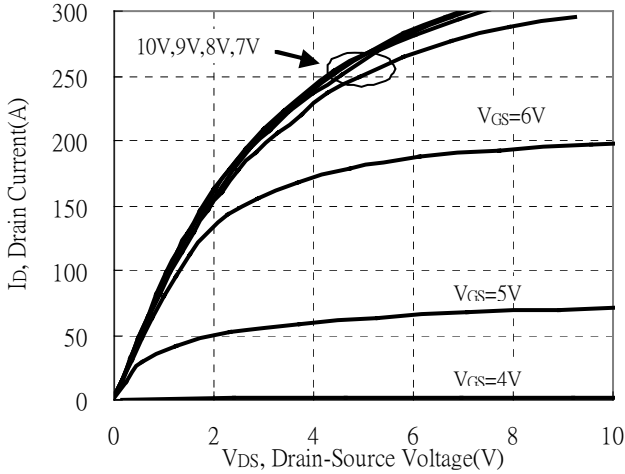
**Characteristics (Tc=25°C, unless otherwise specified)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
<b>Static</b>					
BV <sub>DSS</sub>	100	-	-	V	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA
V <sub>GS(th)</sub>	2.0	2.9	4.0		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA
G <sub>FS</sub>	-	41	-	S	V <sub>DS</sub> =5V, I <sub>D</sub> =20A
I <sub>GSS</sub>	-	-	±100	nA	V <sub>GS</sub> =±20V
I <sub>DSS</sub>	-	-	1	μA	V <sub>DS</sub> =80V, V <sub>GS</sub> =0V
	-	-	25		V <sub>DS</sub> =80V, V <sub>GS</sub> =0V, T <sub>j</sub> =55°C
*R <sub>DS(ON)</sub>	-	9.6	13.5	mΩ	V <sub>GS</sub> =10V, I <sub>D</sub> =50A
	-	10.1	15.8		V <sub>GS</sub> =7V, I <sub>D</sub> =20A
<b>Dynamic</b>					
*Q <sub>g</sub>	-	48	-	nC	I <sub>D</sub> =20A, V <sub>DS</sub> =50V, V <sub>GS</sub> =10V
*Q <sub>gs</sub>	-	20	-		
*Q <sub>gd</sub>	-	10	-		
*t <sub>d(ON)</sub>	-	19	-	ns	V <sub>DS</sub> =50V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V, R <sub>G</sub> =3Ω
*t <sub>r</sub>	-	12	-		
*t <sub>d(OFF)</sub>	-	35	-		
*t <sub>f</sub>	-	11	-		
C <sub>iss</sub>	-	3753	-	pF	V <sub>GS</sub> =0V, V <sub>DS</sub> =30V, f=1MHz
C <sub>oss</sub>	-	250	-		
C <sub>rss</sub>	-	65	-		
<b>Source-Drain Diode</b>					
*I <sub>S</sub>	-	-	70	A	
*V <sub>SD</sub>	-	0.89	1.2	V	I <sub>S</sub> =50A, V <sub>GS</sub> =0V
*t <sub>rr</sub>	-	90	-	ns	I <sub>F</sub> =20A, V <sub>GS</sub> =0V, dI <sub>F</sub> /dt=100A/μs
*Q <sub>rr</sub>	-	135	-	nC	

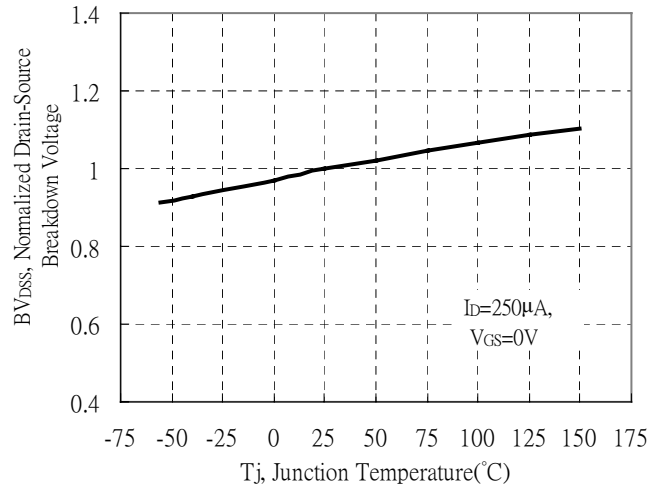
\*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

## Typical Characteristics

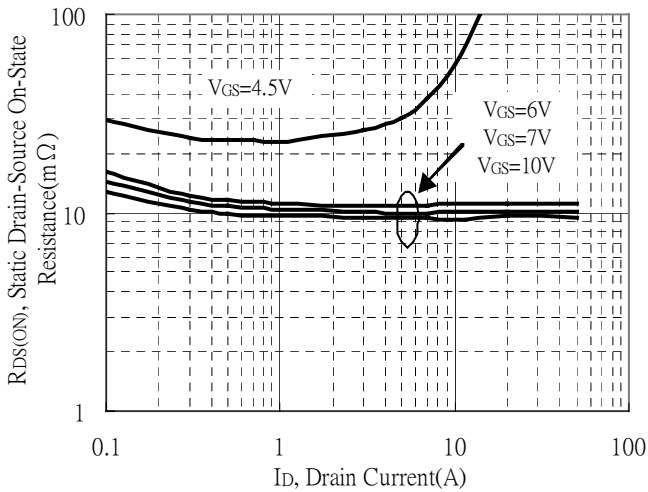
Typical Output Characteristics



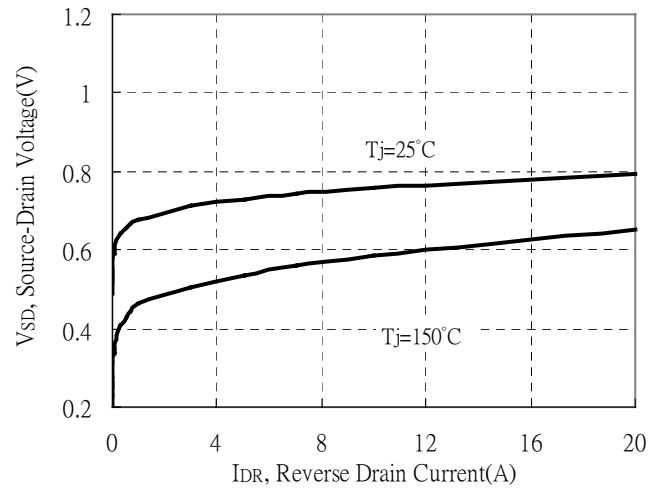
Brekdown Voltage vs Junction Temperature



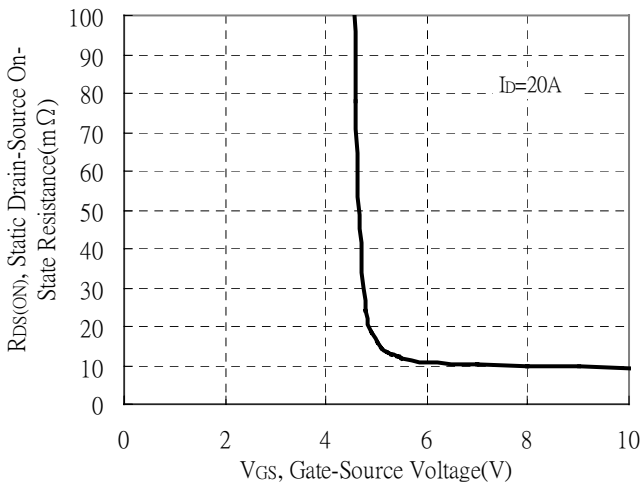
Static Drain-Source On-State resistance vs Drain Current



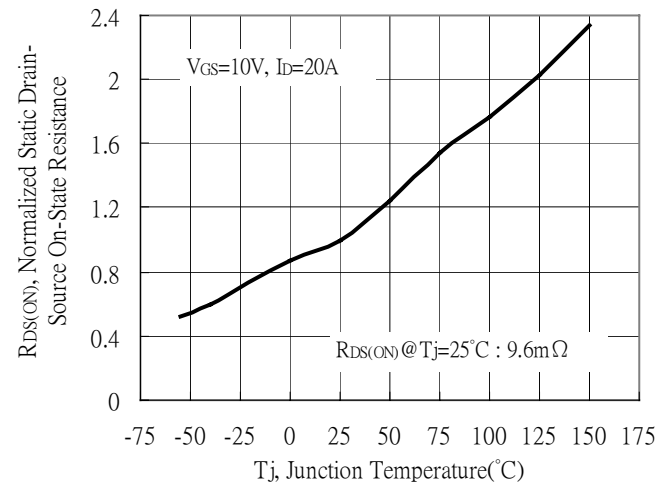
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

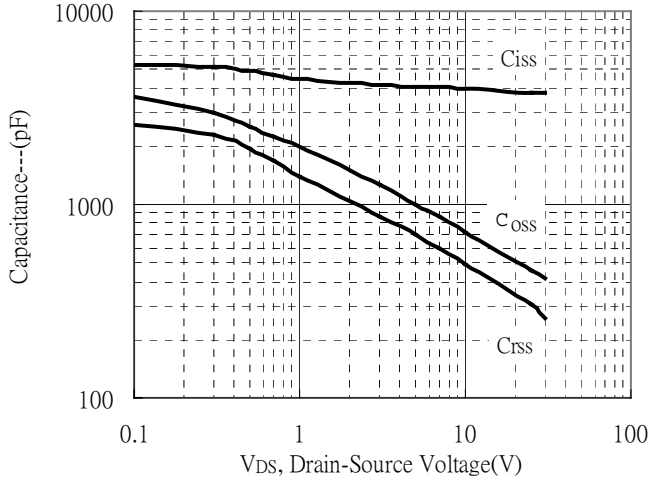


Drain-Source On-State Resistance vs Junction Temperature

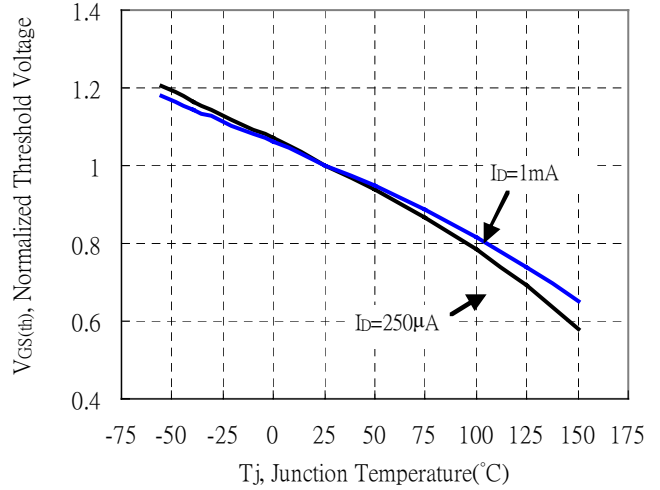


**Typical Characteristics(Cont.)**

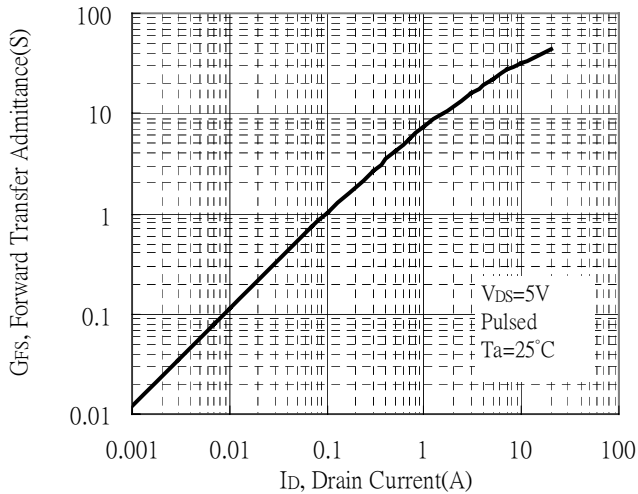
Capacitance vs Drain-to-Source Voltage



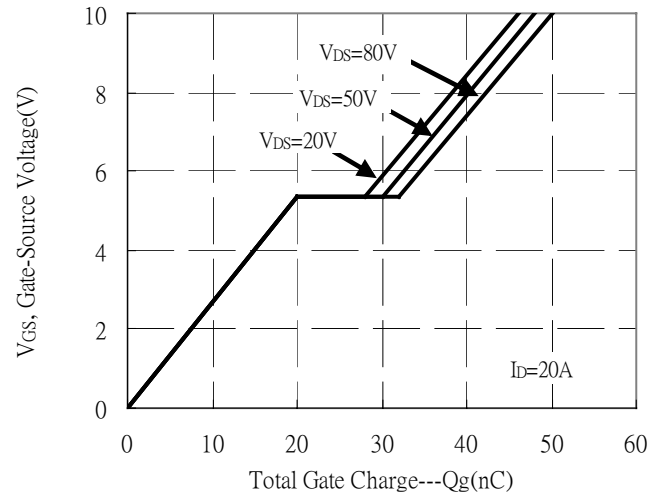
Threshold Voltage vs Junction Temperature



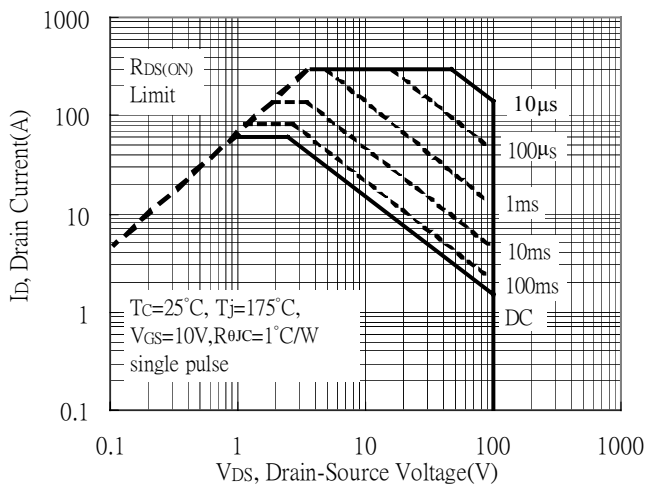
Forward Transfer Admittance vs Drain Current



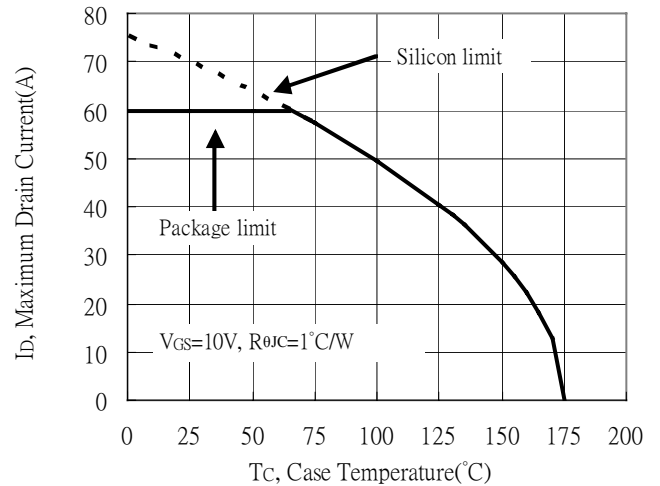
Gate Charge Characteristics



Maximum Safe Operating Area



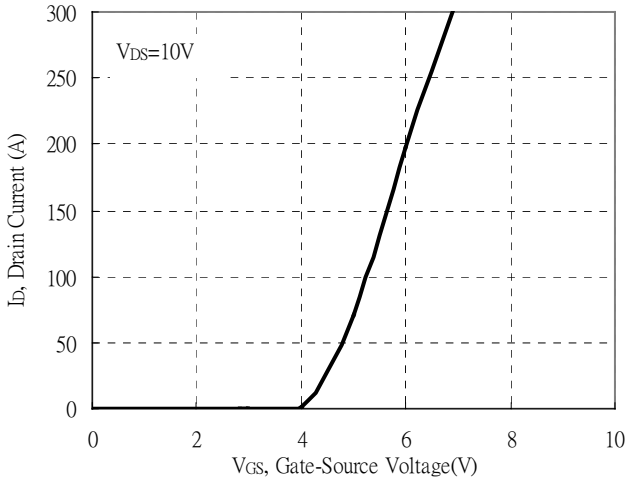
Maximum Drain Current vs Case Temperature



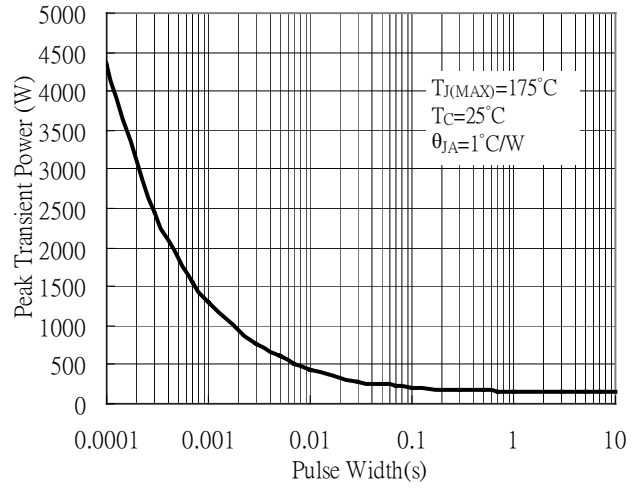


**Typical Characteristics(Cont.)**

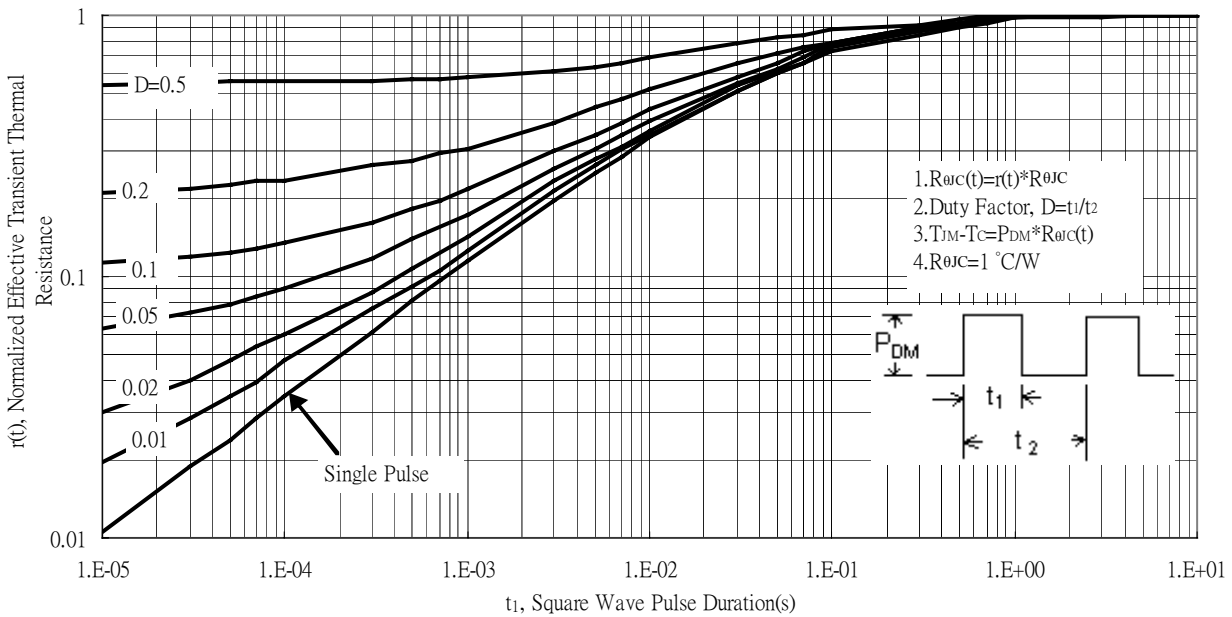
Typical Transfer Characteristics



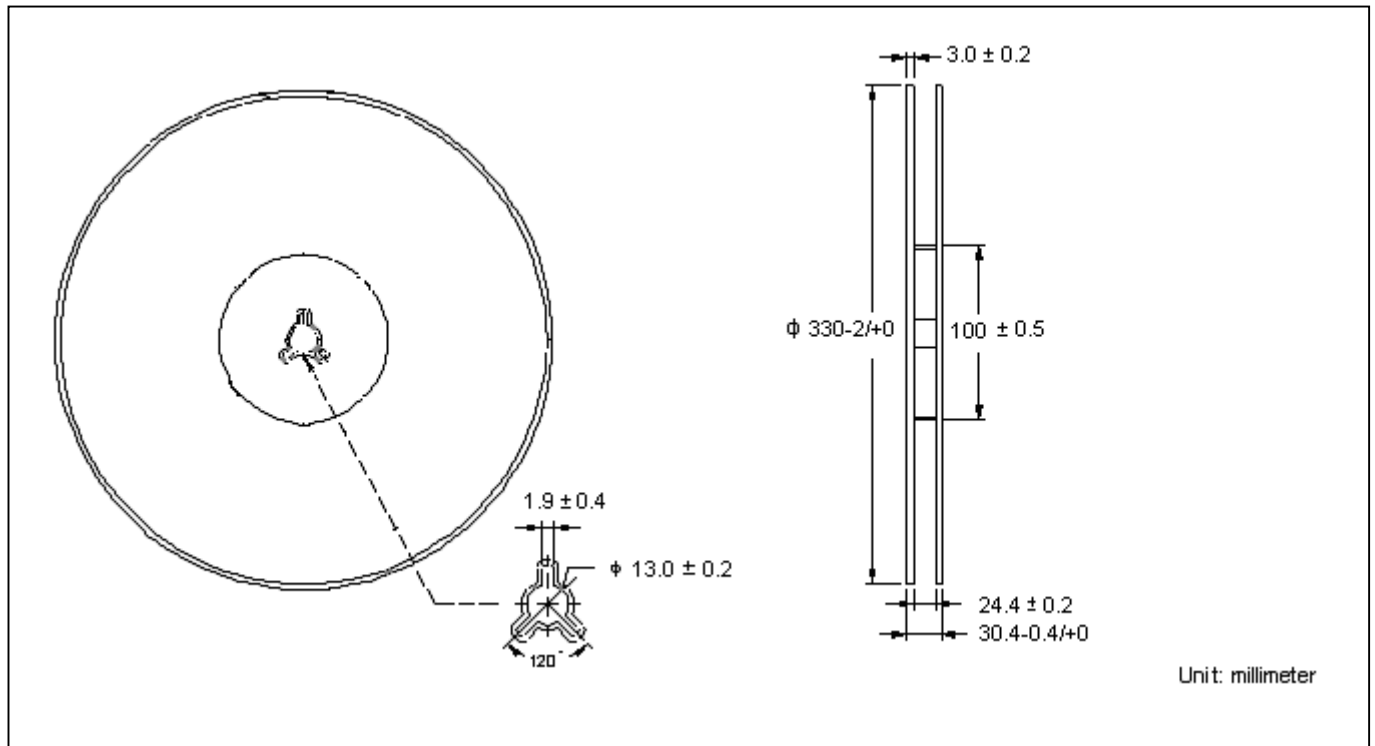
Single Pulse Maximum Power Dissipation



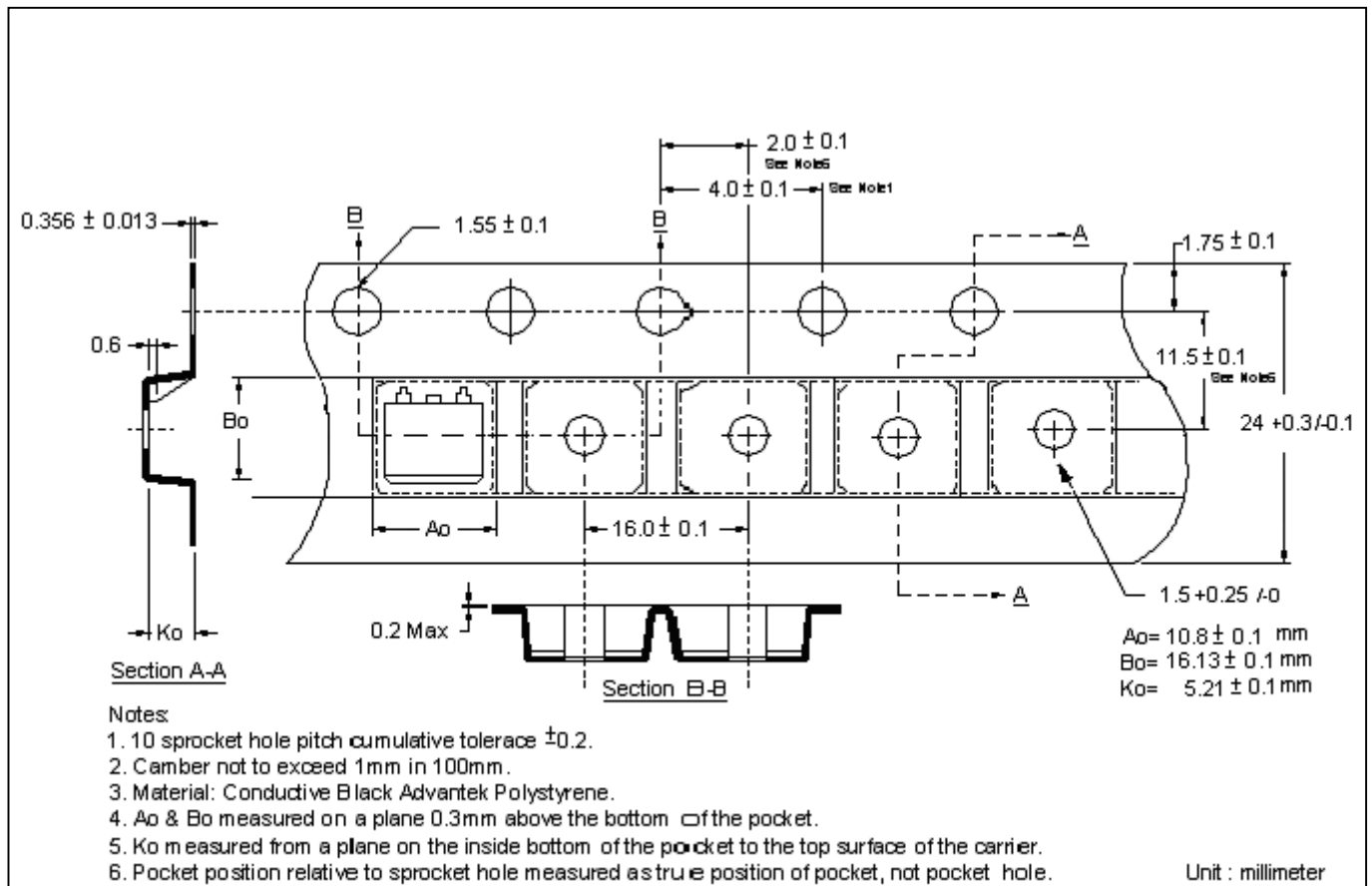
Transient Thermal Response Curves



### Reel Dimension



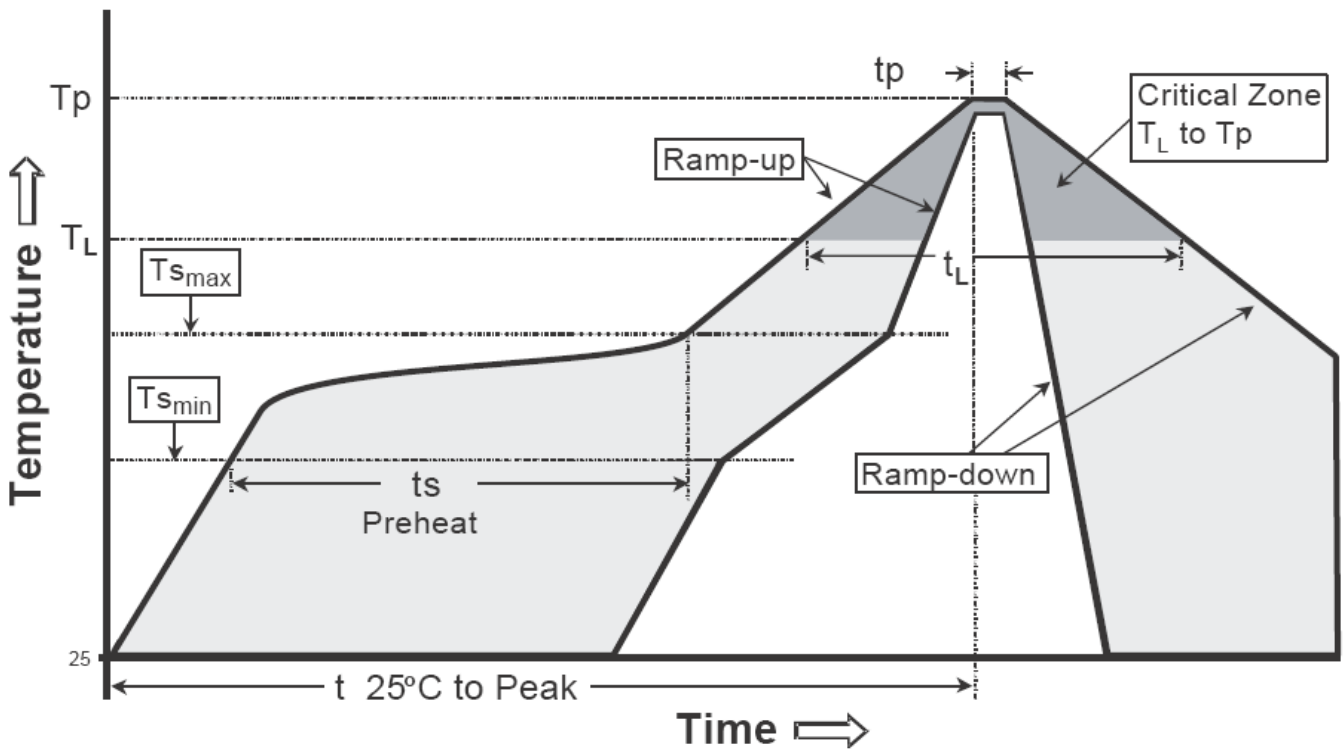
### Carrier Tape Dimension



**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

**Recommended temperature profile for IR reflow**

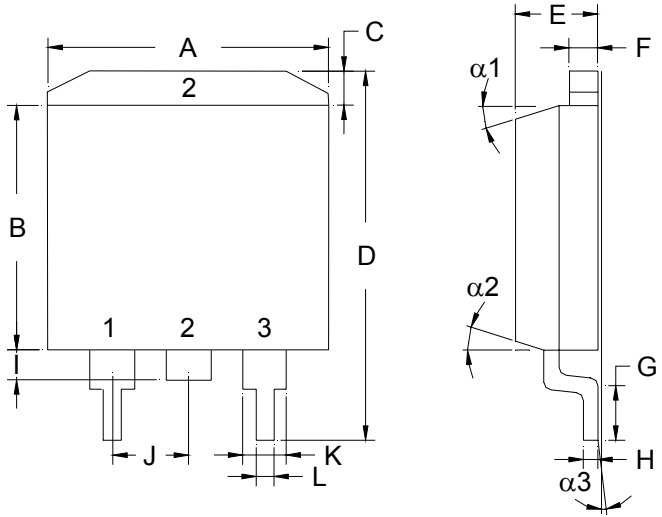


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T <sub>smax</sub> to T <sub>p</sub> )	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T <sub>s min</sub> )	100°C	150°C
-Temperature Max(T <sub>s max</sub> )	150°C	200°C
-Time(t <sub>s min</sub> to t <sub>s max</sub> )	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T <sub>L</sub> )	183°C	217°C
- Time (t <sub>L</sub> )	60-150 seconds	60-150 seconds
Peak Temperature(T <sub>P</sub> )	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

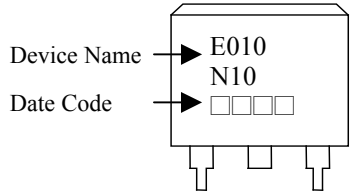
Note : All temperatures refer to topside of the package, measured on the package body surface.



**TO-263 Dimension**



**Marking :**



Device Name → E010  
N10  
Date Code → □□□□

Style : Pin 1.Gate 2.Drain 3.Source

3-Lead Plastic Surface Mounted Package  
 CYStek Package Code : F3

\*:Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.3800	0.4050	9.65	10.29	I	0.0500	0.0700	1.27	1.78
B	0.3300	0.3700	8.38	9.40	J	-	*0.1000	-	*2.54
C	-	0.0550	-	1.40	K	0.0450	0.0550	1.14	1.40
D	0.5750	0.6250	14.61	15.88	L	0.0200	0.0390	0.51	0.99
E	0.1600	0.1900	4.06	4.83	$\alpha 1$	-	-	6°	8°
F	0.0450	0.0550	1.14	1.40	$\alpha 2$	-	-	6°	8°
G	0.0900	0.1100	2.29	2.79	$\alpha 3$	-	-	0°	5°
H	0.0180	0.0290	0.46	0.74					

**Notes :** 1.Controlling dimension : millimeters.  
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material :**

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

**Important Notice:**

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.