

N-Channel Enhancement Mode Power MOSFET

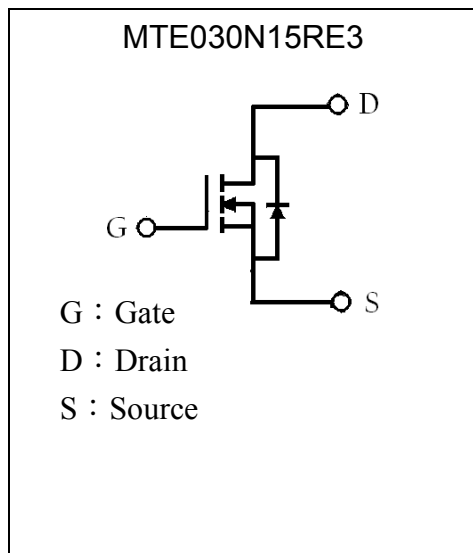
MTE030N15RE3

BV_{DSS}	150V
$I_D@V_{GS}=10V, T_C=25^\circ C$	36A
$I_D@V_{GS}=10V, T_A=25^\circ C$	4.6A
$R_{DS(ON)}@V_{GS}=10V, I_D=30A$	33.3mΩ (typ)

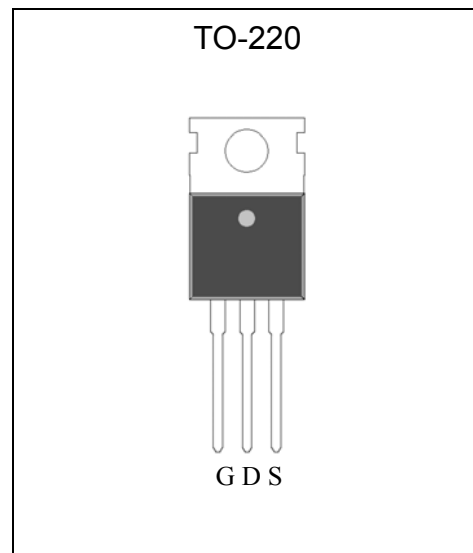
Features

- Low Gate Charge
- Simple Drive Requirement
- Repetitive Avalanche Rated
- Fast Switching Characteristic
- Pb-free lead plating and RoHS compliant package

Symbol

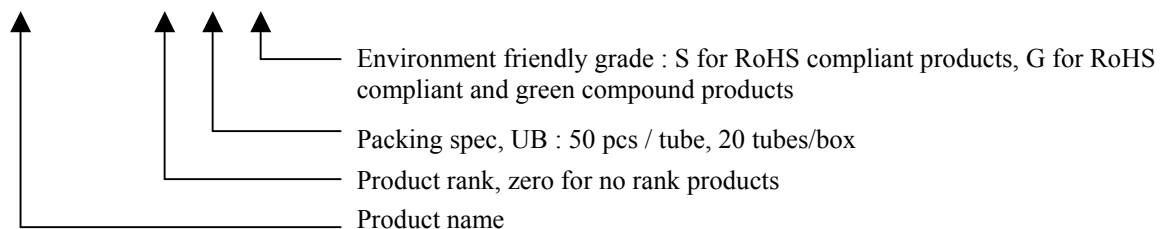


Outline



Ordering Information

Device	Package	Shipping
MTE030N15RE3-0-UB-X	TO-220 (Pb-free lead plating package)	50 pcs/tube, 20 tubes/box, 4 boxes / carton





Absolute Maximum Ratings ($T_C=25^{\circ}C$, unless otherwise noted)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V_{DS}	150	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current @ $V_{GS}=10V, T_C=25^{\circ}C$	I_D	36	A
Continuous Drain Current @ $V_{GS}=10V, T_C=100^{\circ}C$		25.5	
Pulsed Drain Current (Note 1)	I_{DM}	144	
Continuous Drain Current @ $V_{GS}=10V, T_A=25^{\circ}C$	I_{DSM}	4.6	
Continuous Drain Current @ $V_{GS}=10V, T_A=70^{\circ}C$		3.7	
Avalanche Current @ $L=0.1mH$	I_{AS}	36	
Avalanche Energy @ $L=5mH, I_D=15A, V_{DD}=50V$ (Note 2)	E_{AS}	560	mJ
Repetitive Avalanche Energy @ $L=0.05mH$	E_{AR}	13	
Total Power Dissipation ($T_C=25^{\circ}C$)	P_D	136	W
Total Power Dissipation ($T_C=100^{\circ}C$)		68	
Total Power Dissipation ($T_A=25^{\circ}C$)		2.4	
Total Power Dissipation ($T_A=100^{\circ}C$)		1.2	
Operating Junction and Storage Temperature	T_j, T_{stg}	$-55 \sim +175$	$^{\circ}C$

Note : 1. Pulse width limited by maximum junction temperature
 2. 100% tested by conditions of $L=0.1mH, I_{AS}=20A, V_{GS}=10V, V_{DD}=50V$

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{\theta JC}$	1.1	$^{\circ}C/W$
Thermal Resistance, Junction-to-ambient, max	$R_{\theta JA}$	62.5	

Characteristics ($T_C=25^{\circ}C$, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV_{DSS}	150	-	-	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta BV_{DSS}/\Delta T_j$	-	0.1	-	$V/^{\circ}C$	Reference to $25^{\circ}C, I_D=250\mu A$
$V_{GS(th)}$	2.0	-	4.0	V	$V_{DS} = V_{GS}, I_D=250\mu A$
G_{FS}	-	16	-	S	$V_{DS} = 10V, I_D=20A$
I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 30V$
I_{DSS}	-	-	1	μA	$V_{DS} = 120V, V_{GS} = 0V$
	-	-	25		$V_{DS} = 100V, V_{GS} = 0V, T_j=125^{\circ}C$
$*R_{DS(ON)}$	-	33.3	42	$m\Omega$	$V_{GS} = 10V, I_D=30A$
Dynamic					
$*Q_g$	-	34.8	52	nC	$I_D=20A, V_{DS}=75V, V_{GS}=10V$
$*Q_{gs}$	-	11.3	-		
$*Q_{gd}$	-	9.6	-		



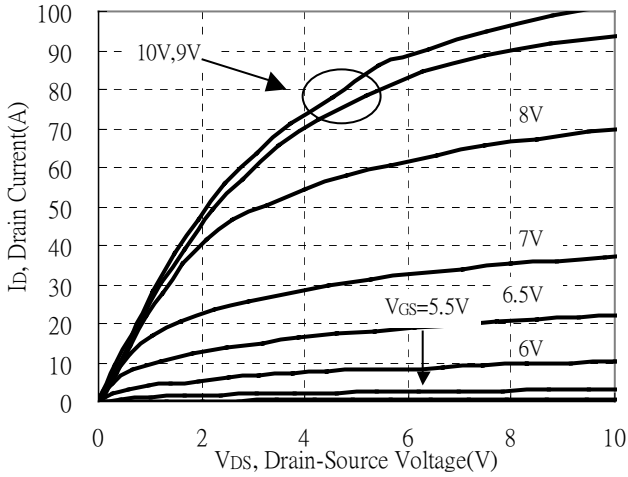
*td(ON)	-	21.2	-	ns	V _{DS} =75V, I _D =20A, V _{GS} =10V, R _G =3Ω
*tr	-	20.6	-		
*td(OFF)	-	34.6	-		
*tf	-	9	-		
Ciss	-	1773	-	pF	V _{GS} =0V, V _{DS} =75V, f=1MHz
Coss	-	104	-		
Crss	-	12	-		
Rg	-	2.2	-	Ω	f=1MHz
Source-Drain Diode					
*I _S	-	-	43	A	
*I _{SM}	-	-	172		
*V _{SD}	-	0.9	1.2	V	I _S =30A, V _{GS} =0V
*trr	-	57	-	ns	I _F =20A, V _{GS} =0V, dI _F /dt=100A/μs
*Qrr	-	143	-	nC	

*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

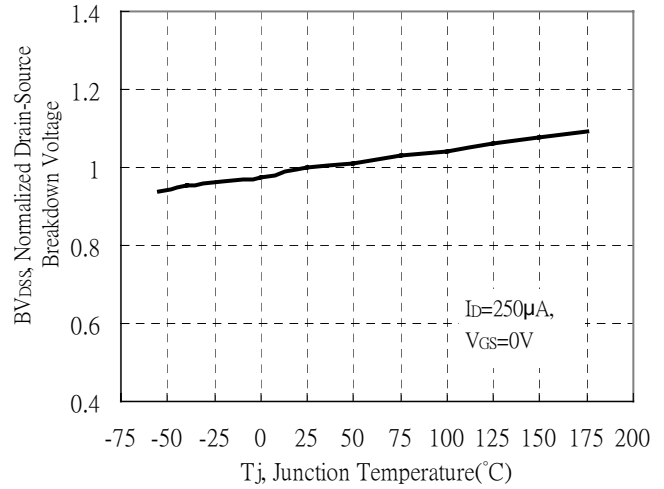


Typical Characteristics

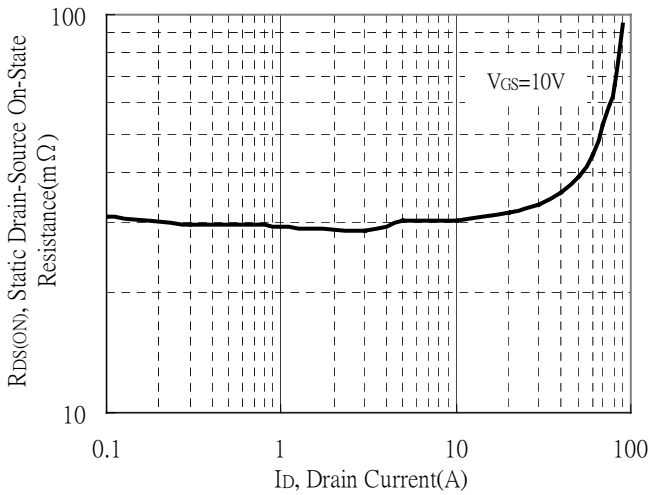
Typical Output Characteristics



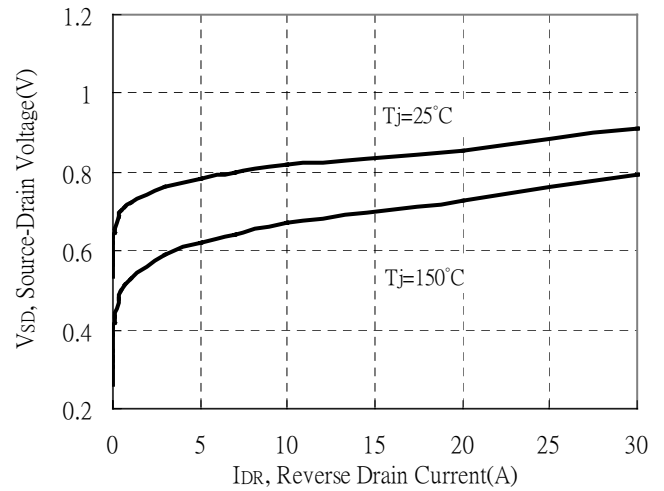
Brekdown Voltage vs Junction Temperature



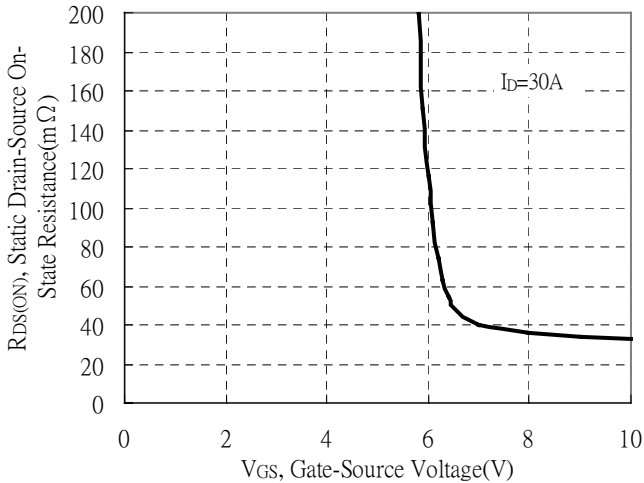
Static Drain-Source On-State resistance vs Drain Current



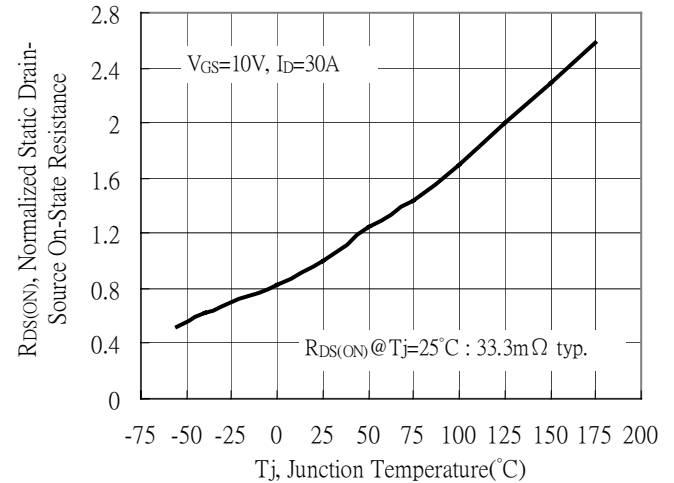
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

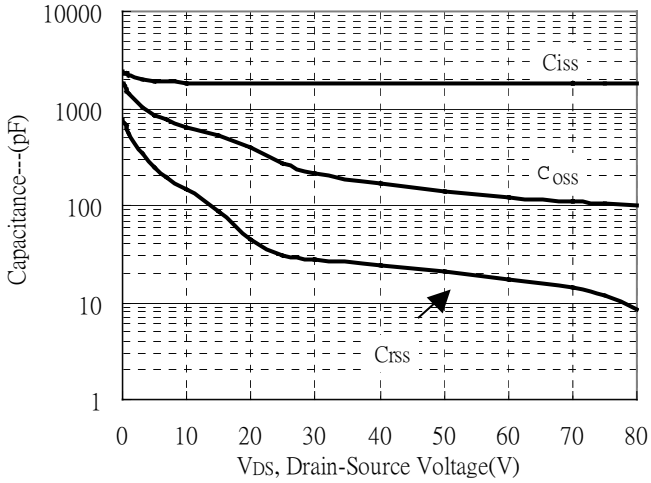


Drain-Source On-State Resistance vs Junction Temperature

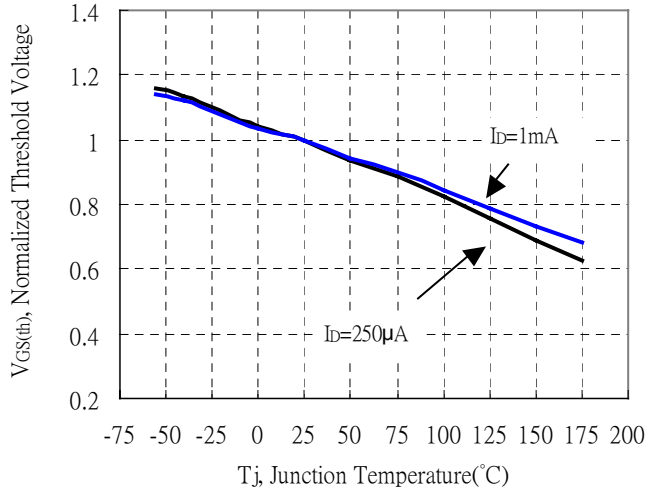


Typical Characteristics(Cont.)

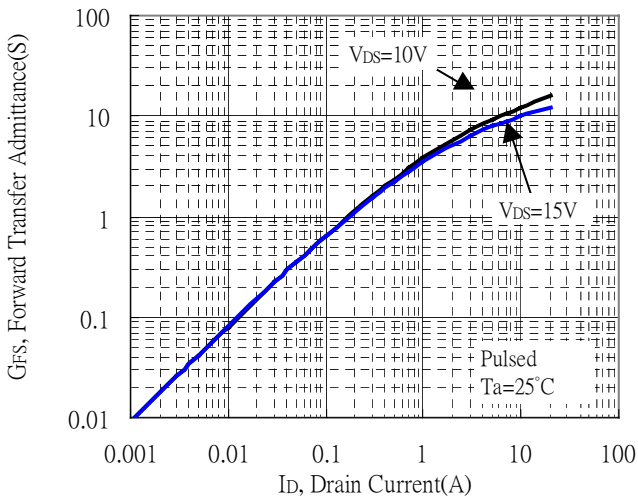
Capacitance vs Drain-to-Source Voltage



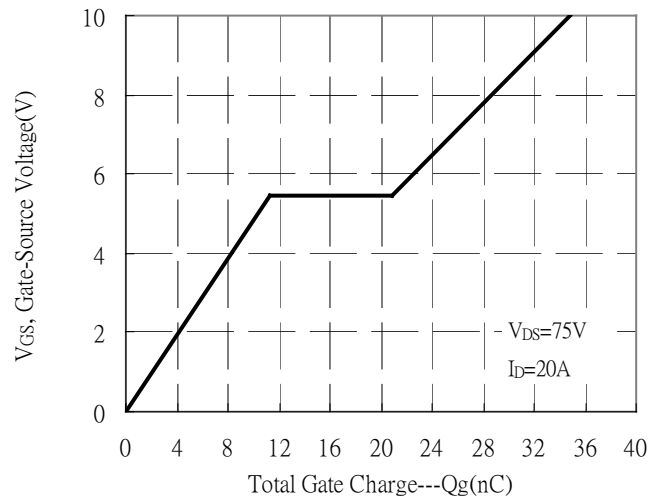
Threshold Voltage vs Junction Temperature



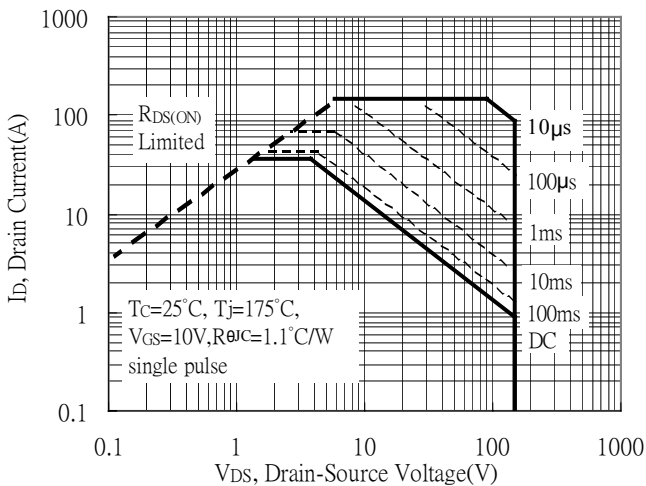
Forward Transfer Admittance vs Drain Current



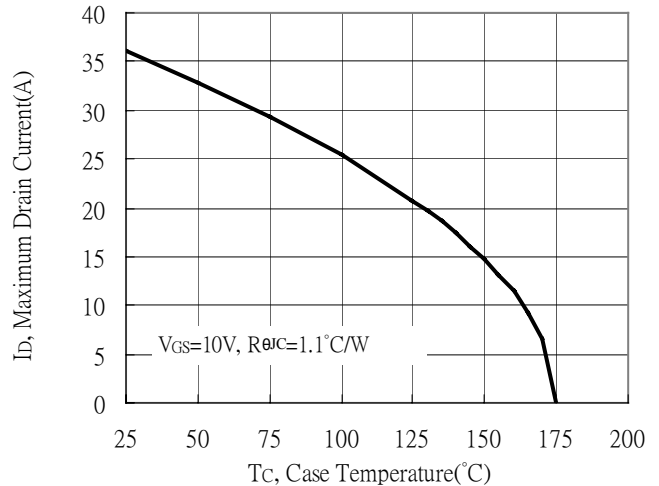
Gate Charge Characteristics



Maximum Safe Operating Area



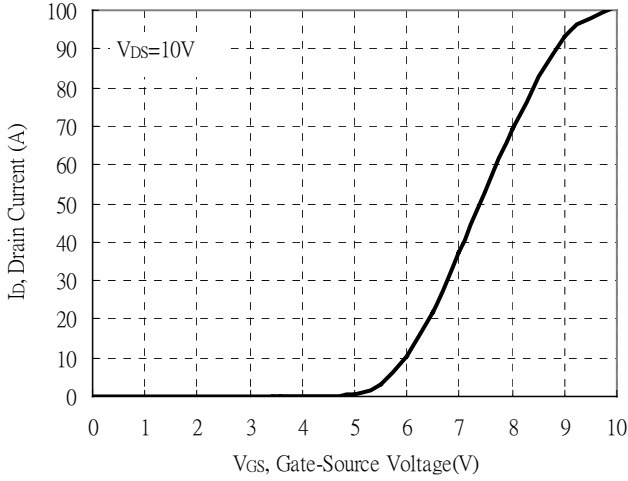
Maximum Drain Current vs Case Temperature



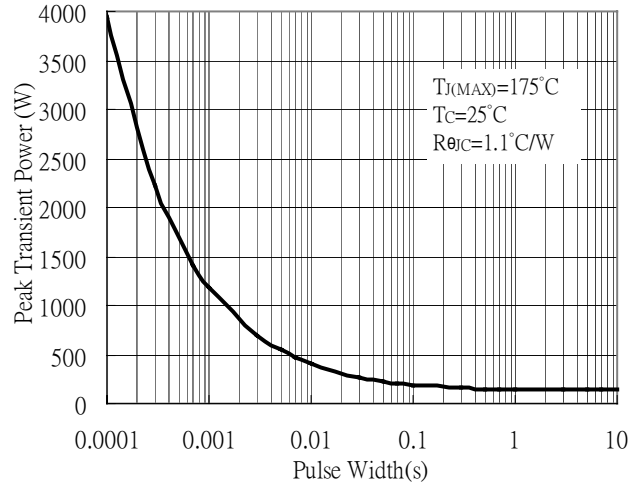


Typical Characteristics(Cont.)

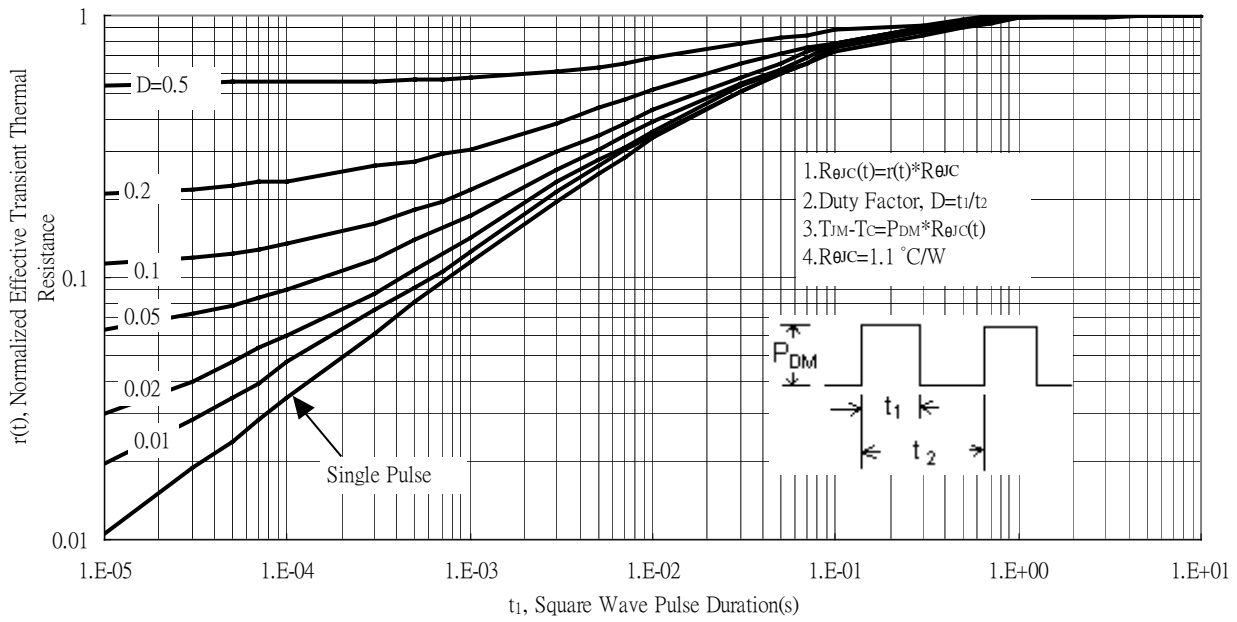
Typical Transfer Characteristics



Single Pulse Maximum Power Dissipation

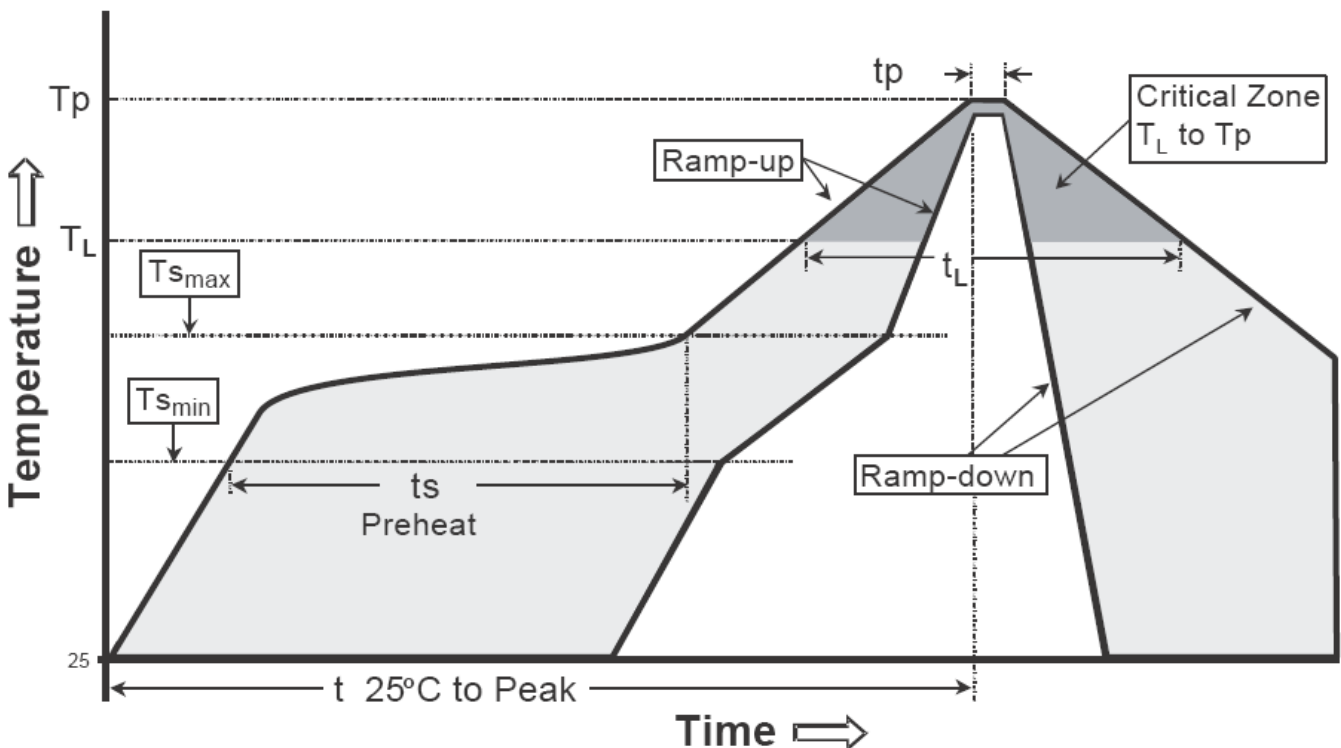


Transient Thermal Response Curves



Recommended wave soldering condition

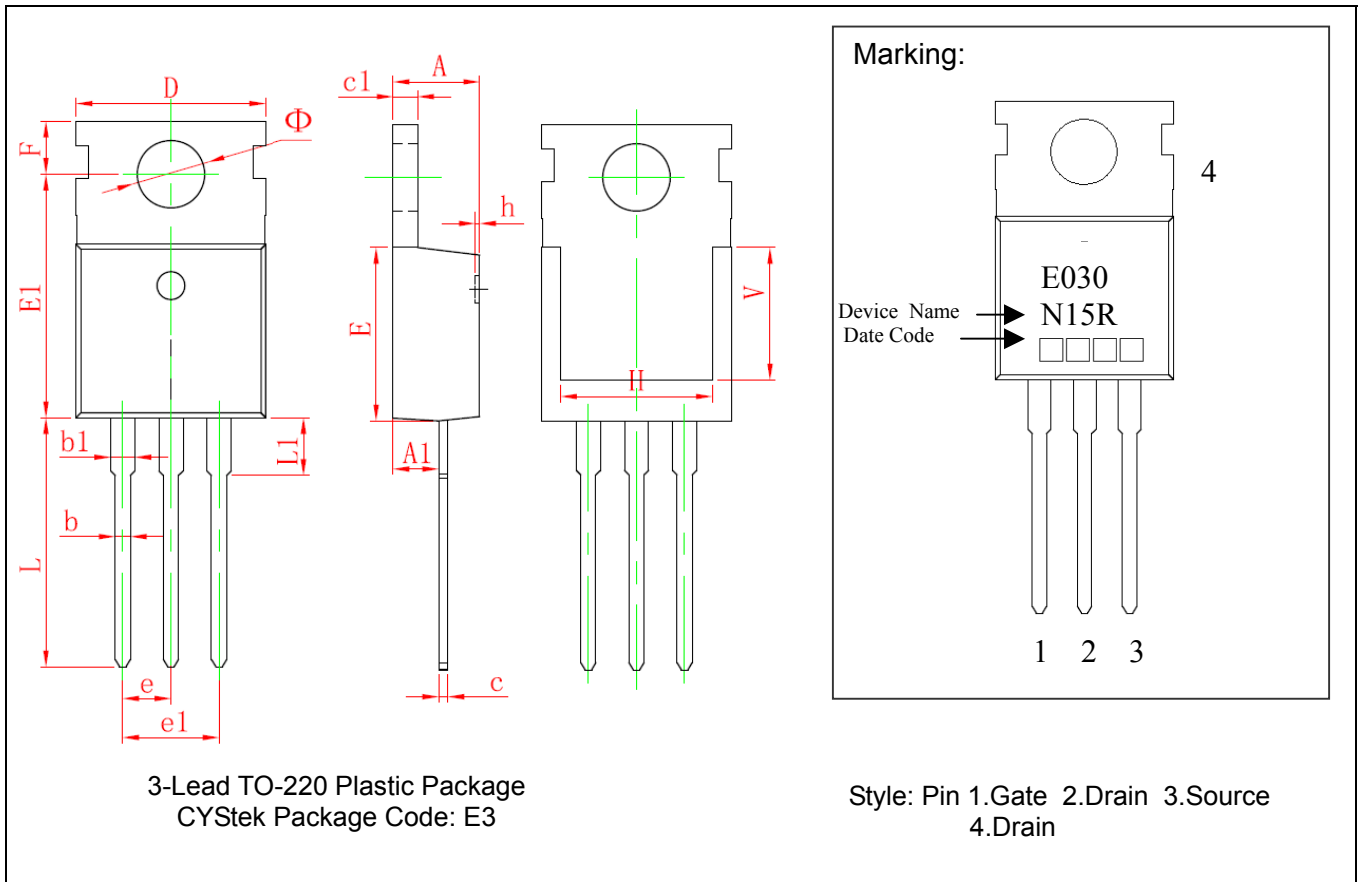
Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

Recommended temperature profile for IR reflow


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-220 Dimension



*: Typical

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181	e	2.540*		0.100*	
A1	2.250	2.550	0.089	0.100	e1	4.980	5.180	0.196	0.204
b	0.710	0.910	0.028	0.036	F	2.650	2.950	0.104	0.116
b1	1.170	1.370	0.046	0.054	H	7.900	8.100	0.311	0.319
c	0.330	0.650	0.013	0.026	h	0.000	0.300	0.000	0.012
c1	1.200	1.400	0.047	0.055	L	12.900	13.400	0.508	0.528
D	9.910	10.250	0.390	0.404	L1	2.850	3.250	0.112	0.128
E	8.950	9.750	0.352	0.384	V	7/500	REF	0.295	REF
E1	12.650	12.950	0.498	0.510	Φ	3.400	3.800	0.134	0.150

- Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.