N-Channel Enhancement Mode Power MOSFET

MTE130N20KE3

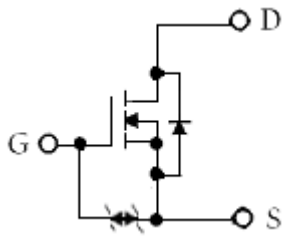
BV_{DSS}	200V
I_D	18A
$R_{DSON(TYP)}$ @ V_{GS}=10V, I_D=9A	143mΩ

Features

- Low Gate Charge
- Simple Drive Requirement
- ESD Diode Protected Gate
- Fast Switching Characteristic
- RoHS compliant package

Symbol

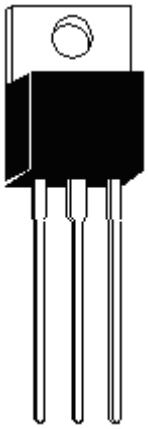
MTE130N20KE3



G : Gate D : Drain S : Source

Outline

TO-220



G D S

Ordering Information

Device	Package	Shipping
MTE130N20KE3-0-UB-S	TO-220 (RoHS compliant package)	50 pcs/tube, 20 tubes/box, 4 boxes / carton

Environment friendly grade : S for RoHS compliant products, G for RoHS compliant and green compound products

Packing spec, UB : 50 pcs / tube, 20 tubes/box

Product rank, zero for no rank products

Product name

Absolute Maximum Ratings (T_C=25°C, unless otherwise noted)

Parameter			Symbol	Limits	Unit
Drain-Source Voltage			V_{DS}	200	V
Gate-Source Voltage			V_{GS}	±20	
Continuous Drain Current @ T_C=25°C(silicon limit)			I_D	18	A
Continuous Drain Current @ T_C=100°C(silicon limit)				13	
Pulsed Drain Current		(Note 3)	I_{DM}	34	
Continuous Drain Current @ T_A=25°C		(Note 2)	I_{DSM}	2.4	
Continuous Drain Current @ T_A=70°C		(Note 2)		1.9	
Avalanche Current		(Note 3)	I_{AS}	10	
Avalanche Energy @ L=100μH, I_D=10A, V_{DD}=50V		(Note 2)	E_{AS}	5	mJ
Power Dissipation	T_C=25°C	(Note 1)	P_D	125	W
	T_C=100°C	(Note 1)		62.5	
Power Dissipation	T_A=25°C	(Note 2)	P_{DSM}	2	W
	T_A=70°C	(Note 2)		1.3	
Operating Junction and Storage Temperature			Tj, Tstg	-55~+175	°C

Thermal Data

Parameter		Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max		$R_{th,j-c}$	1.2	°C/W
Thermal Resistance, Junction-to-ambient, max, t≤10s	(Note 2)	$R_{th,j-a}$	15	°C/W
Thermal Resistance, Junction-to-ambient, max	(Note 2)		62.5	°C/W

Note : 1. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

2. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2 oz. copper, in a still air environment with T_A=25°C. The power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

3. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175°C. Ratings are based on low frequency and low duty cycles to keep initial T_J=25°C.

4. The maximum current limited by package is 60A.

5. The static characteristics are obtained using <300μs pulses, duty cycle 0.5% maximum.

6. The $R_{\theta JA}$ is the sum of thermal resistance from junction to case $R_{\theta JC}$ and case to ambient.

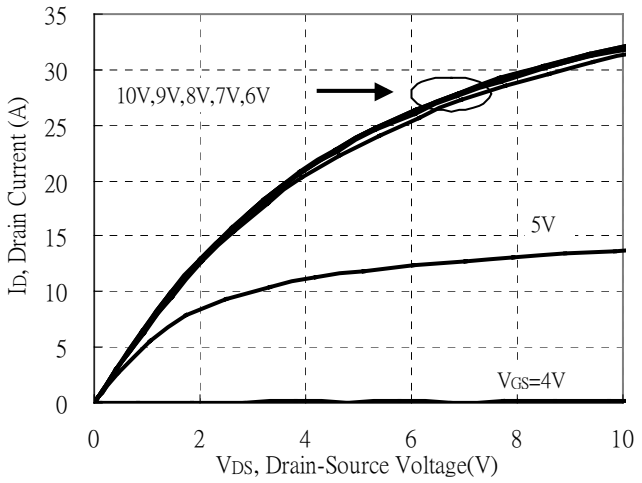
Characteristics (T_C=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV_{DSS}	200	-	-	V	V_{GS}=0V, I_D=250μA
$\Delta BV_{DSS}/\Delta Tj$	-	0.2	-	V/°C	Reference to 25°C, I_D=250μA
$V_{GS(th)}$	2.0	3.2	4.0	V	V_{DS} = V_{GS}, I_D=250μA
G_{FS}	-	15	-	S	V_{DS} =10V, I_D=9A
I_{GSS}	-	-	±10	μA	V_{GS}=±20V
I_{DSS}	-	-	1		V_{DS} =180V, V_{GS} =0V
	-	-	10		V_{DS} =180V, V_{GS} =0V, Tj=125°C
*$R_{DS(ON)}$	-	143	185	mΩ	V_{GS} =10V, I_D=9A
Dynamic					
*Qg	-	22	-	nC	V_{DS}=160V, I_D=18A, V_{GS}=10V
*Qgs	-	5.5	-		
*Qgd	-	9.4	-		
*$t_{d(ON)}$	-	21	-	ns	V_{DS}=100V, I_D=18A, V_{GS}=10V, R_G=6Ω
*tr	-	32	-		
*$t_{d(OFF)}$	-	40	-		
*t_f	-	30	-		
Ciss	-	972	-	pF	V_{GS}=0V, V_{DS}=25V, f=1MHz
Coss	-	85	-		
Crss	-	37	-		
Source-Drain Diode					
*I_S	-	-	18	A	
*I_{SM}	-	-	34		
*V_{SD}	-	0.87	1.2	V	I_S=18A, V_{GS}=0V
*trr	-	90	-	ns	I_F=18A, V_{GS}=0, dI_F/dt=100A/μs
*Qrr	-	260	-	nC	

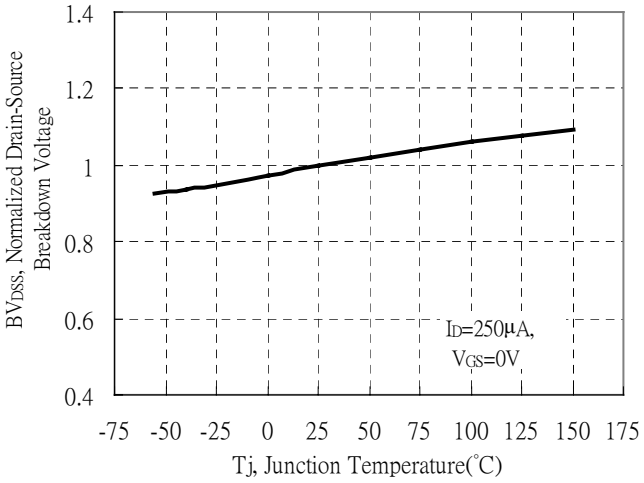
*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Typical Characteristics

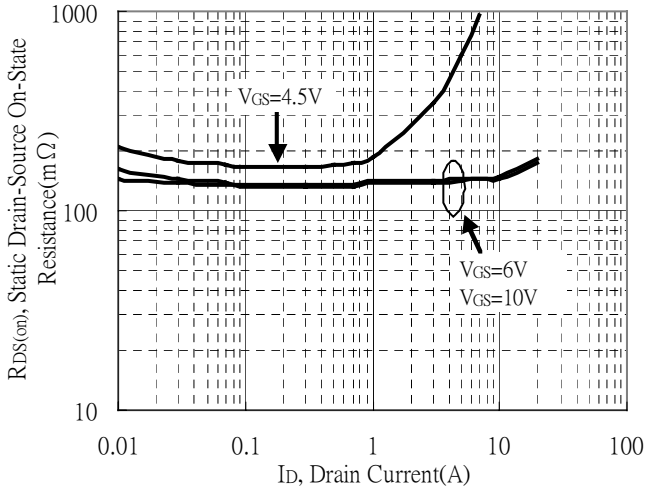
Typical Output Characteristics



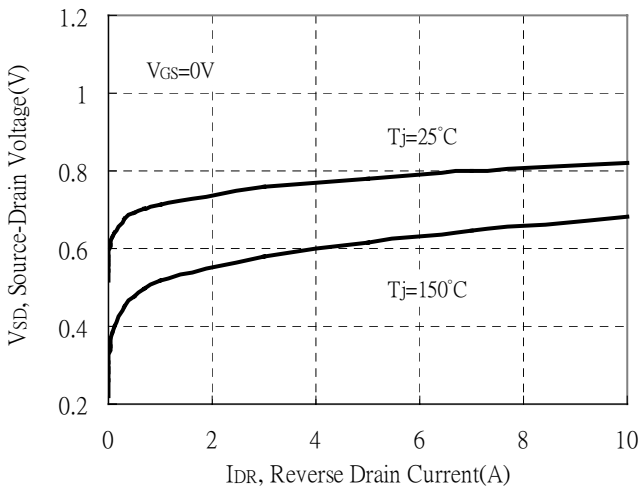
Brekdown Voltage vs Ambient Temperature



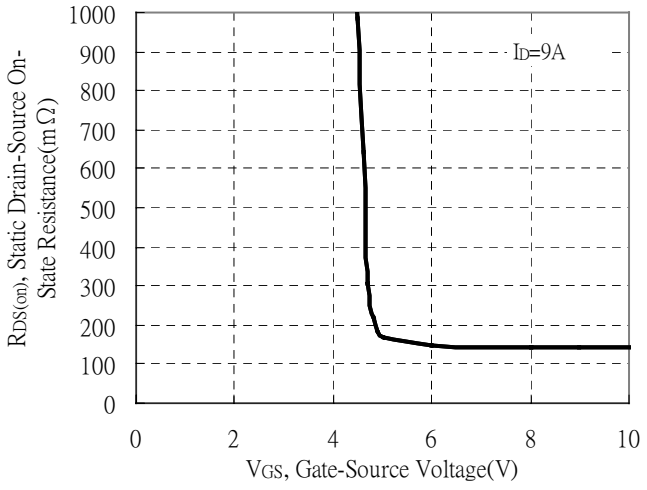
Static Drain-Source On-State resistance vs Drain Current



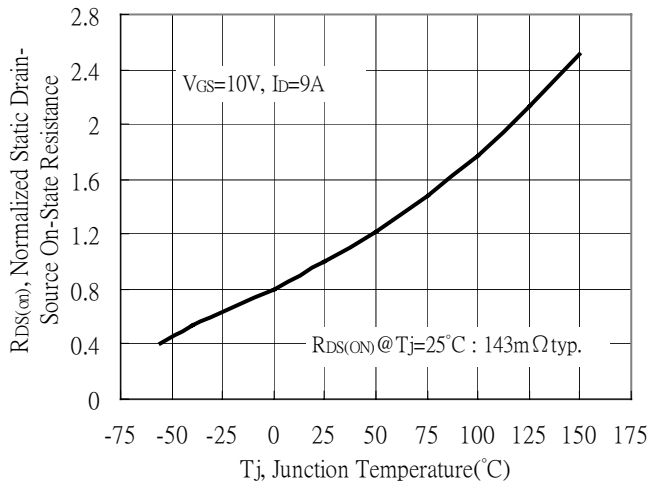
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

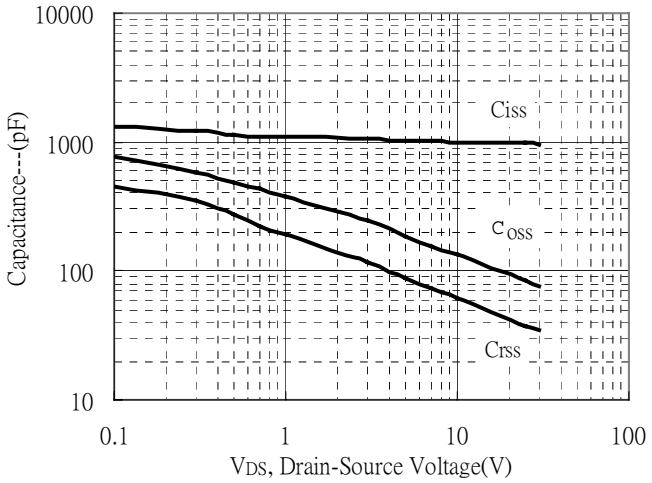


Drain-Source On-State Resistance vs Junction Tempearture

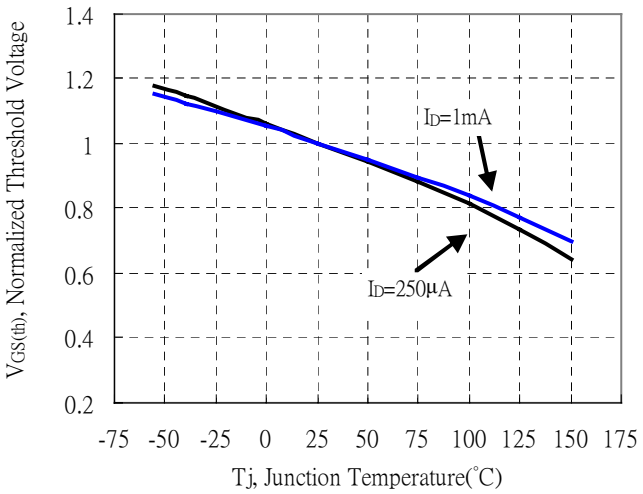


Typical Characteristics(Cont.)

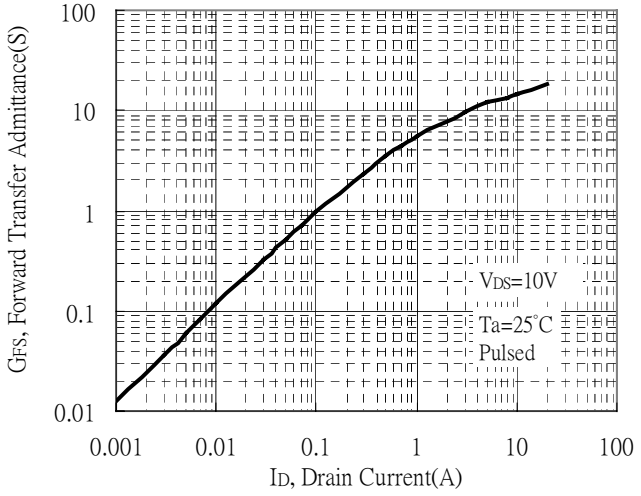
Capacitance vs Drain-to-Source Voltage



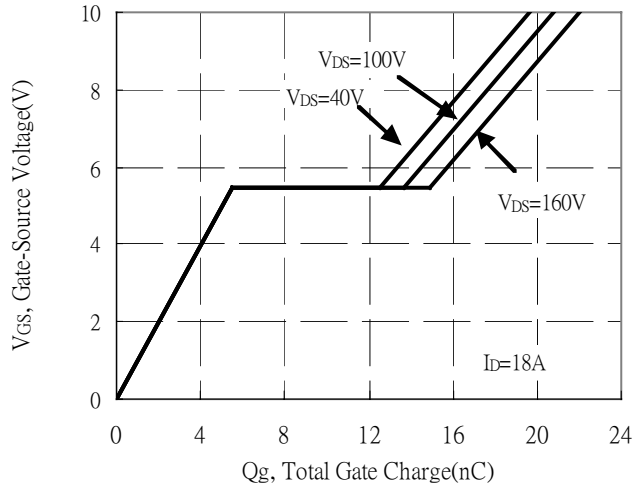
Threshold Voltage vs Junction Tempearture



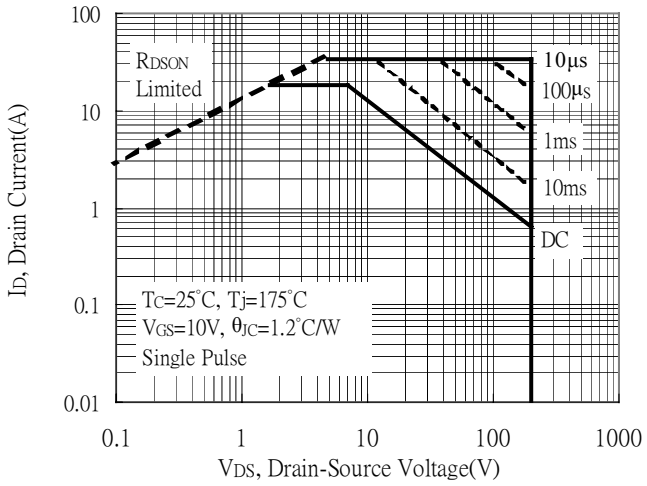
Forward Transfer Admittance vs Drain Current



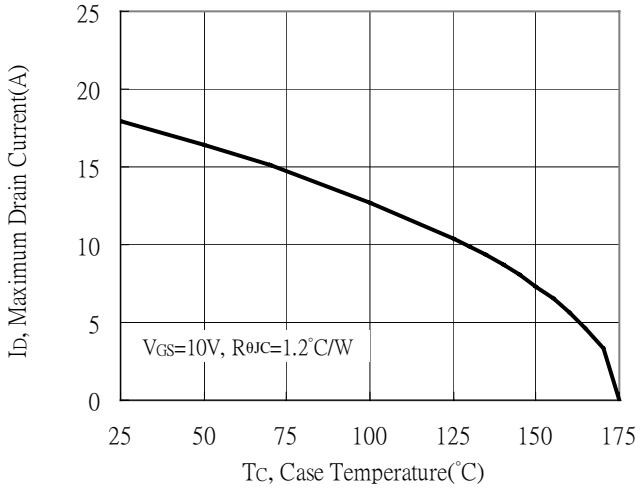
Gate Charge Characteristics



Maximum Safe Operating Area

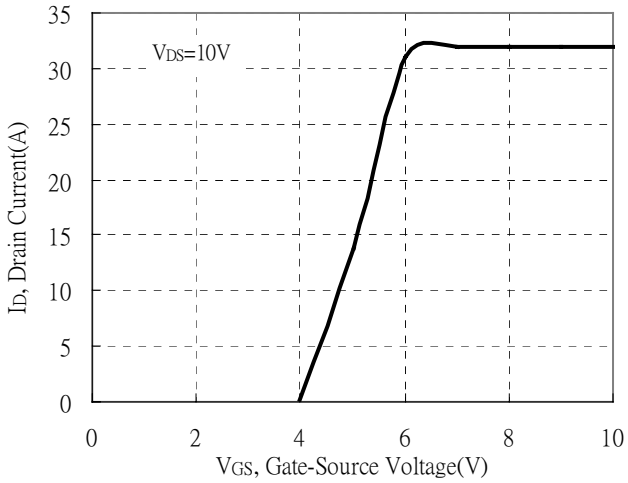


Maximum Drain Current vs Case Temperature

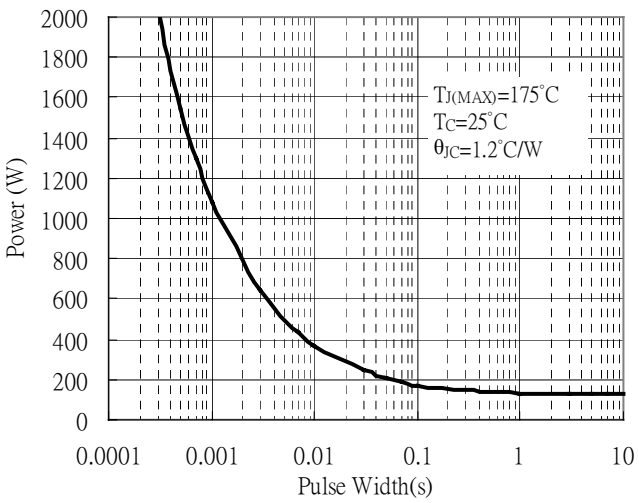


Typical Characteristics(Cont.)

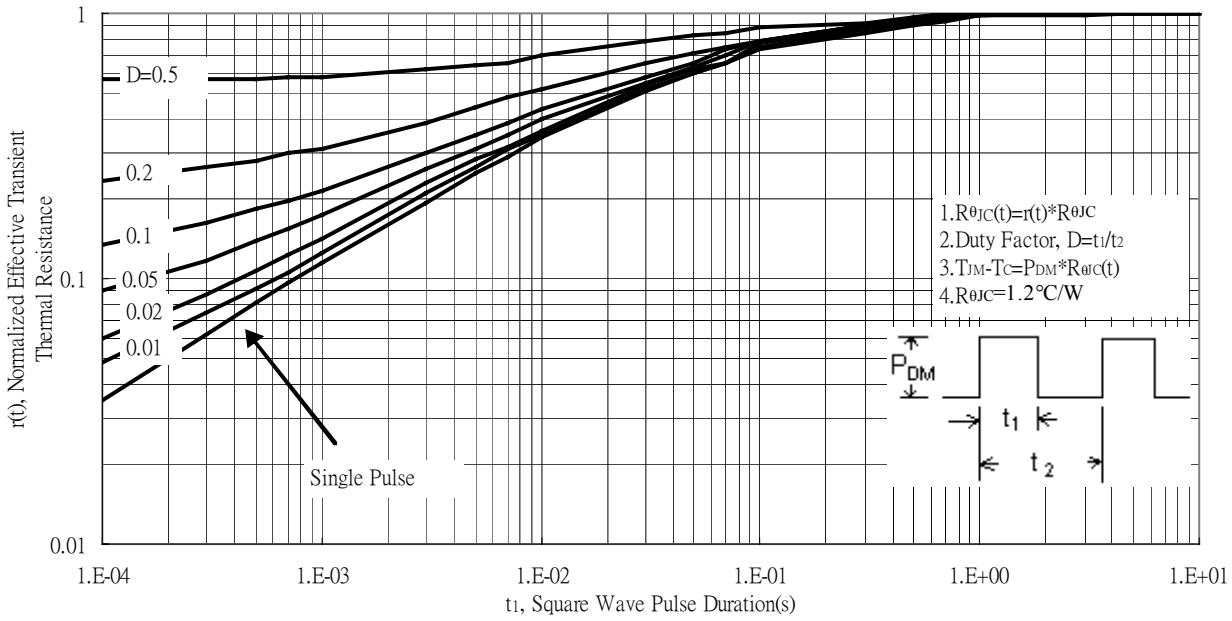
Typical Transfer Characteristics



Single Pulse Power Rating, Junction to Case



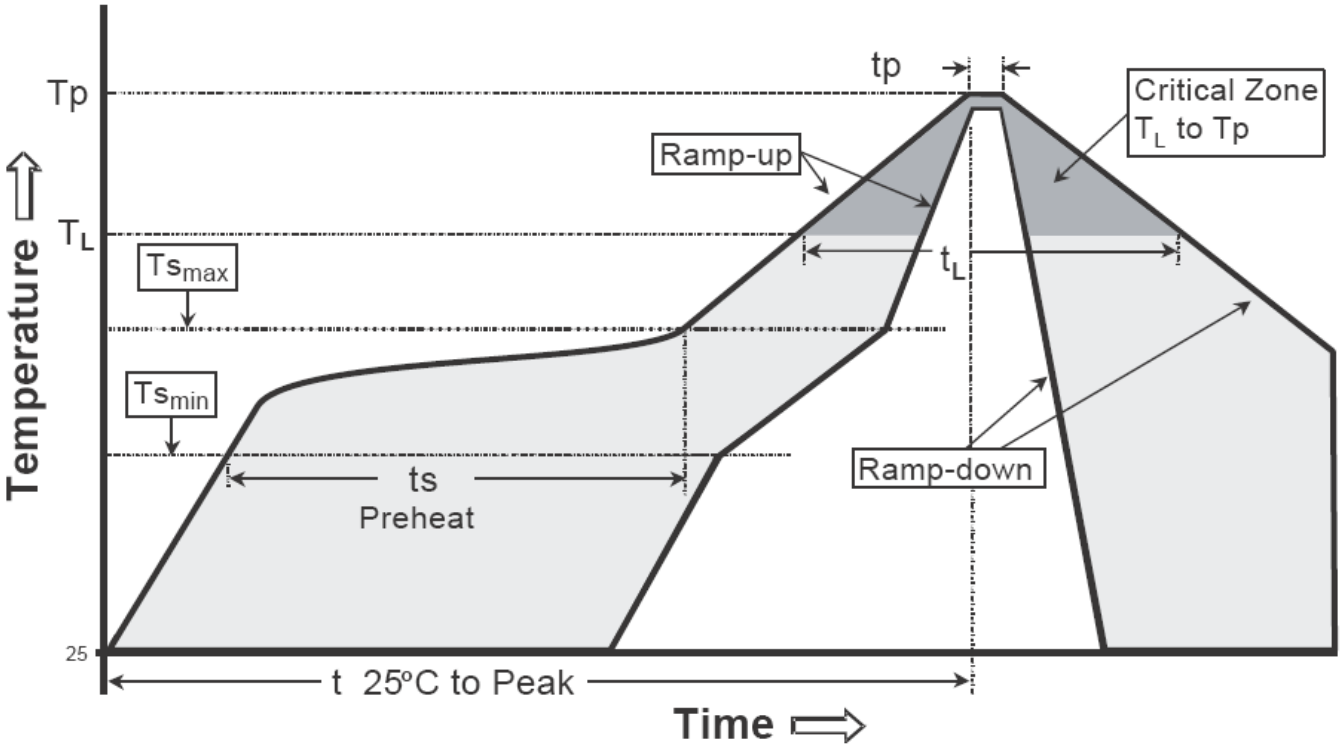
Transient Thermal Response Curves



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

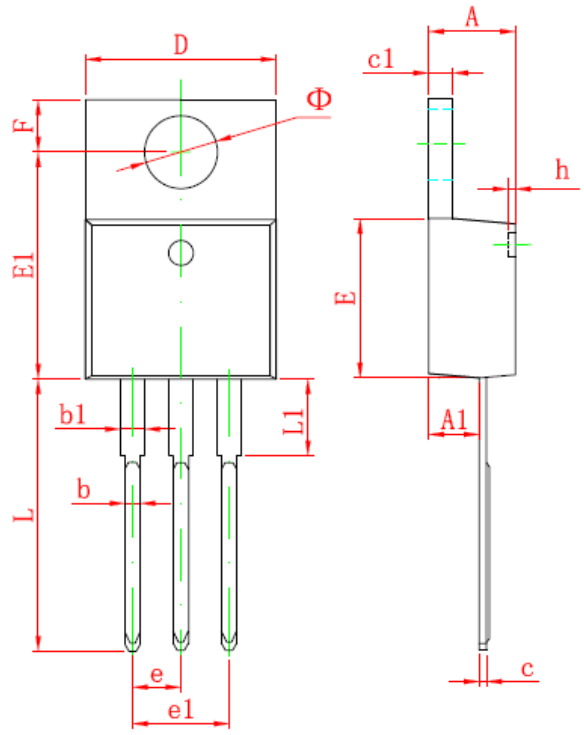
Recommended temperature profile for IR reflow



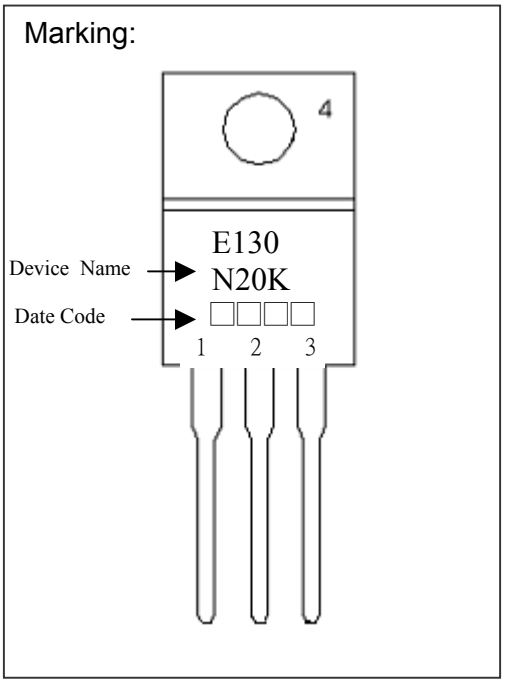
Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(T_S min) −Temperature Max(T_S max) −Time($t_{s\ min}$ to $t_{s\ max}$)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: −Temperature (T_L) − Time (t_L)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak Temperature(T_P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-220 Dimension



3-Lead TO-220 Plastic Package
CYStek Package Code: E3



Style: Pin 1.Gate 2.Drain 3.Source
4.Drain

*: Typical

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	4.470	4.670	0.176	0.184	E1	12.060	12.460	0.475	0.491
A1	2.520	2.820	0.099	0.111	e	2.540*		0.100*	
b	0.710	0.910	0.028	0.036	e1	4.980	5.180	0.196	0.204
b1	1.170	1.370	0.046	0.054	F	2.590	2.890	0.102	0.114
c	0.310	0.530	0.012	0.021	h	0.000	0.300	0.000	0.012
c1	1.170	1.370	0.046	0.054	L	13.400	13.800	0.528	0.543
D	10.010	10.310	0.394	0.406	L1	3.560	3.960	0.140	0.156
E	8.500	8.900	0.335	0.350	Φ	3.735	3.935	0.147	0.155

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.