e·MMC™ Memory

MTFC2GMTEA-WT, MTFC4GMTEA-WT, MTFC8GLTEA-WT, MTFC16GLTAM-WT, MTFC16GLTDV-WT, MTFC16GJTEC-WT, MTFC32GLTDM-WT, MTFC32GLTDI-WT, MTFC32GJTED-WT, MTFC64GJTEF-WT

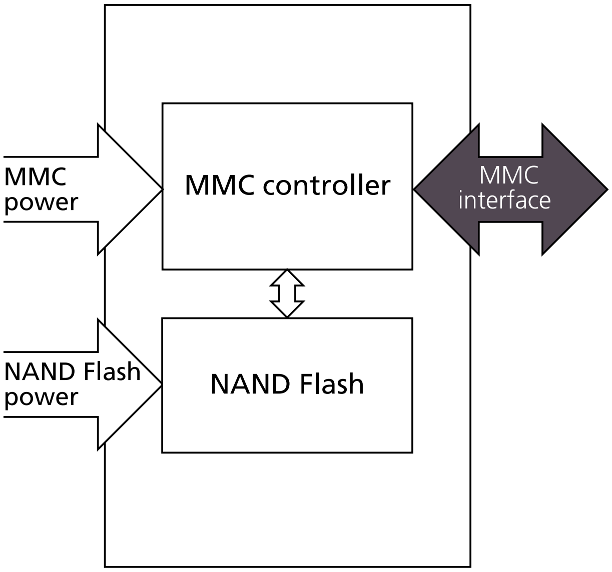
Features

- MultiMediaCard (MMC) controller and NAND Flash
- 153- or 169-ball WFBGA/VFBGA/TFBGA (RoHS 6/6-compliant)
- V_{CC}: 2.7–3.6V
- V_{CCQ} (dual voltage): 1.65–1.95V; 2.7–3.6V
- Temperature ranges
  - Operating temperature: –25˚C to +85˚C
  - Storage temperature: –40˚C to +85˚C
- Typical current consumption
  - Standby current: 110–180µA (dependent on part number)
  - Active current (RMS): 70mA (2GB), 80mA (4GB, 8GB, 16GB, 32GB, 64GB)

MMC-Specific Features

- JEDEC/MMC standard version 4.41-compliant (JEDEC Standard No. 84-A441) – SPI mode not supported (see www.jedec.org/sites/default/files/docs/JESD84-A441.pdf)
  - Advanced 11-signal interface
  - x1, x4, and x8 I/Os, selectable by host
  - MMC mode operation
  - Command classes: class 0 (basic); class 2 (block read); class 4 (block write); class 5 (erase); class 6 (write protection); class 7 (lock card)
  - Temporary write protection
  - 52 MHz clock speed (MAX)
  - Boot operation (high-speed boot)
  - Sleep mode
  - Replay-protected memory block (RPMB)
  - Secure erase and trim
  - Hardware reset signal
  - Multiple partitions with enhanced attribute
  - Permanent and power-on write protection
  - Double data rate (DDR) function
  - High-priority interrupt (HPI)

Figure 1: Micron e·MMC Device



MMC-Specific Features (Continued)

  - Background operation
  - Reliable write
  - Backward-compatible with previous MMC modes
- ECC and block management implemented

e·MMC Performance

Table 1: MLC Partition Performance

Condition	Part Number			Units
	MTFC2GMTEA-WT	MTFC4GMTEA-WT, MTFC8GLTEA-WT MTFC16GLTAM-WT, MTFC16GLTDV-WT MTFC32GLTDM-WT, MTFC32GLTDI-WT	MTFC16GJTEC-WT MTFC32GJTED-WT MTFC64GJTEF-WT	
Sequential write	6.6	13.5	20	MB/s
Sequential read	30	44	44	MB/s
Random write	TBD	90	100	IOPS
Random read	TBD	1080	1100	IOPS

Note: 1. Sequential access of 1MB chunk; random access of 4KB chunk. Additional performance data, such as power consumption or timing for different device modes, will be provided in a separate document upon customer request.

Part Numbering Information

Micron®*e*·MMC memory devices are available in different configurations and densities.

Figure 2: e·MMC Part Numbering

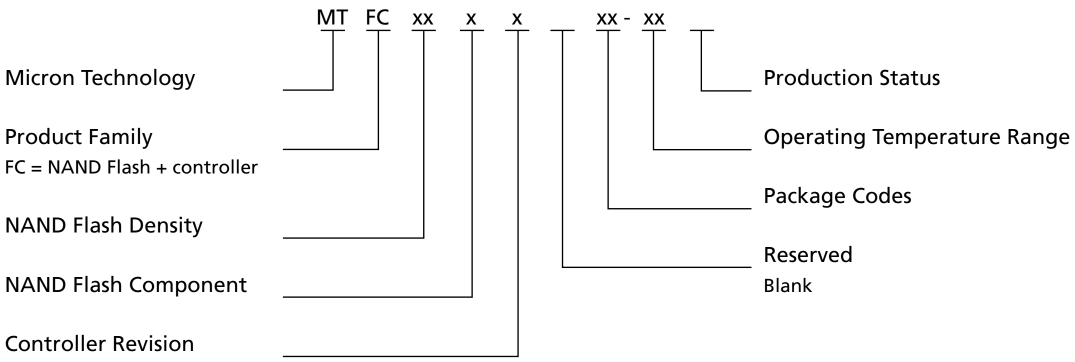


Table 2: Ordering Information

Base Part Number	Density	Package	Shipping Media
MTFC2GMTEA-WT	2GB	153-ball WFBGA 11.5mm x 13.0mm x 0.8mm	Tray
			Tape and reel
MTFC4GMTEA-WT	4GB	153-ball WFBGA 11.5mm x 13.0mm x 0.8mm	Tray
			Tape and reel
MTFC8GLTEA-WT	8GB	153-ball WFBGA 11.5mm x 13.0mm x 0.8mm	Tray
			Tape and reel
MTFC16GLTAM-WT	16GB	153-ball VFBGA 11.5mm x 13.0mm x 1.0mm	Tray
			Tape and reel
MTFC16GLTDV-WT	16GB	169-ball VFBGA 12.0mm x 16.0mm x 1.0mm	Tray
			Tape and reel
MTFC16GJTEC-WT	16GB	169-ball WFBGA 14.0mm x 18.0mm x 0.8mm	Tray
			Tape and reel
MTFC32GLTDM-WT	32GB	153-ball TFBGA 11.5mm x 13.0mm x 1.2mm	Tray
			Tape and reel
MTFC32GLTDI-WT	32GB	169-ball TFBGA 12.0mm x 16.0mm x 1.2mm	Tray
			Tape and reel
MTFC32GJTED-WT	32GB	169-ball VFBGA 14.0mm x 18.0mm x 1.0mm	Tray
			Tape and reel
MTFC64GJTEF-WT	64GB	169-ball TFBGA 14.0mm x 18.0mm x 1.2mm	Tray
			Tape and reel

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General Description

Micron *e*·MMC is a communication and mass data storage device that includes a MultiMediaCard (MMC) interface, a NAND Flash component, and a controller on an advanced 11-signal bus, which is compliant with the MMC system specification. Its low cost, small size, Flash technology independence, and high data throughput make *e*·MMC ideal for smart phones, digital cameras, PDAs, MP3 players, and other portable applications.

The nonvolatile *e*·MMC draws no power to maintain stored data, delivers high performance across a wide range of operating temperatures, and resists shock and vibration disruption.

Signal Descriptions

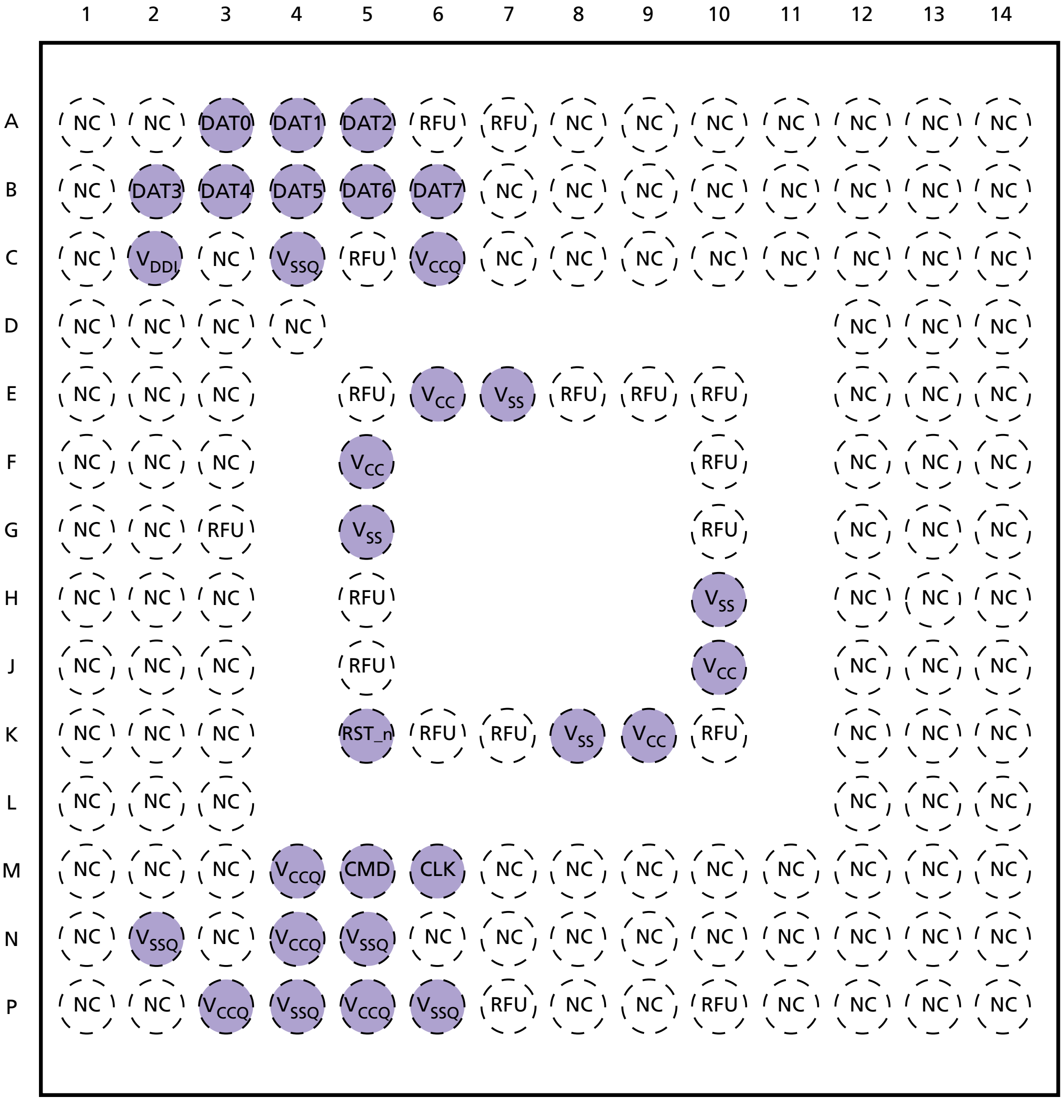
Table 3: Signal Descriptions

Symbol	Type	Description
CLK	Input	Clock: Each cycle of the clock directs a transfer on the command line and on the data line(s). The frequency can vary between the minimum and the maximum clock frequency.
RST_n	Input	Reset: The RST_n signal is used by the host for resetting the device, moving the device to the pre-idle state. By default, the RST_n signal is temporarily disabled in the device. The host must set ECSD register byte 162, bits[1:0] to 0x1 to enable this functionality before the host can use it.
CMD	I/O	Command: This signal is a bidirectional command channel used for command and response transfers. The CMD signal has two bus modes: open-drain mode and push-pull mode (see Operating Modes). Commands are sent from the MMC host to the device, and responses are sent from the device to the host.
DAT[7:0]	I/O	Data I/O: These are bidirectional data signals. The DAT signals operate in push-pull mode. By default, after power-on or assertion of the RST_n signal, only DAT0 is used for data transfer. The MMC controller can configure a wider data bus for data transfer either using DAT[3:0] (4-bit mode) or DAT[7:0] (8-bit mode). e·MMC includes internal pull-up resistors for data lines DAT[7:1]. Immediately after entering the 4-bit mode, the device disconnects the internal pull-up resistors on the DAT[3:1] lines. Upon entering the 8-bit mode, the device disconnects the internal pull-ups on the DAT[7:1] lines.
V_{CC}	Supply	V_{CC}: NAND interface (I/F) I/O and NAND Flash power supply.
V_{CCQ}	Supply	V_{CCQ}: e·MMC controller core and e·MMC I/F I/O power supply.
V_{SS}[1]	Supply	V_{SS}: NAND I/F I/O and NAND Flash ground connection.
V_{SSQ}[1]	Supply	V_{SSQ}: e·MMC controller core and e·MMC I/F ground connection.
V_{DDI}		Internal voltage node: At least a 0.1µF capacitor is required to connect V_{DDI} to ground. A 1µF capacitor is recommended. Do not tie to supply voltage or ground.
NC	–	No connect: No internal connection is present.
RFU	–	Reserved for future use: No internal connection is present. Leave it floating externally.

Note: 1. V_{SS} and V_{SSQ} are connected internally.

153-Ball Signal Assignments

Figure 3: 153-Ball FBGA (top view, ball down)

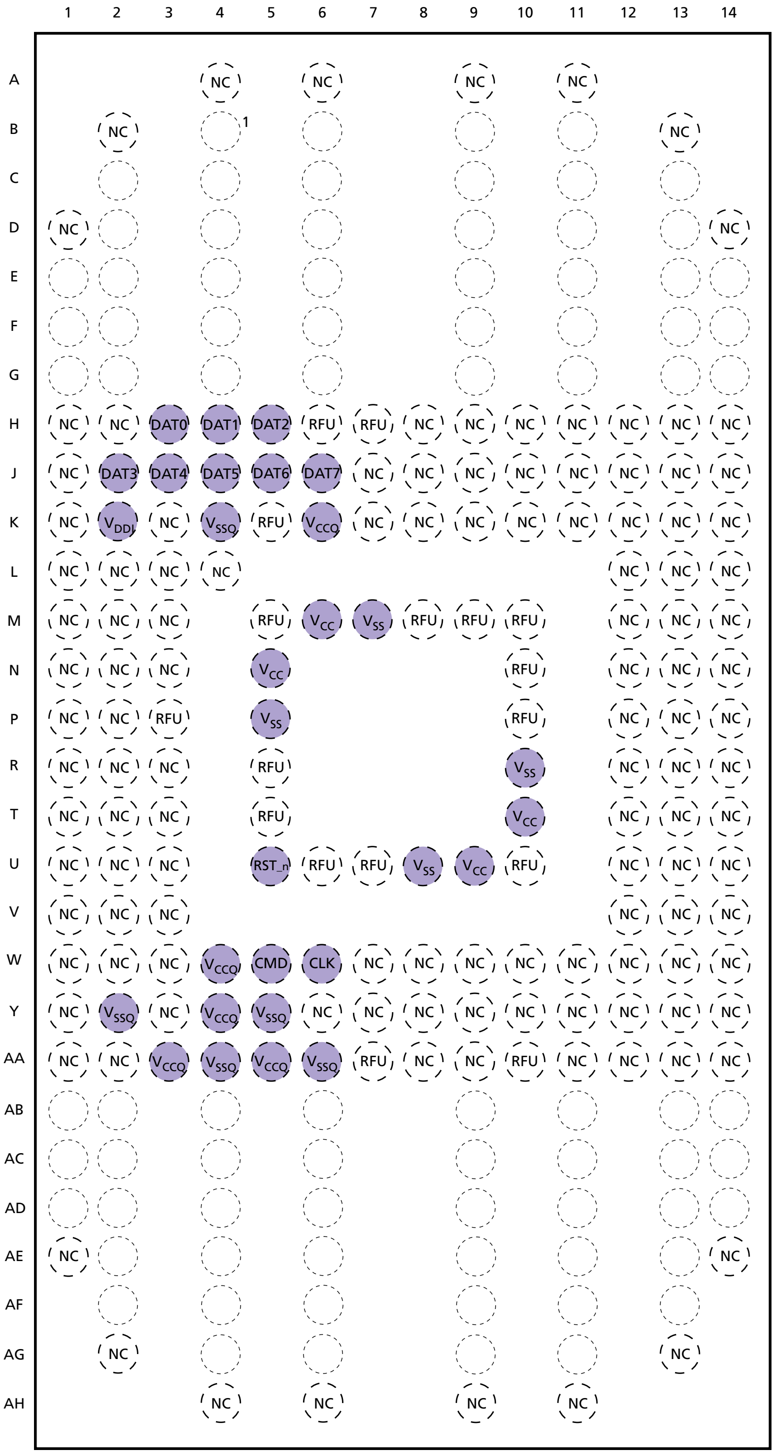


	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC	NC	DAT0	DAT1	DAT2	RFU	RFU	NC	NC	NC	NC	NC	NC	NC
B	NC	DAT3	DAT4	DAT5	DAT6	DAT7	NC	NC	NC	NC	NC	NC	NC	NC
C	NC	V_{DDI}	NC	V_{SSQ}	RFU	V_{CCQ}	NC	NC	NC	NC	NC	NC	NC	NC
D	NC	NC	NC	NC								NC	NC	NC
E	NC	NC	NC		RFU	V_{CC}	V_{SS}	RFU	RFU	RFU		NC	NC	NC
F	NC	NC	NC		V_{CC}					RFU		NC	NC	NC
G	NC	NC	RFU		V_{SS}					RFU		NC	NC	NC
H	NC	NC	NC		RFU					V_{SS}		NC	NC	NC
J	NC	NC	NC		RFU					V_{CC}		NC	NC	NC
K	NC	NC	NC		RST_n	RFU	RFU	V_{SS}	V_{CC}	RFU		NC	NC	NC
L	NC	NC	NC									NC	NC	NC
M	NC	NC	NC	V_{CCQ}	CMD	CLK	NC	NC	NC	NC	NC	NC	NC	NC
N	NC	V_{SSQ}	NC	V_{CCQ}	V_{SSQ}	NC	NC	NC	NC	NC	NC	NC	NC	NC
P	NC	NC	V_{CCQ}	V_{SSQ}	V_{CCQ}	V_{SSQ}	RFU	NC	NC	RFU	NC	NC	NC	NC

Notes:
1. Some test pads on the device are not shown. They are not solder balls and are for Micron internal use only.
2. Some previous versions of the JEDEC product or mechanical specification had defined reserved for future use (RFU) balls as no connect (NC) balls. NC balls assigned in the previous specifications could have been connected to ground on the system board. To enable new feature introduction, some of these balls are assigned as RFU in the v4.4 mechanical specification. Any new PCB footprint implementations should use the new ball assignments and leave the RFU balls floating on the system board.

169-Ball Signal Assignments

Figure 4: 169-Ball FBGA (top view, ball down)



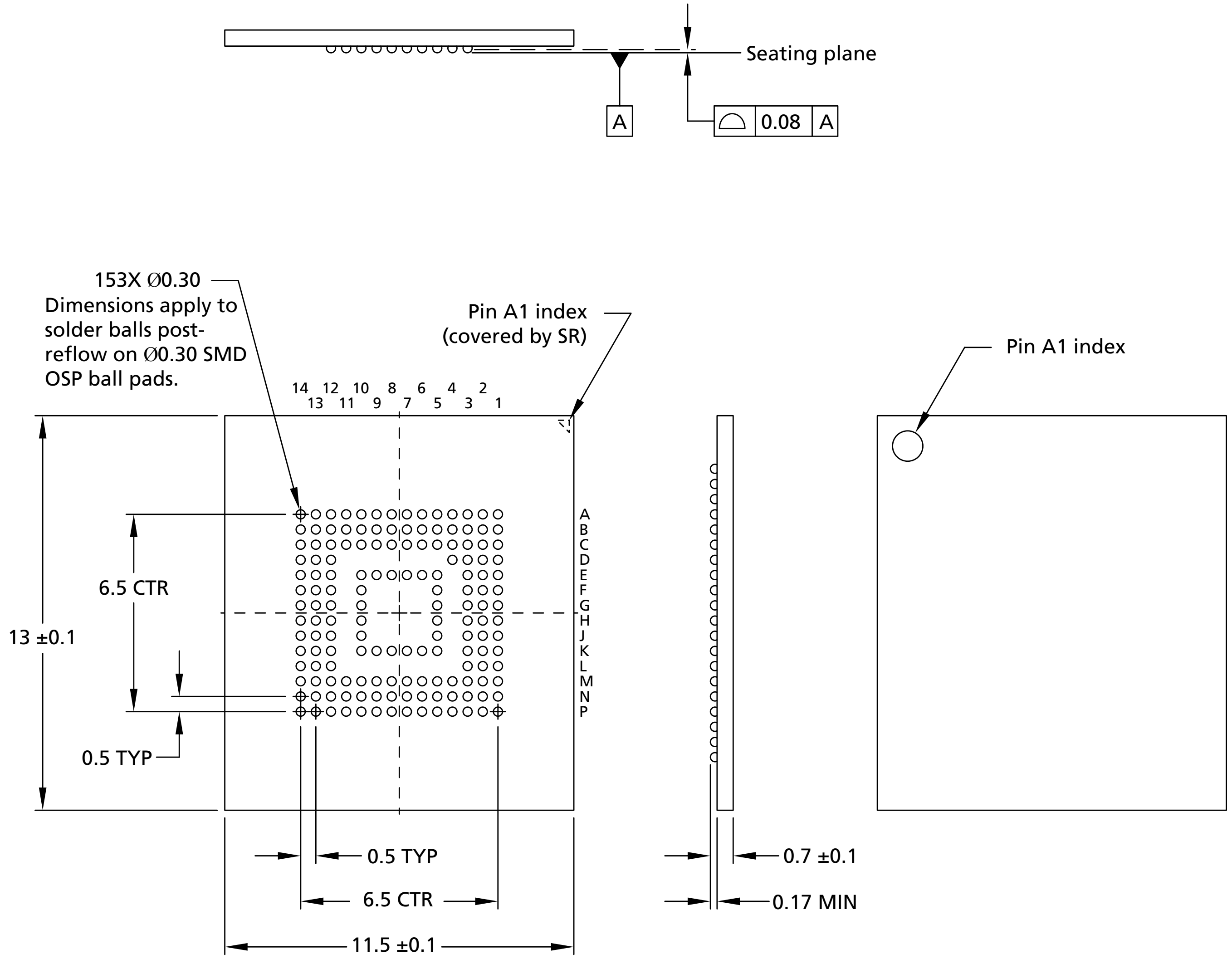
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A				NC		NC			NC		NC			
B		NC		[1]									NC	
C														
D	NC													NC
E														
F														
G														
H	NC	NC	DAT0	DAT1	DAT2	RFU	RFU	NC	NC	NC	NC	NC	NC	NC
J	NC	DAT3	DAT4	DAT5	DAT6	DAT7	NC	NC	NC	NC	NC	NC	NC	NC
K	NC	V_{DDI}	NC	V_{SSQ}	RFU	V_{CCQ}	NC	NC	NC	NC	NC	NC	NC	NC
L	NC	NC	NC	NC								NC	NC	NC
M	NC	NC	NC		RFU	V_{CC}	V_{SS}	RFU	RFU	RFU		NC	NC	NC
N	NC	NC	NC		V_{CC}					RFU		NC	NC	NC
P	NC	NC	RFU		V_{SS}					RFU		NC	NC	NC
R	NC	NC	NC		RFU					V_{SS}		NC	NC	NC
T	NC	NC	NC		RFU					V_{CC}		NC	NC	NC
U	NC	NC	NC		RST_n	RFU	RFU	V_{SS}	V_{CC}	RFU		NC	NC	NC
V	NC	NC	NC									NC	NC	NC
W	NC	NC	NC	V_{CCQ}	CMD	CLK	NC	NC	NC	NC	NC	NC	NC	NC
Y	NC	V_{SSQ}	NC	V_{CCQ}	V_{SSQ}	NC	NC	NC	NC	NC	NC	NC	NC	NC
AA	NC	NC	V_{CCQ}	V_{SSQ}	V_{CCQ}	V_{SSQ}	RFU	NC	NC	RFU	NC	NC	NC	NC
AB														
AC														
AD														
AE	NC													NC
AF														
AG		NC											NC	
AH				NC		NC			NC		NC			

Notes: 1. Empty balls do not denote actual solder balls; they are position indicators only.

2. Some test pads on the device are not shown. They are not solder balls and are for Micron internal use only.
3. Some previous versions of the JEDEC product or mechanical specification had defined reserved for future use (RFU) balls as no connect (NC) balls. NC balls assigned in the previous specifications could have been connected to ground on the system board. To enable new feature introduction, some of these balls are assigned as RFU in the v4.4 mechanical specification. Any new PCB footprint implementations should use the new ball assignments and leave the RFU balls floating on the system board.

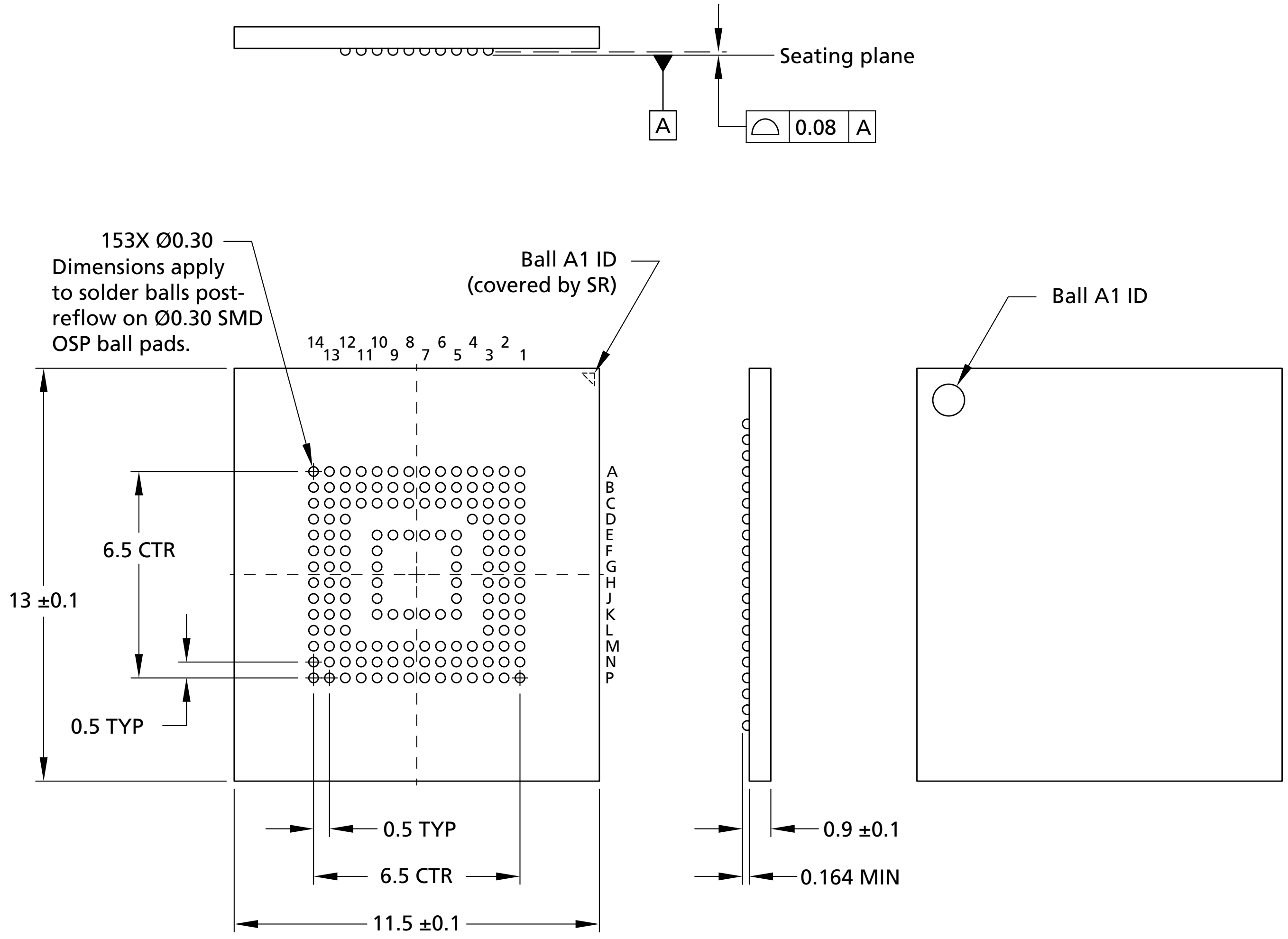
Package Dimensions

Figure 5: 153-Ball WFBGA – 11.5mm x 13.0mm x 0.8mm (Package Code: EA)



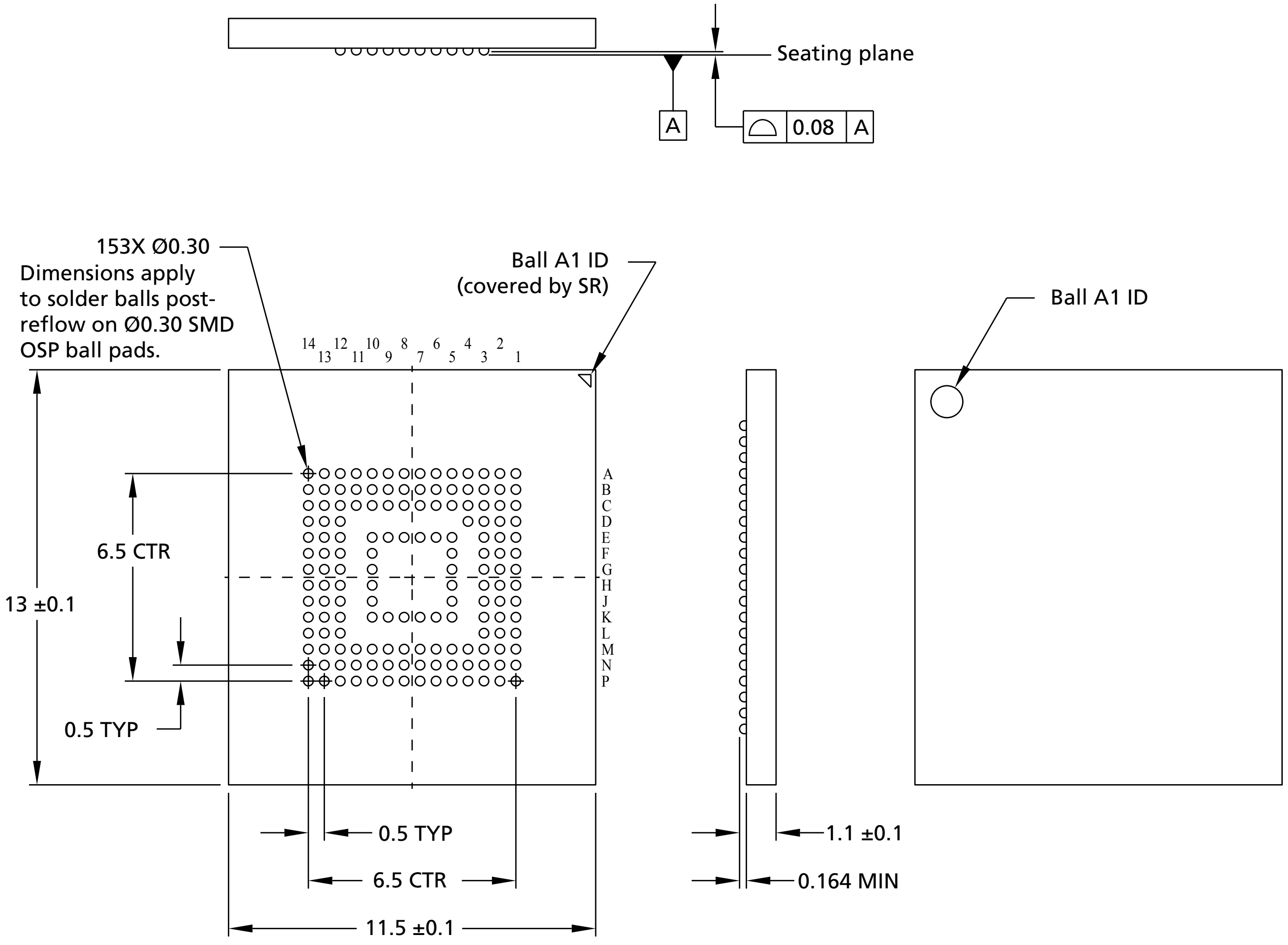
Note: 1. Dimensions are in millimeters.

Figure 6: 153-Ball VFBGA – 11.50mm x 13.00mm x 1.00mm (Package Code: AM)



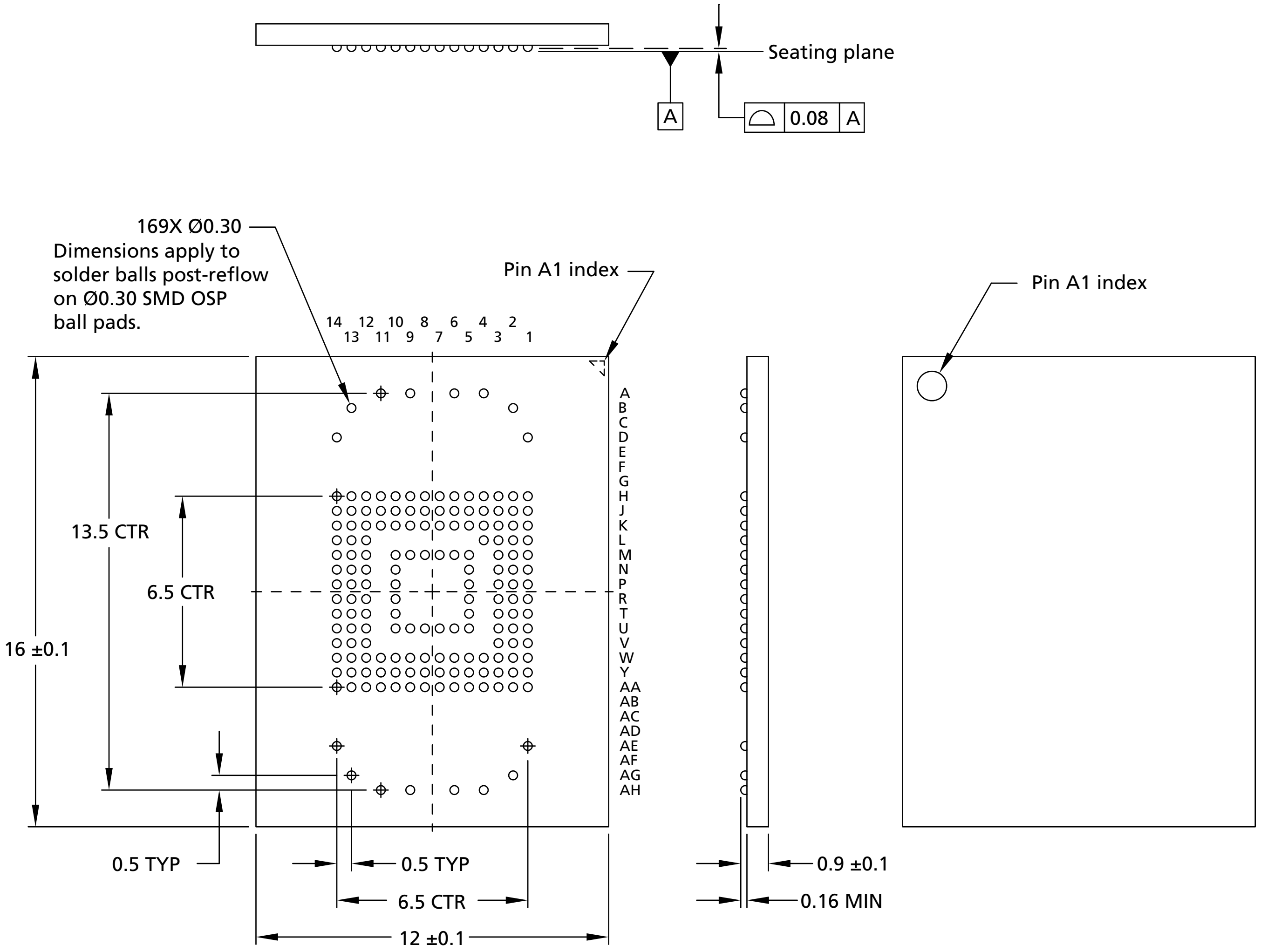
Note: 1. Dimensions are in millimeters.

Figure 7: 153-Ball TFBGA – 11.50mm x 13.00mm x 1.2mm (Package Code: DM)



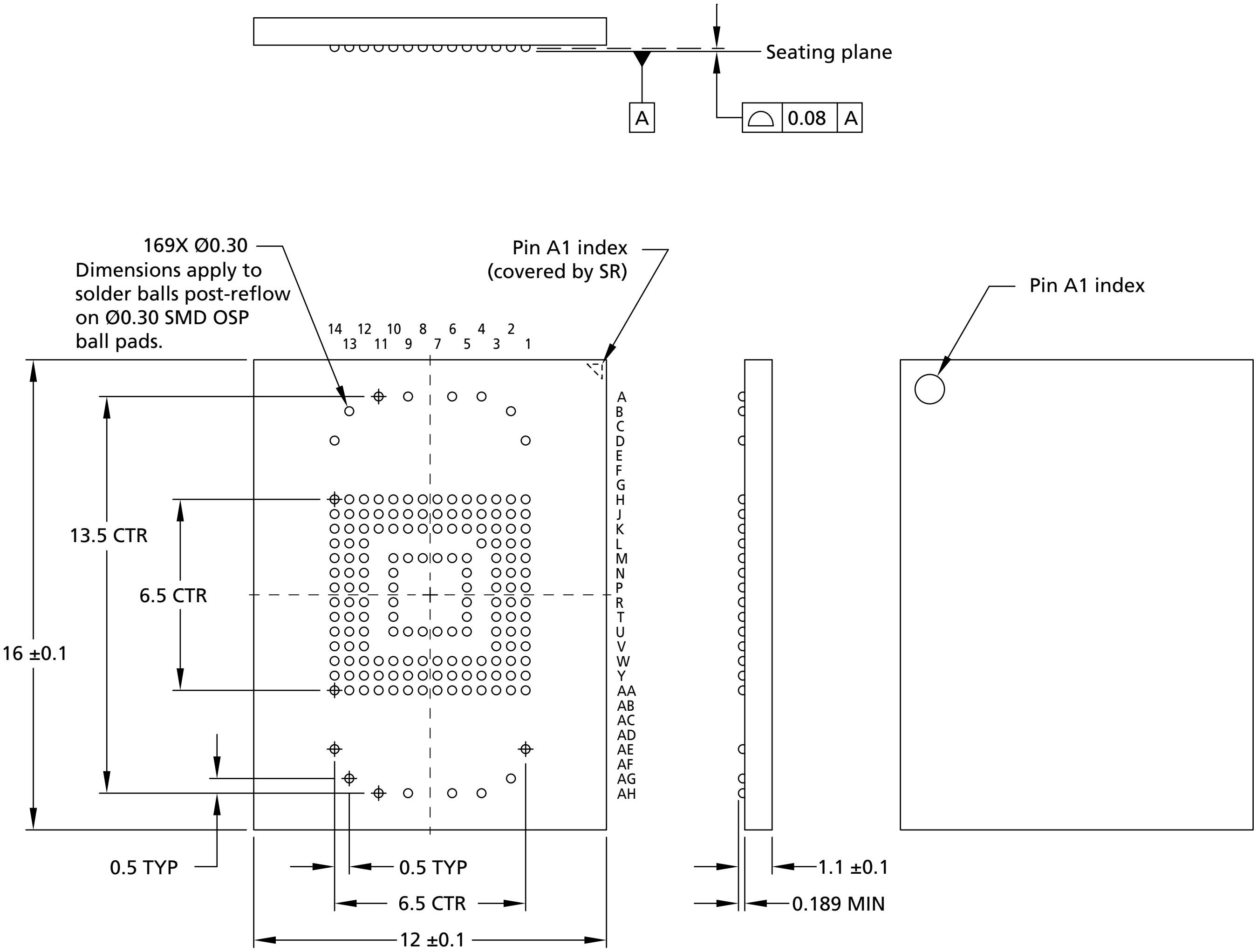
Note: 1. Dimensions are in millimeters.

Figure 8: 169-Ball VFBGA – 12.0mm x 16.00mm x 1.0mm (Package Code: DV)



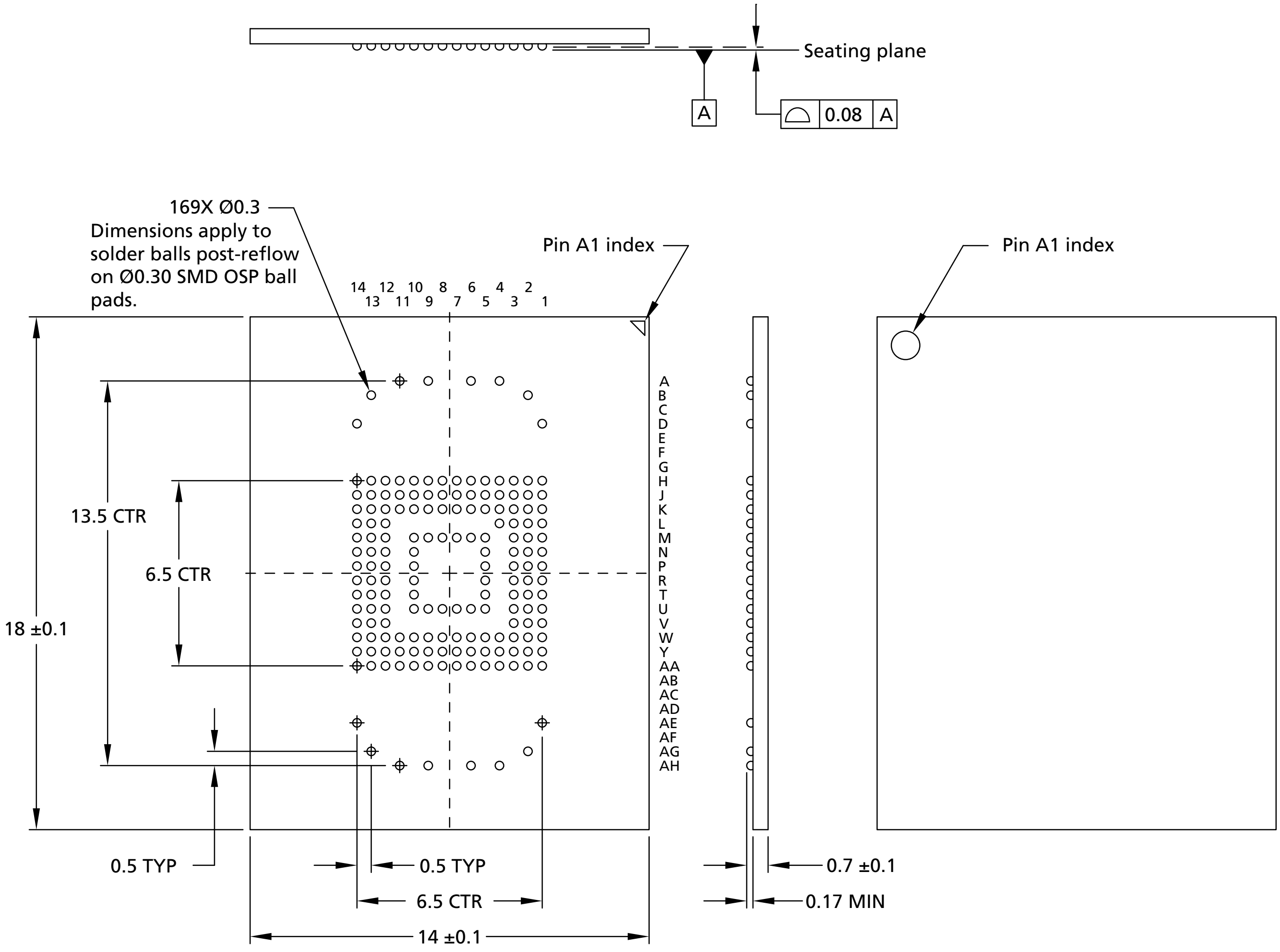
Note: 1. Dimensions are in millimeters.

Figure 9: 169-Ball TFBGA – 12.0mm x 16.00mm x 1.2mm (Package Code: DI)



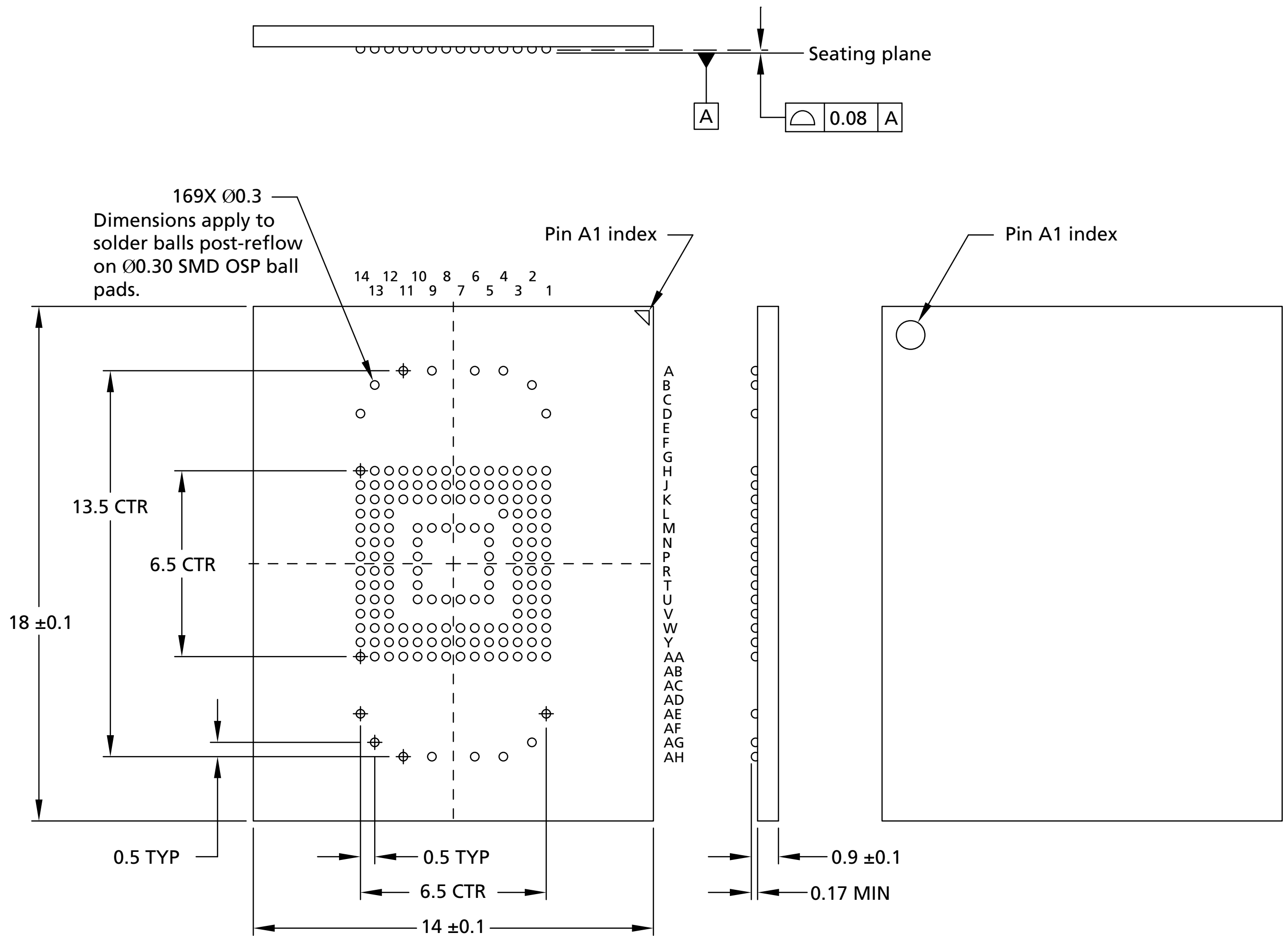
Note: 1. Dimensions are in millimeters.

Figure 10: 169-Ball WFBGA – 14.0mm x 18.00mm x 0.8mm (Package Code: EC)



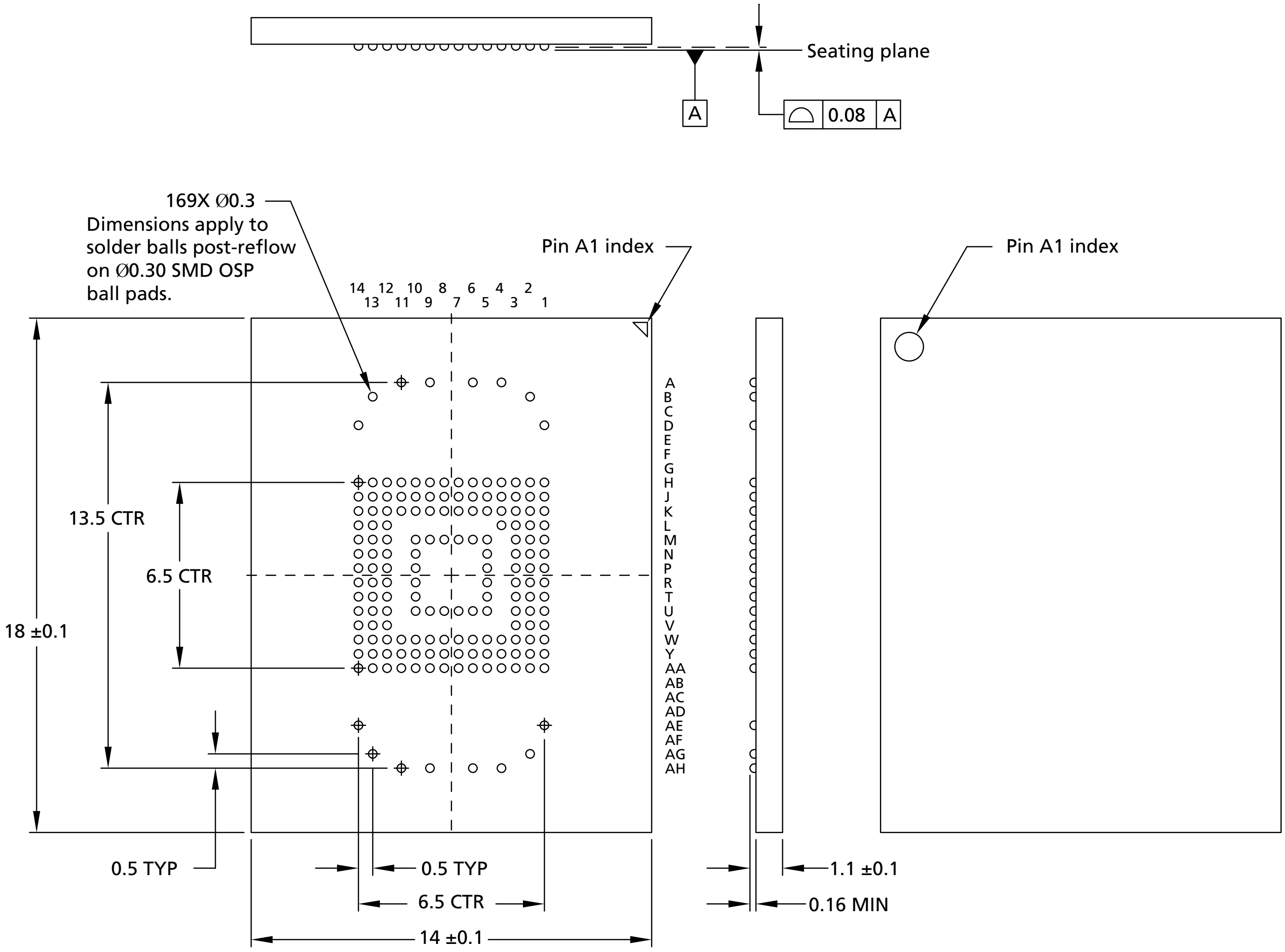
Note: 1. Dimensions are in millimeters.

Figure 11: 169-Ball VFBGA – 14.0mm x 18.00mm x 1.0mm (Package Code: ED)



Note: 1. Dimensions are in millimeters.

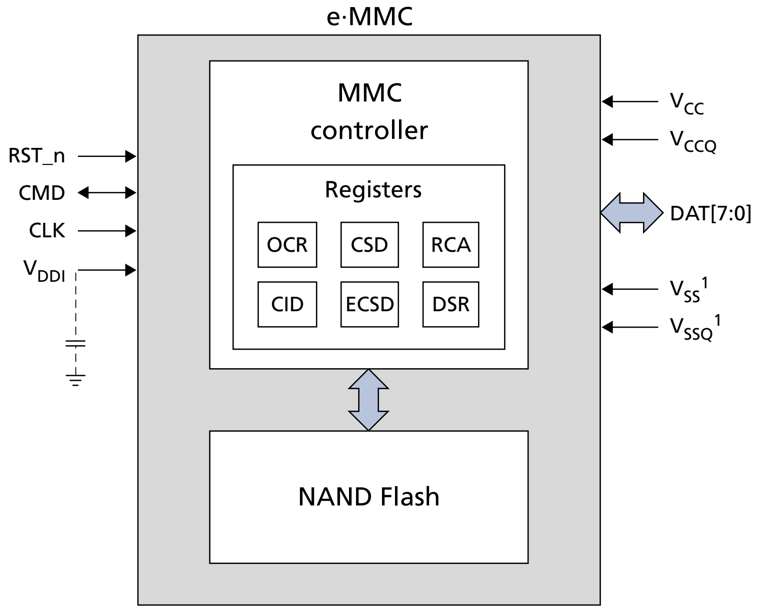
Figure 12: 169-Ball TFBGA – 14.0mm x 18.00mm x 1.2mm (Package Code: EF)



Note: 1. Dimensions are in millimeters.

Architecture

Figure 13: e·MMC Functional Block Diagram



Note: 1. V_{SS} and V_{SSQ} are internally connected.

MMC Protocol Independent of NAND Flash Technology

The MMC specification defines the communication protocol between a host and a device. The protocol is independent of the NAND Flash features included in the device. The device has an intelligent on-board controller that manages the MMC communication protocol.

The controller also handles block management functions such as logical block allocation and wear leveling. These management functions require complex algorithms and depend entirely on NAND Flash technology (generation or memory cell type).

The device handles these management functions internally, making them invisible to the host processor.

Defect and Error Management

Micron *e*·MMC incorporates advanced technology for defect and error management. If a defective block is identified, the device completely replaces the defective block with one of the spare blocks. This process is invisible to the host and does not affect data space allocated for the user.

The device also includes a built-in error correction code (ECC) algorithm to ensure that data integrity is maintained.

To make the best use of these advanced technologies and ensure proper data loading and storage over the life of the device, the host must exercise the following precautions:

- Check the status after WRITE, READ, and ERASE operations.
- Avoid power-down during WRITE and ERASE operations.

CID Register

The card identification (CID) register is 128 bits wide. It contains the device identification information used during the card identification phase as required by *e*·MMC protocol. Each device is created with a unique identification number.

Table 4: CID Register Field Parameters

Name	Field	Width	CID Bits	CID Value
Manufacturer ID	MID	8	[127:120]	FEh
Reserved	–	6	[119:114]	–
Card/BGA	CBX	2	[113:112]	01h
OEM/application ID	OID	8	[111:104]	–
Product name	PNM	48	[103:56]	–
Product revision	PRV	8	[55:48]	–
Product serial number	PSN	32	[47:16]	–
Manufacturing date	MDT	8	[15:8]	–
CRC7 checksum	CRC	7	[7:1]	–
Not used; always 1	–	1	0	–

CSD Register

The card-specific data (CSD) register provides information about accessing the device contents. The CSD register defines the data format, error correction type, maximum data access time, and data transfer speed, as well as whether the DS register can be used. The programmable part of the register (entries marked with W or E in the following table) can be changed by the PROGRAM_CSD (CMD27) command.

Table 5: CSD Register Field Parameters

Name	Field		Width	Cell Type[1]	CSD Bits	CSD Value
CSD structure	CSD_STRUCTURE		2	R	[127:126]	3h
System specification version	SPEC_VERS		4	R	[125:122]	4h
Reserved[2]	–		2	TBD	[121:120]	–
Data read access time 1	TAAC		8	R	[119:112]	4Fh
Data read access time 2 in CLK cycles (NSAC × 100)	NSAC		8	R	[111:104]	01h
Maximum bus clock frequency	TRAN_SPEED		8	R	[103:96]	32h
Card command classes	CCC		12	R	[95:84]	0F5h
Maximum read data block length	READ_BL_LEN	MTFC2GMTEA	4	R	[83:80]	Ah
		MTFC4GMTEA, MTFC8GLTEA, MTFC16GLTAM, MTFC16GLTDV, MTFC16GJTEC, MTFC32GLTDM, MTFC32GLTDI, MTFC32GJTED, MTFC64GJTEF				9h
Partial blocks for reads supported	READ_BL_PARTIAL		1	R	79	0h
Write block misalignment	WRITE_BLK_MISALIGN		1	R	78	0h
Read block misalignment	READ_BLK_MISALIGN	MTFC2GMTEA	1	R	77	1h
		MTFC4GMTEA, MTFC8GLTEA, MTFC16GLTAM, MTFC16GLTDV, MTFC16GJTEC, MTFC32GLTDM, MTFC32GLTDI, MTFC32GJTED, MTFC64GJTEF				0h
DS register implemented	DSR_IMP		1	R	76	1h
Reserved	–		2	R	[75:74]	–

Table 5: CSD Register Field Parameters (Continued)

Name	Field		Width	Cell Type[1]	CSD Bits	CSD Value
Device size	C_SIZE	MTFC2GMTEA	12	R	[73:62]	EAFh
		MTFC4GMTEA, MTFC8GLTEA, MTFC16GLTAM, MTFC16GLTDV, MTFC16GJTEC, MTFC32GLTDM, MTFC32GLTDI, MTFC32GJTED, MTFC64GJTEF				FFFh
Maximum read current at $V_{DD,min}$	VDD_R_CURR_MIN		3	R	[61:59]	7h
Maximum read current at $V_{DD,max}$	VDD_R_CURR_MAX		3	R	[58:56]	7h
Maximum write current at $V_{DD,min}$	VDD_W_CURR_MIN		3	R	[55:53]	7h
Maximum write current at $V_{DD,max}$	VDD_W_CURR_MAX		3	R	[52:50]	7h
Device size multiplier	C_SIZE_MULT		3	R	[49:47]	7h
Erase group size	ERASE_GRP_SIZE		5	R	[46:42]	1Fh
Erase group size multiplier	ERASE_GRP_MULT		5	R	[41:37]	1Fh
Write protect group size	WP_GRP_SIZE	MTFC2GMTEA	5	R	[36:32]	03h
		MTFC4GMTEA				07h
		MTFC8GLTEA				0Fh
		MTFC16GLTAM, MTFC16GLTDV, MTFC16GJTEC, MTFC32GLTDM, MTFC32GLTDI, MTFC32GJTED, MTFC64GJTEF				1Fh
Write protect group enable	WP_GRP_ENABLE		1	R	31	1h
Manufacturer default ECC	DEFAULT_ECC		2	R	[30:29]	00h
rite-speed factor	R2W_FACTOR		3	R	[28:26]	02h
Maximum write data block length	WRITE_BL_LEN		4	R	[25:22]	09h
Partial blocks for writes supported	WRITE_BL_PARTIAL		1	R	21	0h
Reserved	–		4	R	[20:17]	–
Content protection application	CONTENT_PROT_APP		1	R	16	0h
File-format group	FILE_FORMAT_GRP		1	R/W	15	0h
Copy flag (OTP)	COPY		1	R/W	14	0h
Permanent write protection	PERM_WRITE_PROTECT		1	R/W	13	0h
Temporary write protection	TMP_WRITE_PROTECT		1	R/W/E	12	0h
File format	FILE_FORMAT		2	R/W	[11:10]	00h
ECC	ECC		2	R/W/E	[9:8]	00h

Table 5: CSD Register Field Parameters (Continued)

Name	Field	Width	Cell Type[1]	CSD Bits	CSD Value
CRC	CRC	7	R/W/E	[7:1]	–
Not used; always 1	–	1	–	0	1h

Notes:
1. R = Read-only

   R/W = One-time programmable and readable

   R/W/E = Multiple writable with value kept after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable

   TBD = To be determined
2. Reserved bits should be read as 0.

ECSD Register

The 512-byte extended card-specific data (ECSD) register defines device properties and selected modes. The most significant 320 bytes are the properties segment. This segment defines device capabilities and cannot be modified by the host. The lower 192 bytes are the modes segment. The modes segment defines the configuration in which the device is working. The host can change the properties of modes segments using the SWITCH command.

Table 6: ECSD Register Field Parameters

Name	Field		Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Value
Properties Segment						
Reserved[2]	–		7	–	[511:505]	–
Supported command sets	S_CMD_SET		1	R	504	1h
HPI features	HPI_FEATURES		1	R	503	3h
Background operations support	BKOPS_SUPPORT		1	R	502	1h
Reserved	–		255	–	[501:247]	–
Background operations status	BKOPS_STATUS		1	R	246	00h
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM		4	R	[245:242]	–
First initialization time after partitioning (first CMD1 to device ready)	INI_TIMEOUT_AP	MTFC2GMTEA	1	R	241	7Ch
		MTFC4GMTEA				7Ah
		MTFC8GLTEA MTFC16GJTEC				F6h
		MTFC16GLTAM MTFC16GLTDV MTFC32GLTDM MTFC32GLTDI MTFC32GJTED MTFC64GJTEF				FFh
Reserved	–		1	–	240	–
Power class for 52 MHz, DDR at 3.6V[3]	PWR_CL_DDR_52_360		1	R	239	00h
Power class for 52 MHz, DDR at 1.95V[3]	PWR_CL_DDR_52_195		1	R	238	00h
Reserved	–		2	–	[237:236]	–
Minimum write performance for 8-bit at 52 MHz in DDR mode	MIN_PERF_DDR_W_8_52		1	R	235	00h
Minimum read performance for 8-bit at 52 MHz in DDR mode	MIN_PERF_DDR_R_8_52		1	R	234	00h
Reserved	–		1	–	233	–

Table 6: ECSD Register Field Parameters (Continued)

Name	Field		Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Value
TRIM multiplier	TRIM_MULT	MTFC2GMTEA MTFC4GMTEA MTFC8GLTEA MTFC16GLTAM MTFC16GLTDV MTFC32GLTDM MTFC32GLTDI	1	R	232	06h
		MTFC16GJTEC MTFC32GJTED MTFC64GJTEF				0Fh
Secure feature support	SEC_FEATURE_SUPPORT		1	R	231	15h
SECURE ERASE multiplier	SEC_ERASE_MULT	MTFC2GMTEA MTFC4GMTEA MTFC8GLTEA MTFC16GLTAM MTFC16GLTDV MTFC32GLTDM MTFC32GLTDI	1	R	230	02h
		MTFC16GJTEC MTFC32GJTED MTFC64GJTEF				06h
SECURE TRIM multiplier	SEC_TRIM_MULT	MTFC2GMTEA MTFC4GMTEA MTFC8GLTEA MTFC16GLTAM MTFC16GLTDV MTFC32GLTDM MTFC32GLTDI	1	R	229	03h
		MTFC16GJTEC MTFC32GJTED MTFC64GJTEF				09h
Boot information	BOOT_INFO		1	R	228	07h
Reserved	–		1	–	227	–
Boot partition size	BOOT_SIZE_MULT	MTFC2GMTEA	1	R	226	08h
		MTFC4GMTEA MTFC8GLTEA				10h
		MTFC16GLTAM MTFC16GLTDV MTFC16GJTEC				20h
		MTFC32GLTDM MTFC32GLTDI MTFC32GJTED MTFC64GJTEF				40h

Table 6: ECSD Register Field Parameters (Continued)

Name	Field		Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Value
Access size	ACC_SIZE	MTFC2GMTEA	1	R	225	05h
		MTFC4GMTEA MTFC8GLTEA MTFC16GLTAM MTFC16GLTDV MTFC32GLTDM MTFC32GLTDI				06h
		MTFC16GJTEC MTFC32GJTED MTFC64GJTEF				07h
High-capacity erase unit size	HC_ERASE_GRP_SIZE	MTFC2GMTEA	1	R	224	00h
		MTFC4GMTEA MTFC8GLTEA MTFC16GLTAM MTFC16GLTDV MTFC32GLTDM MTFC32GLTDI				08h
		MTFC16GJTEC MTFC32GJTED MTFC64GJTEF				10h
High-capacity erase timeout	ERASE_TIMEOUT_MULT		1	R	223	01h
Reliable write-sector count	REL_WR_SEC_C		1	R	222	08h
High-capacity write protect group size	HC_WP_GRP_SIZE	MTFC2GMTEA	1	R	221	00h
		MTFC4GMTEA				01h
		MTFC8GLTEA, MTFC16GJTEC				02h
		MTFC16GLTAM MTFC16GLTDV MTFC32GJTED				04h
		MTFC32GLTDM MTFC32GLTDI MTFC64GJTEF				08h
Sleep current (V_{CC})	S_C_VCC		1	R	220	08h
Sleep current (V_{CCQ})	S_C_VCCQ		1	R	219	08h
Reserved	–		1	–	218	–
Sleep/awake timeout	S_A_TIMEOUT		1	R	217	10h
Reserved	–		1	–	216	–

Table 6: ECSD Register Field Parameters (Continued)

Name	Field		Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Value
Sector count	SEC_COUNT	MTFC2GMTEA	4	R	[215:212]	00000000h
		MTFC4GMTEA				0072C000h
		MTFC8GLTEA				00EA8000h
		MTFC16GLTAM MTFC16GLTDV				01DA0000h
		MTFC16GJTEC				01D50000h
		MTFC32GLTDM MTFC32GLTDI				03B80000h
		MTFC32GJTED				03B40000h
		MTFC64GJTEF				07700000h
Reserved	–		1	–	211	–
Minimum write performance for 8-bit at 52 MHz	MIN_PERF_W_8_52		1	R	210	08h
Minimum read performance for 8-bit at 52 MHz	MIN_PERF_R_8_52		1	R	209	08h
Minimum write performance for 8-bit at 26 MHz and 4-bit at 52 MHz	MIN_PERF_W_8_26_4_52		1	R	208	08h
Minimum read performance for 8-bit at 26 MHz and 4-bit at 52 MHz	MIN_PERF_R_8_26_4_52		1	R	207	08h
Minimum write performance for 4-bit at 26 MHz	MIN_PERF_W_4_26		1	R	206	08h
Minimum read performance for 4-bit at 26 MHz	MIN_PERF_R_4_26		1	R	205	08h
Reserved	–		1	–	204	–
Power class for 26 MHz at 3.6V[3]	PWR_CL_26_360		1	R	203	00h
Power class for 52 MHz at 3.6V[3]	PWR_CL_52_360		1	R	202	00h
Power class for 26 MHz at 1.95V[3]	PWR_CL_26_195		1	R	201	00h
Power class for 52 MHz at 1.95V[3]	PWR_CL_52_195		1	R	200	00h
Partition switching timing	PARTITION_SWITCH_TIME		1	R	199	01h
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	MTFC2GMTEA MTFC4GMTEA	1	R	198	02h
		MTFC8GLTEA MTFC16GLTAM MTFC16GLTDV MTFC16GJTEC MTFC32GLTDM MTFC32GLTDI MTFC32GJTED MTFC64GJTEF				05h
Reserved	–		1	–	197	–

Table 6: ECSD Register Field Parameters (Continued)

Name	Field	Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Value
Card type	CARD_TYPE	1	R	196	07h
Reserved	–	1	–	195	–
CSD structure version	CSD_STRUCTURE	1	R	194	2h
Reserved	–	1	–	193	–
Extended CSD revision	EXT_CSD_REV	1	R	192	5h
Modes Segment					
Command set	CMD_SET	1	R/W/E_P	191	0h
Reserved	–	1	–	190	–
Command set revision	CMD_SET_REV	1	R	189	00h
Reserved	–	1	–	188	–
Power class	POWER_CLASS	1	R/W/E_P	187	00h
Reserved	–	1	–	186	–
High-speed interface timing	HS_TIMING	1	R/W/E_P	185	00h
Reserved	–	1	–	184	–
Bus width mode	BUS_WIDTH	1	W/E_P	183	00h
Reserved	–	1	–	182	–
Erased memory content	ERASED_MEM_CONT	1	R	181	00h
Reserved	–	1	–	180	–
Partition configuration	PARTITION_CONFIG	1	R/W/E, R/W/E_P	179	00h
Boot configuration protection	BOOT_CONFIG_PROT	1	R/W, R/W/C_P	178	00h
Boot bus width	BOOT_BUS_WIDTH	1	R/W/E	177	00h
Reserved	–	1	–	176	–
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	175	00h
Reserved	–	1	–	174	–
Boot area write protection register	BOOT_WP	1	R/W, R/W/C_P	173	00h
Reserved	–	1	–	172	–
User write protection register	USER_WP	1	R/W, R/W/C_P, R/W/E_P	171	00h
Reserved	–	1	–	170	–
Firmware configuration	FW_CONFIG	1	R/W	169	00h
RPMB size	RPMB_SIZE_MULT	1	R	168	01h
Write reliability setting register[3]	WR_REL_SET	1	R/W	167	1Fh
Write reliability parameter register	WR_REL_PARAM	1	R	166	00h
Reserved	–	1	–	165	–

Table 6: ECSD Register Field Parameters (Continued)

Name	Field		Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Value
Manually start background operations	BKOPS_START		1	W/E_P	164	–
Enable background operations handshake	BKOPS_EN		1	R/W	163	00h
Hardware reset function	RST_n_FUNCTION		1	R/W	162	00h
HPI management	HPI_MGMT		1	R/W/E_P	161	00h
Partitioning support	PARTITIONING_SUPPORT		1	R	160	03h
Maximum enhanced area size	MAX_ENH_SIZE_MULT	MTFC2GMTEA	3	R	[159:157]	0001D6h
		MTFC4GMTEA				0001CBh
		MTFC8GLTEA MTFC16GJTEC				0001D5h
		MTFC16GLTAM MTFC16GLTDV MTFC32GJTED				0001DAh
		MTFC32GLTDM MTFC32GLTDI MTFC64GJTEF				0001DCh
Partitions attribute	PARTITIONS_ATTRIBUTE		1	R/W	156	00h
Partitioning setting	PARTITION_SETTING_COMPLETED		1	R/W	155	00h
General-purpose partition size	GP_SIZE_MULT_GP3		12	R/W	[154:152]	000000h
	GP_SIZE_MULT_GP2				[151:149]	
	GP_SIZE_MULT_GP1				[148:146]	
	GP_SIZE_MULT_GP0				[145:143]	
Enhanced user data area size	ENH_SIZE_MULT		3	R/W	[142:140]	000000h
Enhanced user data start address	ENH_START_ADDR		4	R/W	[139:136]	00000000h
Reserved	–		1	–	135	–
Bad block management mode	SEC_BAD_BLK_MGMNT		1	R/W	134	00h
Reserved	–		134	–	[133:0]	–

Notes: 1. R = Read-only

R/W = One-time programmable and readable

R/W/E = Multiple writable with the value kept after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable

R/W/C_P = Writable after the value is cleared by a power cycle and assertion of the RST_n signal (the value not cleared by CMD0 reset) and readable

R/W/E_P = Multiple writable with the value reset after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable

W/E_P = Multiple writable with the value reset after power cycle, assertion of the RST_n signal, and any CMD0 reset, and not readable

TBD = To be determined

2. Reserved bits should be read as 0.
3. Micron has tested power failure under best application knowledge conditions with positive results. Customers may request a dedicated test for their specific application condition.

DC Electrical Specifications – Device Power

The device current consumption for various device configurations is defined in the power class fields of the ECSD register.

V_{CC} is used for the NAND Flash device and its interface voltage; V_{CCQ} is used for the controller and the *e*·MMC interface voltage.

Figure 14: Device Power Diagram

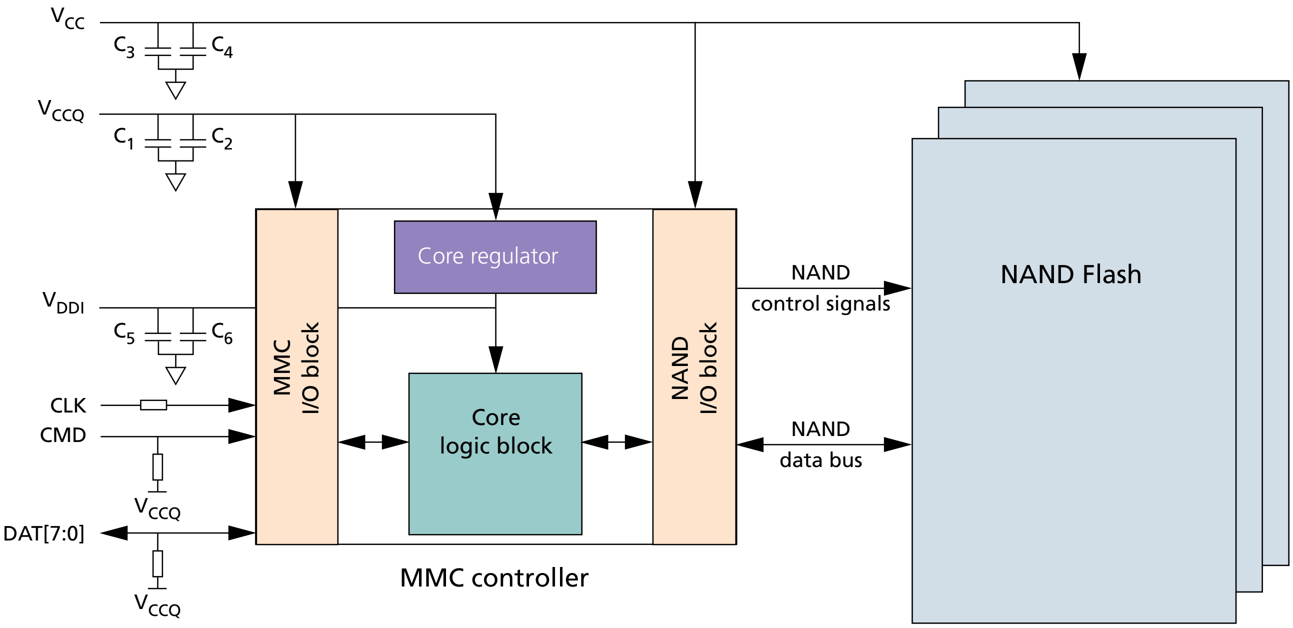


Table 7: Power Domains

Parameter	Symbol	Comments
Host interface	V_{CCQ}	High voltage range = 3.3V (nominal) Low voltage range = 1.8V (nominal)
Memory	V_{CC}	High voltage range = 3.3V (nominal)
Internal	V_{DDi}	The internal regulator connection to an external decoupling capacitor

Table 8: Capacitor and Resistance Specifications

Parameter	Symbol	Min	Max	Typ	Units	Notes
Pull-up resistance: CMD	R_CMD	4.7	50	10	kΩ	1
Pull-up resistance: DAT[7:0]	R_DAT	10	50	50	kΩ	1
Pull-up resistance: RST_n	R_RST_n	4.7	50	50	kΩ	2
CLK/CMD/DAT[7:0] impedance		45	55	50	Ω	3
Serial resistance on CLK	SR_CLK	0	47	22	Ω	

Table 8: Capacitor and Resistance Specifications (Continued)

Parameter	Symbol	Min	Max	Typ	Units	Notes
V_{DDQ} capacitor	C1, C2	2.2 ±0.1	4.7 ±0.22	2.2 ±0.1	µF	4
V_{DD} capacitor (≤8GB)	C3, C4	2.2 ±0.1	4.7 ±0.22	2.2 ±0.1	µF	5
V_{DD} capacitor (>8GB)				4.7 ±0.22	µF	
V_{DDi} capacitor (C_{reg})	C5, C6	1	4.7 ±0.1	1 ±0.1	µF	6

Notes:
1. Used to prevent bus floating.
2. If host does not use H/W RESET (RST_n), pull-up resistance is not needed on RST_n line (Extended CSD register [162] = 0 b).
3. Impedance match.
4. The coupling capacitor should be connected with V_{DDQ} and V_{SSQ} as closely as possible.
5. The coupling capacitor should be connected with V_{DD} and V_{SS} as closely as possible.
6. The coupling capacitor should be connected with V_{DDi} and V_{SSi} as closely as possible.

Revision History

Rev. B – 3/12

- Updated CSD and ESCD register values

Rev. A – 1/12

- Initial release.

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
www.micron.com/productsupport Customer Comment Line: 800-932-4992

This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.