9100 U.2 and HHHL NVMe PCIe SSDs

MTFDHAL800MCE, MTFDHAL1T6MCE, MTFDHAL3T2MCE, MTFDHAL1T2MCF, MTFDHAL2T4MCF, MTFDHAX800MCE, MTFDHAX1T6MCE, MTFDHAX3T2MCE, MTFDHAX1T2MCF, MTFDHAX2T4MCF

Features

- Micron® 16nm MLC NAND Flash
- PCIe® Gen3: HHHL x4; U.2 x4
- NVMe™ 1.1b, plus Command Effects Log
- Capacity[1]
  - 9100 PRO: 800GB, 1.6TB, 3.2TB
  - 9100 MAX: 1.2TB, 2.4TB
- Endurance (total bytes written)
  - 800GB: Up to 2.4PB
  - 1.2TB: Up to 4.8PB
  - 1.6TB: Up to 4.8PB
  - 2.4TB: Up to 9.6PB
  - 3.2TB: Up to 9.6PB
- Industry-standard 512- and 4096-byte sector sizes
- Power: ~7W idle, selectable 20W, 25W or unlimited (30W MAX)
- Surprise insertion/surprise removal (SISR) and hot-plug capable (U.2 form factor only)
- Power-backed cache
- Steady state performance[2] (varies by capacity and form factor)
  - Sequential 128KB read: 3.0 GB/s
  - Sequential 128KB write: 2.0 GB/s
  - Random 4KB read: 750,000 IOPS
  - Random 4KB write: 300,000 IOPS
- Latency to media performance, typical (QD = 1)
  - READ: 120µs, WRITE: 30µs
- Reliability
  - MTBF: 2 million hours[3]
  - Field-upgradable firmware
  - UBER: <1 sector per 10^{17} bits read
- NVMe-MI 1.0 over SMBus for drive management
- SMART command set support
- Temperature[4]
  - 0°C to 85°C SMART temperature
  - 0°C to 55°C ambient
  - Temperature protection
- Mechanical/electrical
  - U.2: 69.85 x 15.00 x 100.5mm, 12V (-6%/+8%)
  - HHHL: 68.9 x 18.71 x 167.65mm, 12V (-6%/+8%)
- Shock
  - U.2: 1000G/1ms
  - HHHL: 500G /1ms
- Vibration: 3.1 G_{RMS} 5–800Hz @ 30 min/axis

Controller Features

- NVMe controller
  - Number of queues: 128 SQ/CQ pairs
  - Round robin arbitration
- Interrupt support coalescing
- NVMe command set attributes
  - Completion queue entry size: 16 bytes
  - Submission queue entry size: 64 bytes

Notes:
1. User capacity: 1GB = 1 billion bytes; 1TB = 1 trillion bytes.
2. Steady state as defined by SNIA Solid State Storage Performance Test Specification Enterprise v1.1.
3. Based on population statistics that are not relevant to individual units and a T_{CASE} of 60° C.
4. Operating temperature is the drive case temperature as measured by the SMART temperature. See air flow recommendations.

Native Drivers

- Microsoft Windows Server® 2016
- Red Hat® Enterprise Linux (RHEL) 6.5+
- CentOS® 6.5+
- SUSE® Linux Enterprise Server 11 SP4, 12+
- Ubuntu® 12.04.03+, 14.04+
- VMware® 5.5, 6.0+

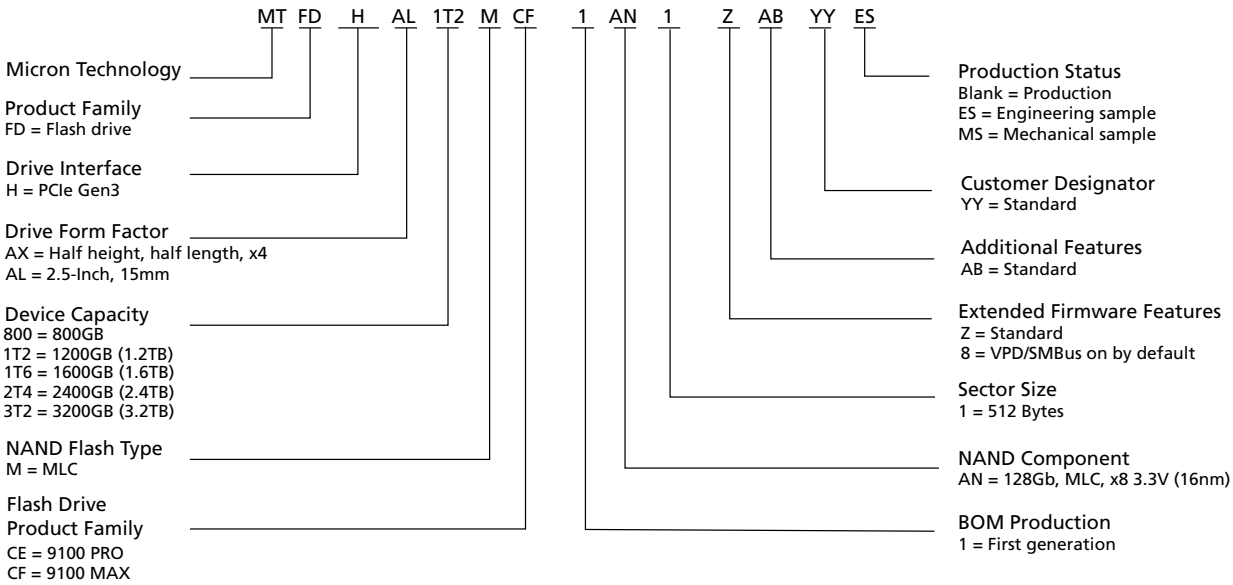
Custom Drivers

- Microsoft Windows Server 2012 R2, Hyper-V (recommended)
- RHEL 6.1-6.4
- CentOS 6.1-6.4
- SUSE Linux Enterprise Server 11 SP1-SP3

Part Numbering Information

The Micron® 9100 SSD is available in different configurations and capacities. Visit www.micron.com for a list of valid part numbers.

Figure 1: Part Number Chart



Warranty: Contact your Micron sales representative for further information regarding the product, including product warranties.

General Description

Micron's 9100 is a family of high-performance NVMe SSDs. The 9100 utilizes a PCIe Gen3 interface, the innovative Non-Volatile Memory Express protocol and Micron's own high-speed NAND to provide high throughput and IOPS, very low latency, and consistent quality of service. Reliability assurance measures include cyclic redundancy checks (CRC), redundant array of independent NAND (RAIN), capacitor-backed power loss protection and Micron's extensive validation, quality and reliability testing. It features thermal monitoring and protection, SMART attributes for status polling and NVMe-MI 1.0 for out-of-band management.

The device comes in two form factors: half-height/half-length (HHHL) add-in card (AIC) and 2.5-inch U.2 (small form factor 8639), both of which utilize a PCIe x4 Gen3 host interface. All capacities are available in both form factors.

The 9100 has two endurance classes: the 9100 PRO for read-centric use at roughly 1 drive writes per day (DWPD); and the 9100 MAX for mixed-use workloads at about 3 DWPD. The PRO version comes in 800GB, 1.6TB and 3.2TB capacities, while the MAX is sized at either 1.2TB or 2.4TB.

Logical Block Address Configuration

The number of logical block addresses (LBAs) reported by the device ensures sufficient storage space for the specified capacity.

Table 1: LBA Count in Accordance with IDEMA LBA1-03

Capacity	512-Byte Sector LBA Count	4KB Sector LBA Count
800GB	1,562,824,368	195,353,046
1.2TB	2,344,225,968	293,028,246
1.6TB	3,125,627,568	390,703,446
2.4TB	4,688,430,768	586,053,846
3.2TB	6,251,233,968	781,404,246

Performance

Table 2: Drive Performance

Specification	9100 PRO			9100 MAX		Unit
	U.2 and HHHL			U.2 and HHHL		
	800GB	1.6TB	3.2TB	1.2TB	2.4TB	
Sequential read (128KB I/O size)	2.05	2.8	3.2	2.9	3.2	GB/s
Sequential write (128KB I/O size)	0.69	1.3	2.2	1.3	2.2	
Random read (4KB I/O size)	525,000	700,000	750,000	700,000	750,000	IOPS
Random write (4KB I/O size)	50,000	120,000	160,000	210,000	300,000	
Random READ latency, QD = 1 (TYP)	120					µs
Random WRITE latency, QD = 1 (TYP)	30					

Notes:
1. Performance specifications shown are with power limiting off. See Electrical Characteristics section for more details.
2. Performance is steady state as defined by SNIA Solid State Storage Performance Test Specification Enterprise v1.1.
3. Performance may vary up to 10% over life of drive.

Table 3: Quality of Service

Specification Quality of Service (99.9%)	Queue Depth = 1	Unit
READ latency	230	µs
WRITE latency	70	µs

Note:
1. Quality of service is measured using random 4KB workloads at steady state.

Functional Description

Mean Time to Failure

The mean time to failure (MTTF) for the device can be calculated based on the component reliability data using the methods referenced in the Telcordia SR-322 reliability prediction procedures for electronic equipment and measured during Reliability Demonstration Test.

Table 4: MTTF

Capacity	MTTF (Operating Hours)
All	2.0 million

Endurance

SSD endurance is dependent on many factors, including: usage conditions applied to the drive, drive performance and capacity, formatted sector size, error correction codes (ECCs) in use, internal NAND PROGRAM/ERASE cycles, write amplification factor, wear-leveling efficiency of the drive, over-provisioning ratio, valid user data on the drive, drive temperature, NAND process parameters, and data retention time.

The device is designed to operate under a wide variety of conditions, while delivering the maximum performance possible and meeting enterprise market demands.

While actual endurance varies depending on conditions, the drive lifetime can be estimated based on capacity, assumed fixed-use models, ECC, and formatted sector size. Lifetime estimates for the device are shown in the following tables in total bytes written.

Table 5: Total Bytes Written

Model	Capacity	Sequential Writes	Random Writes (4KB)	Unit
9100 PRO	800GB	2.4	0.79	PB
	1.6TB	4.8	1.75	
	3.2TB	9.6	3.28	
9100 MAX	1.2TB	4.8	3.5	
	2.4TB	9.6	6.57	

Note: 1. Values shown are based on system modeling.

Data Retention

Data retention refers to the capability of the SSD media (that is, NAND flash) to retain programmed data. The three primary factors that affect data retention are:

- Power-on/power-off state: Data retention generally improves when the SSD is in use (that is, not shelved in a power-off state).
- Temperature: Data retention decreases as the temperature increases.
- Number of PROGRAM/ERASE cycles on the media: When the SSD ships from the factory, it is typically able to retain user data for up to 5 years in a powered-off state.

Data retention is guaranteed for three months at 40ºC (MAX), which assumes worst-case power and media wear (the SSD remains in a powered-off state and has reached end of life).

Wear Leveling

The device uses sophisticated wear-leveling algorithms to maximize endurance by distributing PROGRAM/ERASE cycles uniformly across all blocks in the array. Both static and dynamic wear leveling are utilized to optimize the drive's lifespan.

Both types of wear leveling aim to distribute "hot" data away from blocks that have experienced relatively heavy wear. Static wear leveling accomplishes this by moving data that has not been modified for an extended period of time out of blocks which have seen few P/E cycles and into more heavily worn blocks. This frees up fresher blocks for new data while reducing expected wear on tired blocks. Dynamic wear leveling, by contrast, acts on in-flight data to ensure it is preferentially written to the least-worn free blocks rather than those closer to the end of their rated life. These techniques are used together within the controller to optimally balance the wear profile of the NAND array.

Firmware Update Capability

The SSD supports firmware updates as defined by the NVMe specification. Once a download operation completes, an ACTIVATE command must be issued.

Power Loss Subsystem and Rebuild

The SSD supports an unexpected power loss with a power-backed write cache. No user data is lost during an unexpected power loss. When power is subsequently restored, the SSD returns to a ready state within a maximum of 120 seconds.

Boot

The 9100 is not intended to be a bootable device. Boot functionality is not validated by Micron, and any use in this manner is done at the user's own risk. Please visit Micron.com to find other SSD products that are recommended for boot.

SMBus Sideband Management

If the system management bus (SMBus) is configured to be enabled, the SSD uses the SMBus interface for presenting product data, monitoring drive health, checking drive status before power-up, and error posting.

Two protocols are supported: NVMe Basic Management Command revision 1.0 and Enterprise SSD Form Factor interface with its accompanying vital product data (VPD) definition.

Management data and vital product data may be accessed at fixed addresses with +3.3V_{AUX} prior to powering up the drive completely. This data continues to be available at this fixed address when the drive is fully powered up.

Table 6: Out of Band Management Details

Out of Band Protocol	SMBus Address	Alternate Address (due to bit shift)	Data
Enterprise SSD Form Factor	0x53	0xA6	Vital Product Data (VPD)
NVMe Management Interface 1.0	0x6A	0xD4	Subsystem Management Data (SMD)

Notes:
1. SMBus addresses will appear at an alternate address in certain tools due to the inclusion of a direction bit in the SMBus spec.
2. Out of band management is disabled by default.

Table 7: Vital Product Data Structure (VPD)

Address	#Bytes	Function	Value	Byte Offset	Description
0x53 (7 bit) or 0xA6 (8 bit)	3	Class Code	02h	0	Device Type and Programming Interface
			08h	1	
			01h	2	
	2	ID	44h	3	PCI-SIG Vendor ID
			13h	4	
	20		Varies	5-24	Serial Number
	40		Varies	25-64	Model Number
	1	PCIe Port0 Capabilities	03h	65	Maximum Link Speed
	1		04h	66	Maximum Link Width
	1	PCIe Port1 Capabilities	00h	67	Maximum Link Speed
	1		00h	68	Maximum Link Width
	1	Initial Power Requirements	0Ah	69	12V power rail initial power requirement (W)
	2	Reserved	0		
	1	Maximum Power Requirements	19h	72	12V power rail maximum power requirement (W)
	2	Reserved	0		
	2	Capability List Pointer	4Dh	75	16b pointer to start of capability list, see Table 8
			00h	76	

Table 8: Capability List Pointer

Pointer Value	#Bytes	Value	Byte Offset	Description
0x4D	2	A5h	0	PCI-SIG Vendor Specific Capability
		00h	1	
	2	00h	2	Pointer to next capability
		00h	3	
	2	44h	4	PCI-SIG Vendor ID
		13h	5	
	2	0		Reserved
	2	Varies	8	Temperature Value (°C) x 100
		Varies	9	

Electrical Characteristics

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 9: Power Consumption

Specification	Power Mode	9100 PRO			9100 MAX	
		800GB	1.6TB	3.2TB	1.2TB	2.4TB
Active power	Unlimited	7–30W	30W	30W	30W	30W
	25W limiting	7–16W	7–21W	7–25W	7–21W	7–25W
Idle power	All	7W	7W	7W	7W	7W

Note: 1. Power varies significantly depending on IO workload.

Table 10: Operating Voltage

Electrical Characteristic		Value
12V power rail	Operating voltage	12Vdc (–6% to 8%)
	MAX/MIN rise time	50ms/1ms
	MAX/MIN fall time	5s/1ms
	Inrush current (typical peak)	1.5A
	MAX average current (RMS)	2.5A
$3.3V_{AUX}$ power rail	Operating voltage	3.3V (–8% to 8%)
	MAX/MIN rise time	50ms/1ms
	MAX/MIN fall time	5s/1ms
	MAX average current	20mA

Environmental Conditions

Table 11: Temperature and Airflow

Temperature and Airflow	HHHL Add-In Card	2.5" U.2	Notes
Operating temperature (as indicated by the SMART temperature attribute)	0°C to 85°C	0°C to 85°C	1
Operating ambient temperature	0°C to 55°C	Ambient: 0°C to 35°C; Case: 0°C to 70°C	2
Operating airflow	300 LFM at 25°C ambient	450 LFM at 25°C ambient	3, 4
Storage temperature	–40°C to 85°C	–40°C to 85°C	5
Humidity	25% to 95% non-condensing	25% to 95% non-condensing	

Notes:
1. If SMART temperature exceeds 70°C, performance will be throttled.
2. Temperature of air impinging on the SSD.
3. Airflow must flow along the length of the drive parallel to and through any cooling fins.
4. Airflow is measured upstream of the drive before any acceleration as the air goes around the drive.
5. Contact Micron for additional information.

Table 12: Shock and Vibration

Shock and Vibration	HHHL Add-In Card	2.5" U.2
Shock (non-operational)	500G at 1ms half-sine	1000G at 1ms half-sine
Vibration (non-operational)	3.1 GRMS 5–800Hz at 30 min/axis	3.1 GRMS 5–800Hz at 30 min/axis

Note:
1. Shock and vibration ratings refer to ability to withstand stress events only. Prolonged or repeated exposure to conditions listed or greater stresses may result in permanent damage to the device. Functional operation of the device under these conditions is not implied. See warranty for more information.

Supported Commands

NVMe Admin Command Set

The 9100 supports the following mandatory NVMe admin commands, as described in the NVMe 1.1b specification:

- Delete I/O submission queue
- Create I/O submission queue
- Get log page
- Delete I/O completion queue
- Create I/O completion queue
- Identify
- Abort
- Set features
- Get features
- Asynchronous event request

The following optional NVMe admin commands are also supported:

- Firmware activate
- Firmware image download
- Format NVM

NVMe I/O Command Set

The 9100 supports the following mandatory NVMe I/O commands, as described in the NVMe 1.1b specification:

- Flush
- Write
- Read

The following optional NVMe I/O commands are also supported:

- Dataset management (de-allocate only)

Log Pages

The GET LOG PAGE command can be used to retrieve the following logs:

- 01h - Error information
- 02h - SMART / health information
- 03h - Firmware slot information
- CAh - Vendor Unique SMART
- 05h - Command Effects Log
- F0h - Vendor Unique Commands Log

SMART and Health Information

The SSD supports SMART/Health log information as defined in the NVMe specification as well as extended health information. These logs persist through power cycles and reflect lifetime data.

Table 13: SMART/Health Information (Log Identifier 02h)

Bytes	Name	Description
0	Critical warning	Indicates critical warnings for the state of the controller. Each bit corresponds to a critical warning type; multiple bits may be set. If a bit is cleared to 0, the critical warning does not apply. Critical warnings may result in an asynchronous event notification to the host. • Bit 00: If set to 1, the available spare space has fallen below the threshold. • Bit 01: If set to 1, the temperature has exceeded a critical threshold. • Bit 02: If set to 1, the device reliability has been degraded due to significant media-related errors or any internal error that degrades device reliability. • Bit 03: If set to 1, the media has been placed in read-only mode. • Bit 04: If set to 1, the volatile memory backup device has failed. This field is only valid if the controller has a volatile memory backup solution. • Bits 07:05: Reserved.
2:1	Temperature	Contains the temperature of the overall device (controller and NVM included) in units of Kelvin. If it exceeds the temperature threshold, an asynchronous event may be issued to the host. For the 9100, the value reported is the maximum temperature measured on either the board or controller.
3	Available spare	Contains a normalized percentage (0–100%) of the remaining available spare capacity, beginning at 100% and decreasing.
4	Available spare threshold	When the available spare falls below the threshold indicated in this field, an asynchronous event may be issued to the host. The value is indicated as a normalized percentage (0–100%). Threshold is set to 5%.
5	Percentage used	Contains a vendor-specific estimate of the percentage of the device life used based on the actual device usage and the manufacturer's prediction of device life. A value of 100 indicates that the estimated endurance of the device has been consumed, but may not indicate a device failure. Refer to the JEDEC JESD218 standard for SSD device life and endurance measurement techniques.
31:6	Reserved	Reserved.
47:32	Data units read	Contains the number of 512-byte data units the host has read from the controller; this value does not include metadata. This value is reported in thousands (that is, a value of 1 corresponds to 1000 units of 512 bytes read) and is rounded up. When the LBA size is a value other than 512 bytes, the controller shall convert the amount of data read to 512-byte units.

Table 13: SMART/Health Information (Log Identifier 02h) (Continued)

Bytes	Name	Description
63:48	Data units written	Contains the number of 512-byte data units the host has written to the controller; this value does not include metadata. This value is reported in thousands (that is, a value of 1 corresponds to 1000 units of 512 bytes written) and is rounded up. When the LBA size is a value other than 512 bytes, the controller shall convert the amount of data written to 512-byte units. For the NVM command set, logical blocks written as part of write operations shall be included in this value. Write uncorrectable commands shall not impact this value.
79:64	Host read commands	Contains the number of read commands issued to the controller.
95:80	Host write commands	Contains the number of write commands issued to the controller. For the NVM command set, this is the number of write commands.
111:96	Controller busy time	Contains the amount of time the controller is busy with I/O commands. The controller is busy when there is a command outstanding to an I/O queue (specifically, a command was issued via an I/O submission queue tail doorbell write and the corresponding completion queue entry has not been posted yet to the associated I/O completion queue.) This value is reported in minutes.
127:112	Power cycles	Contains the number of power cycles.
143:128	Power-on hours	Contains the number of power-on hours. This does not include time that the controller was powered and in a low-power state condition.
159:144	Unsafe shutdowns	Contains the number of unsafe shutdowns. This count is incremented when a shutdown notification (CC.SHN) is not received prior to loss of power.
175:160	Media errors	Contains the number of occurrences where the controller detected an unrecovered data integrity error. Errors such as uncorrectable ECC, CRC checksum failure, or LBA tag mismatch are included in this field.
191:176	Number of error info log entries	Contains the number of error information log entries over the life of the controller.
511:192	Reserved	Reserved.

Vendor Unique SMART

In addition to the standard SMART log, the 9100 provides the following details in a vendor unique log:

Table 14: Vendor Unique SMART Attributes (Log Identifier CAh)

Bytes	Name	Description
0:1	F9 - NAND_writes_1GiB	Raw value reports the number of writes to NAND in 1 GiB increments.
3:4	Normalized value	
5:11	Current raw value	
12:13	FA - NAND_reads_1GiB	Raw value reports the number of reads to NAND in 1 GiB increments.
15:16	Normalized value	
17:23	Current raw value	

Table 14: Vendor Unique SMART Attributes (Log Identifier CAh) (Continued)

Bytes	Name	Description
24:25	EA - Thermal throttle status	Raw value indicates throttle status and total throttling time. Byte 0: If set to 1, throttling is active; if set to 0, throttling is not active Bytes 1-4: Total throttling time in minutes since power-on Bytes 5: Reserved
27:28	Normalized value	
29:35	Current raw value	
36:37	E7 - Temperature	Raw value reports the maximum and minimum temperature in Kelvin over the lifetime of the device. Byte 0-1: The maximum temperature sampled from the temperature sensor Bytes 2-3: The minimum temperature sampled from the temperature sensor Bytes 4-5: The current temperature sampled from the temperature sensor
39:40	Normalized value	
41:47	Current raw value	
48:49	E8 - Power consumption	Raw value reports the maximum and minimum average power consumption in watts. Byte 0-1: The maximum power consumption Bytes 2-3: The minimum power consumption Bytes 4-5: The average power consumption
51:52	Normalized value	
53:59	Current raw value	
60:61	AF - Power loss protection	Normalized value reports the power loss protection status: 100 indicates protection was successful; 0 indicates protection failed. A power loss failure indicator will persist until a Format NVM command is executed.
63:64	Normalized value	
65:71	Current raw value	

Get/Set Features

The following features can be configured or retrieved using NVMe SET FEATURES and GET FEATURES commands:

- 02h – Power management – Commands are accepted but values are not returned. A custom power governor feature is utilized for power management.
- 04h – Temperature threshold
- 07h – Number of queues – Maximum supported is 128 for both submission and completion queues.
- 08h – Interrupt coalescing
- 09h – Interrupt vector configuration
- 0Bh – Asynchronous event configuration

Additionally, this custom feature is supported: C6h – Power governor. This feature configures power limiting of the device. The following power modes are supported:

- 00h – 25W
- 01h – 20W
- FFh – No power limiting (30W MAX)

Feature identifier C0h indicates whether an invalid power setting has been set.

Interface Connectors

The host interface connector conforms to the PCIe Electromechanical Specification.

A mechanical indent is used to separate the PCIe power pins from the differential signal contacts. The pins are numbered below in ascending order from left to right. Side B refers to component side. Side A refers to the solder side.

AIC HHHL Pin Assignments

The host interface connector conforms to the PCIe Electromechanical Specification.

A mechanical indent is used to separate the PCIe power pins from the differential signal contacts. The pins are numbered below in ascending order from left to right. Side B refers to component side. Side A refers to the solder side.

Table 15: PCIe Interface Connector Pin Assignments (HHHL Form Factor)

Pin Number	Side B		Side A	
	Name	Description	Name	Description
1	+12V	12V power	PRSNT1#	Hot Plug Presence Detect
2	+12V	12V power	+12V	12V power
3	+12V	12V power	+12V	12V power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	DNU
6	SMDAT	SMBus data	JTAG3	DNU
7	GND	Ground / UART_HOST	JTAG4	DNU
8	+3.3V	3.3V power	JTAG5	DNU
9	JTAG1	DNU	+3.3V	3.3V power
10	3.3Vaux	3.3V auxiliary power	+3.3V	3.3V power
11	WAKE#	DNU	PERST#	PCIe Fundamental Reset
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	PCIe REFCLK p
14	PETp0	PCIe TX Lane 0 p	REFCLK-	PCIe REFCLK n
15	PETn0	PCIe TX Lane 0 n	GND	Ground
16	GND	Ground	PERp0	PCIe RX Lane 0 p
17	PRSNT2#	DNU	PERn0	PCIe RX Lane 0 n
18	GND	Ground	GND	Ground
19	PETp1	PCIe TX Lane 1 p	RSVD	Reserved
20	PETn1	PCIe TX Lane 1 n	GND	Ground
21	GND	Ground	PERp1	PCIe RX Lane 1 p
22	GND	Ground	PERn1	PCIe RX Lane 1 n
23	PETp2	PCIe TX Lane 2 p	GND	Ground
24	PETn2	PCIe TX Lane 2 n	GND	Ground
25	GND	Ground	PERp2	PCIe RX Lane 2 p

Table 15: PCIe Interface Connector Pin Assignments (HHHL Form Factor) (Continued)

Pin Number	Side B		Side A	
	Name	Description	Name	Description
26	GND	Ground	PERn2	PCIe RX Lane 2 n
27	PETp3	PCIe TX Lane 3 p	GND	Ground
28	PETn3	PCIe TX Lane 3 p	GND	Ground
29	GND	Ground	PERp3	PCIe RX Lane 3 p
30	RSVD	Reserved	PERn3	PCIe RX Lane 3 n
31	PRSNT2#	Hot Plug Presence Detect	GND	Ground
32	GND	Ground	RSVD	Reserved

U.2 Pin Assignments

The U.2 2.5-inch form factor follows the SFF-8639 specification and supports built-in latching.

Table 16: PCIe Interface Connector Pin Assignments (U.2 Form Factor)

Pin	Name	Description	Pin	Name	Description
S1	GND	Ground	E7	REFCLK0+	PCIe REFCLK 0 p
S2		DNC	E8	REFCLK0-	PCIe REFCLK 0 p
S3		DNC	E9	GND	Ground
S4	GND	Ground	E10	PETp0	PCIe TX Lane 0 p
S5		DNC	E11	PETn0	PCIe TX Lane 0 n
S6		DNC	E12	GND	Ground
S7	GND	Ground	E13	PERn0	PCIe RX Lane 0 n
E1	REFCLK1+	DNC	E14	PERp0	PCIe RX Lane 0 p
E2	REFCLK1-	DNC	E15	GND	Ground
E3	3.3Vaux	3.3V auxiliary power	E16	RSVD	Reserved
E4	PERST1#	DNC	S8	GND	Ground
E5	PERST0#	PCIe Fundamental Reset	S9		DNC
E6	RSVD	Reserved	S10		DNC
P1		DNC	S11	GND	Ground
P2		DNC	S12		DNC
P3		DNC	S13		DNC
P4	IfDet_N	Interface detect	S14	GND	Ground
P5	GND	Ground	S15	RSVD	Reserved
P6	GND	Ground	S16	GND	Ground
P7		DNC	S17	PETp1	PCIe TX Lane 1 p
P8		DNC	S18	PETn1	PCIe TX Lane 1 n
P9		DNC	S19	GND	Ground
P10	PRSNT_N	Presence detect	S20	PERn1	PCIe RX Lane 1 n

Table 16: PCIe Interface Connector Pin Assignments (U.2 Form Factor) (Continued)

Pin	Name	Description	Pin	Name	Description
P11	Activity	Activity signal from the drive	S21	PERp1	PCIe RX Lane 1 p
P12	Hot-Plug	Ground	S22	GND	Ground
P13	+12V_pre	12V power	S23	PETp2	PCIe TX Lane 2 p
P14	+12V	12V power	S24	PETn2	PCIe TX Lane 2 n
P15	+12V	12V power	S25	GND	Ground
			S26	PERn2	PCIe RX Lane 2 n
			S27	PERp2	PCIe RX Lane 2 p
			S28	GND	Ground
			E17	PETp3	PCIe TX Lane 3 p
			E18	PETn3	PCIe TX Lane 3 n
			E19	GND	Ground
			E20	PERn3	PCIe RX Lane 3 n
			E21	PERp3	PCIe RX Lane 3 p
			E22	GND	Ground
			E23	SMCLK	SMBus clock
			E24	SMDAT	SMBus data
			E25	DualPortEn_N	Dual port enable

Notes:
1. PRSNT_N is open and IfDet_N is grounded to indicate PCIe support.
2. DualPortEn_N pin should be left un-connected or un-driven by the system to enable single port operation with all 4 lanes. If this pin is asserted (driven low) by the system, the SSD will function as PCIe x2 lane only.

PCIe Header

Figure 2: 9100 PRO PCIe Header

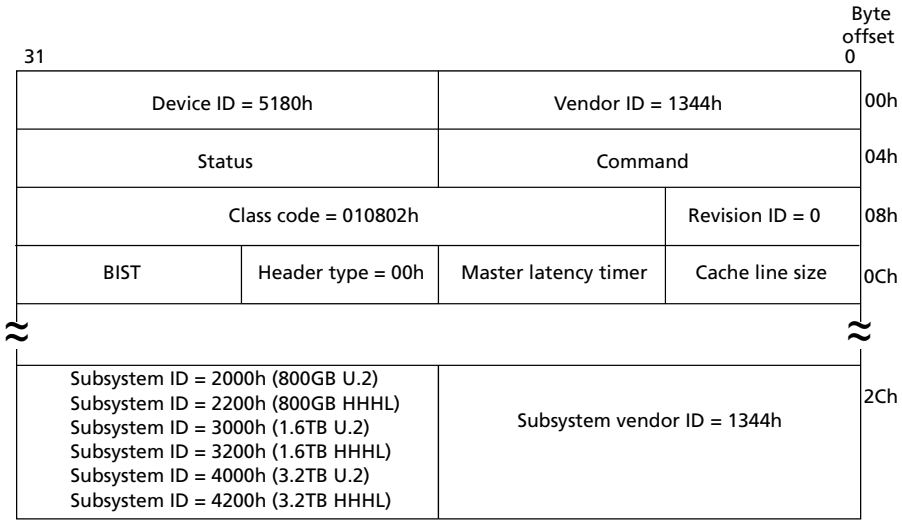
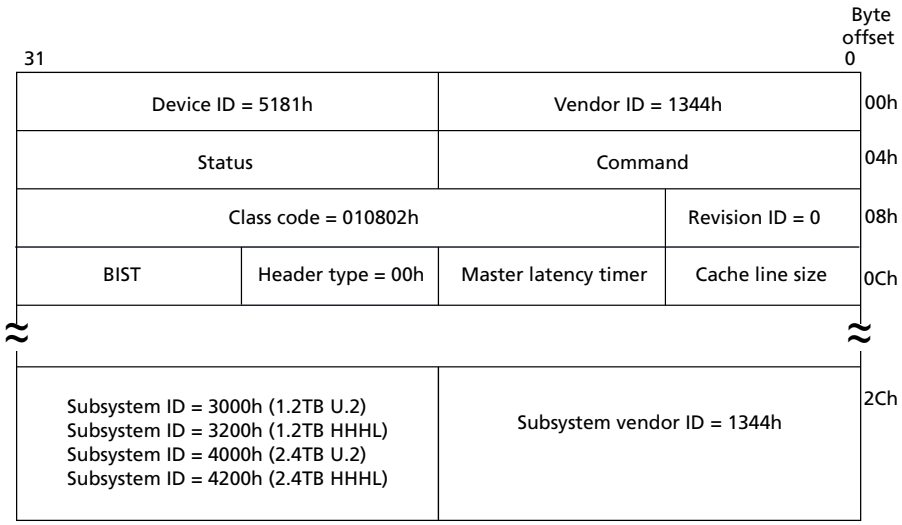


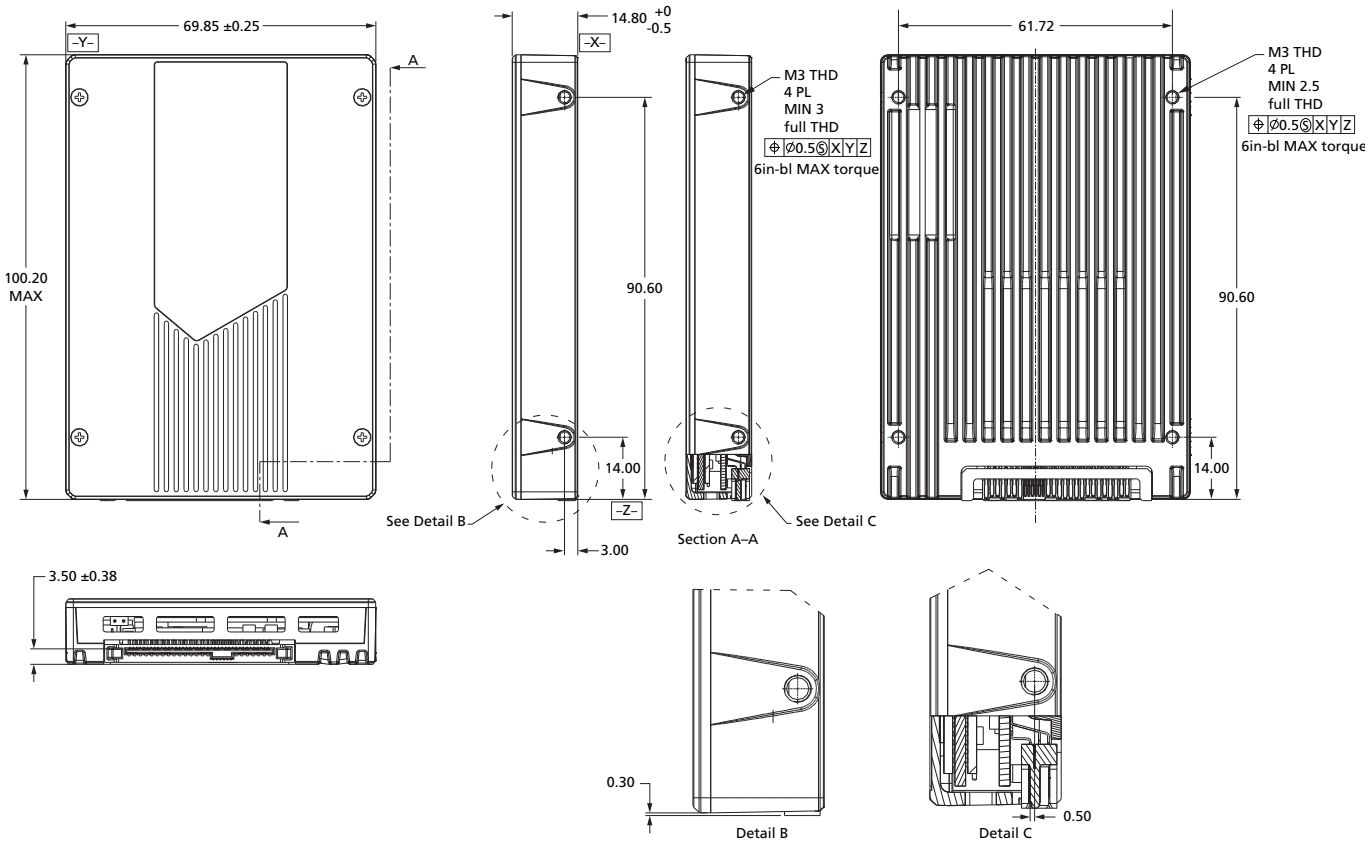
Figure 3: 9100 MAX PCIe Header



Physical Configuration

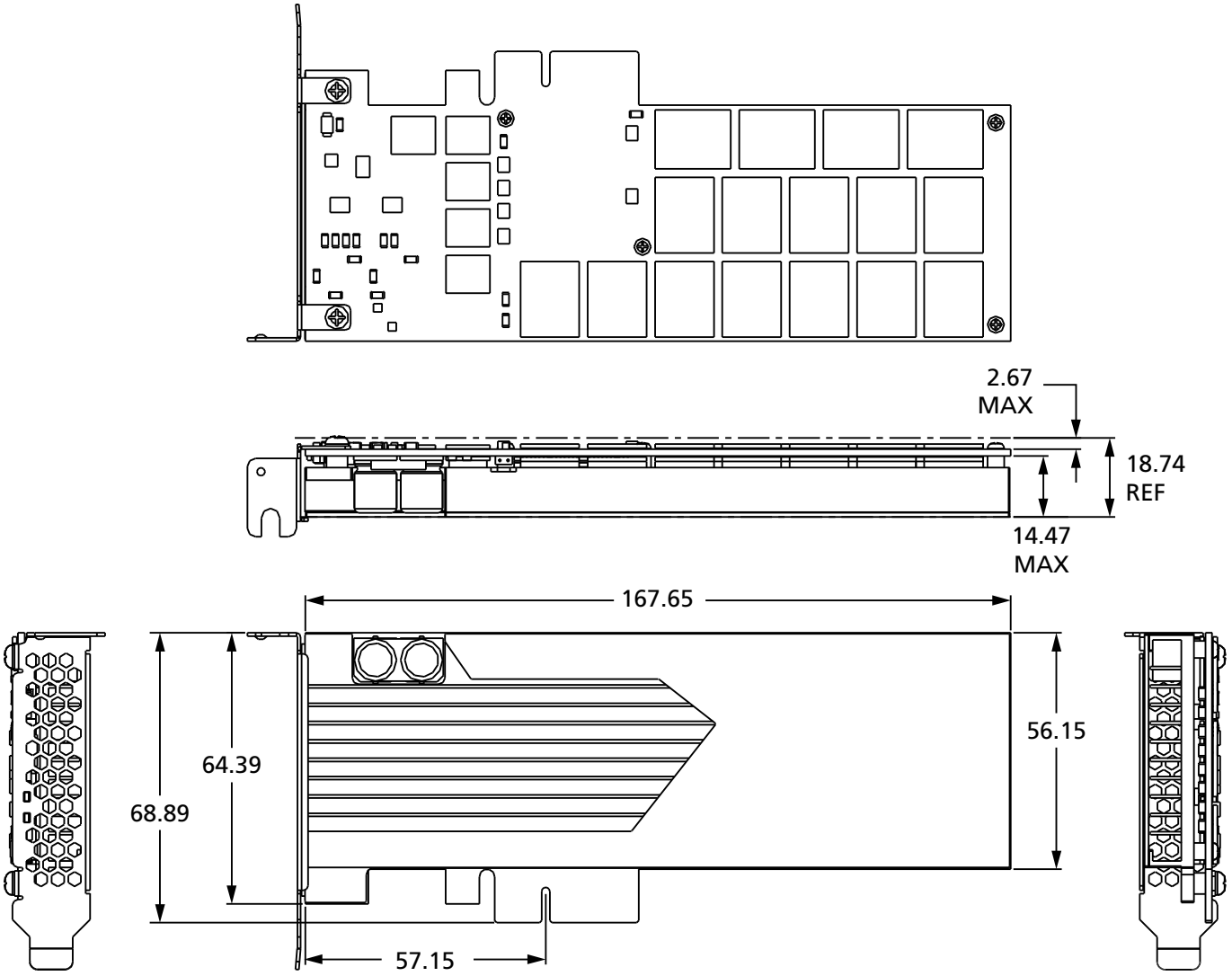
Micron's 9100 conforms to PCI Express CEM and SFF-8639 specifications.

Figure 4: U.2 (2.5") Nominal Dimensions



Note: 1. Length does not include 0.3 connector protrusion.

Figure 5: AIC (HHHL) Nominal Dimensions



Compliance

The device complies with the following specifications:

- CE (Europe): EN 55022 Class B, EN 55024, RoHS
- FCC: CFR Title 47, Part 15, Class B
- UL: UL-60950-1, 2nd Edition
- BSMI (Taiwan): Approval to CNS 13438 Class B
- RCM (Australia, New Zealand): AS/NZS CISPR22 Class B
- KCC RRL (Korea): Approval to KN32 Class B, KN 35
- W.E.E.E.: Compliance with EU WEEE directive 2012/19/EC. Additional obligations may apply to customers who place these products in the markets where WEEE is enforced.
- TUV (Germany): Approval to IEC60950/EN60950
- V_{CCI} (Japan): 2015-04 Class B, CISPR22
- IC (Canada): ICES-003 Class B, CISPR22 Class B
- This Class B digital apparatus complies with Canadian ICES-003.
- Cet appareil numérique de la classe B est conforme à la norme NMB-003 du Canada

FCC Rules

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

References

- PCI Express CEM Specification V2.0
- PCI Express Specification V3.0
- SFF-8639
- IDEMA Specification
- Telcordia SR-322 Procedures
- NVM Express Specification revision 1.1b

Revision History

Rev. J – 07/17

- Added VPD Structure table

Rev. I – 03/17

- Added VPD/SMBus on by default to part numbering chart
- Minor formatting and other corrections

Rev. H – 10/16

- Release version
- Updated operating temperature (SMART)

Rev. G – 06/16

- Changes to performance specifications, with increases on most capacities and some reductions on 800GB
- Voltage tolerance on first page corrected to match Electrical Characteristics section
- Tolerance for 3.3V rail adjusted

Rev. F – 05/16

- Updated Compliance section to include Class B certification

Rev. E – 04/16

- Increase to max power and current in unlimited power mode for two largest capacities
- Added note that boot is not supported

Rev. D – 04/16

- Added part numbers and number scheme information

Rev. C – 03/16

- Noted VMware driver compatibility
- Updated compliance information

Rev. B – 02/16

- Added dimension drawings
- Minor change to QoS
- Further clarification on shock/vibration ratings

Rev. A – 02/16

- Initial release

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.