

N-Channel Enhancement Mode Power MOSFET**MTN10N65FPG** **BV_{DSS} : 650V** **$R_{DS(ON)}$: 0.82 Ω** **I_D : 10A****Description**

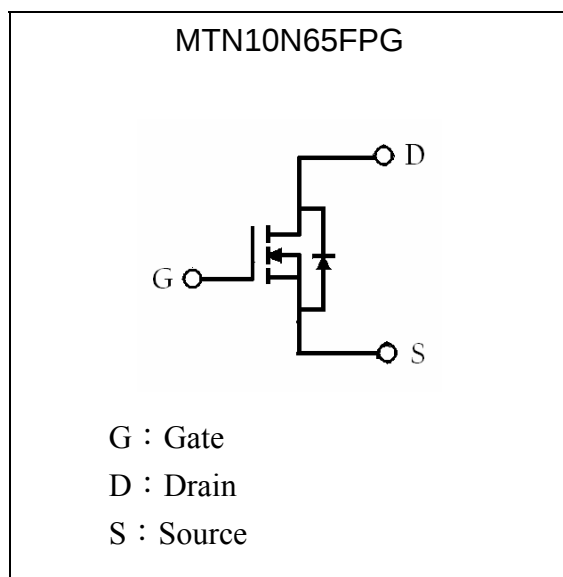
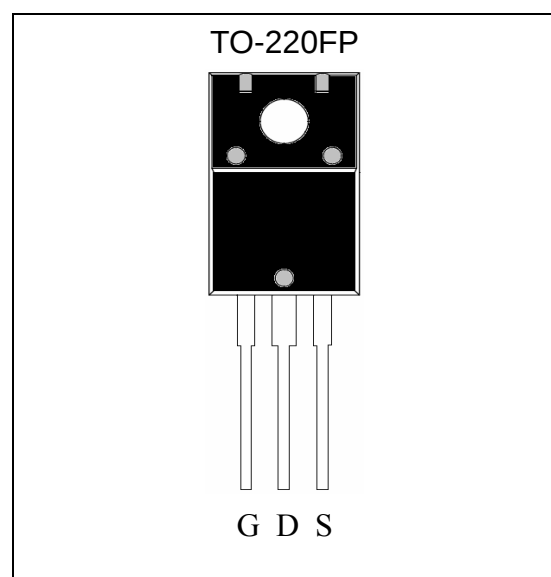
The MTN10N65FPG is a N-channel enhancement-mode MOSFET, providing the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness. The TO-220FP package is universally preferred for all commercial-industrial applications

Features

- Low On Resistance
- Simple Drive Requirement
- Low Gate Charge
- Fast Switching Characteristic
- Insulating package, front/back side insulating voltage=2500V(AC)
- Pb-free lead plating and halogen-free package

Applications

- Power Factor Correction
- LCD TV Power
- Full and Half Bridge Power

Symbol**Outline**

**Absolute Maximum Ratings** ($T_C=25^{\circ}\text{C}$)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage (Note 1)	V_{DS}	650	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current	I_D	10*	A
Continuous Drain Current @ $T_C=100^{\circ}\text{C}$	I_D	6	A
Pulsed Drain Current @ $V_{GS}=10\text{V}$ (Note 2)	I_{DM}	40*	A
Single Pulse Avalanche Energy @ $L=4.3\text{mH}$, $I_D=10\text{Amps}$, $V_{DD}=50\text{V}$	E_{AS}	237	mJ
Repetitive Avalanche Energy	E_{AR}	5	
Peak Diode Recovery dv/dt (Note 3)	dv/dt	3.0	V/ns
Maximum Temperature for Soldering @ Lead at 0.063 in(1.6mm) from case for 10 seconds	T_L	300	$^{\circ}\text{C}$
Maximum Temperature for Soldering @ Package Body for 10 seconds	T_{PKG}	260	$^{\circ}\text{C}$
Total Power Dissipation ($T_C=25^{\circ}\text{C}$)	P_d	50	W
Linear Derating Factor		0.4	W/ $^{\circ}\text{C}$
Operating Junction and Storage Temperature	T_J, T_{stg}	-55~+150	$^{\circ}\text{C}$

*Drain current limited by maximum junction temperature

Note : 1. $T_J=+25^{\circ}\text{C}$ to $+150^{\circ}\text{C}$.

2. Repetitive rating; pulse width limited by maximum junction temperature.

3. $I_{SD} \leq 10\text{A}$, $dI/dt \leq 100\text{A}/\mu\text{s}$, $V_{DD} \leq BVDSS$, $T_J=+150^{\circ}\text{C}$.**Thermal Data**

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{th,j-c}$	2.5	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-ambient, max	$R_{th,j-a}$	100	$^{\circ}\text{C}/\text{W}$

**Characteristics (T_j=25°C, unless otherwise specified)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	650	-	-	V	V _{GS} =0, I _D =250μA
ΔBV _{DSS} /ΔT _j	-	0.6	-	V/°C	Reference to 25°C, I _D =250μA
V _{GS(th)}	2.0	-	4.0	V	V _{DS} = V _{GS} , I _D =250μA
*G _{FS}	-	6.8	-	S	V _{DS} =15V, I _D =5A
I _{GSS}	-	-	±100	nA	V _{GS} =±30
I _{DSS}	-	-	25	μA	V _{DS} =650V, V _{GS} =0
I _{DSS}	-	-	250	μA	V _{DS} =520V, V _{GS} =0, T _j =125°C
*R _{DS(ON)}	-	0.75	0.82	Ω	V _{GS} =10V, I _D =6A
Dynamic					
*Q _g	-	53	-	nC	I _D =10A, V _{DD} =325V, V _{GS} =10V
*Q _{gs}	-	10.7	-		
*Q _{gd}	-	22.3	-		
*t _{d(ON)}	-	19	-	ns	V _{DD} =325V, I _D =10A, V _{GS} =10V, R _G =9.1 Ω
*tr	-	16	-		
*t _{d(OFF)}	-	49	-		
*tf	-	16	-		
Ciss	-	2516	-	pF	V _{GS} =0V, V _{DS} =25V, f=1MHz
Coss	-	182.2	-		
Crss	-	71	-		
Source-Drain Diode					
*V _{SD}	-	-	1.5	V	I _S =10A, V _{GS} =0V
*I _S	-	-	10	A	V _D =V _G =0, V _S =1.3V
*I _{SM}	-	-	40		
*trr	-	352	528	ns	V _{GS} =0, I _F =10A, dI/dt=100A/μs
*Qrr	-	2.9	4.35	μC	

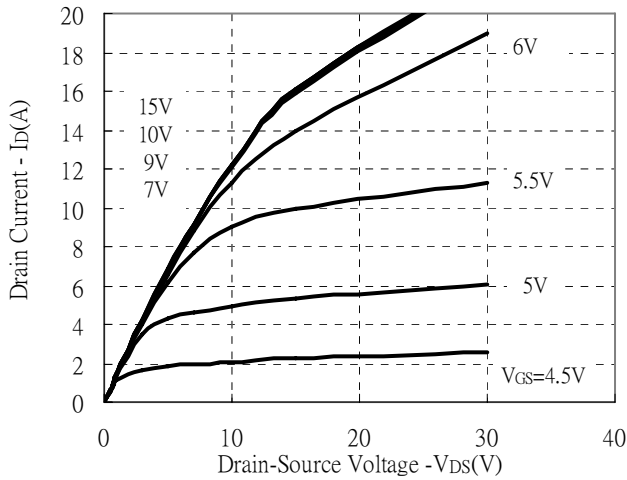
*Pulse Test : Pulse Width ≤300μs, Duty Cycle ≤2%

Ordering Information

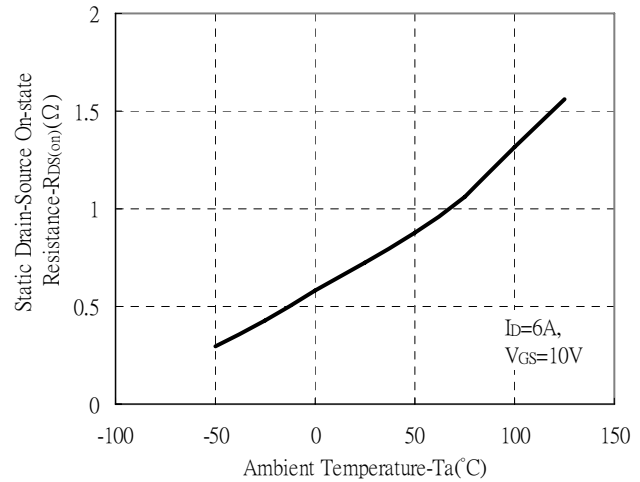
Device	Package	Shipping
MTN10N65FPG	TO-220FP (Pb-free lead plating and halogen-free package)	50 pcs/tube

Typical Characteristics

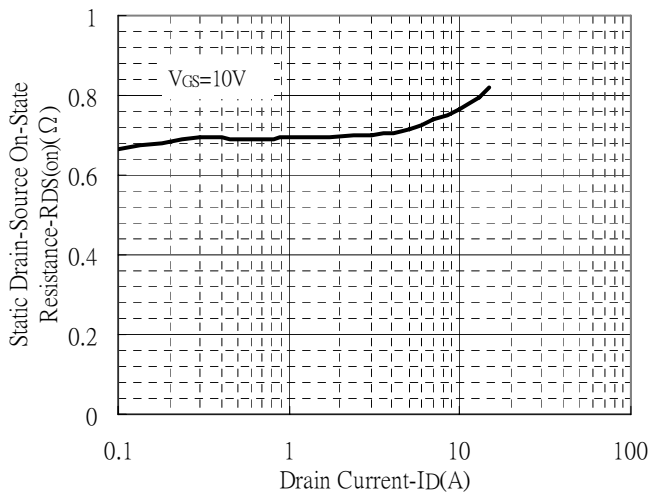
Typical Output Characteristics



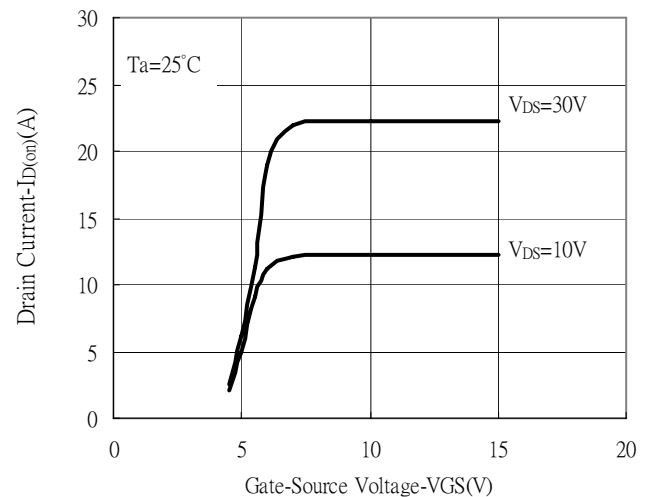
Static Drain-Source On-resistance vs Ambient Temperature



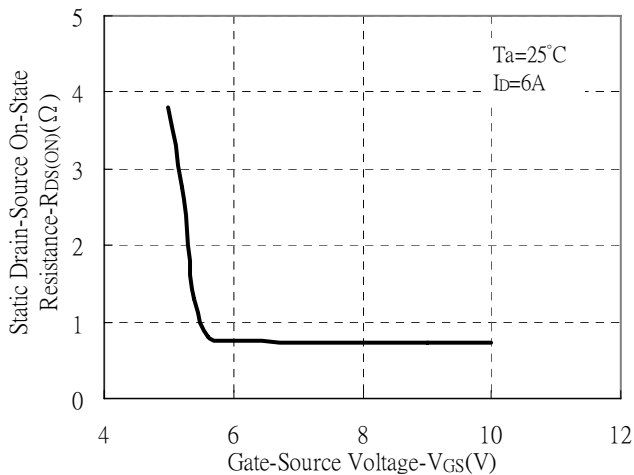
Static Drain-Source On-State resistance vs Drain Current



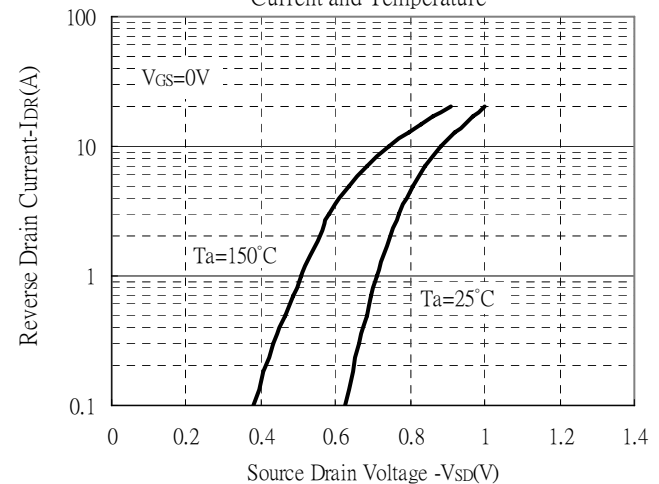
Drain Current vs Gate-Source Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage



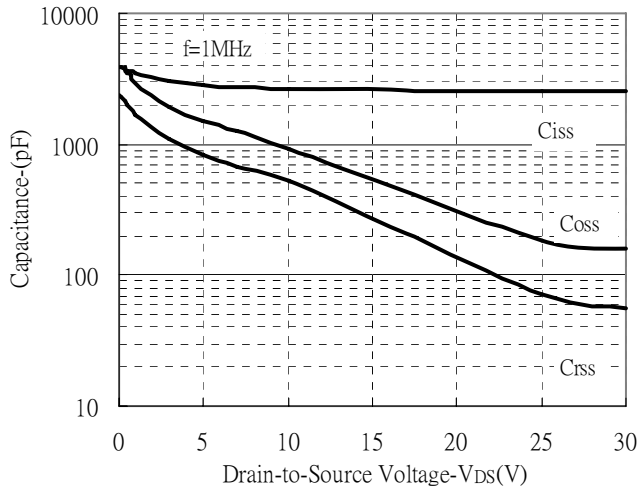
Body Diode Forward Voltage Variation vs Source Current and Temperature



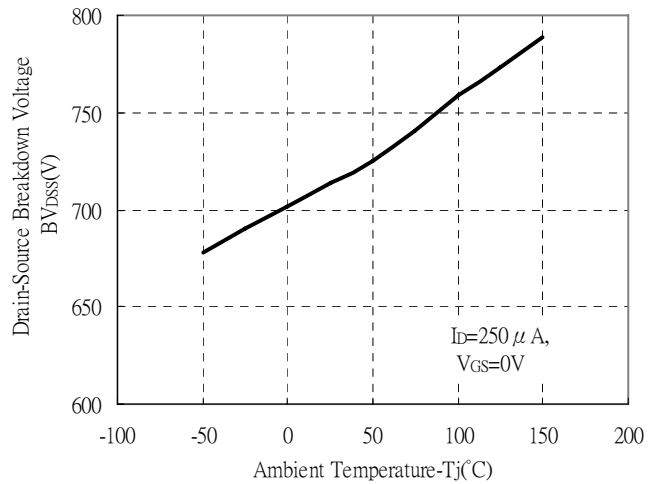


Characteristic Curves(Cont.)

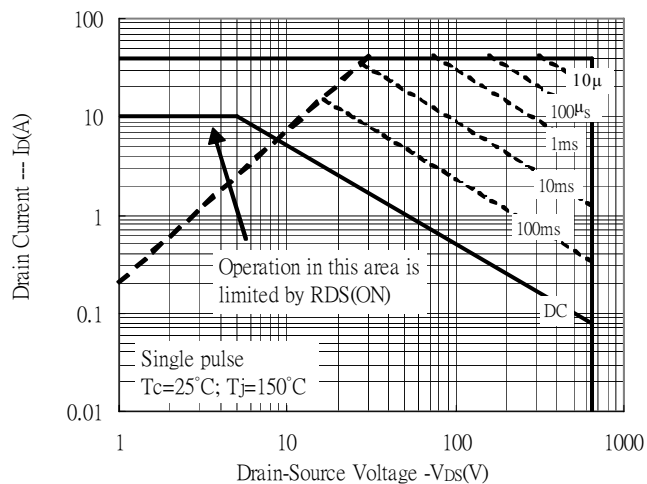
Capacitance vs Reverse Voltage



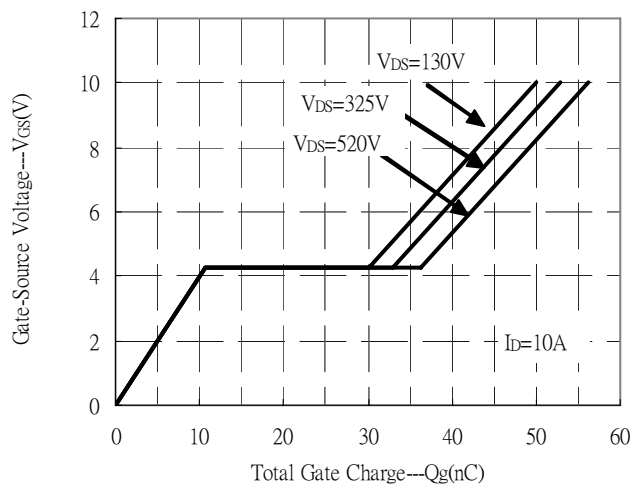
Breakdown Voltage vs Ambient Temperature



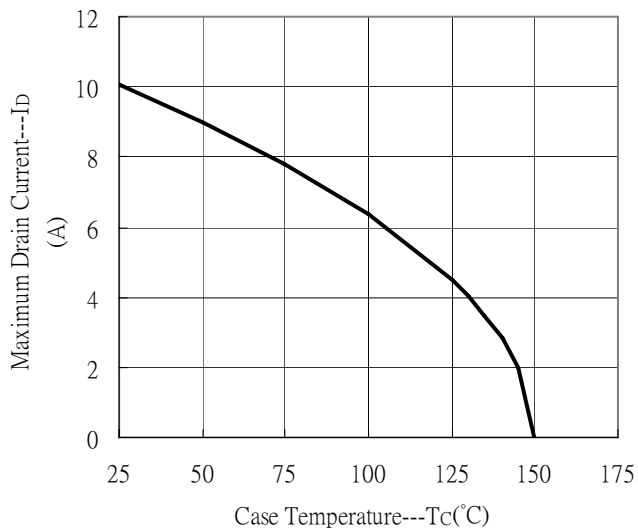
Maximum Safe Operating Area



Gate Charge Characteristics



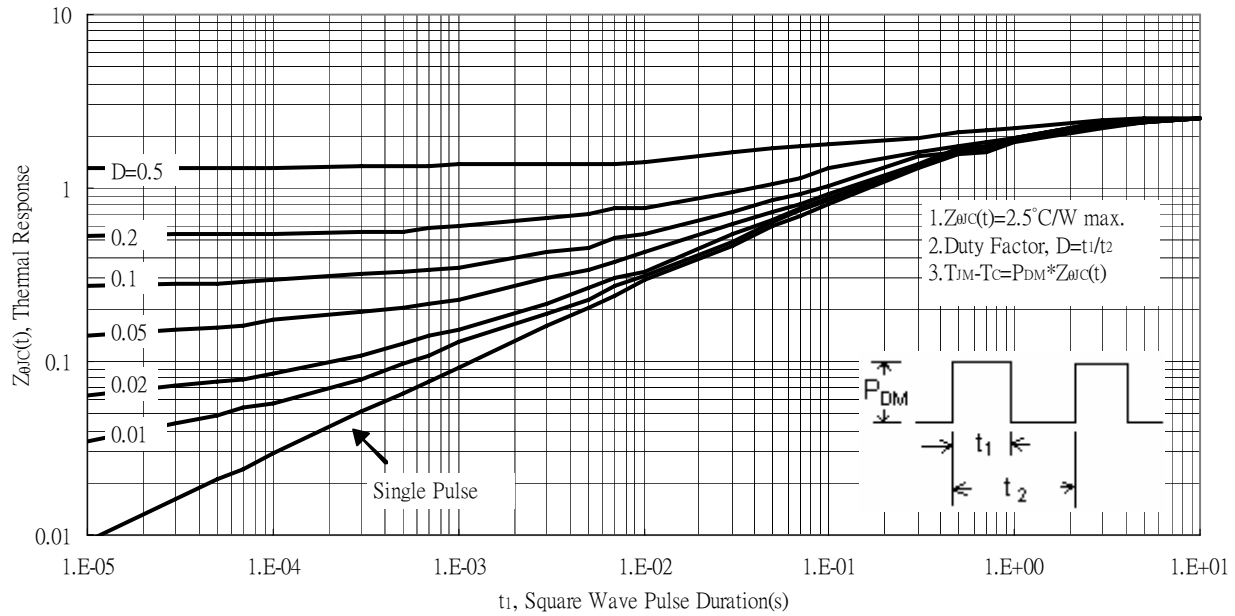
Maximum Drain Current vs Case Temperature





Typical Characteristics(Cont.)

Transient Thermal Response Curves



Test Circuit and Waveforms

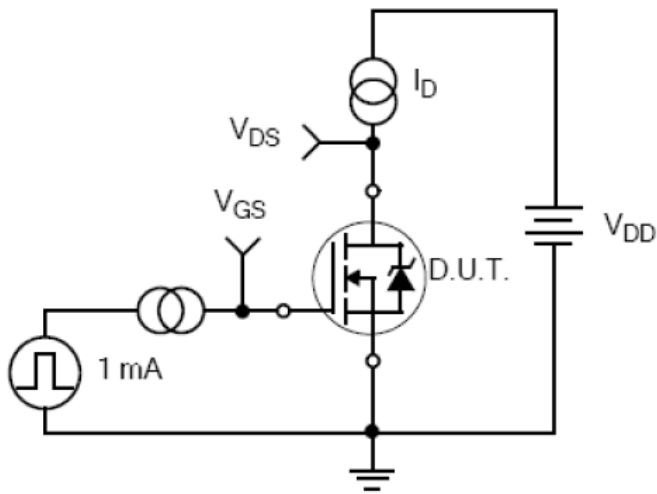


Figure 17. Gate Charge Test Circuit

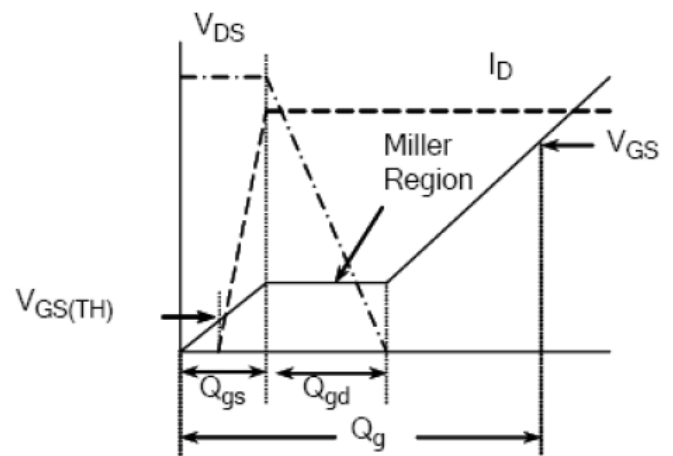


Figure 18. Gate Charge Waveform

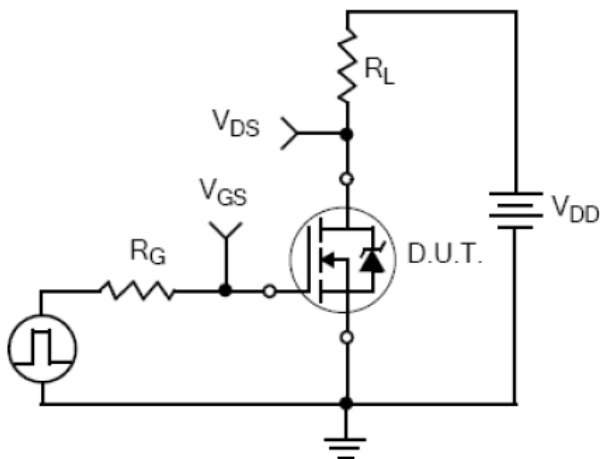


Figure 19. Resistive Switching Test Circuit

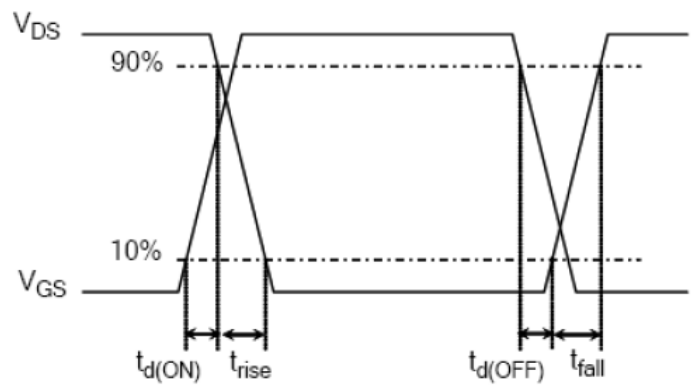


Figure 20. Resistive Switching Waveforms

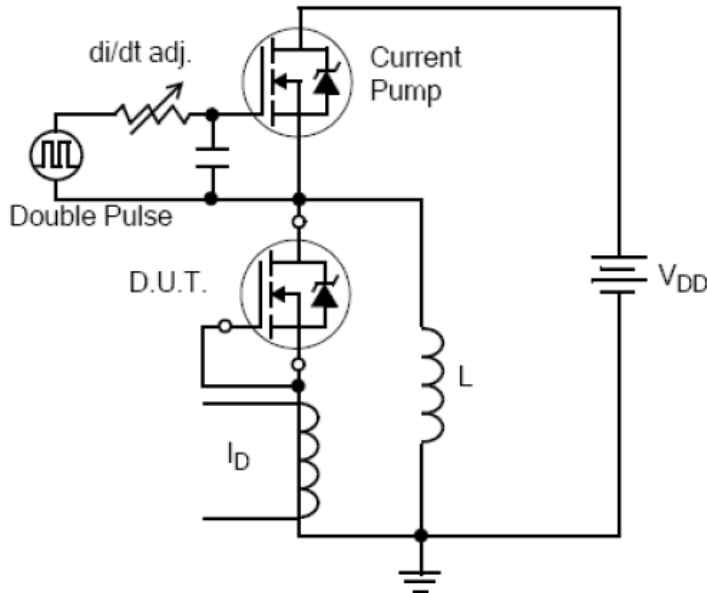
Test Circuit and Waveforms(Cont.)


Figure 21. Diode Reverse Recovery Test Circuit

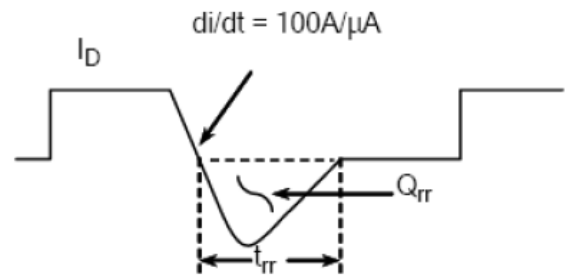


Figure 22. Diode Reverse Recovery Waveform

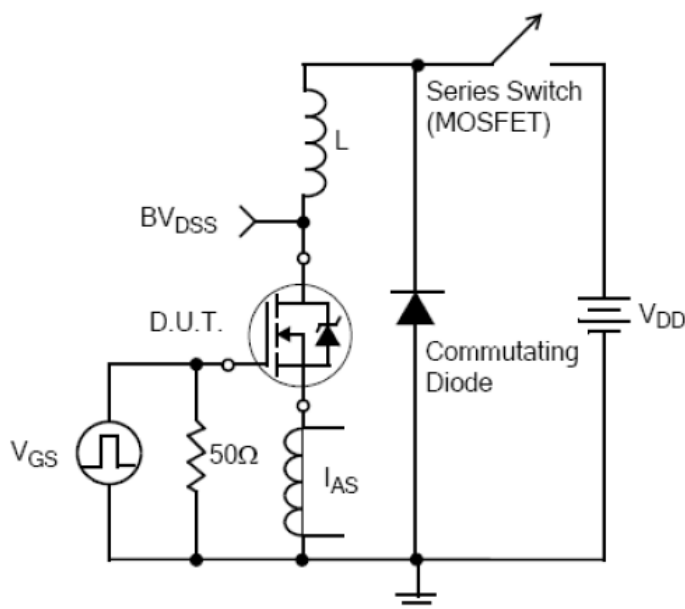


Figure 23. Unclamped Inductive Switching Test Circuit

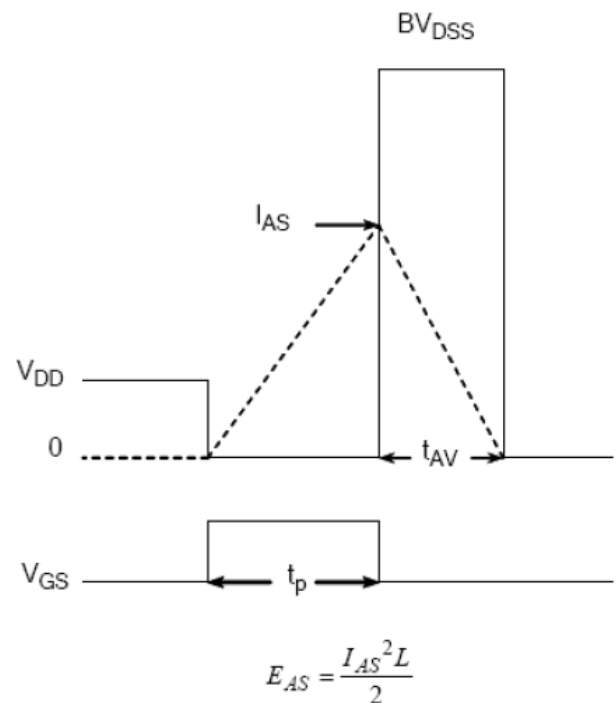
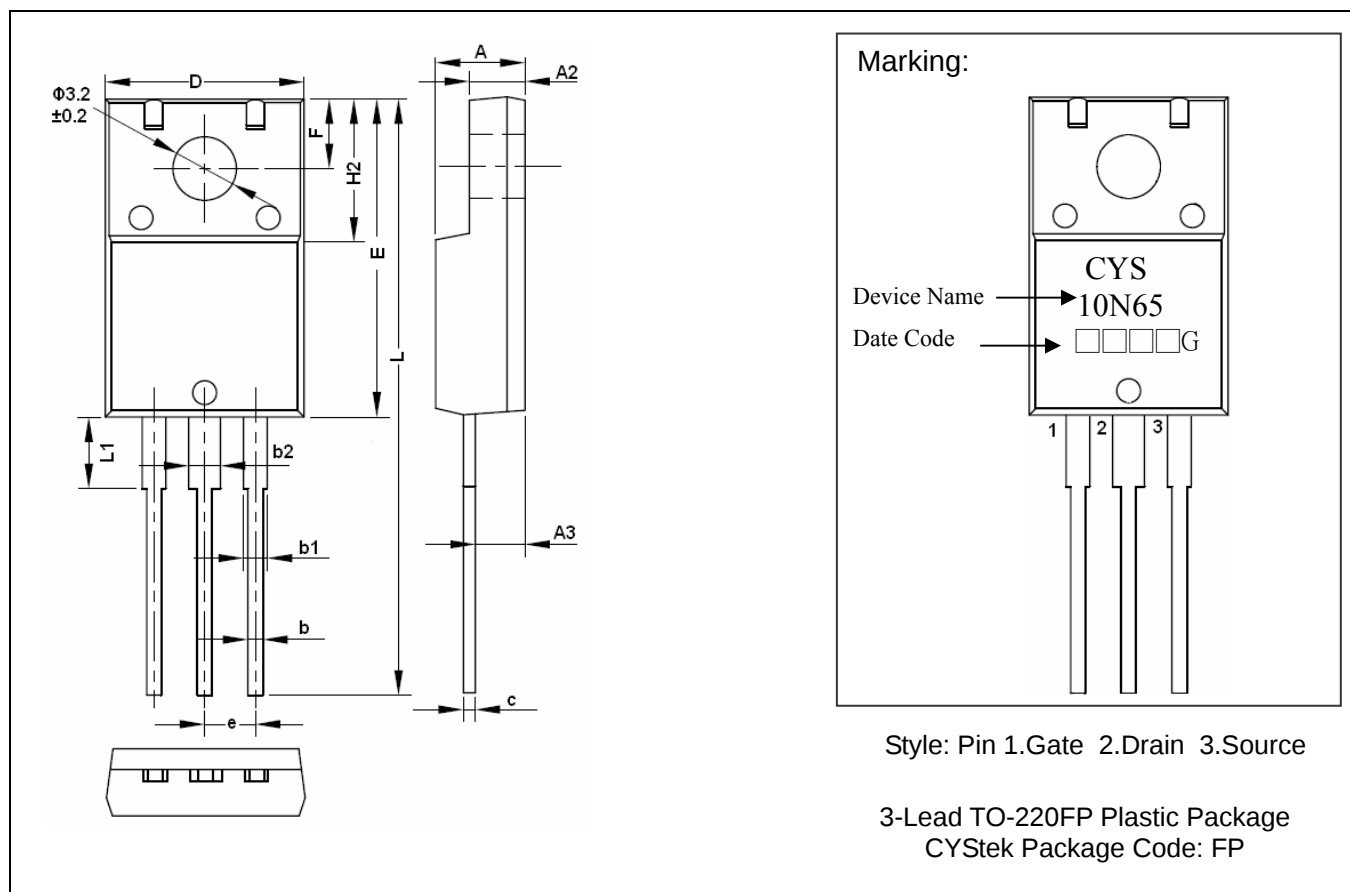


Figure 24. Unclamped Inductive Switching Waveforms

TO-220FP Dimension



*Typical

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	4.20	4.80	0.1654	0.1890	D	9.70	10.30	0.3819	0.4055
A2	2.50	3.10	0.0984	0.1220	E	15.70	16.30	0.6181	0.6417
A3	2.20	2.80	0.0866	0.1102	e	2.35	2.75	0.0925	0.1083
b	0.74	0.78	0.0291	0.0307	F	3.20	3.80	0.1260	0.1496
b1	0.90	1.50	0.0354	0.0591	H2	6.90	7.50	0.2717	0.2953
b2	1.30	1.90	0.0512	0.0748	L	29.20	30.80	1.1496	1.2126
c	0.30	0.90	0.0118	0.0354	L1	3.40	3.80	0.1339	0.1496

Notes: 1.Controlling dimension: millimeters.

2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.

3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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