N-Channel Enhancement Mode Power MOSFET

MTN9N50FP

BV_{DSS} : 500V
$R_{DS(ON)}$: 0.78Ω typ.
I_D : 8.5A

Description

The MTN9N50FP is a N-channel enhancement-mode MOSFET, providing the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness.
The TO-220 package is universally preferred for all commercial-industrial applications

Features

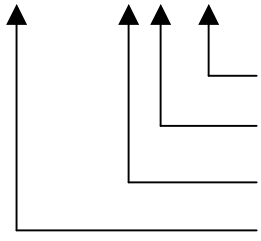
- Low On Resistance
- Simple Drive Requirement
- Low Gate Charge
- Fast Switching Characteristic
- Insulating package, front/back side insulating voltage=2500V(AC)
- RoHS compliant package

Applications

- Ballast
- Inverter

Ordering Information

Device	Package	Shipping
MTN9N50FP-0-UB-S	TO-220FP (RoHS compliant package)	50 pcs/tube, 20 tubes/box, 4 boxes / carton



Environment friendly grade : S for RoHS compliant products, G for RoHS compliant and green compound products

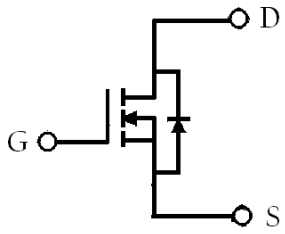
Packing spec, UB : 50 pcs / tube, 20 tubes/box

Product rank, zero for no rank products

Product name

Symbol

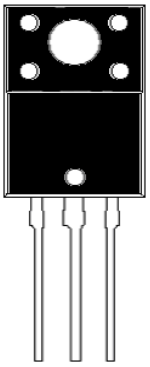
MTN9N50FP



G：Gate
D：Drain
S：Source

Outline

TO-220FP



G D S

Absolute Maximum Ratings (Tc=25°C)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage (Note 1)	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	±30	V
Continuous Drain Current	I_D	8.5*	A
Continuous Drain Current @T_C=100°C	I_D	5.1*	A
Pulsed Drain Current @ V_{GS}=10V (Note 2)	I_{DM}	34*	A
Single Pulse Avalanche Energy (Note 3)	E_{AS}	290	mJ
Avalanche Current (Note 2)	I_{AR}	8	A
Repetitive Avalanche Energy (Note 2)	E_{AR}	12.5	mJ
Peak Diode Recovery dv/dt (Note 4)	dv/dt	3.5	V/ns
Maximum Temperature for Soldering @ Lead at 0.125 in(3.175mm) from case for 10 seconds	T_L	300	°C
Total Power Dissipation (T_C=25℃)	P_D	38.5	W
Linear Derating Factor above 25℃		0.3	W/°C
Operating Junction and Storage Temperature	Tj, Tstg	-55~+150	°C

*Drain current limited by maximum junction temperature

Note : 1. T_J=+25℃ to +150℃.
2. Repetitive rating; pulse width limited by maximum junction temperature.
3. I_{SD}=8A, dI/dt<100A/μs, V_{DD}<BV_{DSS}, T_J=+150℃.
4. I_{AS}=8A, V_{DD}=50V, L=8mH, R_G=25Ω, starting T_J=+25℃.

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{th,j-c}$	3.25	°C/W
Thermal Resistance, Junction-to-ambient, max	$R_{th,j-a}$	62.5	°C/W

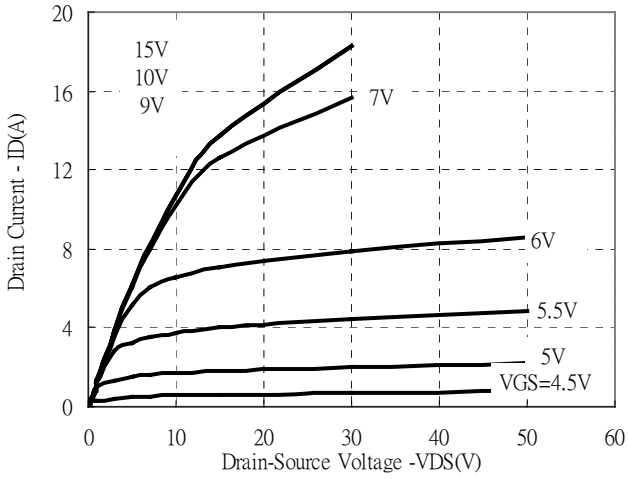
Characteristics (Tj=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV_{DSS}	500	-	-	V	V_{GS}=0, I_D=250μA
$\Delta BV_{DSS}/\Delta Tj$	-	0.6	-	V/°C	Reference to 25°C, I_D=250μA
$V_{GS(th)}$	2.0	-	4.0	V	V_{DS} = V_{GS}, I_D=250μA
*G_{FS}	-	5	-	S	V_{DS} =15V, I_D=4A
I_{GSS}	-	-	±100	nA	V_{GS}=±30
I_{DSS}	-	-	1	μA	V_{DS} =500V, V_{GS} =0
	-	-	25		V_{DS} =400V, V_{GS} =0, Tj=125°C
*$R_{DS(ON)}$	-	0.78	0.85	Ω	V_{GS} =10V, I_D=4A
Dynamic					
*Qg	-	30	-	nC	I_D=8A, V_{DD}=250V, V_{GS}=10V
*Qgs	-	5	-		
*Qgd	-	16	-		
*$t_{d(ON)}$	-	14	-	ns	V_{DD}=250V, I_D=8A, V_{GS}=10V, R_G=10Ω
*tr	-	23	-		
*$t_{d(OFF)}$	-	49	-		
*t_f	-	20	-		
Ciss	-	1411	-	pF	V_{GS}=0V, V_{DS}=25V, f=1MHz
Coss	-	117	-		
Crss	-	26	-		
Source-Drain Diode					
*V_{SD}	-	-	1.5	V	I_S=8A, V_{GS}=0V
*I_S	-	-	8	A	V_D=V_G=0, V_S=1.3V
*I_{SM}	-	-	32		
*trr	-	460	-	ns	V_{GS}=0, I_F=8A, dI/dt=100A/μs
*Qrr	-	4.2	-	μC	

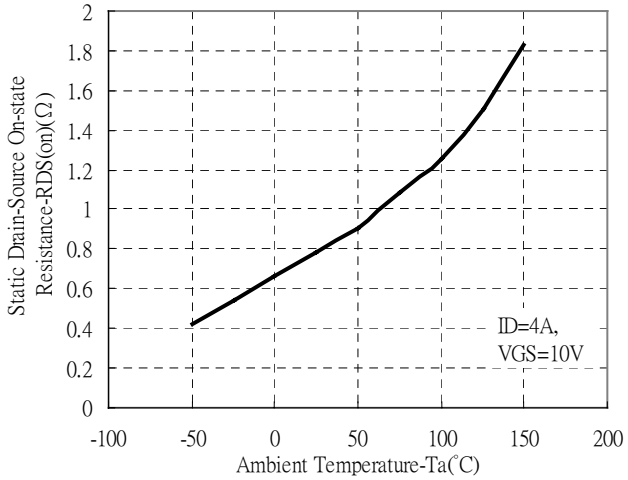
*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Typical Characteristics

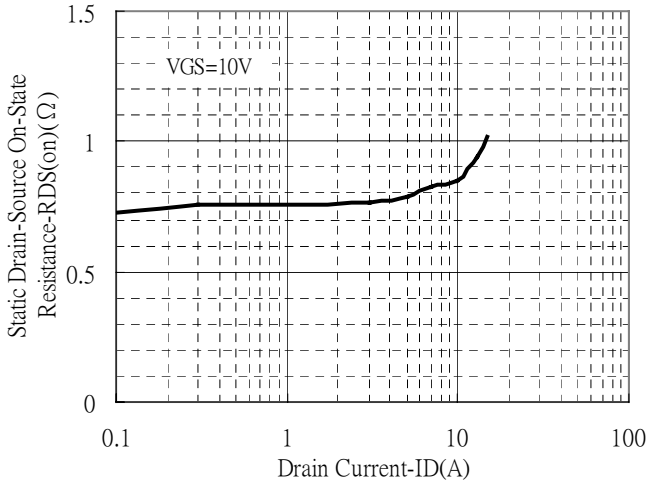
Typical Output Characteristics



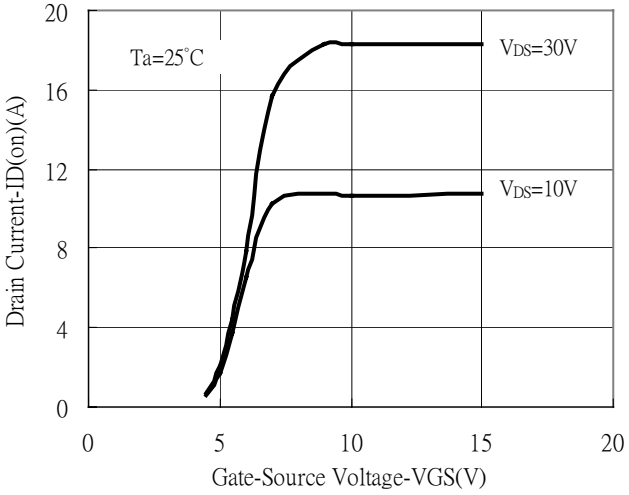
Static Drain-Source On-resistance vs Ambient Temperature



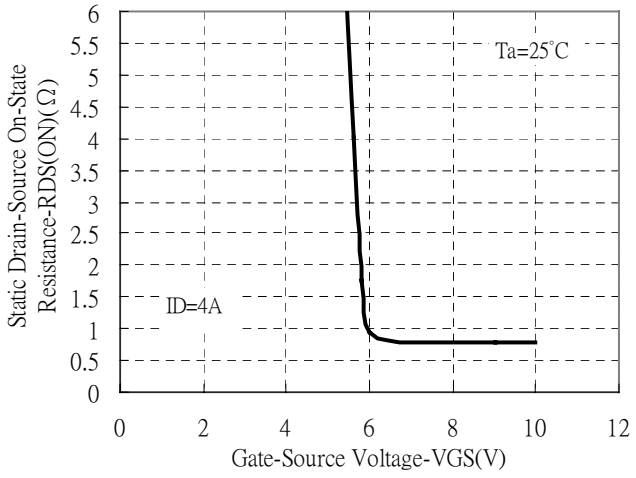
Static Drain-Source On-State resistance vs Drain Current



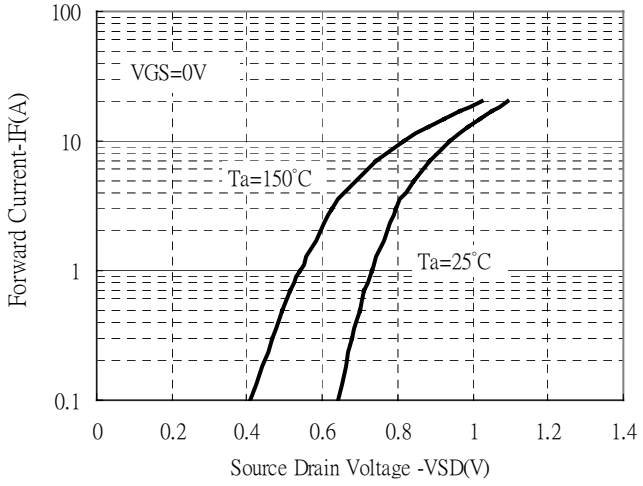
Drain Current vs Gate-Source Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

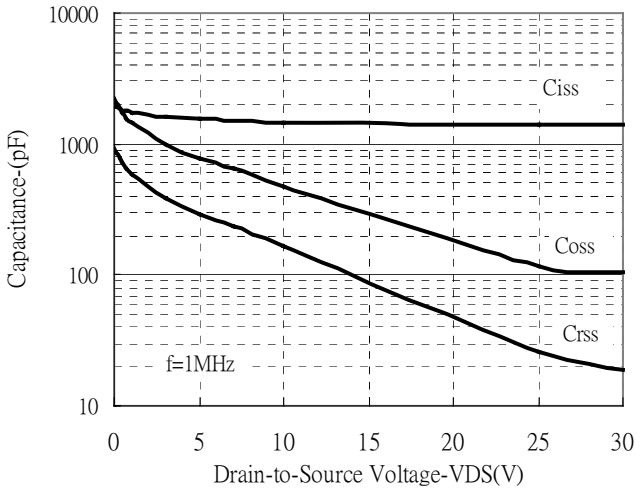


Forward Drain Current vs Source-Drain Voltage

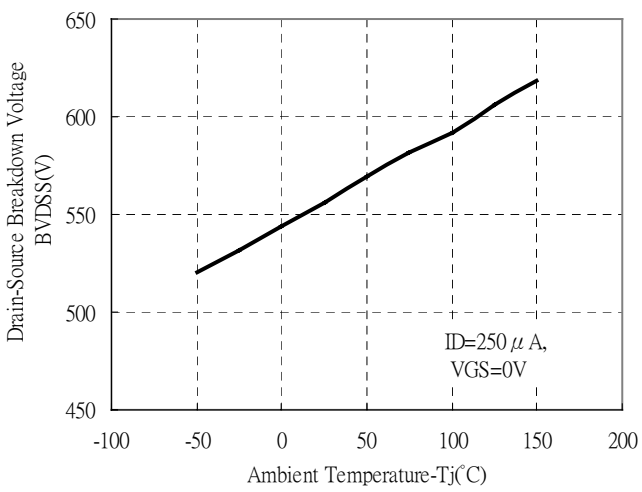


Typical Characteristics(cont.)

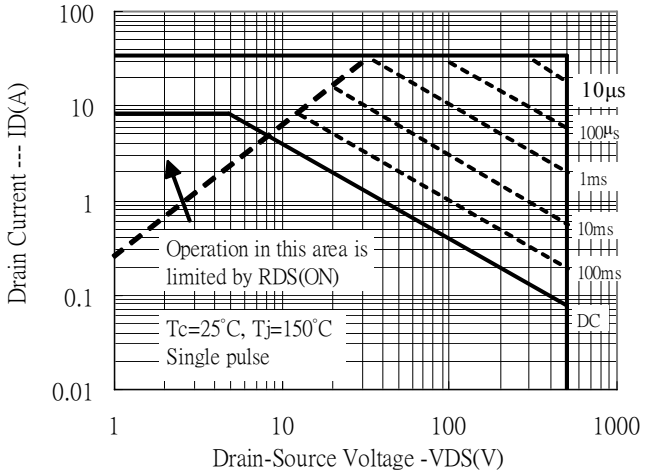
Capacitance vs Reverse Voltage



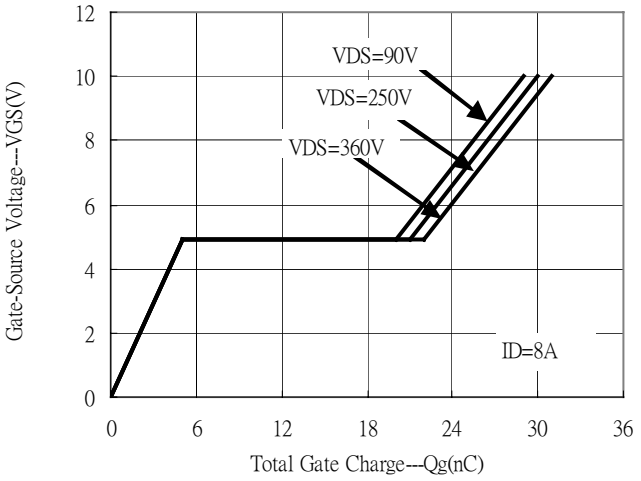
Brekdown Voltage vs Ambient Temperature



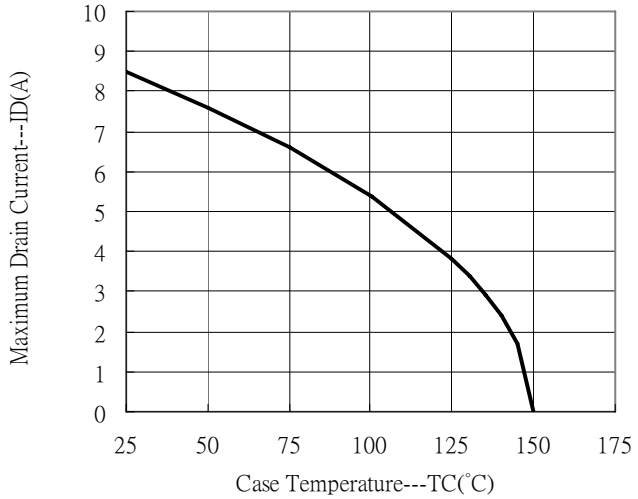
Maximum Safe Operating Area



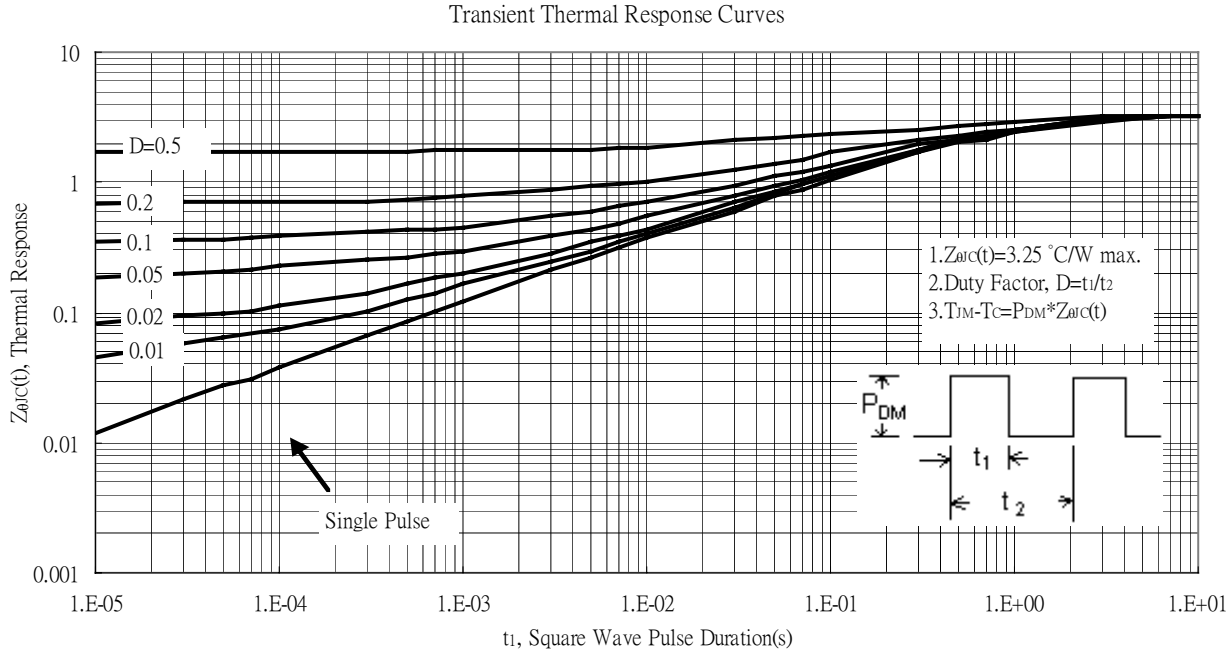
Gate Charge Characteristics



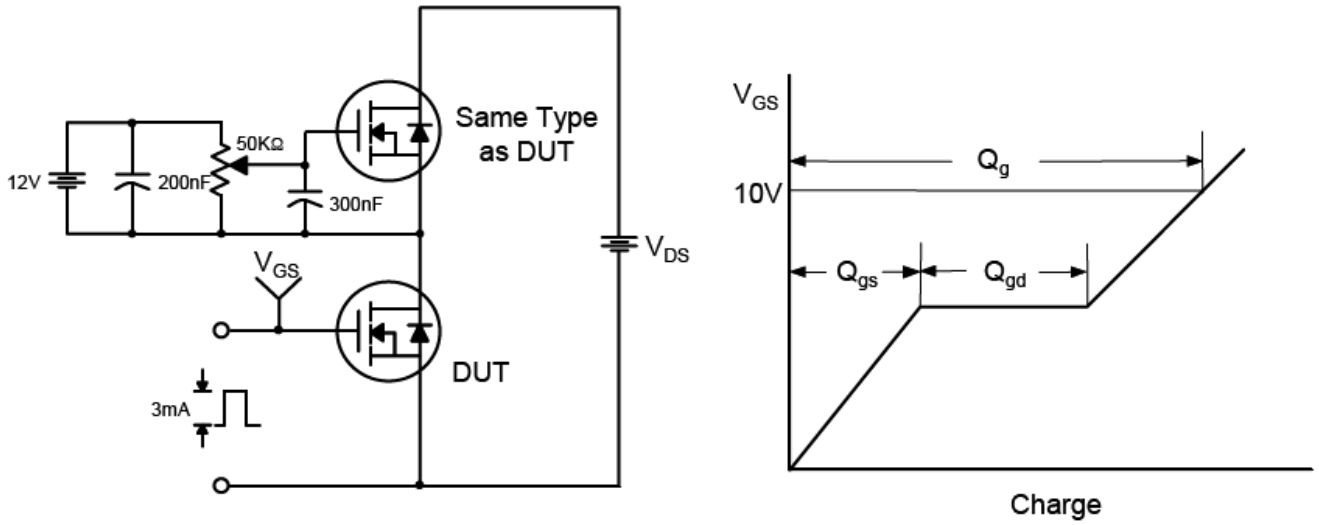
Maximum Drain Current vs Case Temperature



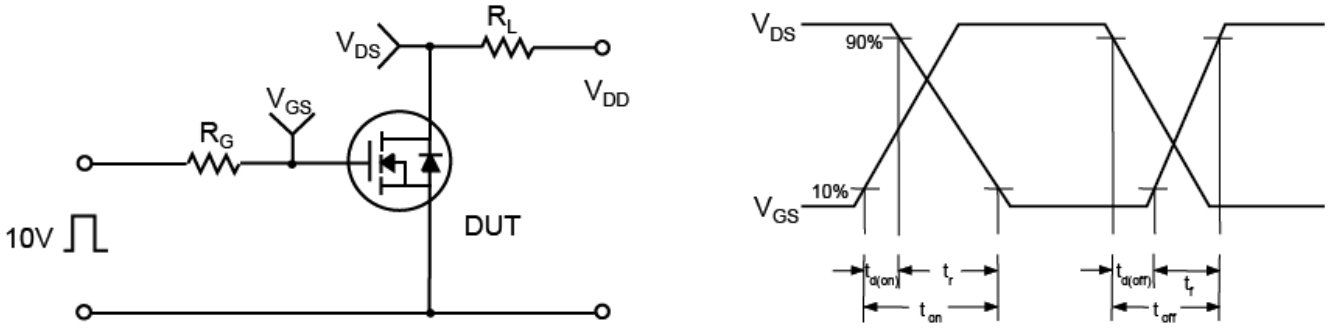
Characteristic Curves(Cont.)



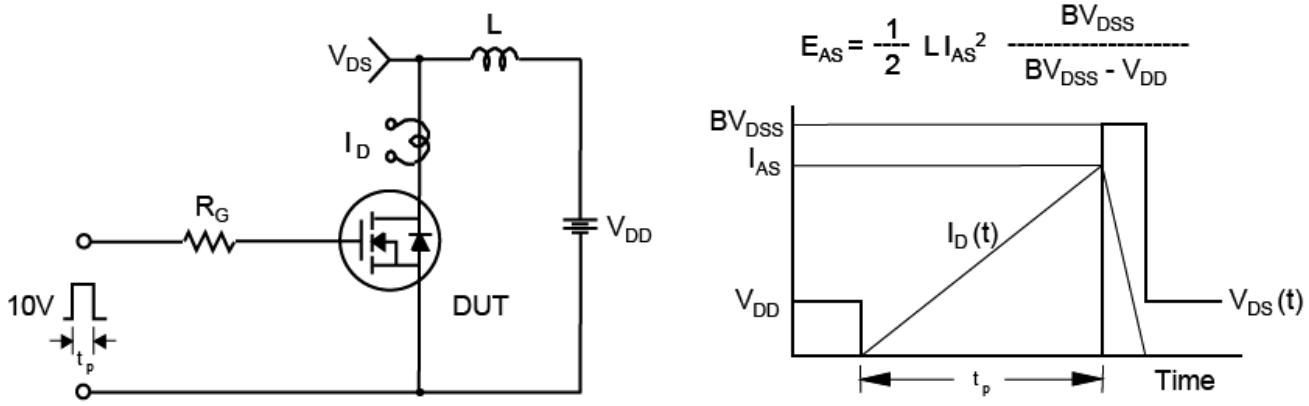
Test Circuit and Waveforms



Resistive Switching Test Circuit & Waveforms

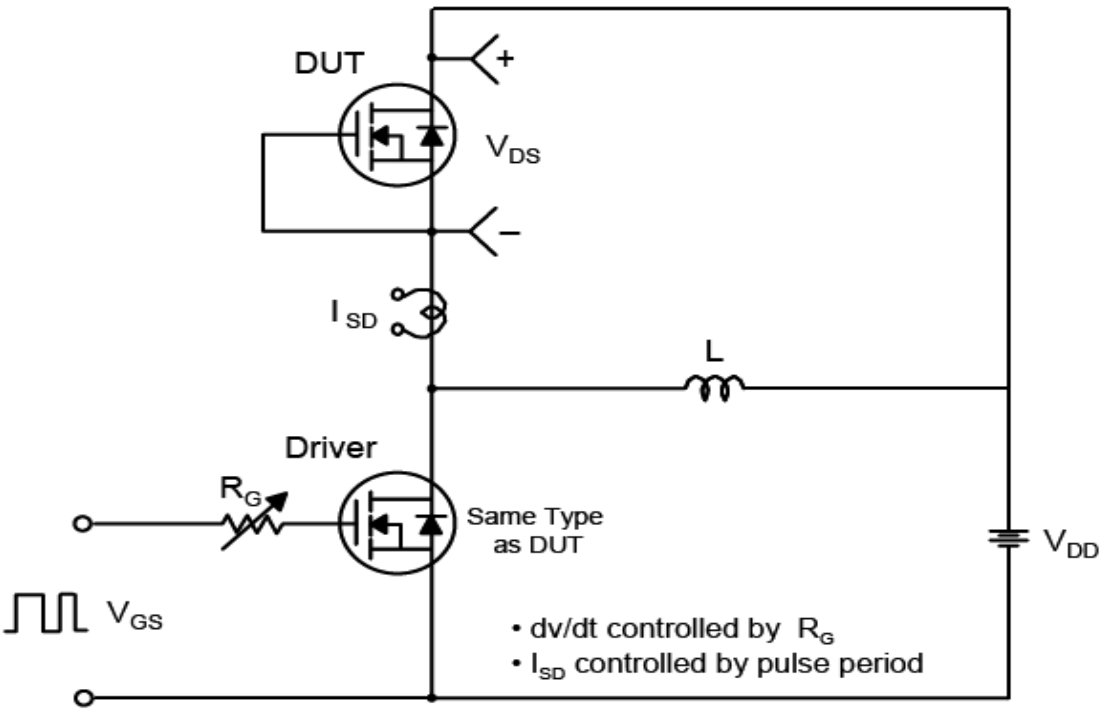


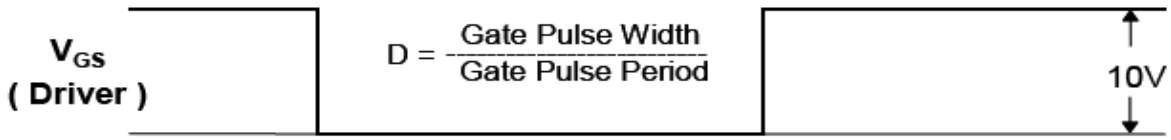
Unclamped Inductive Switching Test Circuit & Waveforms

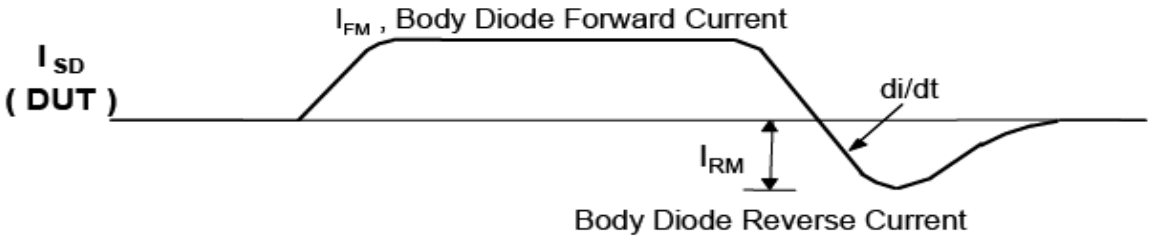


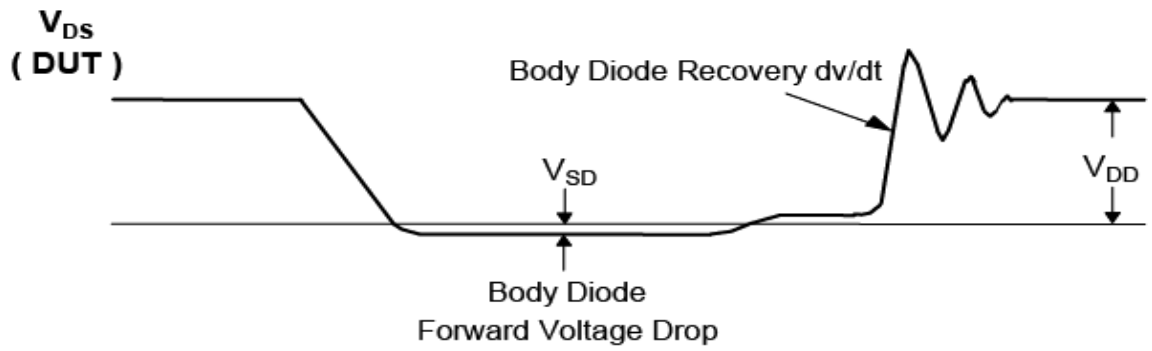
Test Circuit and Waveforms(Cont.)

Peak Diode Recovery dv/dt Test Circuit & Waveforms

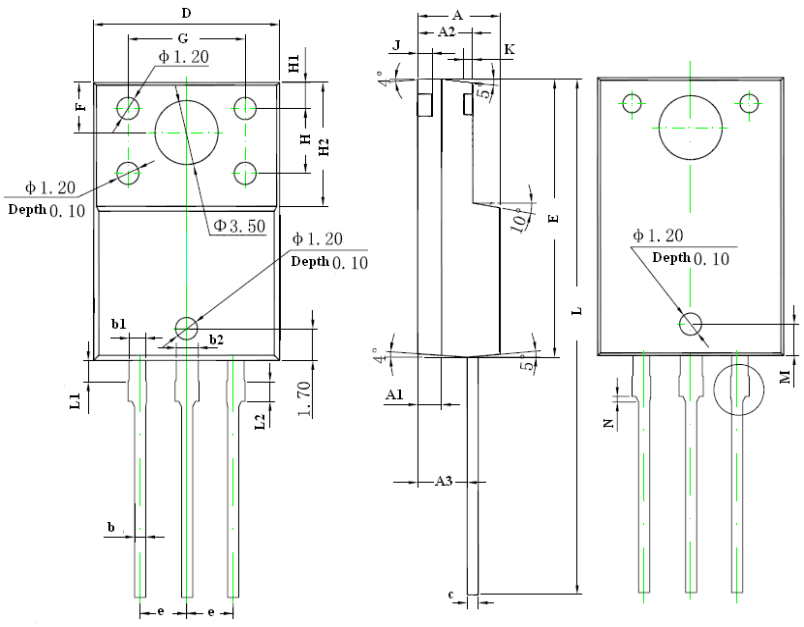


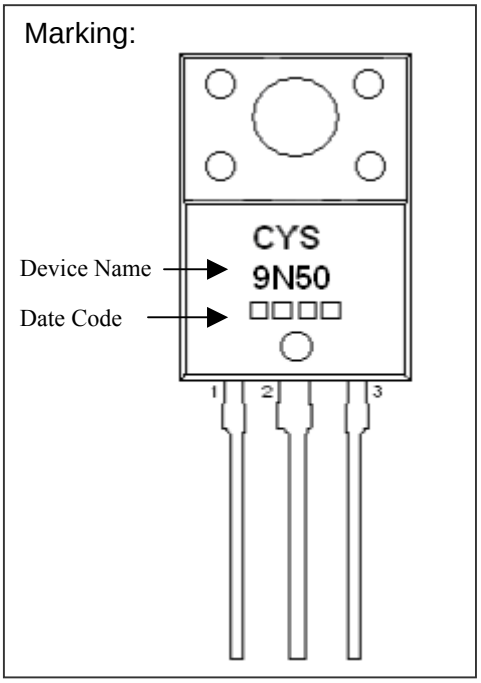






TO-220FP Dimension





3-Lead TO-220FP Plastic Package
CYStek Package Code: FP

Style: Pin 1.Gate 2.Drain 3.Source

*Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.171	0.183	4.35	4.65	G	0.246	0.258	6.25	6.55
A1	0.051 REF		1.300 REF		H	0.138 REF		3.50 REF	
A2	0.112	0.124	2.85	3.15	H1	0.055 REF		1.40 REF	
A3	0.102	0.110	2.60	2.80	H2	0.256	0.272	6.50	6.90
b	0.020	0.030	0.50	0.75	J	0.031 REF		0.80 REF	
b1	0.031	0.041	0.80	1.05	K	0.020		0.50 REF	
b2	0.047 REF		1.20 REF		L	1.102	1.118	28.00	28.40
c	0.020	0.030	0.500	0.750	L1	0.043	0.051	1.10	1.30
D	0.396	0.404	10.06	10.26	L2	0.036	0.043	0.92	1.08
E	0.583	0.598	14.80	15.20	M	0.067 REF		1.70 REF	
e	0.100 *		2.54*		N	0.012 REF		0.30 REF	
F	0.106 REF		2.70 REF						

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.