N-Channel Enhancement Mode Power MOSFET

MTN9N65CFP

BV_{DSS}	650V
I_D @ V_{GS}=10V, T_C=25°C	8.5A
$R_{DSON(TYP)}$ @ V_{GS}=10V, I_D=5.4A	0.65Ω

Description

The MTN9N65CFP is a N-channel enhancement-mode MOSFET, providing the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness.
The TO-220FP package is universally preferred for all commercial-industrial applications

Features

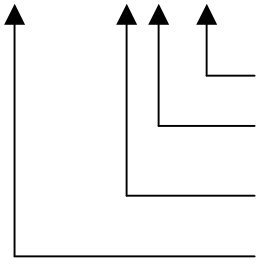
- Low On Resistance
- Simple Drive Requirement
- Low Gate Charge
- Fast Switching Characteristic
- Insulating package, front/back side insulating voltage=2500V(AC)
- RoHS compliant package

Applications

- Power Factor Correction
- LCD TV Power
- Full and Half Bridge Power

Ordering Information

Device	Package	Shipping
MTN9N65CFP-0-UB-S	TO-220FP (RoHS compliant package)	50 pcs/tube, 20 tubes/box, 4 boxes / carton



Environment friendly grade : S for RoHS compliant products, G for RoHS compliant and green compound products

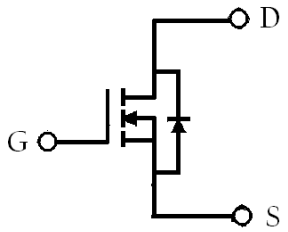
Packing spec, UB : 50 pcs / tube, 20 tubes/box

Product rank, zero for no rank products

Product name

Symbol

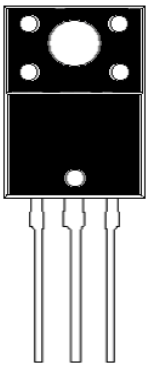
MTN9N65CFP



G：Gate D：Drain S：Source

Outline

TO-220FP



G D S

Absolute Maximum Ratings (Tc=25°C)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage (Note 1)	V_{DS}	650	V
Gate-Source Voltage	V_{GS}	±30	
Continuous Drain Current @V_{GS}=10V, T_C=25°C	I_D	8.5*	A
Continuous Drain Current @V_{GS}=10V, T_C=100°C		5.4*	
Pulsed Drain Current @ V_{GS}=10V (Note 2)	I_{DM}	34*	
Single Pulse Avalanche Current @ L=0.1mH	I_{AS}	8.5	
Single Pulse Avalanche Energy @ L=5mH, I_D=6 Amps, V_{DD}=50V (Note 3)	E_{AS}	90	mJ
Repetitive Avalanche Energy (Note 2)	E_{AR}	5	
Maximum Temperature for Soldering @ Lead at 0.063 in(1.6mm) from case for 10 seconds	T_L	300	°C
Maximum Temperature for Soldering @ Package Body for 10 seconds	T_{PKG}	260	
Total Power Dissipation (T_C=25℃)	P_D	50	W
Linear Derating Factor		0.4	W/°C
Operating Junction and Storage Temperature	Tj, Tstg	-55~+150	°C

*Drain current limited by maximum junction temperature

Note : 1. T_J=+25℃ to +150℃.

2. Pulse width limited by maximum junction temperature.
3. 100% tested by conditions of L=5mH, I_{AS}=3.6A, V_{GS}=10V, V_{DD}=50V.

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction-to-ambient, max	$R_{\theta JA}$	62.5	

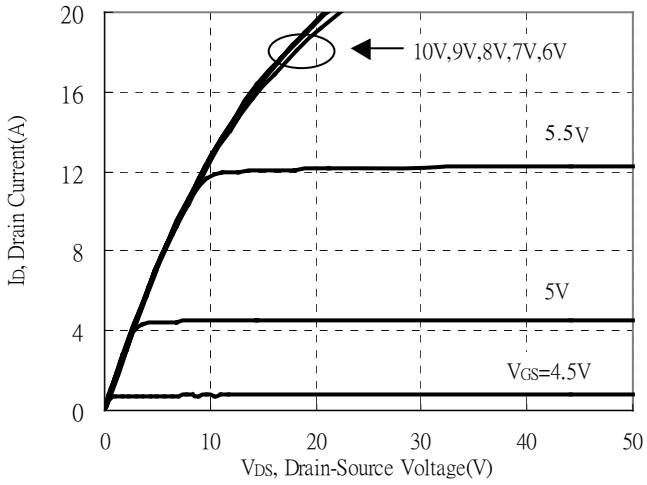
Characteristics (Tj=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV_{DSS}	650	-	-	V	V_{GS}=0V, I_D=250μA
$\Delta BV_{DSS}/\Delta Tj$	-	0.7	-	V/°C	Reference to 25°C, I_D=250μA
$V_{GS(th)}$	2.0	-	4.0	V	V_{DS} = V_{GS}, I_D=250μA
*G_{FS}	-	11.6	-	S	V_{DS} =15V, I_D=5A
I_{GSS}	-	-	±100	nA	V_{GS}=±30V
I_{DSS}	-	-	1	μA	V_{DS} =650V, V_{GS} =0V
I_{DSS}	-	-	10		V_{DS} =520V, V_{GS} =0V, Tj=125°C
*$R_{DS(ON)}$	-	0.65	0.85	Ω	V_{GS} =10V, I_D=5.4A
Dynamic					
*Qg	-	35.4	-	nC	I_D=8.5A, V_{DD}=325V, V_{GS}=10V
*Qgs	-	8.2	-		
*Qgd	-	10.3	-		
*$t_{d(ON)}$	-	18.2	-	ns	V_{DD}=325V, I_D=8.5A, V_{GS}=10V, R_G=2.7Ω
*tr	-	8	-		
*$t_{d(OFF)}$	-	47.8	-		
*t_f	-	9.8	-		
Ciss	-	1689	-	pF	V_{GS}=0V, V_{DS}=25V, f=1MHz
Coss	-	138	-		
Crss	-	25	-		
Source-Drain Diode					
*V_{SD}	-	0.82	1.2	V	I_S=8.5A, V_{GS}=0V
*I_S	-	-	8.5	A	
*I_{SM}	-	-	34		
*trr	-	415	622	ns	V_{GS}=0V, I_F=8.5A, dI_F/dt=100A/μs
*Qrr	-	3.6	5.4	μC	

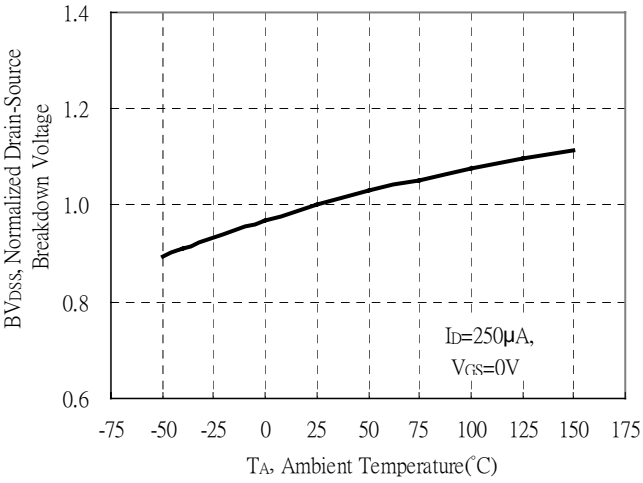
*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Typical Characteristics

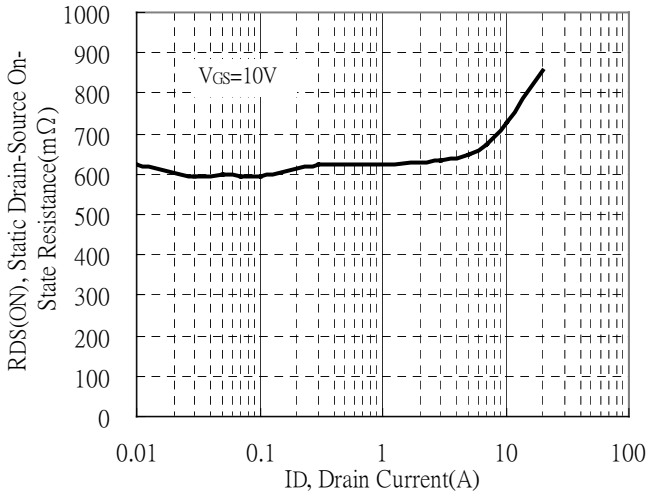
Typical Output Characteristics



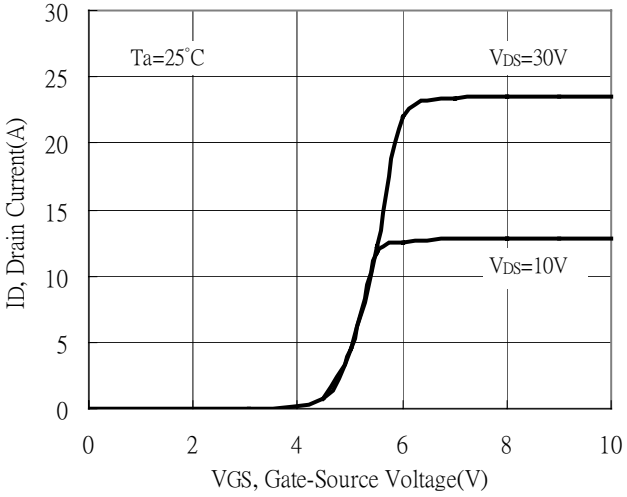
Brekdown Voltage vs Ambient Temperature



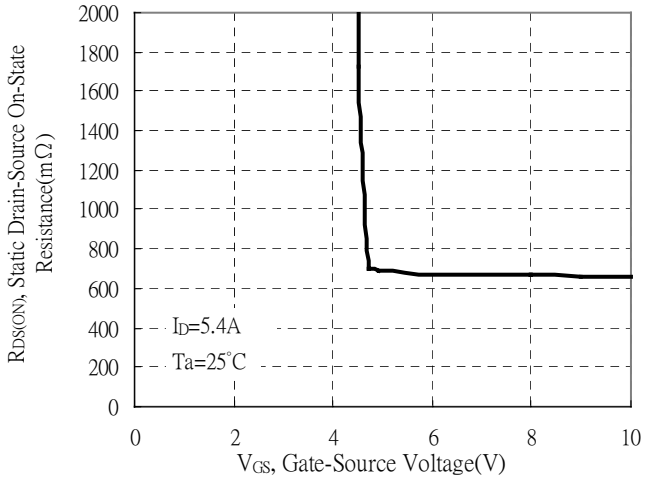
Static Drain-Source On-State resistance vs Drain Current



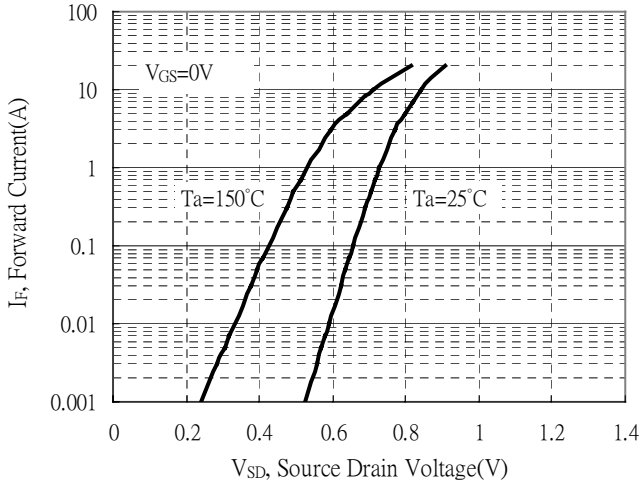
Drain Current vs Gate-Source Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

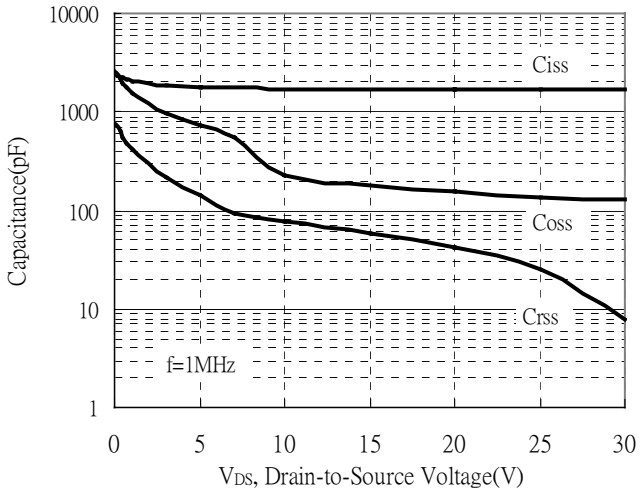


Forward Drain Current vs Source-Drain Voltage

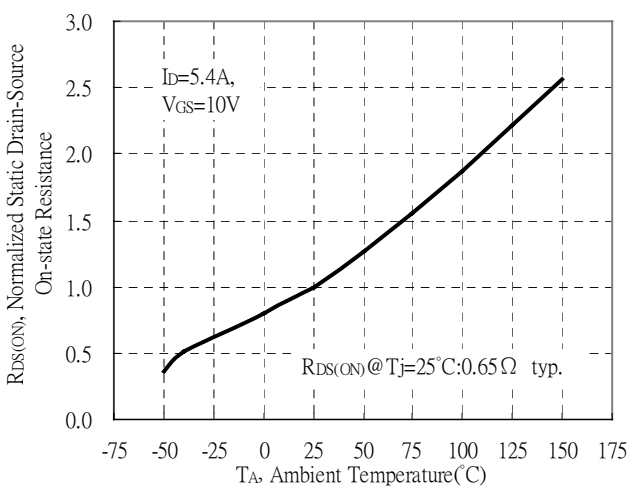


Typical Characteristics(Cont.)

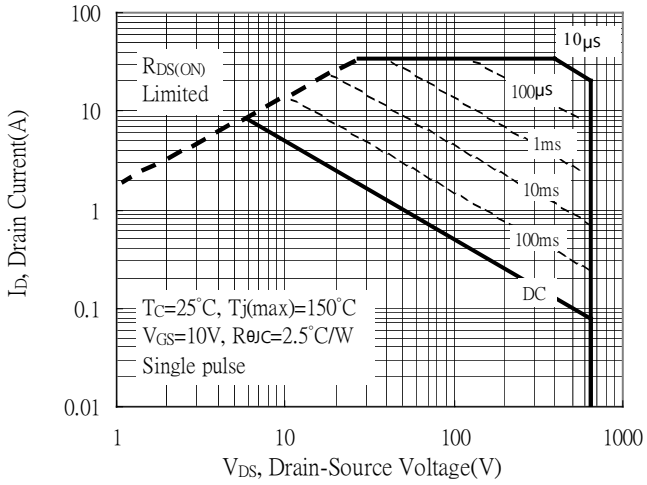
Capacitance vs Reverse Voltage



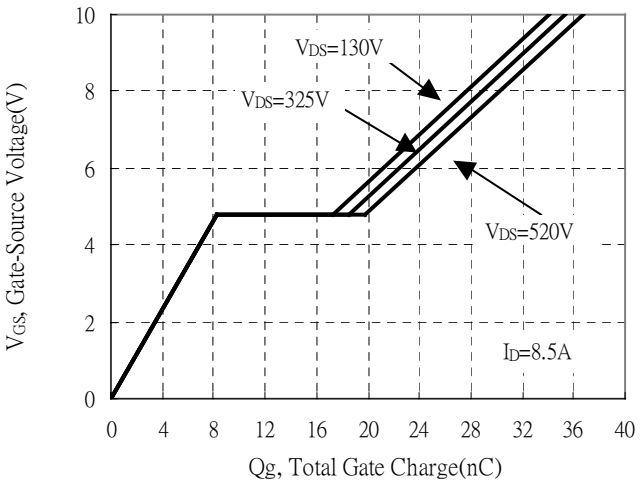
Static Drain-Source On-resistance vs Ambient Temperature



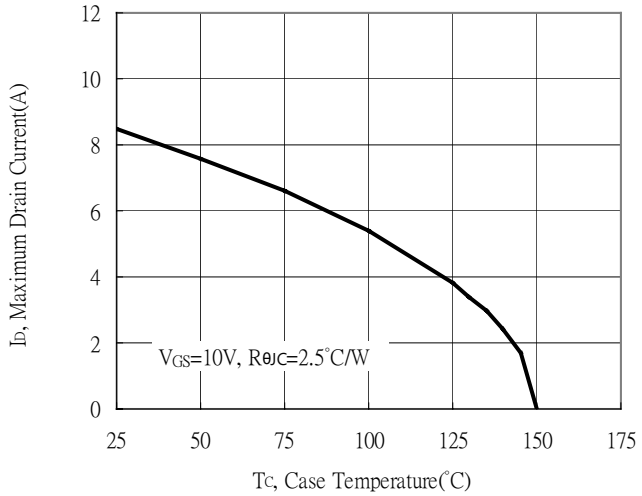
Maximum Safe Operating Area



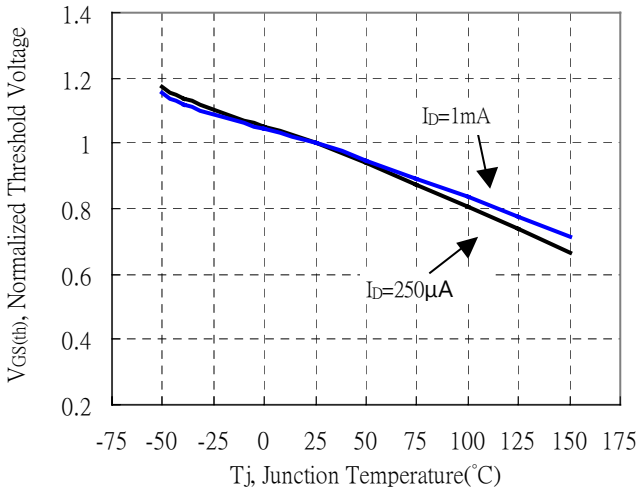
Gate Charge Characteristics



Maximum Drain Current vs Case Temperature

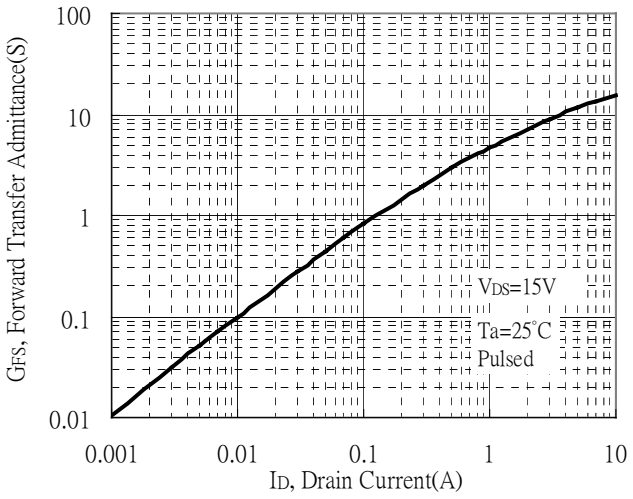


Threshold Voltage vs Junction Tempearture

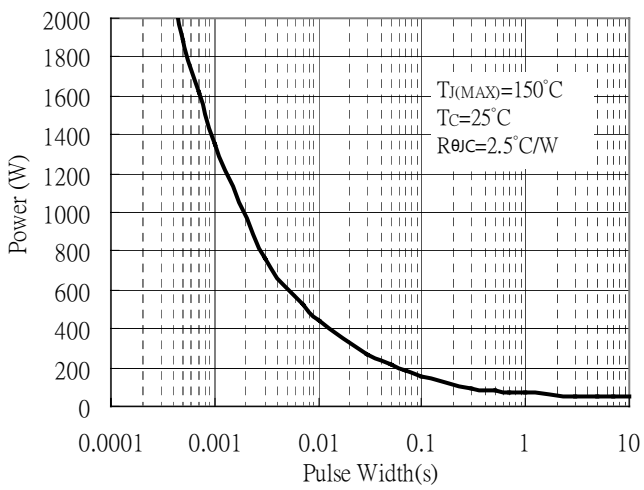


Typical Characteristics(Cont.)

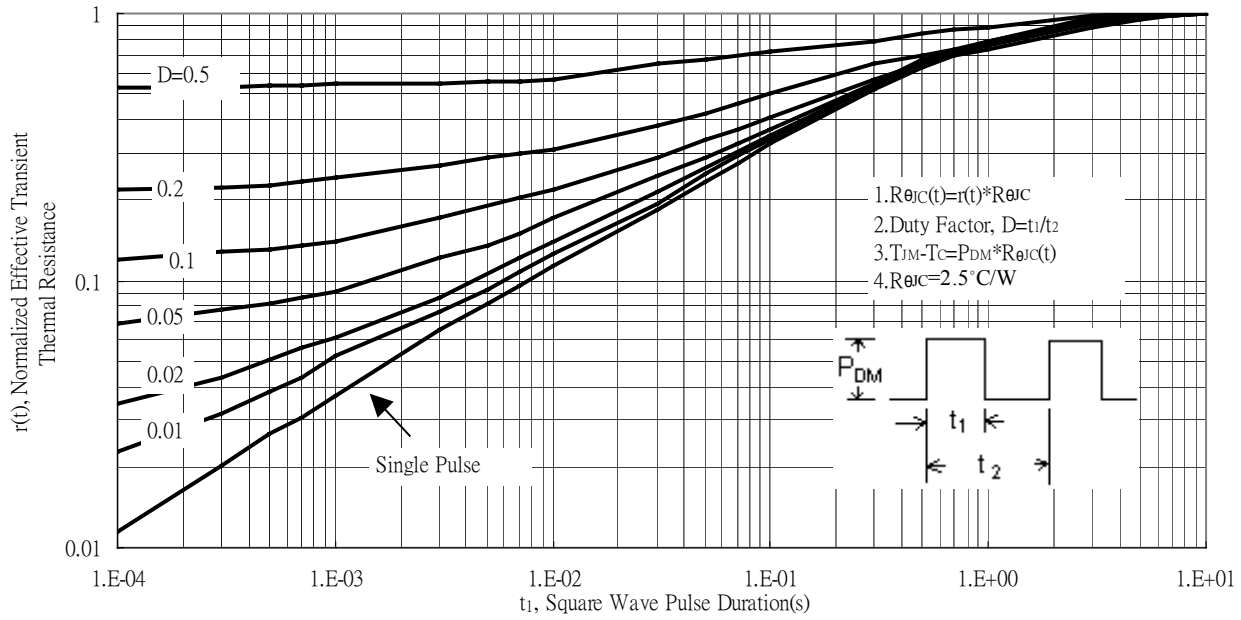
Forward Transfer Admittance vs Drain Current



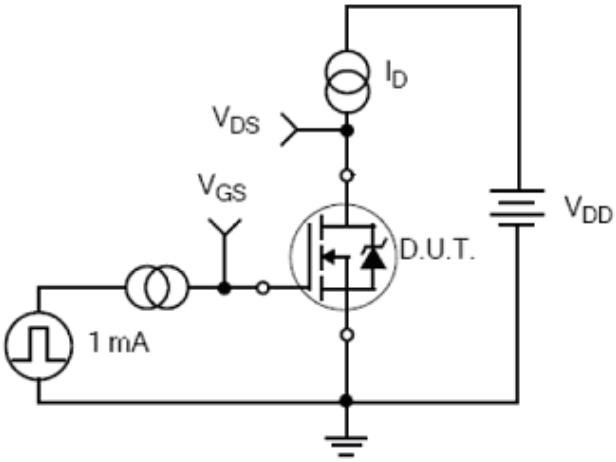
Single Pulse Power Rating, Junction to Case



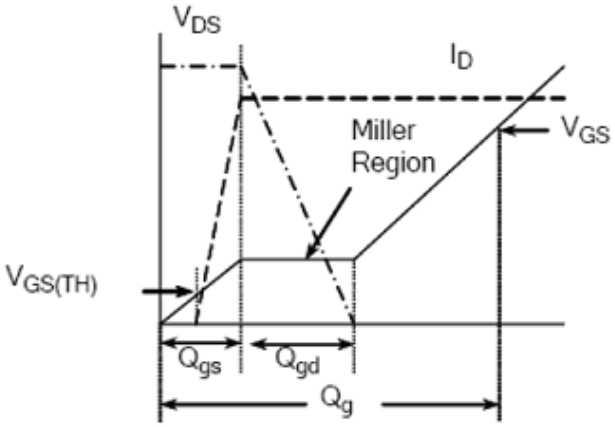
Transient Thermal Response Curves



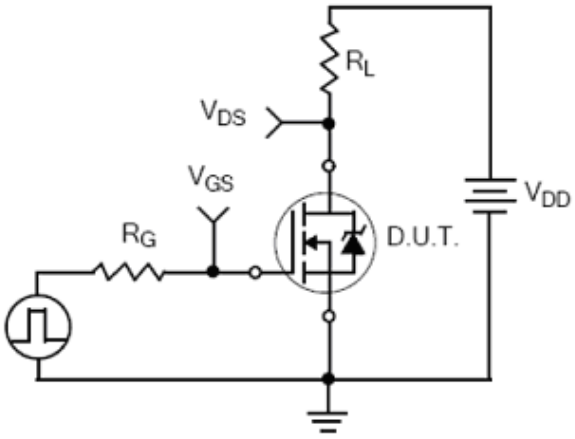
Test Circuit and Waveforms



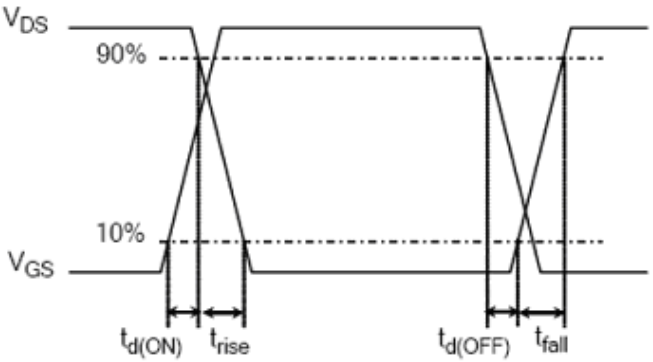
Gate Charge Test Circuit



Gate Charge Waveform

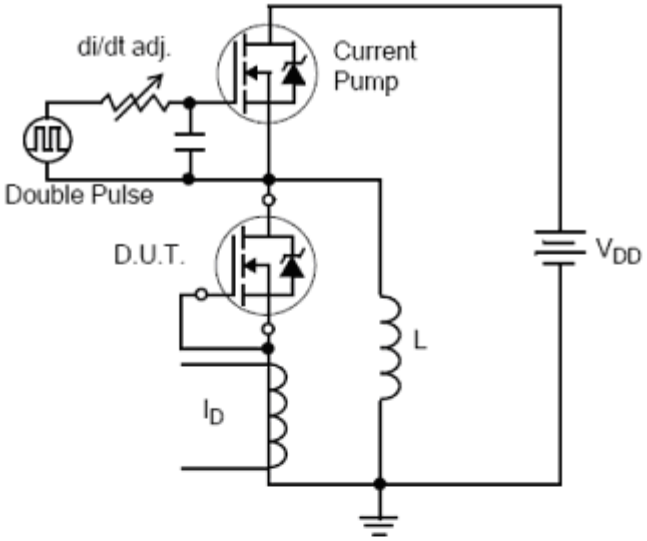


Resistive Switching Test Circuit

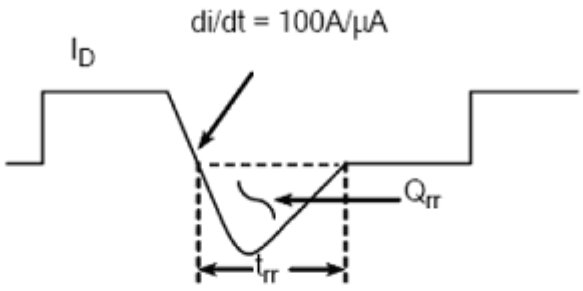


Resistive Switching Waveforms

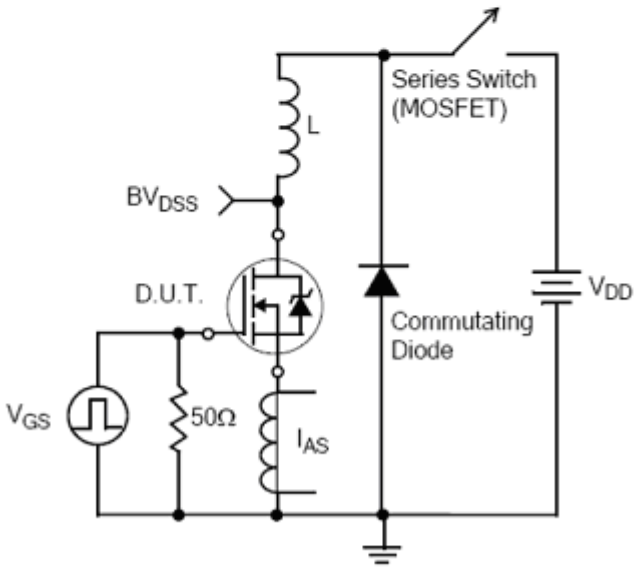
Test Circuit and Waveforms(Cont.)



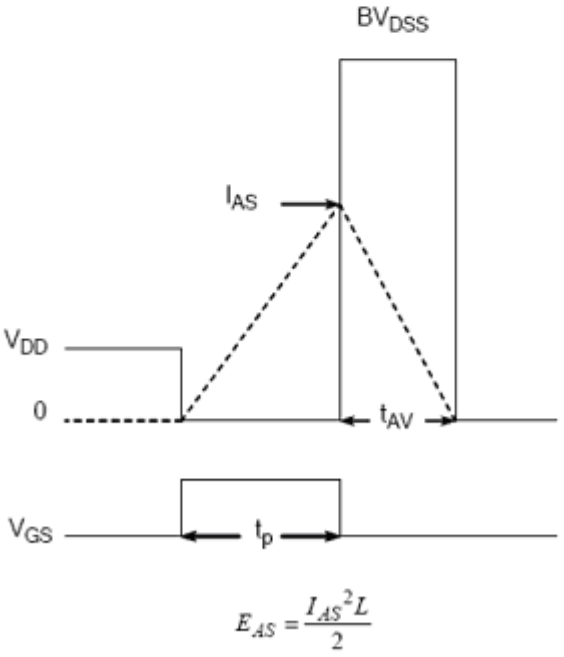
Diode Reverse Recovery Test Circuit



Diode Reverse Recovery Waveform



Unclamped Inductive Switching Test Circuit



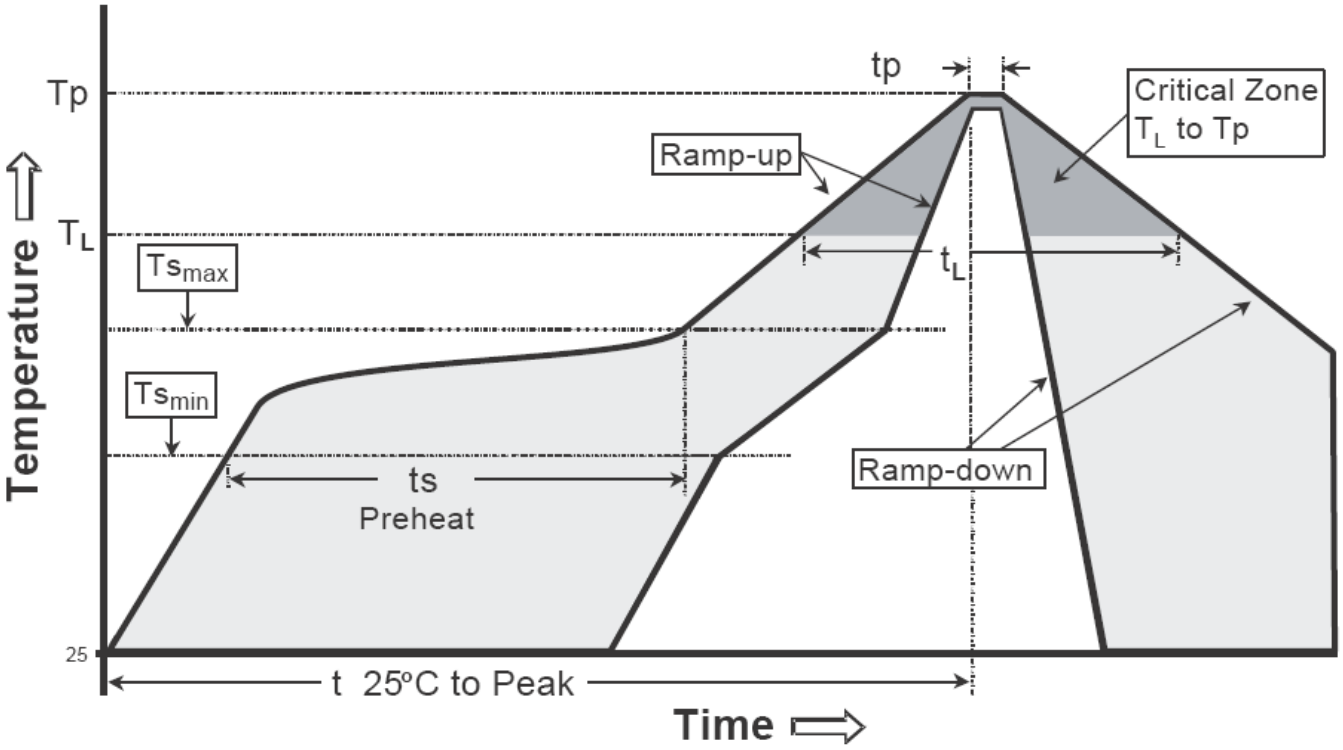
$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

Unclamped Inductive Switching Waveforms

Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

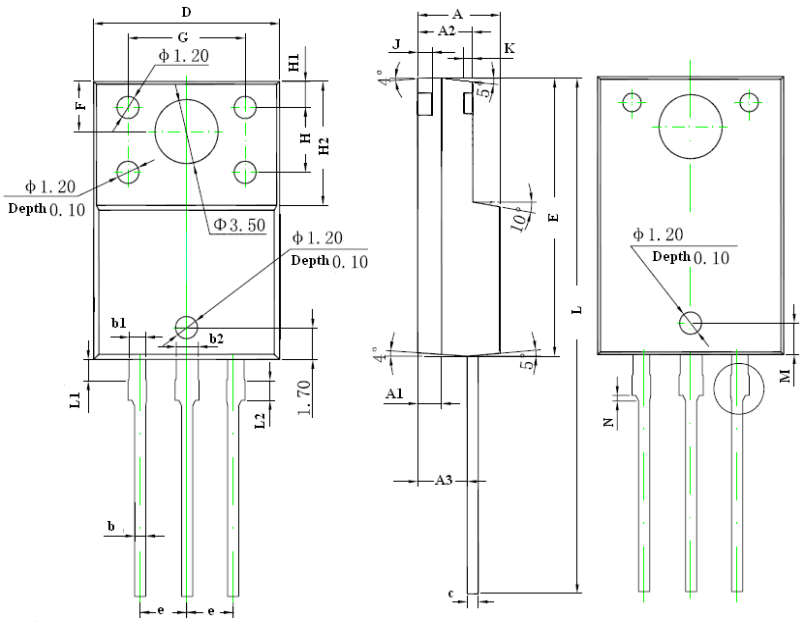
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(Ts min) −Temperature Max(Ts max) −Time(ts min to ts max)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: −Temperature (TL) − Time (tL)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

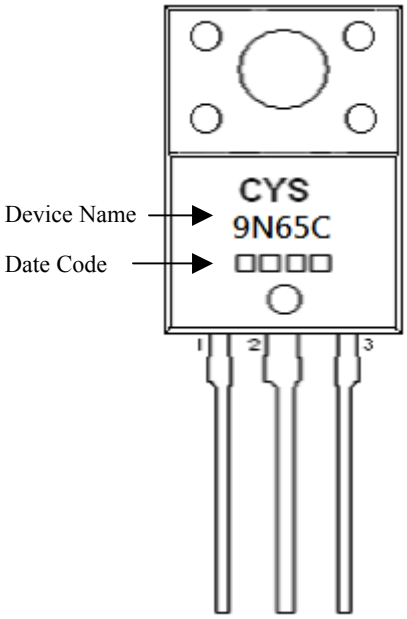
Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-220FP Dimension



3-Lead TO-220FP Plastic Package
CYStek Package Code: FP

Marking:



Style: Pin 1.Gate 2.Drain 3.Source

*Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.171	0.183	4.35	4.65	G	0.246	0.258	6.25	6.55
A1	0.051 REF		1.300 REF		H	0.138 REF		3.50 REF	
A2	0.112	0.124	2.85	3.15	H1	0.055 REF		1.40 REF	
A3	0.102	0.110	2.60	2.80	H2	0.256	0.272	6.50	6.90
b	0.020	0.030	0.50	0.75	J	0.031 REF		0.80 REF	
b1	0.031	0.041	0.80	1.05	K	0.020		0.50 REF	
b2	0.047 REF		1.20 REF		L	1.102	1.118	28.00	28.40
c	0.020	0.030	0.500	0.750	L1	0.043	0.051	1.10	1.30
D	0.396	0.404	10.06	10.26	L2	0.036	0.043	0.92	1.08
E	0.583	0.598	14.80	15.20	M	0.067 REF		1.70 REF	
e	0.100 *		2.54*		N	0.012 REF		0.30 REF	
F	0.106 REF		2.70 REF						

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.