Asymmetric Dual N-Channel Enhancement Mode MOSFET

MTNN8451KQ8

	FET1	FET 2
BV_{DSS}	30V	30V
I_D	6.8A	10.2A
$R_{DSON(TYP.)}$@V_{GS}=10V	15mΩ	11mΩ
$R_{DSON(TYP.)}$@V_{GS}=4.5V	23mΩ	18mΩ

Description

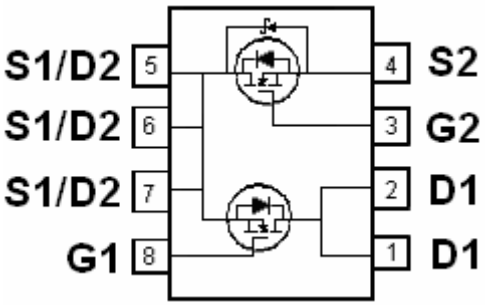
The MTNN8451KQ8 uses advanced trench technology to provide excellent $R_{DS(on)}$ and low gate charge. The two MOSFETs make a compact and efficient switch and synchronous rectifier combination for use in DC-DC converters. A Schottky diode in parallel with the synchronous MOSFET to boost efficiency further.
The SOP-8 package is universally preferred for all commercial-industrial surface mount applications.

Features

- Simple drive requirement
- Low on-resistance
- Fast switching speed
- Pb-free lead plating and halogen-free package

Equivalent Circuit

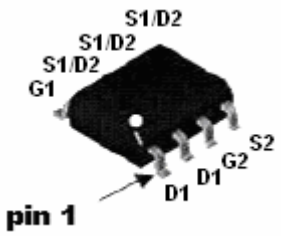
MTNN8451KQ8



G：Gate
S：Source
D：Drain

Outline

SOP-8



Absolute Maximum Ratings (Tc=25°C, unless otherwise noted)

Parameter		Symbol	Limits		Unit
			FET 1	FET 2	
Drain-Source Breakdown Voltage		BV_{DSS}	30	30	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current (Note 2)	T_A=25 °C, V_{GS}=10V	I_D	6.8	10.2	A
	T_A=70 °C, V_{GS}=10V		5.4	8.1	A
Pulsed Drain Current (Note 1)		I_{DM}	30	40	A
Power Dissipation		P_D	1.2 (Note 2)	2 (Note 2)	W
			0.7 (Note 3)	1.1 (Note 3)	W
Operating Junction and Storage Temperature Range		Tj; Tstg	-55~+150		°C

Thermal Data

Parameter	Symbol	Value		Unit
Thermal Resistance, Junction-to-case, max	$R_{th,j-c}$	40		°C/W
Thermal Resistance, Junction-to-ambient, max	$R_{th,j-a}$	104 (Note 2)	62.5 (Note 2)	°C/W
		178 (Note 3)	114 (Note 3)	°C/W

Note : 1.Pulse width limited by maximum junction temperature.
2.Surface mounted on 1 in² copper pad of FR-4 board, pulse width≤10s.
3.Surface mounted on minimum copper pad, pulse width≤10s.

FET 1 Electrical Characteristics (Tj=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV_{DSS}	30	-	-	V	V_{GS}=0, I_D=250μA
$V_{GS(th)}$	1.0	1.7	2.5	V	V_{DS}=V_{GS}, I_D=250μA
I_{GSS}	-	-	±100	nA	V_{GS}=±20V, V_{DS}=0
I_{DSS}	-	-	1	μA	V_{DS}=30V, V_{GS}=0
	-	-	10	μA	V_{DS}=24V, V_{GS}=0, Tj=125°C
*$R_{DS(ON)}$	-	15	20	mΩ	V_{GS}=10V, I_D=6A
	-	23	28	mΩ	V_{GS}=4.5V, I_D=4A
*G_{FS}	-	7.6	-	S	V_{DS}=5V, I_D=5A
Dynamic					
Ciss	-	727	-	pF	V_{DS}=15V, V_{GS}=0, f=1MHz
Coss	-	79	-	pF	
Crss	-	70	-	pF	
*$td_{(ON)}$	-	3.7	-	ns	V_{DS}=15V, I_D=1A, V_{GS}=10V, R_G=3Ω
*tr	-	3.2	-	ns	
*$td_{(OFF)}$	-	10	-	ns	
*tf	-	3.6	-	ns	
*Qg	-	9.3	-	nC	V_{DS}=15V, I_D=6A, V_{GS}=10V
*Qgs	-	2.6	-	nC	
*Qgd	-	3.2	-	nC	
Rg	-	2.2	-	Ω	V_{GS}=15mV, V_{DS}=0V, f=1MHz

Body Diode					
*I_S	-	-	3	A	
*I_{SM}	-	-	12		
*V_{SD}	-	0.73	1	V	V_{GS}=0V, I_S=1A
*trr	-	15	-	ns	I_S=6A, V_{GS}=0V, dI/dt=100A/μs
*Qrr	-	9	-	nC	

*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

FET 2 Electrical Characteristics (Tj=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV_{DSS}	30	-	-	V	V_{GS}=0, I_D=250μA
$V_{GS(th)}$	1.0	1.8	2.5		V_{DS}=V_{GS}, I_D=250μA
I_{GSS}	-	-	±100	nA	V_{GS}=±20V, V_{DS}=0
I_{DSS}	-	-	50	μA	V_{DS}=24V, V_{GS}=0
	-	-	25	mA	V_{DS}=24V, V_{GS}=0, Tj=125°C
*$R_{DS(ON)}$	-	11	15	mΩ	V_{GS}=10V, I_D=9A
	-	18	23		V_{GS}=4.5V, I_D=7A
*G_{FS}	-	9	-	S	V_{DS}=5V, I_D=5A
Dynamic					
Ciss	-	1090	-	pF	V_{DS}=15V, V_{GS}=0, f=1MHz
Coss	-	149	-		
Crss	-	105	-		
*$td_{(ON)}$	-	5.8	-	ns	V_{DS}=15V, I_D=1A, V_{GS}=10V, R_G=3Ω
*tr	-	4.7	-		
*$td_{(OFF)}$	-	16	-		
*tf	-	5.4	-		
*Qg	-	12.7	-	nC	V_{DS}=15V, I_D=9A, V_{GS}=10V
*Qgs	-	4.5	-		
*Qgd	-	4.6	-		
Rg	-	2	-	Ω	V_{GS}=15mV, V_{DS}=0V, f=1MHz
Body Diode					
*I_S	-	-	4.5	A	
*I_{SM}	-	-	18		
*V_{SD}	-	0.5	0.6	V	V_{GS}=0V, I_S=1A
*trr	-	20	-	ns	I_S=9A, V_{GS}=0V, dI/dt=100A/μs
*Qrr	-	12	-	nC	

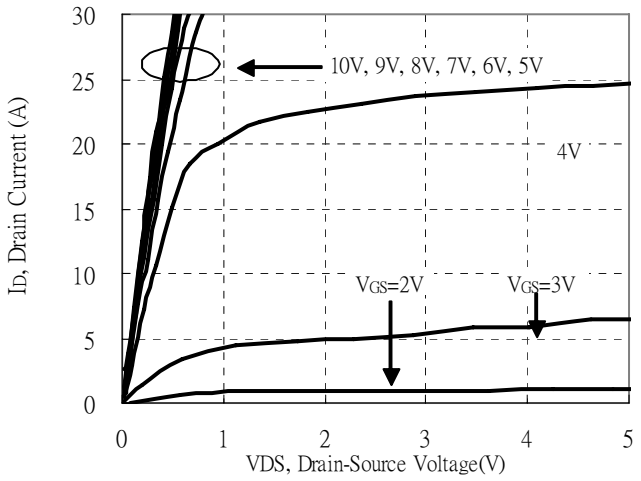
*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Ordering Information

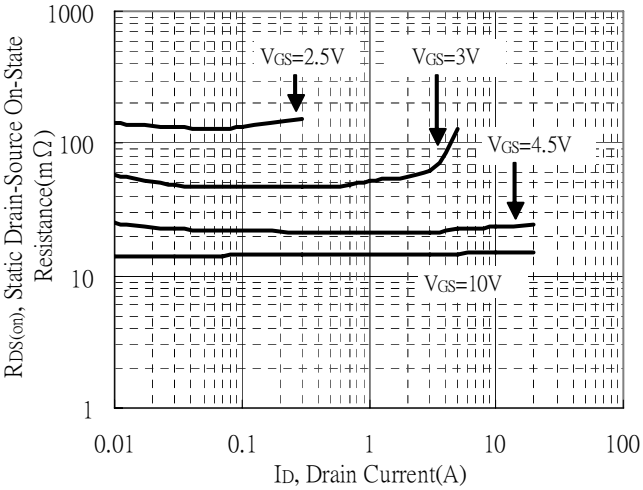
Device	Package	Shipping	Marking
MTNN8451KQ8	SOP-8 (Pb-free lead plating & halogen-free package)	2500 pcs / Tape & Reel	8451

Typical Characteristics : FET 1

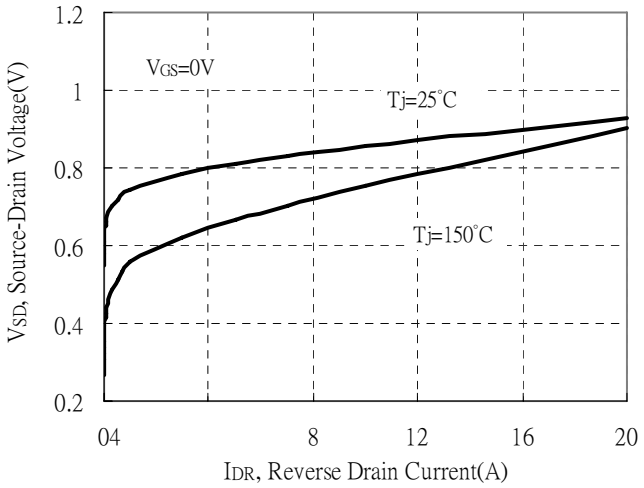
Typical Output Characteristics



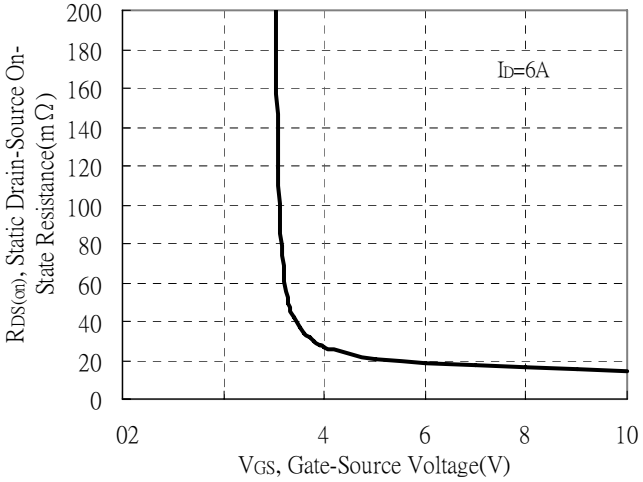
Static Drain-Source On-State resistance vs Drain Current



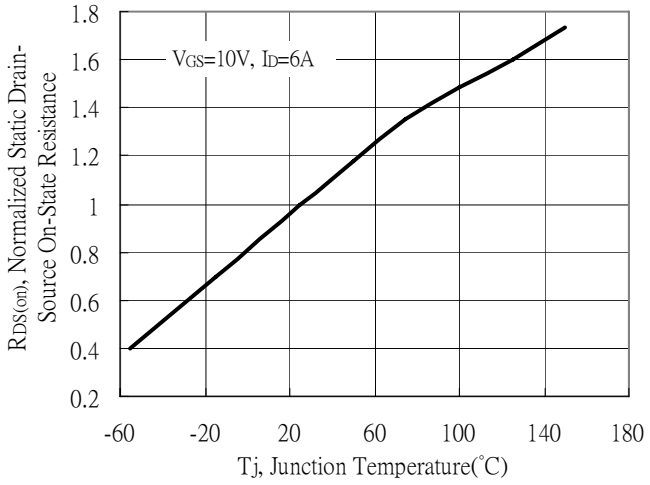
Reverse Drain Current vs Source-Drain Voltage



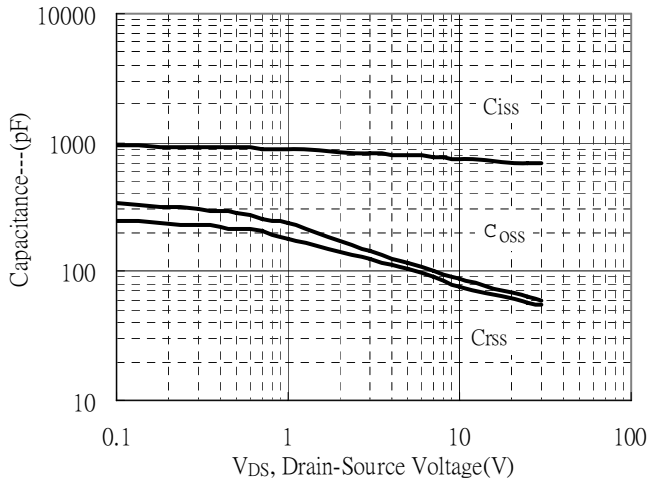
Static Drain-Source On-State Resistance vs Gate-Source Voltage



Drain-Source On-State Resistance vs Junction Tempearture

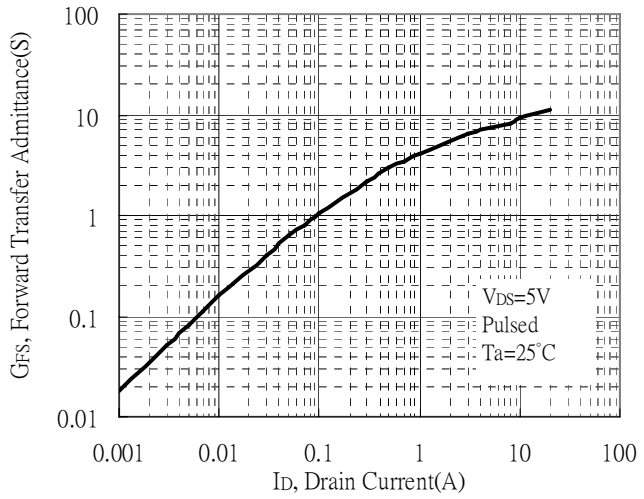


Capacitance vs Drain-to-Source Voltage

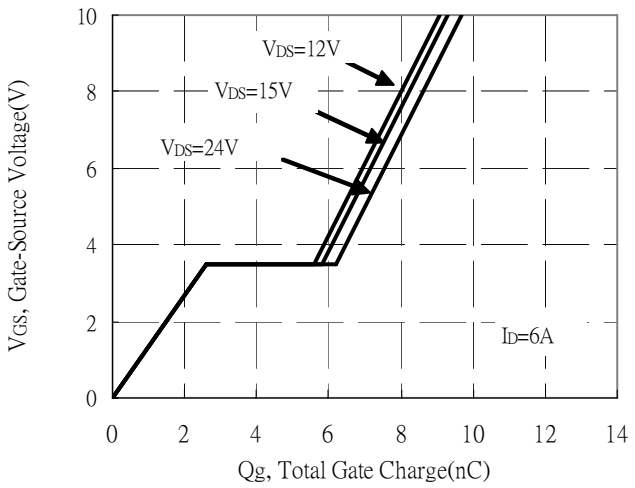


Typical Characteristics(Cont.) : FET 1

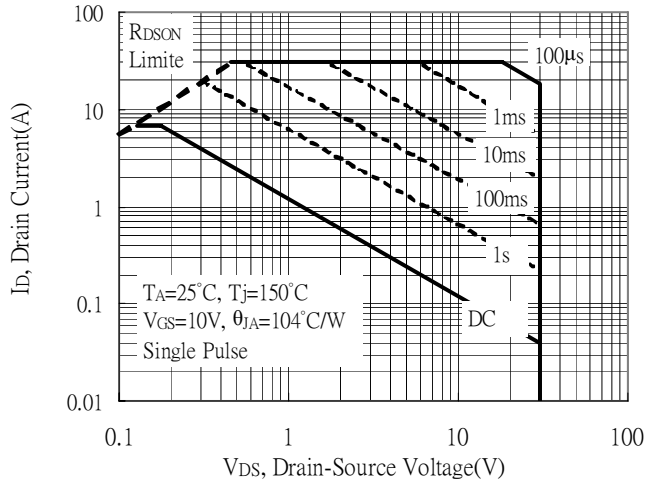
Forward Transfer Admittance vs Drain Current



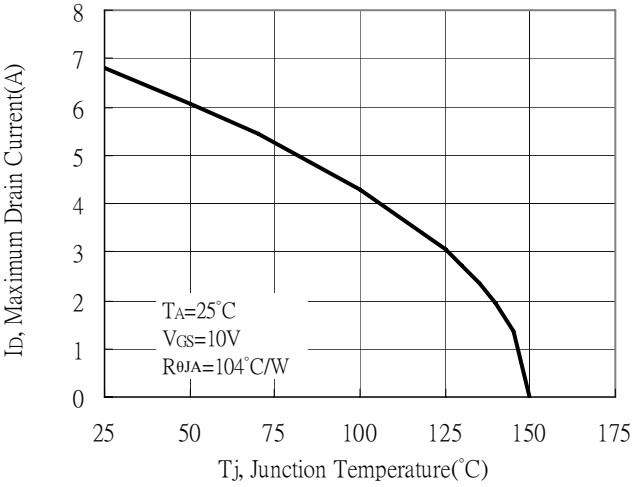
Gate Charge Characteristics



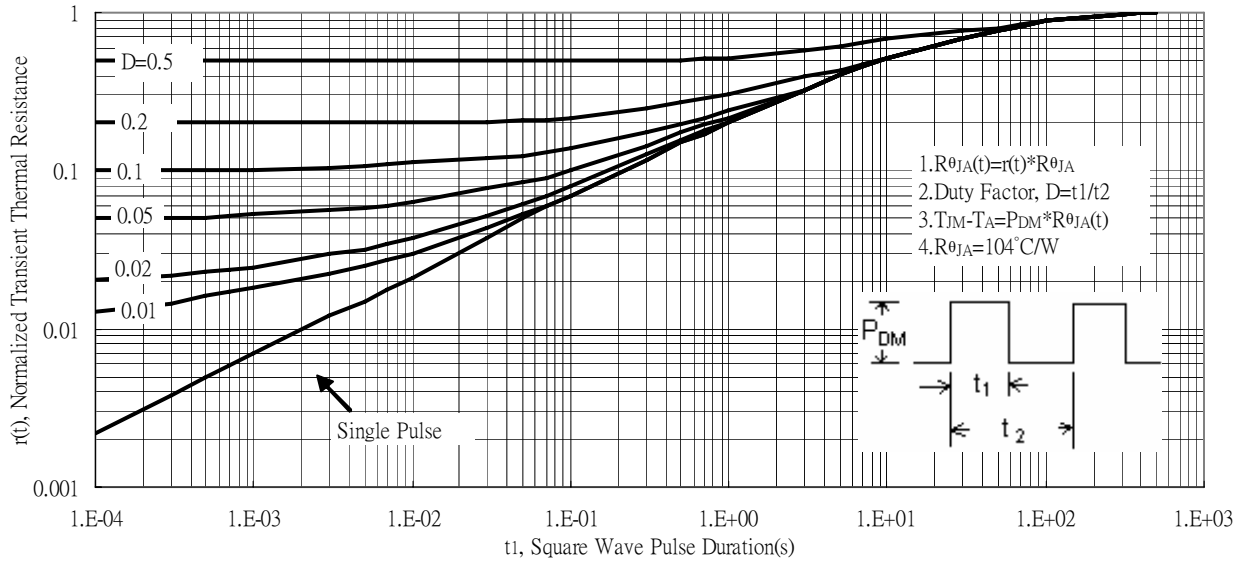
Maximum Safe Operating Area



Maximum Drain Current vs Case Temperature

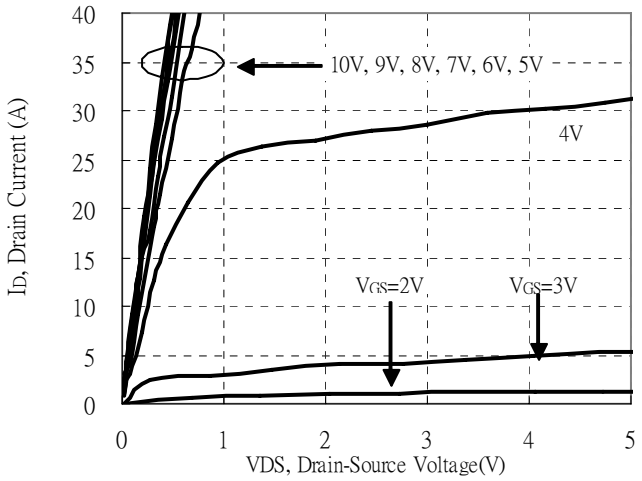


Transient Thermal Response Curves

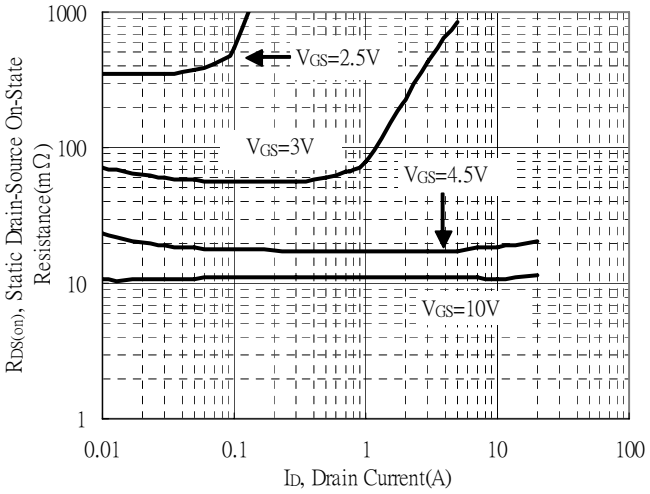


Typical Characteristics : FET 2

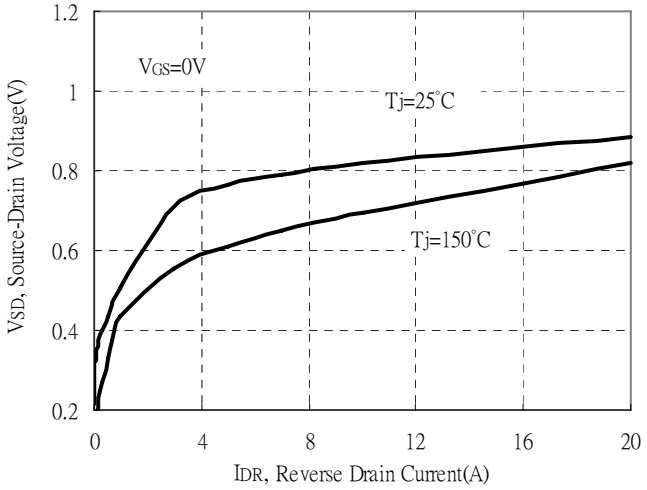
Typical Output Characteristics



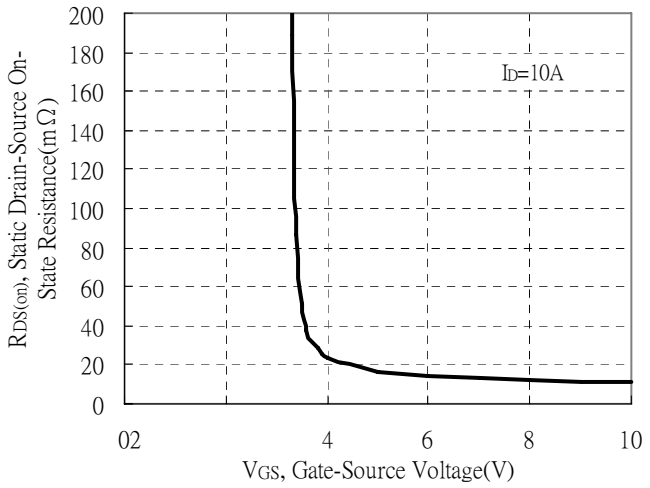
Static Drain-Source On-State resistance vs Drain Current



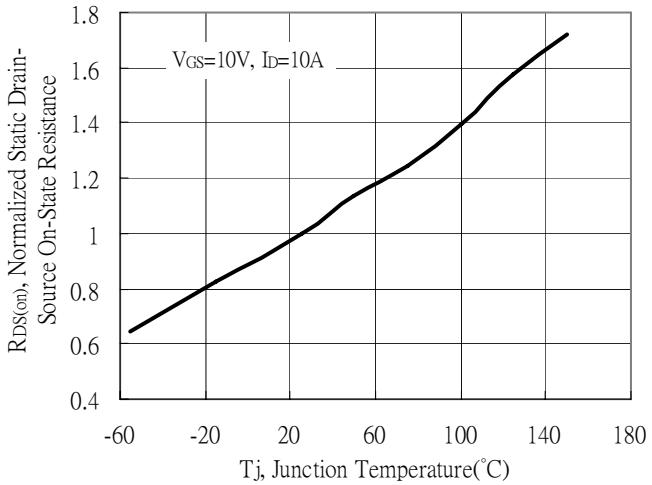
Reverse Drain Current vs Source-Drain Voltage



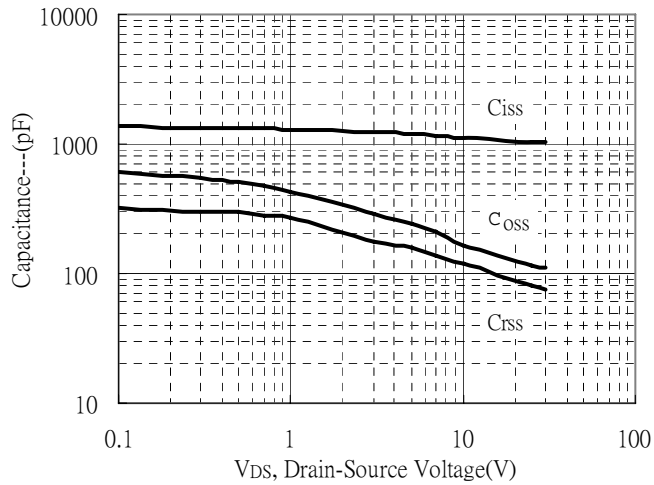
Static Drain-Source On-State Resistance vs Gate-Source Voltage



Drain-Source On-State Resistance vs Junction Tempearture

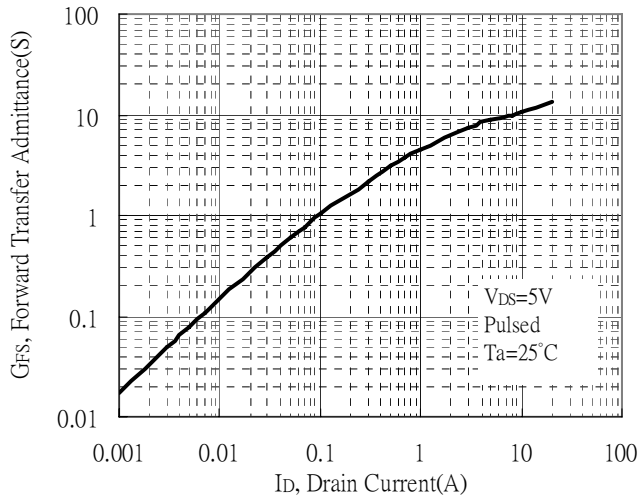


Capacitance vs Drain-to-Source Voltage

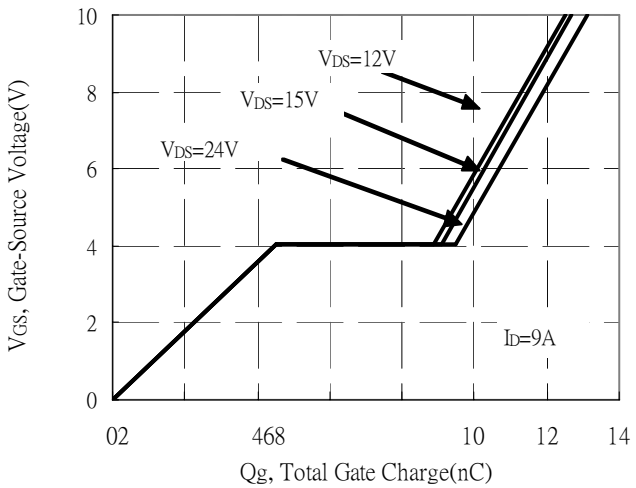


Typical Characteristics(Cont.) : FET 2

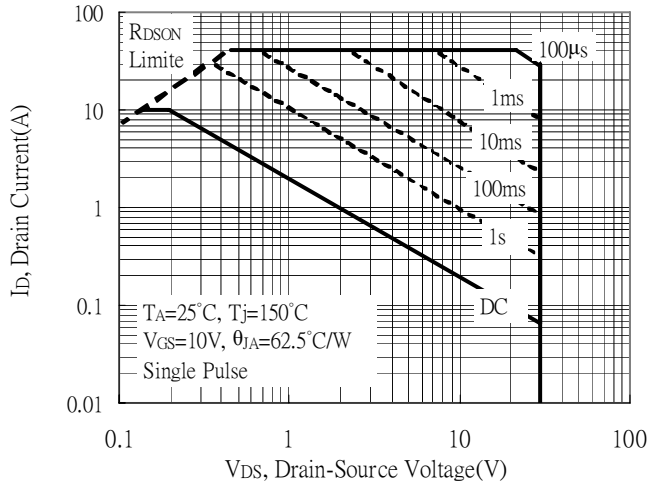
Forward Transfer Admittance vs Drain Current



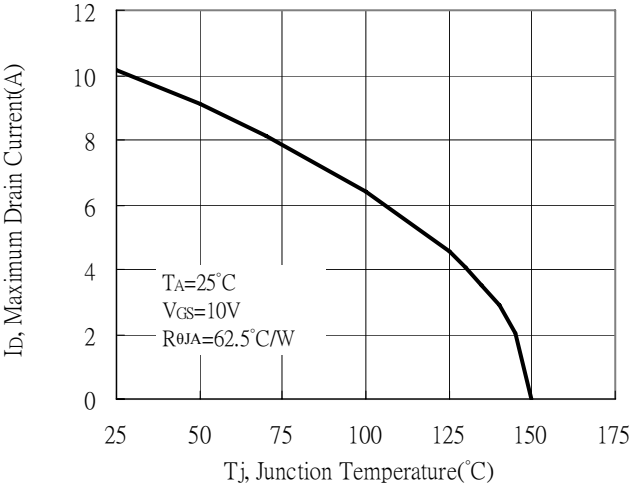
Gate Charge Characteristics



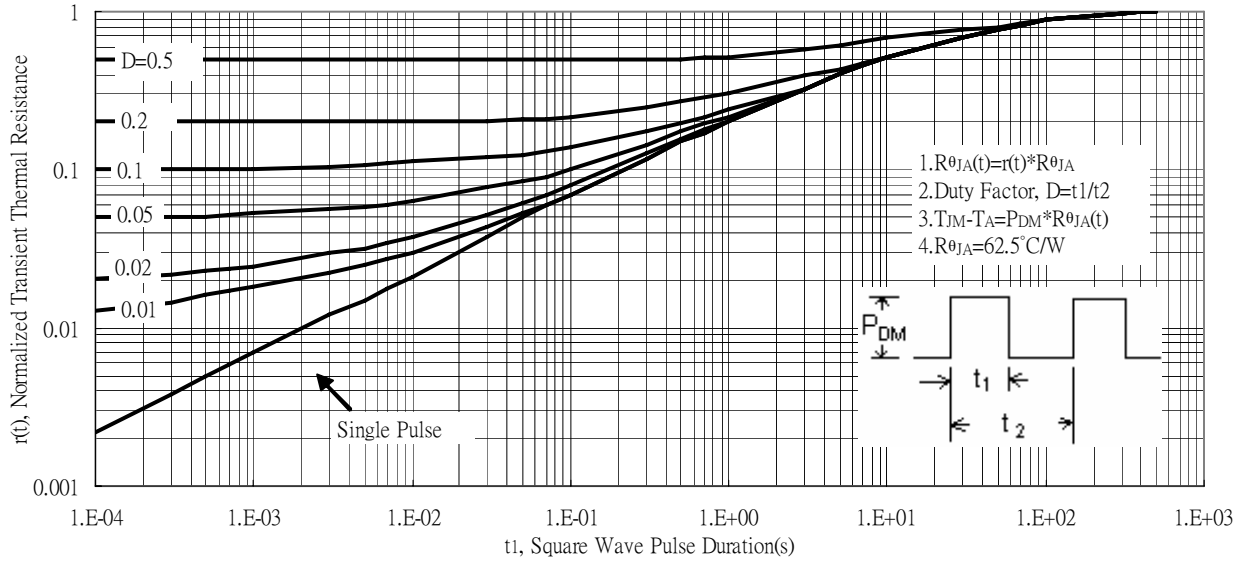
Maximum Safe Operating Area



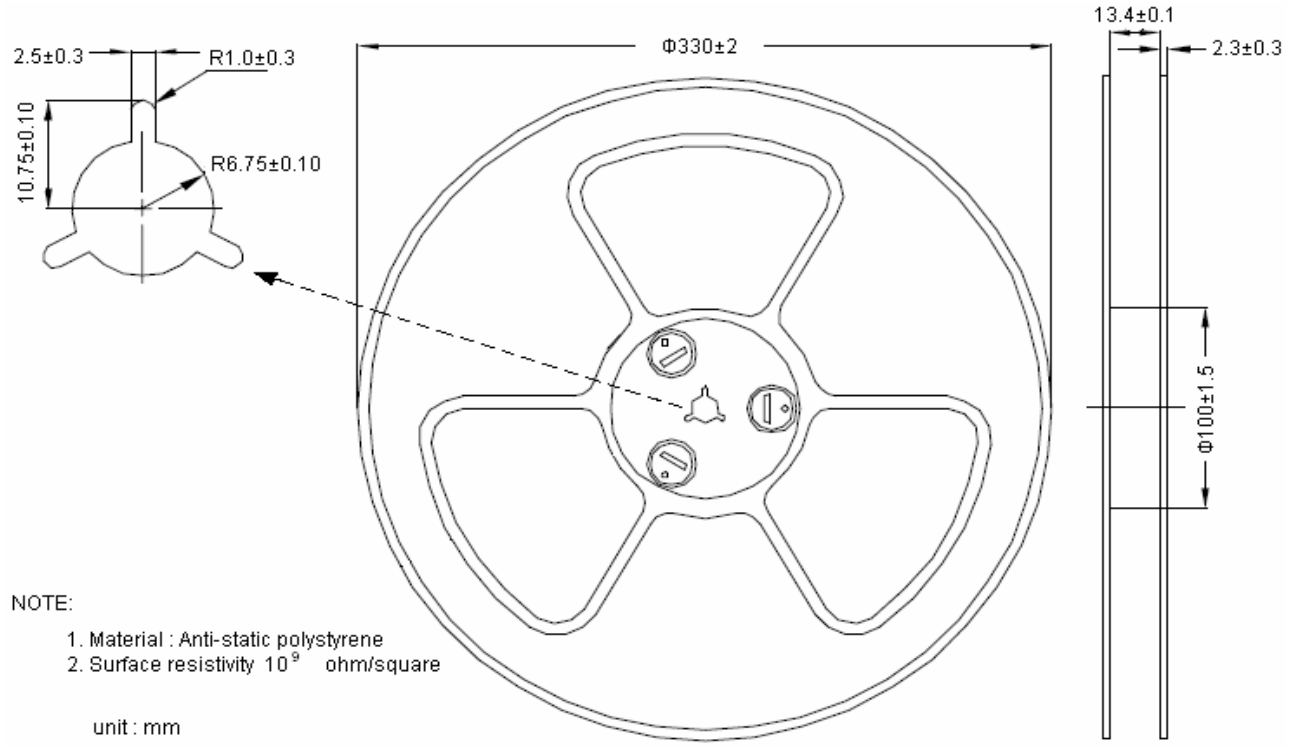
Maximum Drain Current vs Case Temperature



Transient Thermal Response Curves



Reel Dimension

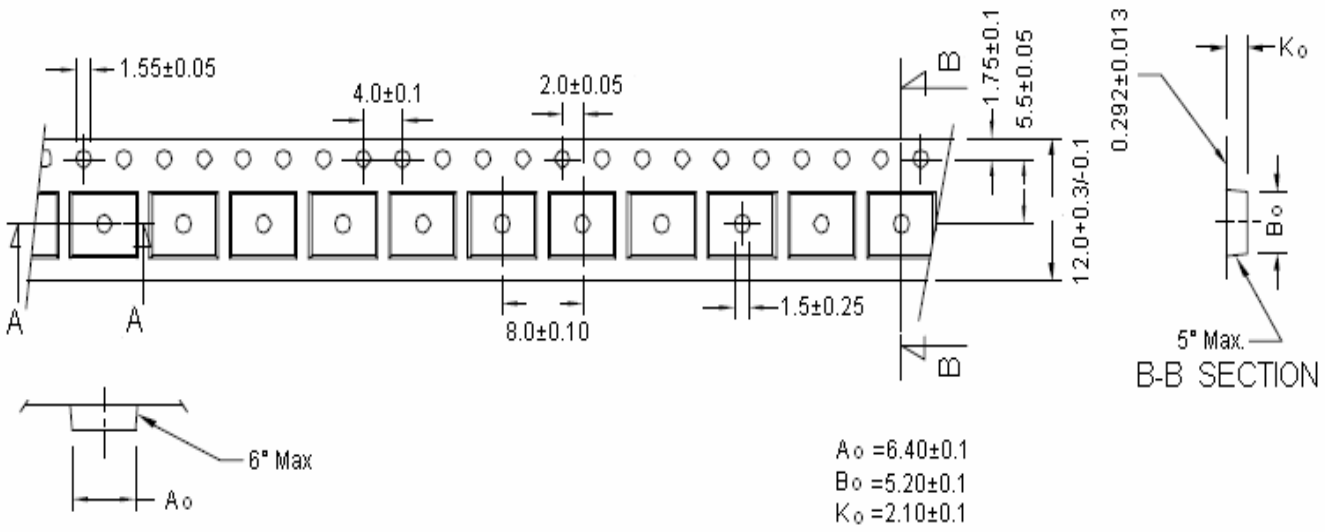


NOTE:

1. Material : Anti-static polystyrene
2. Surface resistivity 10^9 ohm/square

unit : mm

Carrier Tape Dimension



Notes:

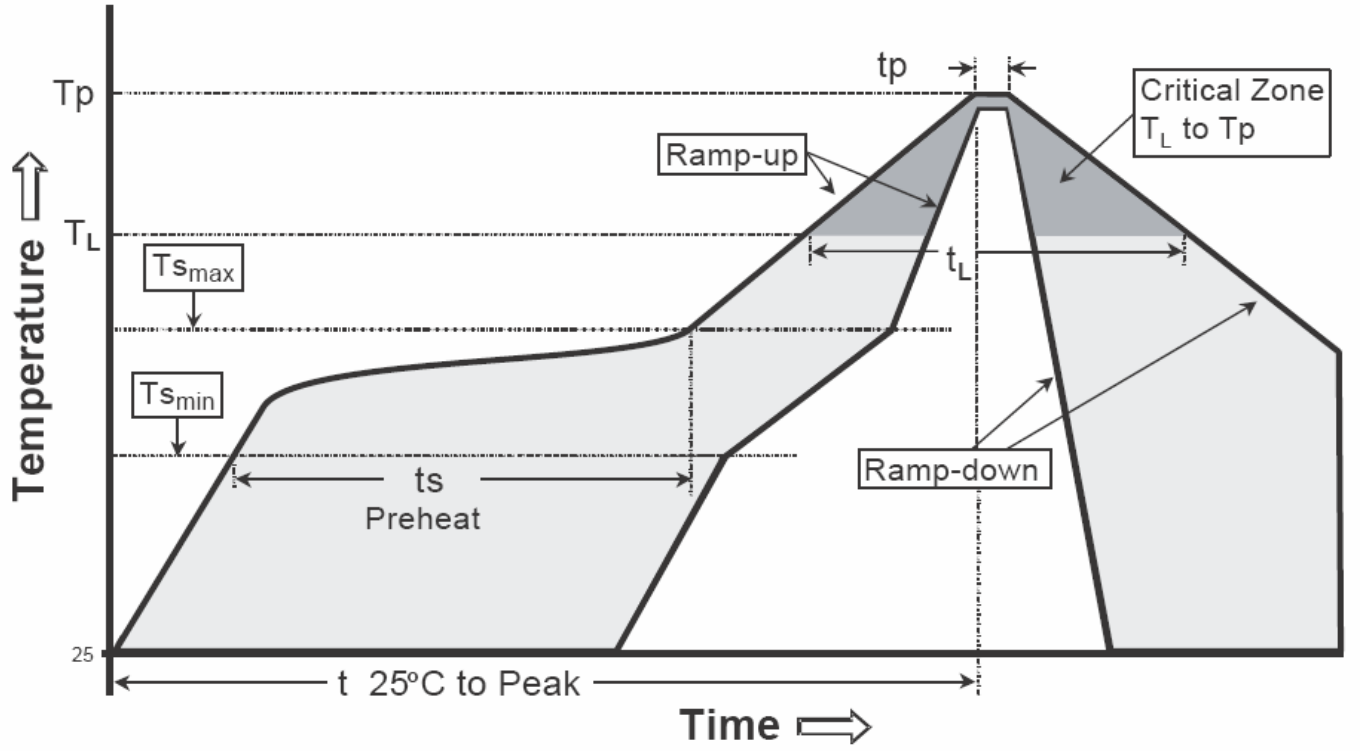
1. 10 sprocket hole pitch cumulative tolerance ±0.2.
2. Camber not to exceed 1mm in 100mm.
3. Material: conductive black polystyrene
4. Ao & Bo measured on a plane 0.3mm above the bottom of the pocket.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Uni : millimeter

Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

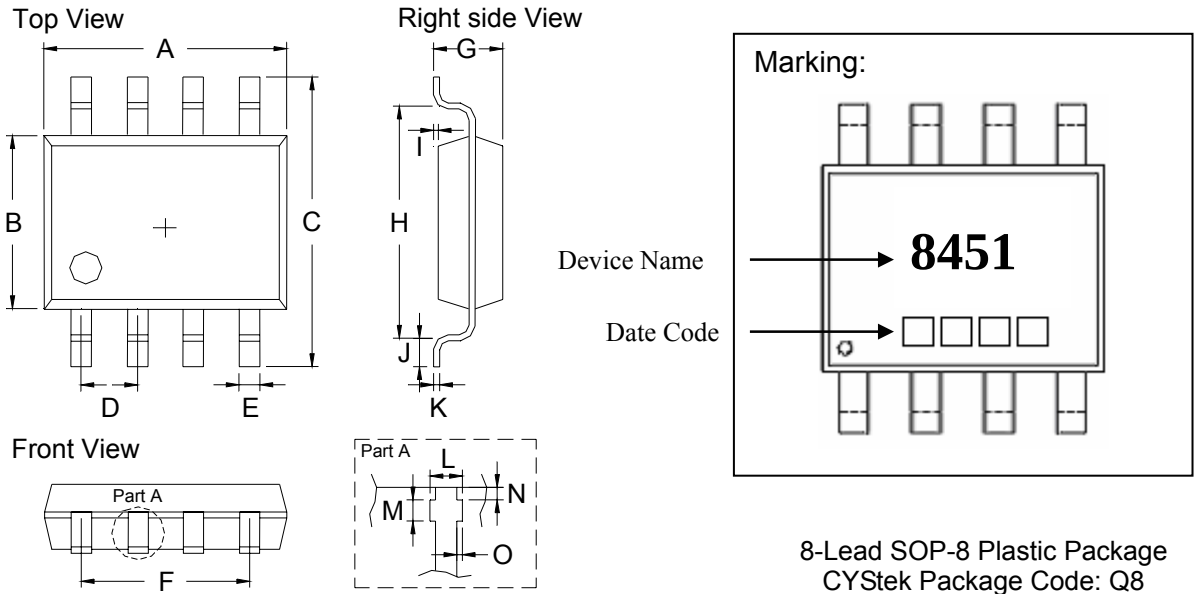
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(T_S min) −Temperature Max(T_S max) −Time($t_{s\ min}$ to $t_{s\ max}$)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: −Temperature (T_L) − Time (t_L)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak Temperature(T_P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

SOP-8 Dimension



8-Lead SOP-8 Plastic Package
CYStek Package Code: Q8

*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1909	0.2007	4.85	5.10	I	0.0019	0.0078	0.05	0.20
B	0.1515	0.1555	3.85	3.95	J	0.0118	0.0275	0.30	0.70
C	0.2283	0.2441	5.80	6.20	K	0.0074	0.0098	0.19	0.25
D	0.0480	0.0519	1.22	1.32	L	0.0145	0.0204	0.37	0.52
E	0.0145	0.0185	0.37	0.47	M	0.0118	0.0197	0.30	0.50
F	0.1472	0.1527	3.74	3.88	N	0.0031	0.0051	0.08	0.13
G	0.0570	0.0649	1.45	1.65	O	0.0000	0.0059	0.00	0.15
H	0.1889	0.2007	4.80	5.10					

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.