MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTP10N10M

Advance Information

Power Field Effect Transistor

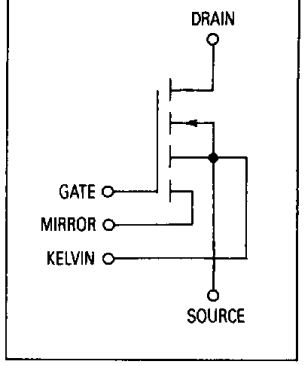
N-Channel Enhancement-Mode Silicon Gate with Current Sensing Capability

TMOS SENSEFET DEVICE
10 AMPERES
$R_{DS(on)}$ = 0.25 OHM
100 VOLTS

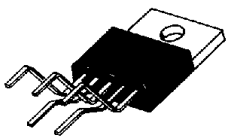
This TMOS Power FET with current sensing capability is designed for all power control applications where it is desirable to sense current such as in power supplies and motor controls. This device allows current sensing with minimum power loss.

- "Lossless" Current Sensing for Maximum Efficiency
  — Sense Current is Reduced by a Factor of Over 1000
- Ideal for Short Circuit/Overload Protection
- Simplifies Many Circuits When Used With Current Mode Integrated Circuits Such as the MC34129
- Kelvin Source Contact to Maximize Accuracy
- Rugged — SOA is Power Dissipation Limited
- Low $R_{DS(on)}$ — 0.25 Ohms Maximum

TMOS®



NOTES
1. Handling precautions to protect against electrostatic discharge is mandatory
2. Do not use the mirror FET independent of the power FET
3. It is recommended that the mirror terminal (M) be shorted to the source terminal (S) when current sensing is not required.



CASE 314B-03

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	100	Vdc
Drain-to-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	100	Vdc
Gate-to-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain-to-Mirror Voltage	V_{DMS}	100	Vdc
Gate-to-Mirror Voltage	V_{GM}	±20	Vdc
Drain Current — Continuous — Pulsed	I_D I_{DM}	10 25	Adc
Sense Current — Continuous — Pulsed	I_M I_{MM}	6 14	mA
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case Junction-to-Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	260	°C

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{MS} = 0 unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-to-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	100	—	—	Vdc
Drain-to-Mirror Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DMS}$	100	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 100 V, V_{GS} = 0) (V_{DS} = 100 V, V_{GS} = 0, T_J = 100°C)	I_{DSS}	— —	— —	0.2 1	mAdc
Gate-Body Leakage Current — Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	—	100	nAdc
Gate-Body Leakage Current — Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mAdc) (T_J = 100°C)	$V_{GS(th)}$	2 1.5	3 —	4.5 4	Vdc
Static Drain-to-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 5 Adc)	$R_{DS(on)}$	—	0.16	0.25	Ohms
Static Drain-to-Mirror On-Resistance (V_{GS} = 10 V, I_D = 10 A, R_{SENSE} = 0)	$r_{DM(on)}$	—	288	—	Ohms
Drain-to-Source On-Voltage (V_{GS} = 10 Vdc) (I_D = 10 A) (I_D = 5 A, T_J = 100°C)	$V_{DS(on)}$	— —	1.9 —	2.7 2.8	Vdc
Forward Transconductance (V_{GS} = 10 Vdc, I_D = 5 Adc)	g_{FS}	2.5	—	—	mhos
Current Mirror Ratio (Cell Ratio) (R_{SENSE} = 0, I_D = 10 A, V_{GS} = 10 V)	n	1750	1800	1850	—
DYNAMIC CHARACTERISTICS					
Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 f = 1 MHz See Figure 6	C_{iss}	—	—	500	pF
Output Capacitance		C_{oss}	—	—	300	
Transfer Capacitance		C_{rss}	—	—	100	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	V_{DD} = 25 V, I_D = 5 A R_{gen} = 50 Ohms	$t_{d(on)}$	—	—	50	ns
Rise Time		t_r	—	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	—	100	
Fall Time		t_f	—	—	50	
Total Gate Charge	V_{DS} = 80 V, I_D = 10 A V_{GS} = 10 V See Figure 4	Q_g	—	16	25	nC
Gate-Source Charge		Q_{gs}	—	7	—	
Gate-Drain Charge		Q_{gd}	—	9	—	
SOURCE-DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	I_S = 10 A	V_{SD}	—	2	—	Vdc
Forward Turn-On Time		t_{on}	—	20	—	ns
Reverse Recovery Time		t_{rr}	—	700	—	

*Indicates Pulse Test Pulse Width = 300 μs max, Duty Cycle = 2%

TYPICAL CHARACTERISTICS

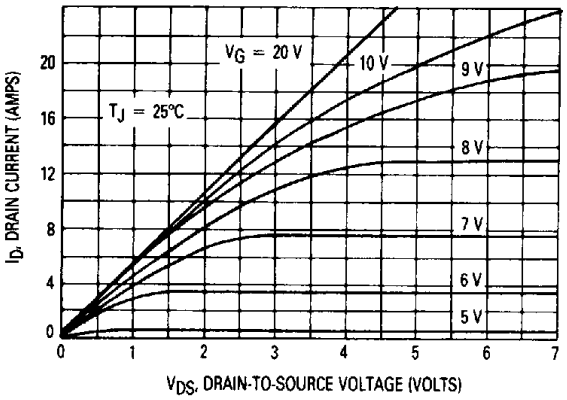


Figure 1. On-Region Characteristics

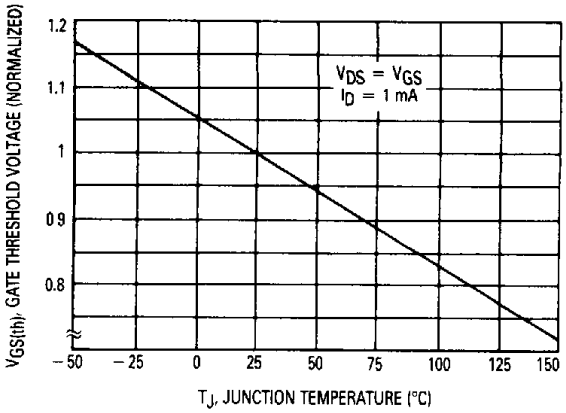


Figure 2. Gate Threshold Voltage Variation with Temperature

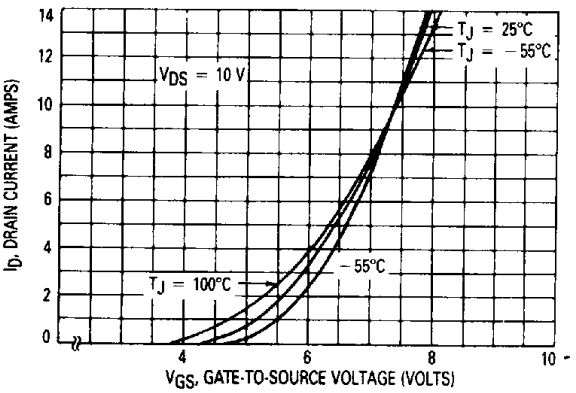


Figure 3. Transfer Characteristics

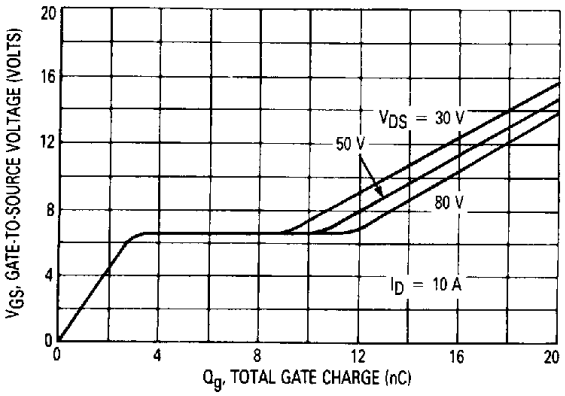


Figure 4. Stored Charge Variation

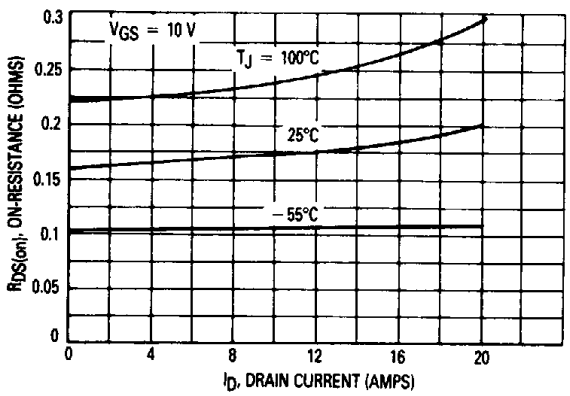


Figure 5. On-Resistance versus Drain Current

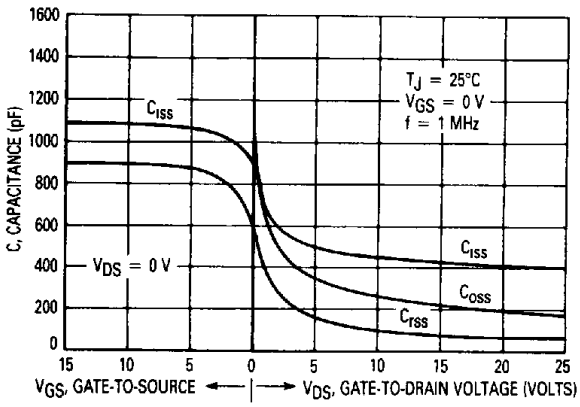


Figure 6. Capacitance Variation

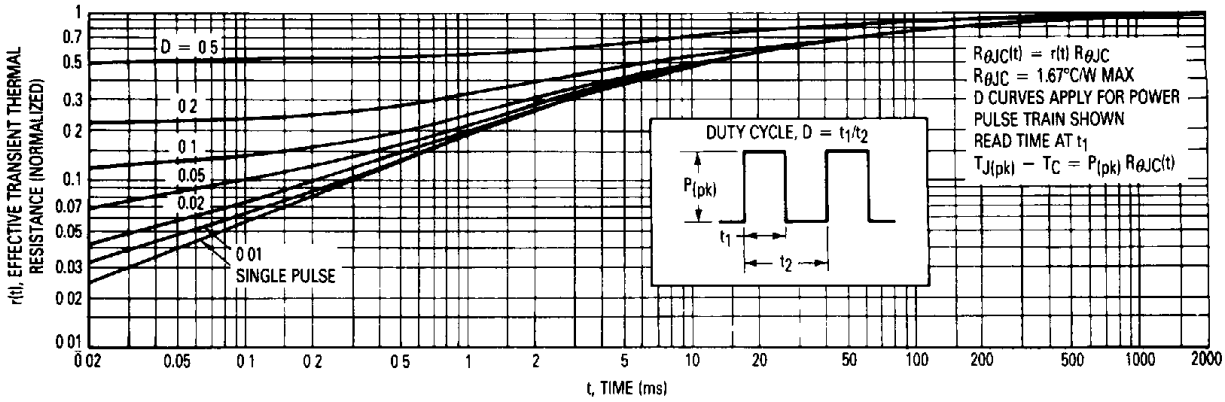


Figure 7. Thermal Response

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SAFE OPERATING AREA INFORMATION

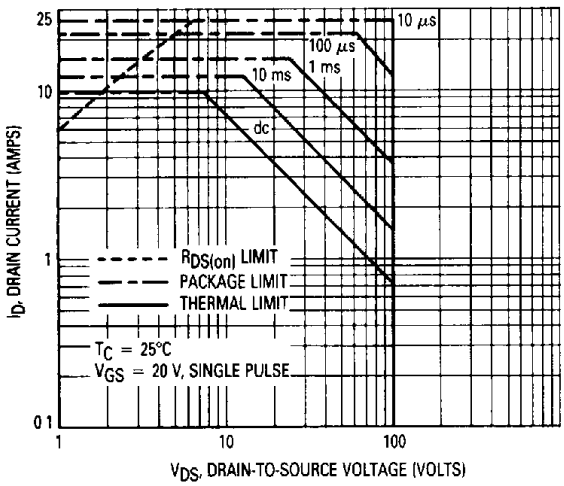


Figure 8. Maximum Rated Forward Biased Safe Operating Area

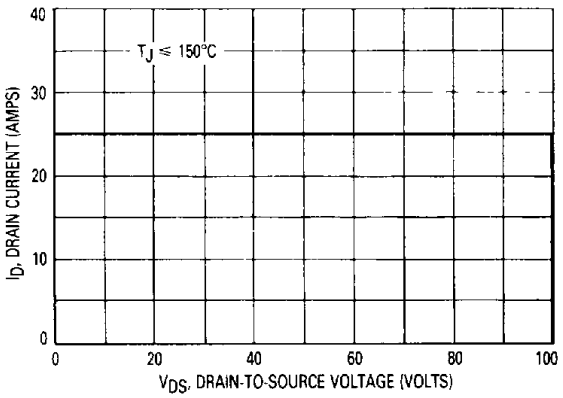


Figure 9. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

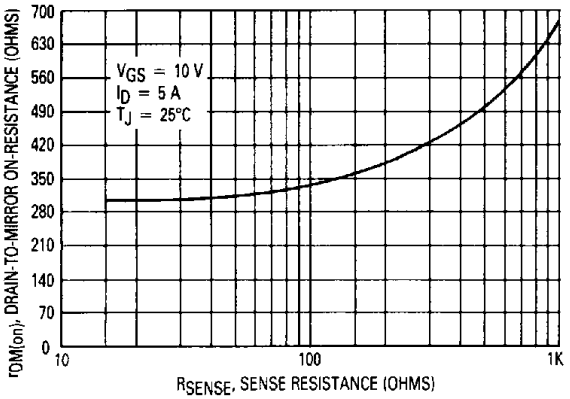


Figure 10. Drain-to-Mirror On-Resistance versus Sense Resistance

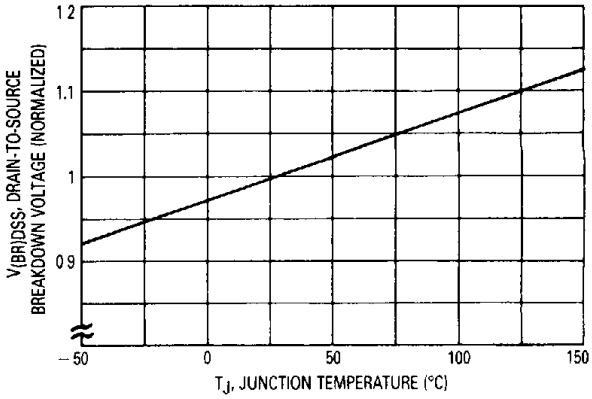


Figure 11. Normalized Drain-To-Source Breakdown Voltage versus Temperature

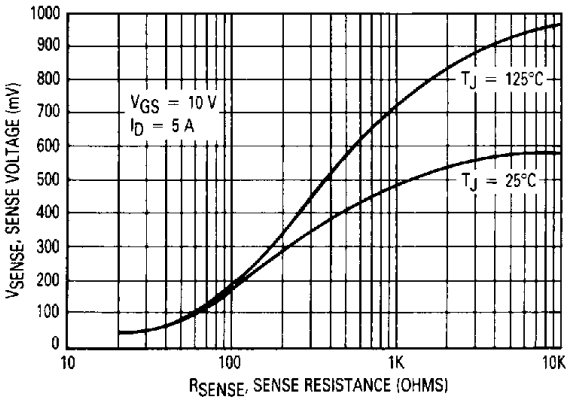


Figure 12. Sense Voltage versus Sense Resistance

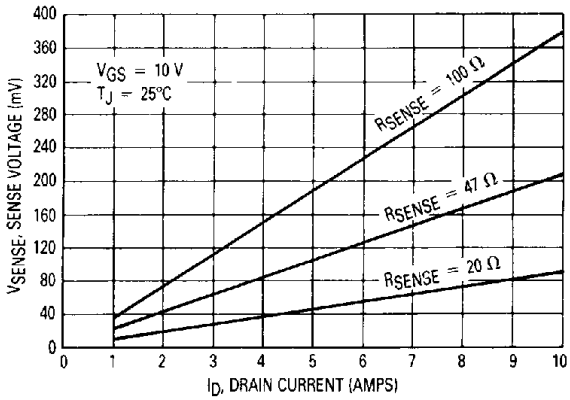


Figure 13. Drain Current versus Sense Voltage

USING SENSEFET PRODUCTS

In practical applications, less sense current will flow than that calculated by using the current mirror ratio, n. Shown in Figure 1 is a model of the SENSEFET device. It is seen that R_{SENSE} decreases the voltage across $R_{DM(on)}$ and decreases the sense current. An additional decrease in sense current occurs due to the decreased voltage across the mirror transistors. For this reason, a modified current mirror ratio, n′ must be calculated. The equation to calculate n′ is derived from the MOSFET square law model in the linear region,

$$n' = \frac{n}{1 - \dfrac{V_{SE}(V_{GS} - V_T - 1/2\ V_{SE})}{V_{DS(on)}(V_{GS} - V_T - 1/2\ V_{DS(on)})}}$$

$$n' \approx \frac{n}{1 - V_{SE}/V_{DS(on)}} \quad (1)$$

(for V_{SE}, $V_{DS(on)} << V_{GS} - V_T$).

Where, V_{GS} = Gate-to-Source Voltage,
V_T = Gate-to-Source Threshold Voltage

and V_{SE} = Sense Voltage = $\dfrac{R_{SENSE}\ I_D}{n'}$. (2)

Hence, n′ can be calculated from equation (1) and the result used in equation (2) to find the value of R_{SENSE}. The value of R_{SENSE} should be kept below 100 Ω for most accurate results.

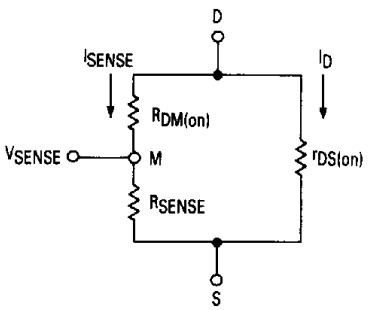


Figure 14. SENSEFET Model

These equations were derived using die level source as the ground reference, neglecting contact and wire bond resistance to the source pin. In practice these parasitic resistances can cause significant errors at high currents, therefore it is mandatory to reference the gate drive signal and measure $V_{DS(on)}$ and V_{SENSE} with respect to the Kelvin pin.

Figure 15 illustrates the correct SENSEFET configuration.

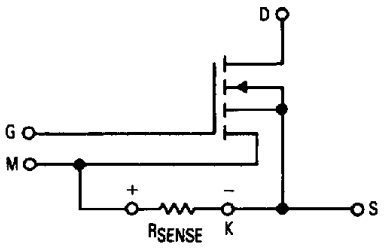
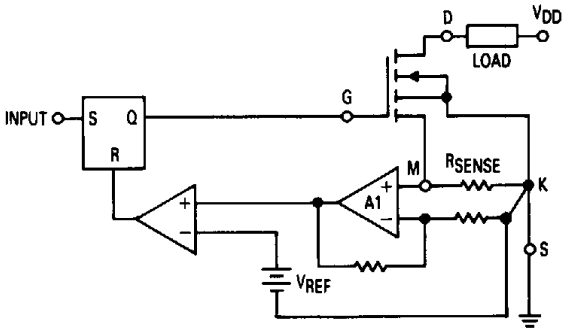


Figure 15. SENSEFET Configuration

SENSEFET APPLICATIONS CONSIDERATIONS

- Double Pulse Suppression: In PWM circuits it is critically important to include double pulse suppression in the control circuit topology. If the current limit loop is allowed to oscillate at its natural frequency, failure of the SENSEFET device is likely due to over-dissipation. By syncing the current limit loop to the clock with a latch, double pulse suppression architectures solve this problem, and provide effective protection from overload stress.
- Noise Suppression: Noise pickup in the current sensing circuitry of SENSEFET systems can be a first order design issue. Layout, therefore is critical. In addition, some spike limiting capacitance across R_{SENSE} is often desirable, provided that it is placed right at the current sensing circuitry's input terminals. To help with the layout problem, a Kelvin source connection is provided. The Kelvin connection gives SENSEFET devices separate power and signal source pins. This feature can be used advantageously with circuits such as the MC34129 current mode controller and MC33034 brushless dc motor drive, which also have dual grounds.
- Ground Loop Errors: Lossless current sensing is a technique that looks for 100 mV signals in a loop that may carry tens or even hundreds of amps. The potential for ground loop error in this kind of situation is a first order design consideration. In particular, current flowing from the SENSEFET device's source into a non-zero ground impedance can easily create voltage drops which are significant with respect to SENSEFET signal levels. Here again, the Kelvin connection is a useful tool. Tying the current limit circuitry's voltage reference to the Kelvin terminal as shown in Figure 16 eliminates errors that can be developed by high currents flowing in a power ground.



Set A1 gain to match sense voltage to V_{REF} at max I_D.

Figure 16. Typical Current Sensing with a SENSEFET Device

- Temperature Stability: With very low values of R_{SENSE}, temperature tracking depends primarily upon the matching of monolithic devices and is generally within a few percent for a 100°C change in temperature. As R_{SENSE} is increased, however, temperature coefficient becomes less dependent upon matching and more a function of the power section's on-voltage. In the limit where R_{SENSE} is very large, sense voltage approximates $V_{DS(on)}$ and tracks its temperature coefficient. It is not unusual to see V_{SENSE} change less than 5% for a 100°C change in temperature provided that R_{SENSE} is less than 10% of $R_{DM(on)}$. On the other hand, changes of 50% are not unusual when R_{SENSE} exceeds $R_{DM(on)}$.
- There is a parasitic reverse diode on the current mirror MOSFET as well as the power MOSFET. Diode reverse recovery currents will cause a sense voltage spike that may have to be filtered from the sense circuitry.