



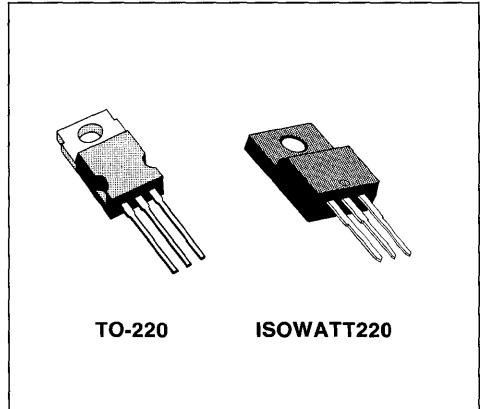
**N - CHANNEL ENHANCEMENT MODE  
LOW THRESHOLD POWER MOS TRANSISTORS**

PRELIMINARY DATA

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
MTP15N05L	50 V	0.15 Ω	15 A
MTP15N05LFI	50 V	0.15 Ω	10 A
MTP15N06L	60 V	0.15 Ω	15 A
MTP15N06LFI	60 V	0.15 Ω	10 A

- LOGIC LEVEL (+5V) CMOS/TTL COMPATIBLE INPUT
- HIGH INPUT IMPEDANCE
- ULTRA FAST SWITCHING

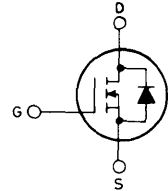
N - channel enhancement mode POWER MOS field effect transistors. The low input voltage - logic level - and easy drive make these devices ideal for automotive and industrial applications. Typical uses are in relay and actuator driving in the automotive environment.



TO-220

ISOWATT220

**INTERNAL SCHEMATIC DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS**

		TO-220	MTP15N06L	MTP15N05L	
		ISOWATT220	MTP15N06LFI	MTP15N05LFI	
V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> = 0)		60	50	V
V <sub>DGR</sub>	Drain-gate voltage (R <sub>GS</sub> = 20 KΩ)		60	50	V
V <sub>GS</sub>	Gate-source voltage			± 15	V
			<b>TO-220</b>	<b>ISOWATT220</b>	
I <sub>D</sub>	Drain current (cont.) at T <sub>c</sub> = 25°C		15	10	A
I <sub>D</sub>	Drain current (cont.) at T <sub>c</sub> = 100°C		9.5	6.3	A
I <sub>DM</sub> (*)	Drain current (pulsed)		40	40	A
P <sub>tot</sub>	Total dissipation at T <sub>c</sub> < 25°C		75	30	W
	Derating factor		0.6	0.24	W/°C
T <sub>stg</sub>	Storage temperature			- 65 to 150	°C
T <sub>j</sub>	Max. operating junction temperature			150	°C

(\*) Pulse width limited by safe operating area

**THERMAL DATA**

**TO-220 | ISOWATT220**

$R_{thj - case}$	Thermal resistance junction-case	max	1.67	4.16	°C/W
$R_{thj - amb}$	Thermal resistance junction-ambient	max	62.5		°C
$T_L$	Maximum lead temperature for soldering purpose	max	275		°C

**ELECTRICAL CHARACTERISTICS** ( $T_{case} = 25^\circ\text{C}$  unless otherwise specified)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
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**OFF**

$V_{(BR) DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ for <b>MTP15N06L/FI</b> for <b>MTP15N05L/FI</b>	$V_{GS} = 0$	60 50		V V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$	$T_c = 125^\circ\text{C}$		1 50	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 15\text{ V}$			-	$\pm 100$ nA

**ON \*\***

$V_{GS (th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ $I_D = 1\text{ mA}$ $V_{DS} = V_{GS}$ $I_D = 1\text{ mA}$	$T_c = 100^\circ\text{C}$	1 0.75		2 1.5	V V
$R_{DS (on)}$	Static drain-source on resistance	$V_{GS} = 5\text{ V}$ $I_D = 7.5\text{ A}$				0.15	$\Omega$
$V_{DS (on)}$	Drain-source on voltage	$V_{GS} = 5\text{ V}$ $I_D = 15\text{ A}$ $V_{GS} = 5\text{ V}$ $I_D = 7.5\text{ A}$	$T_c = 100^\circ\text{C}$			3 1.5	V V

**DYNAMIC**

$g_{fs}$	Forward transconductance	$V_{DS} = 15\text{ V}$	$I_D = 7.5\text{ A}$	5			mho
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ $V_{GS} = 0$	$f = 1\text{ MHz}$			900	pF
$C_{oss}$	Output capacitance					450	pF
$C_{rss}$	Reverse transfer capacitance					200	pF

**SWITCHING**

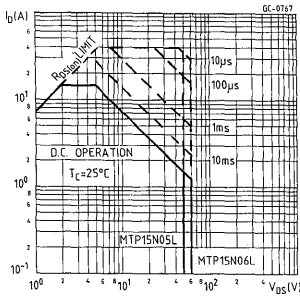
$t_d (on)$	Turn-on time	$V_{DD} = 25\text{ V}$ $V_i = 5\text{ V}$	$I_D = 7.5\text{ A}$ $R_i = 50\ \Omega$			40	ns
$t_r$	Rise time					260	ns
$t_d (off)$	Turn-off delay time					200	ns
$t_f$	Fall time					200	ns
$Q_g$	Total Gate Charge	$V_{DD} = 48\text{ V}$ $V_{GS} = 5\text{ V}$	$I_D = 15\text{ A}$			14	nC
$Q_{gs}$	Gate-source charge					7	nC
$Q_{gd}$	Gate-drain charge					7	nC

ELECTRICAL CHARACTERISTICS (Continued)

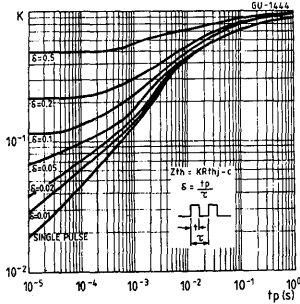
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current			15	A
$I_{SDM}^{(*)}$	Source-drain current (pulsed)			60	A
$V_{SD}^{**}$	Forward on voltage	$I_{SD} = 15\text{ A}$	$V_{GS} = 0$	1.8	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 15\text{ A}$	$di/dt = 100\text{ A}/\mu\text{s}$	300	ns

\*\* Pulsed: Pulse duration  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$   
 (\*) Pulse width limited by safe operating area

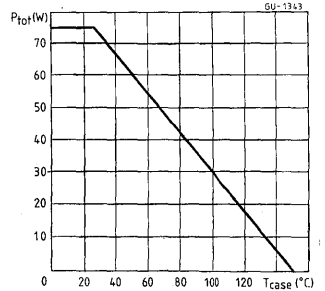
Safe operating areas (standard package)



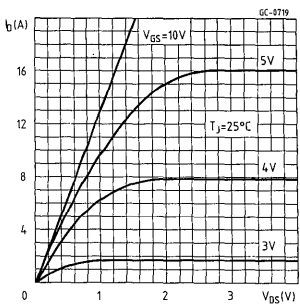
Thermal impedance (standard package)



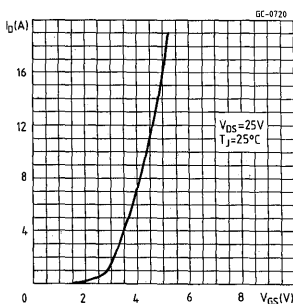
Derating curve (standard package)



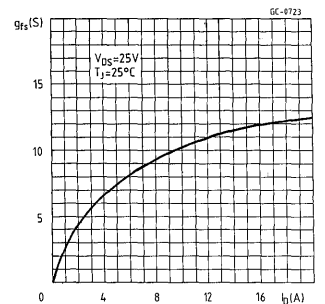
Output characteristics



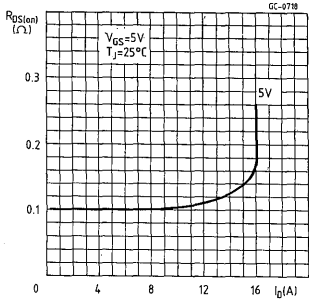
Transfer characteristics



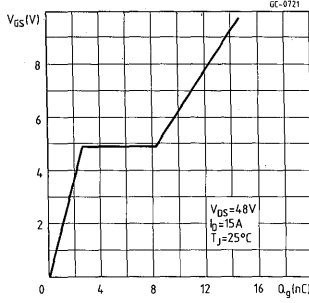
Transconductance



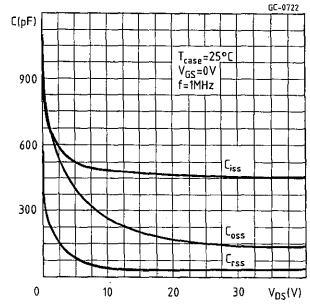
Static drain-source on resistance



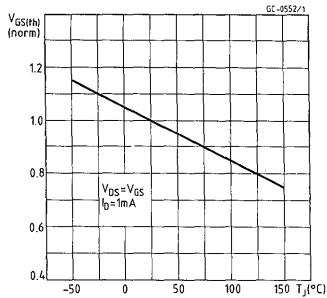
Gate charge vs gate-source voltage



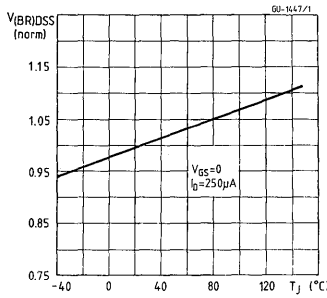
Capacitance variation



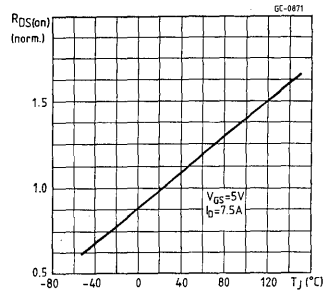
Normalized gate threshold voltage vs temperature



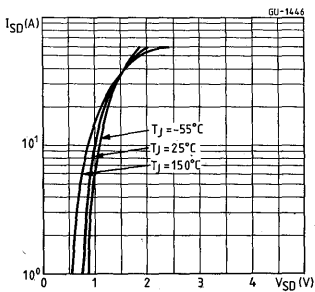
Normalized breakdown voltage vs temperature



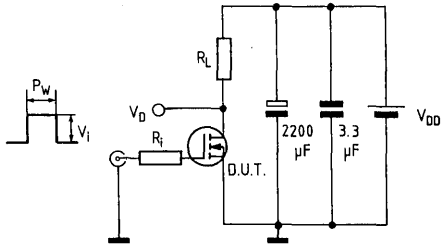
Normalized on resistance vs temperature



Source-drain diode forward characteristics

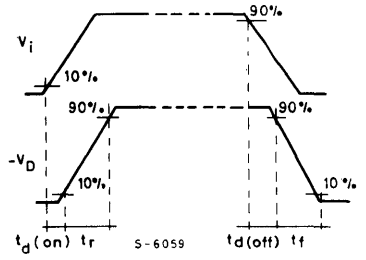


Switching times test circuit for resistive load

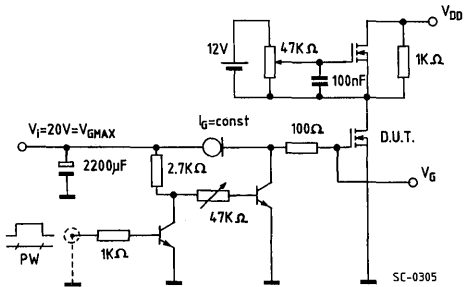


Pulse width  $\leq 100 \mu\text{s}$   
 Duty cycle  $\leq 2\%$

Switching time waveforms for resistive load

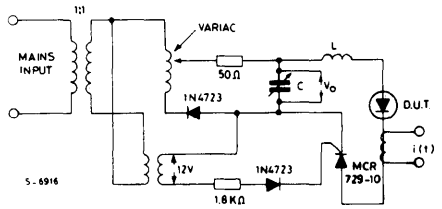


Gate charge test circuit



PW adjusted to obtain required  $V_G$

Body-drain diode  $t_{rr}$  measurement  
 Jedec test circuit



**ISOWATT220 PACKAGE CHARACTERISTICS AND APPLICATION.**

ISOWATT220 is fully isolated to 2000V dc. Its thermal impedance, given in the data sheet, is optimised to give efficient thermal conduction together with excellent electrical isolation.

The structure of the case ensures optimum distances between the pins and heatsink. The ISOWATT220 package eliminates the need for external isolation so reducing fixing hardware. Accurate moulding techniques used in manufacture assure consistent heat spreader-to-heatsink capacitance.

ISOWATT220 thermal performance is better than that of the standard part, mounted with a 0.1mm mica washer. The thermally conductive plastic has a higher breakdown rating and is less fragile than mica or plastic sheets. Power derating for ISOWATT220 packages is determined by:

$$P_D = \frac{T_j - T_c}{R_{th}}$$

from this  $I_{Dmax}$  for the POWER MOS can be calculated:

$$I_{Dmax} \leq \sqrt{\frac{P_D}{R_{DS(on)} \text{ (at } 150^\circ\text{C)}}}$$

**THERMAL IMPEDANCE OF ISOWATT220 PACKAGE**

Fig. 1 illustrates the elements contributing to the thermal resistance of transistor heatsink assembly, using ISOWATT220 package.

The total thermal resistance  $R_{th(tot)}$  is the sum of each of these elements.

The transient thermal impedance,  $Z_{th}$  for different pulse durations can be estimated as follows:

1 - for a short duration power pulse less than 1ms;

$$Z_{th} < R_{thJ-C}$$

2 - for an intermediate power pulse of 5ms to 50ms:

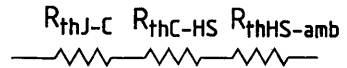
$$Z_{th} = R_{thJ-C}$$

3 - for long power pulses of the order of 500ms or greater:

$$Z_{th} = R_{thJ-C} + R_{thC-HS} + R_{thHS-amb}$$

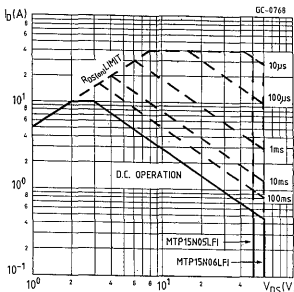
It is often possible to discern these areas on transient thermal impedance curves.

Fig. 1

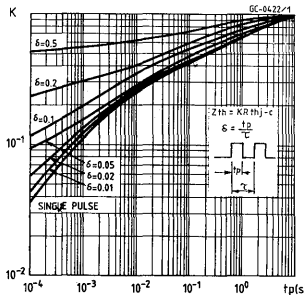


**ISOWATT DATA**

**Safe operating areas**



**Thermal impedance**



**Derating curve**

