Advance Information
Power Field Effect Transistor
### P-Channel Enhancement-Mode
Silicon Gate TMOS

This TMOS Power FET is designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MTP20P06

TMOS

TMOS POWER FET
20 AMPERES
$r_{DS(on)}$ = 0.2 OHM
60 VOLTS

CASE 221A-04
TO-220AB
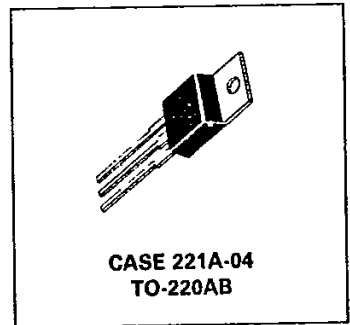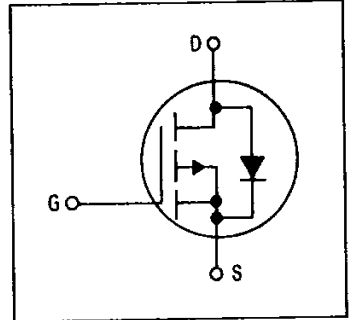
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	60	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50 \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	20 72	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 0.8	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	$R_{\theta JC}$	1.25	°C/W
— Junction to Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	— —	10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc

(continued)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS*					
Gate Threshold Voltage ($V_{DS} = V_{GS}$, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 10 Adc)		$r_{DS(on)}$	—	0.2	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 20 Adc) (I_D = 10 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	4.2 4	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 10 A)		g_{FS}	5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	1400	pF
Output Capacitance		C_{oss}	—	700	
Reverse Transfer Capacitance		C_{rss}	—	300	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 10 Amp, R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	350	
Turn-Off Delay Time		$t_{d(off)}$	—	150	
Fall Time		t_f	—	160	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = 20 Amp, V_{GS} = 10 V) See Figure 12	Q_g	30 (Typ)	60	nC
Gate-Source Charge		Q_{gs}	20 (Typ)	—	
Gate-Drain Charge		Q_{gd}	10 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = 20 Amp, V_{GS} = 0)	V_{SD}	4 (Typ)	4.2	Vdc
Forward Turn-On Time		t_{on}	100 (Typ)	—	ns
Reverse Recovery Time		t_{rr}	120 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to center of pad)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
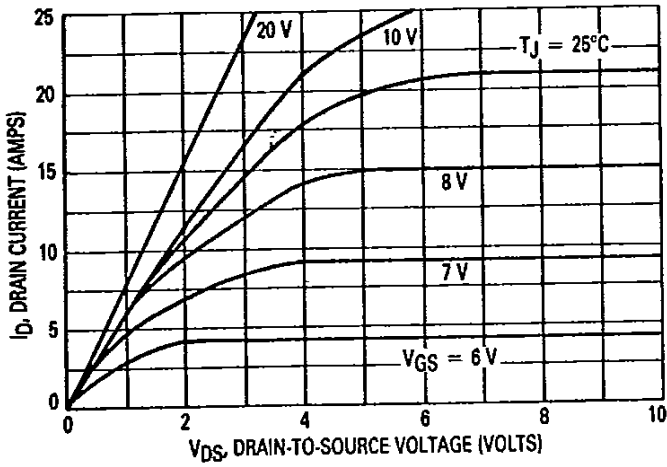
TYPICAL ELECTRICAL CHARACTERISTICS

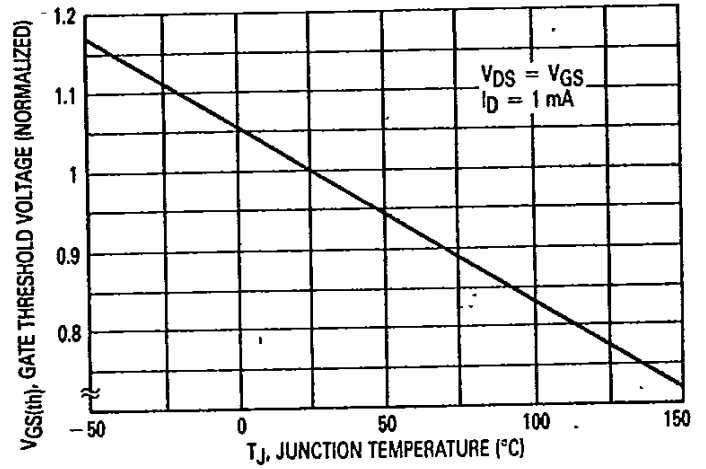**Figure 1. On-Region Characteristics**

**Figure 2. Gate-Threshold Variation
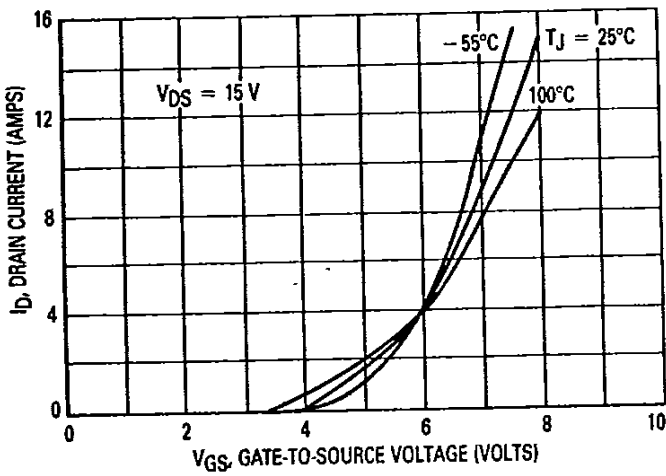With Temperature**

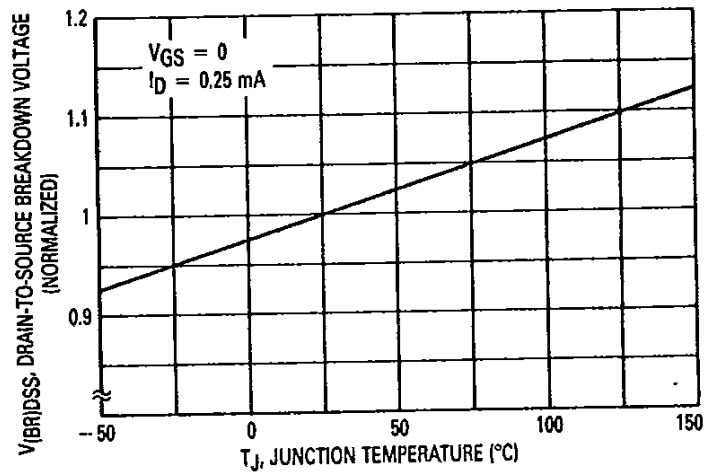

Figure 3. Transfer Characteristics
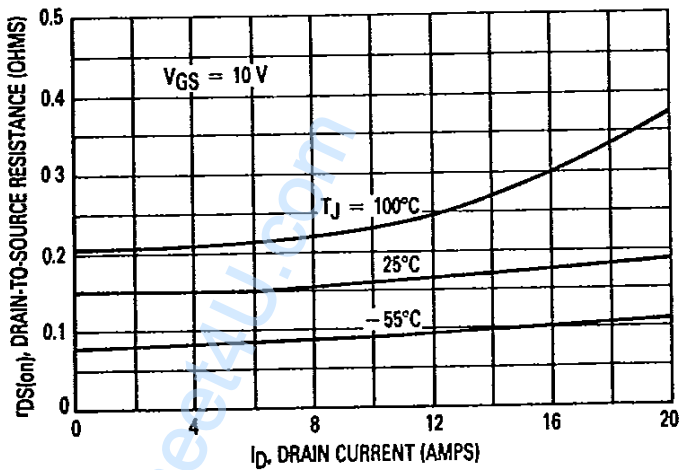

**Figure 4. Breakdown Voltage Variation
With Temperature**

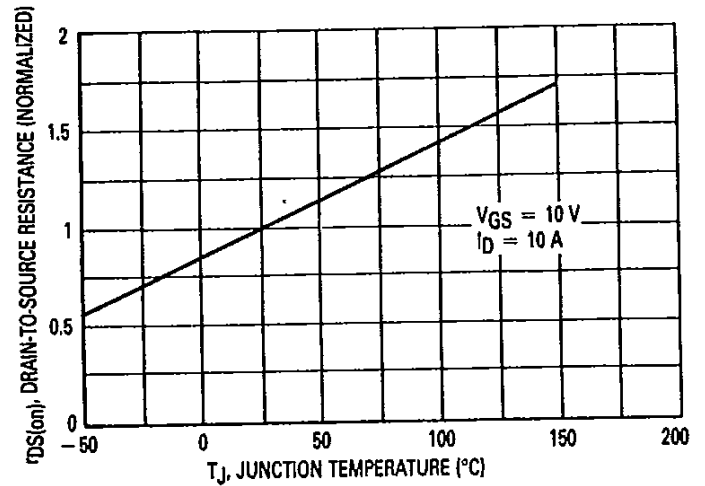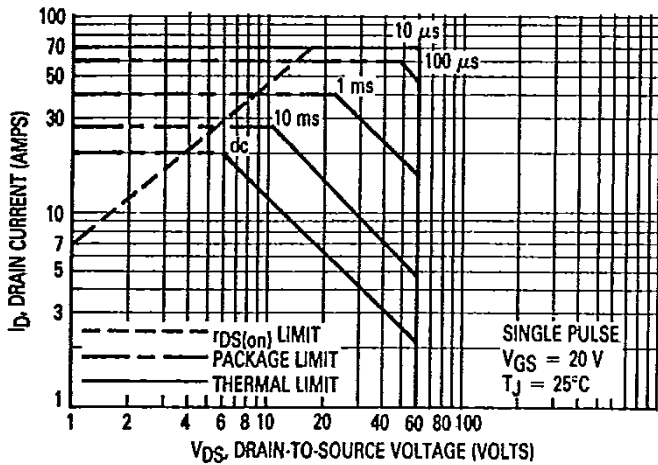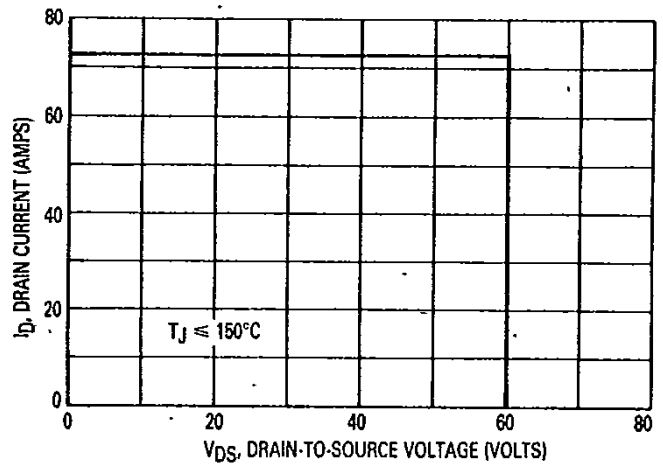**Figure 5. On-Resistance versus Drain Current**

**Figure 6. On-Resistance Variation
With Temperature**

SAFE OPERATING AREA INFORMATION

Figure 7. Maximum Rated Forward Biased Safe Operating Area

Figure 8. Maximum Rated Switching Safe Operating Area

### FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$
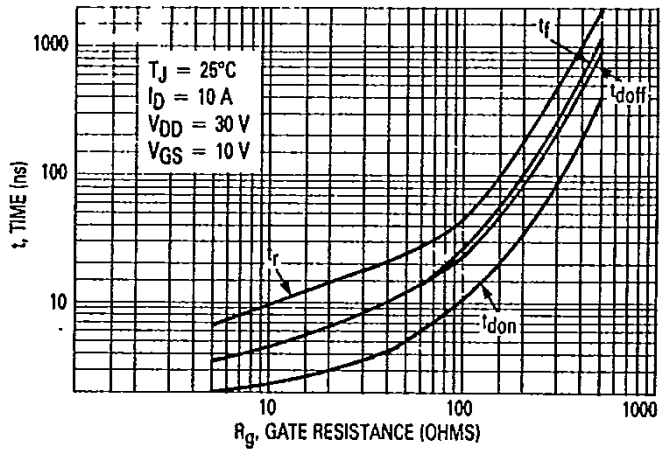
Figure 9. Resistive Switching Time Variation versus Gate Resistance
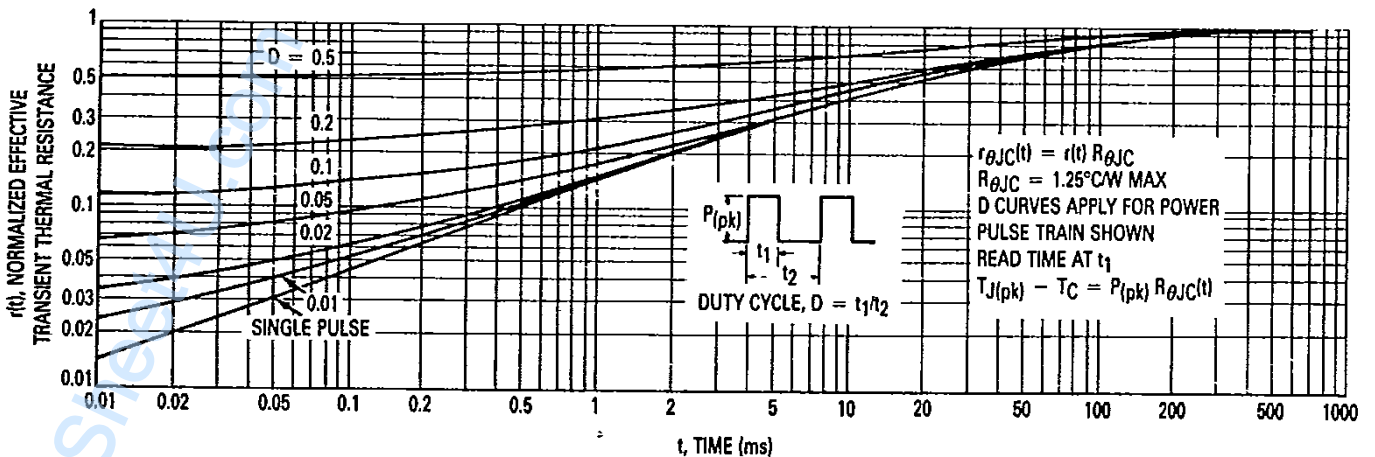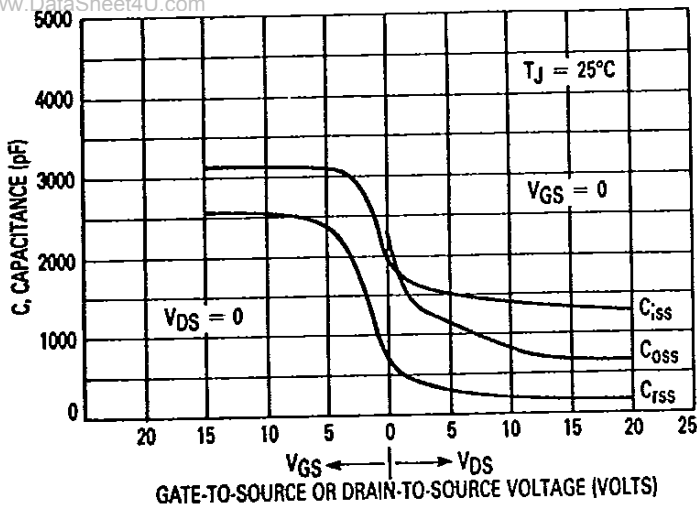

Figure 10. Thermal Response
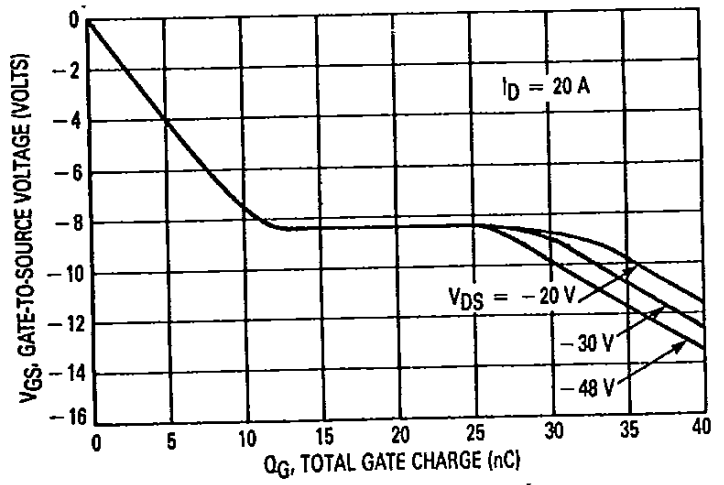
Figure 11. Capacitance Variation

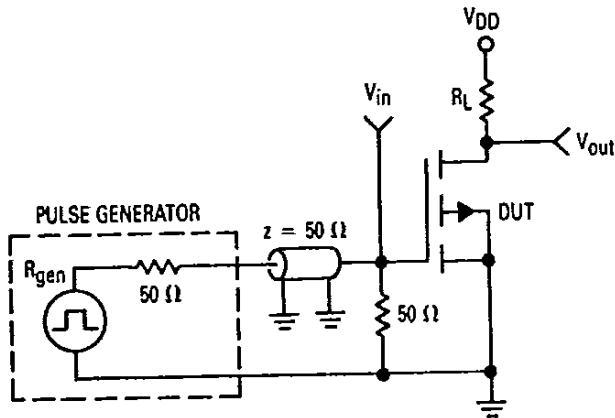Figure 12. Gate Charge versus Gate-To-Source Voltage
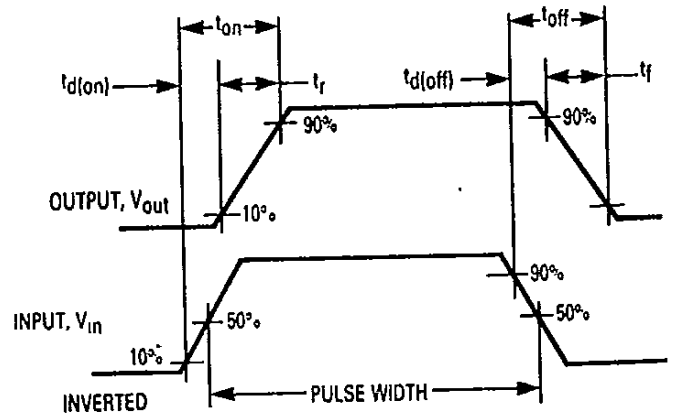
RESITIVE SWITCHING

Figure 13. Switching Test Circuit

Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	3570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5
PIN 1 GATE
2 DRAIN
3 SOURCE
4 DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: INCH
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED

CASE 221A-04
TO-220AB