

Designer's™ Data Sheet

Power Field Effect Transistor
P-Channel Enhancement-Mode Silicon Gate

MTP23P06

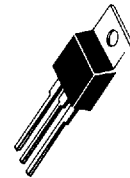
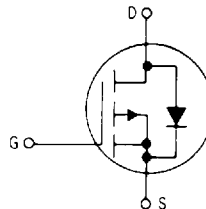
Motorola Preferred Device

This TMOS Power FET is designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Ultra Low $r_{DS(on)}$ P-Channel Series



TMOS POWER FET
23 AMPERES
 $r_{DS(on)} = 0.12 \text{ OHM}$
60 VOLTS



CASE 221A-06
TO-220AB

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|-----------------------|----------------------|---------------|
| Drain-to-Source Voltage | V_{DSS} | 60 | Vdc |
| Drain-Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$) | V_{DGR} | 60 | Vdc |
| Gate-Source Voltage — Continuous — Non-Repetitive ($t_p \leq 50 \mu s$) | V_{GS} V_{GSM} | ± 15 ± 20 | Vdc |
| Drain Current — Continuous — Pulsed | I_D I_{DM} | 23 75 | Adc |
| Total Power Dissipation Derate above 25°C | P_D | 125 0.8 | Watts W/°C |
| Operating and Storage Temperature Range | T_J, T_{stg} | -55 to 150 | °C |

THERMAL CHARACTERISTICS

| | | | |
|--|------------------------------------|-------------|------|
| Thermal Resistance — Junction to Case — Junction to Ambient | $R_{\theta JC}$ $R_{\theta JA}$ | 1.0 62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds | T_L | 260 | °C |

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|----------------|--------|-----|-----|------|
|----------------|--------|-----|-----|------|

OFF CHARACTERISTICS

| | | | | |
|--|---------------|--------|------------|------|
| Drain-Source Breakdown Voltage ($V_{GS} = 0, I_D = 0.25 \text{ mA}$) | $V_{(BR)DSS}$ | 60 | — | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS} = \text{Rated } V_{DSS}, V_{GS} = 0$) ($V_{DS} = \text{Rated } V_{DSS}, V_{GS} = 0, T_J = 125^\circ\text{C}$) | I_{DSS} | — — | 0.1 1.0 | mAdc |
| Gate-Body Leakage Current, Forward ($V_{GSF} = 15 \text{ Vdc}, V_{DS} = 0$) | I_{GSSF} | — | 100 | nAdc |
| Gate-Body Leakage Current, Reverse ($V_{GSR} = 15 \text{ Vdc}, V_{DS} = 0$) | I_{GSSR} | — | 100 | nAdc |

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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Preferred devices are Motorola recommended choices for future use and best overall value.

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ELECTRICAL CHARACTERISTICS — continued ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|----------------|--------|-----|-----|------|
|----------------|--------|-----|-----|------|

ON CHARACTERISTICS*

| | | | | |
|---|--------------|------------|------------|------|
| Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 1.0\text{ mA}$) ($T_J = 100^\circ\text{C}$) | $V_{GS(th)}$ | 2.0 1.5 | 4.5 4.0 | Vdc |
| Static Drain-to-Source On-Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 11.5\text{ Adc}$) | $r_{DS(on)}$ | — | 0.12 | Ohm |
| Drain-to-Source On-Voltage ($V_{GS} = 10\text{ V}$) ($I_D = 23\text{ Adc}$) ($I_D = 11.5\text{ Adc}$, $T_J = 100^\circ\text{C}$) | $V_{DS(on)}$ | — — | 3.3 3.0 | Vdc |
| Forward Transconductance ($V_{DS} = 15\text{ V}$, $I_D = 11.5\text{ A}$) | g_{FS} | 5.0 | — | mhos |

DYNAMIC CHARACTERISTICS

| | | | | | |
|------------------------------|--|-----------|---|------|----|
| Input Capacitance | ($V_{DS} = 25\text{ V}$, $V_{GS} = 0$, $f = 1.0\text{ MHz}$) See Figure 11 | C_{iss} | — | 1700 | pF |
| Output Capacitance | | C_{oss} | — | 900 | |
| Reverse Transfer Capacitance | | C_{rss} | — | 400 | |

SWITCHING CHARACTERISTICS*

| | | | | | |
|---------------------|--|--------------|----------|-----|----|
| Turn-On Delay Time | ($V_{DD} = 25\text{ V}$, $I_D = 23\text{ Amp}$, $R_{gen} = 13\text{ Ohms}$) See Figures 9, 13 and 14 | $t_{d(on)}$ | — | 30 | ns |
| Rise Time | | t_r | — | 170 | |
| Turn-Off Delay Time | | $t_{d(off)}$ | — | 140 | |
| Fall Time | | t_f | — | 120 | |
| Total Gate Charge | ($V_{DS} = 0.8\text{ Rated }V_{DSS}$, $I_D = 23\text{ Amp}$, $V_{GS} = 10\text{ V}$) See Figure 12 | Q_g | 80 (Typ) | 120 | nC |
| Gate-Source Charge | | Q_{gs} | 10 (Typ) | — | |
| Gate-Drain Charge | | Q_{gd} | 30 (Typ) | — | |

SOURCE-DRAIN DIODE CHARACTERISTICS*

| | | | | | |
|-----------------------|---|----------|-----------|-----|-----|
| Forward On-Voltage | ($I_S = 23\text{ Amp}$, $V_{GS} = 0$) | V_{SD} | 2.2 (Typ) | 3.5 | Vdc |
| Forward Turn-On Time | | t_{on} | 100 (Typ) | — | ns |
| Reverse Recovery Time | | t_{rr} | 120 (Typ) | — | |

INTERNAL PACKAGE INDUCTANCE (TO-220)

| | | | | |
|--|-------|------------------------|--------|----|
| Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die) | L_d | 3.5 (Typ) 4.5 (Typ) | — — | nH |
| Internal Source Inductance (Measured from the source lead 0.25" from package to center of pad) | L_s | 7.5 (Typ) | — | |

*Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

TYPICAL ELECTRICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

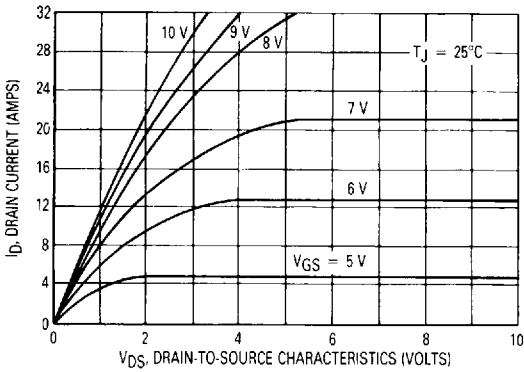


Figure 2. Gate-Threshold Variation With Temperature

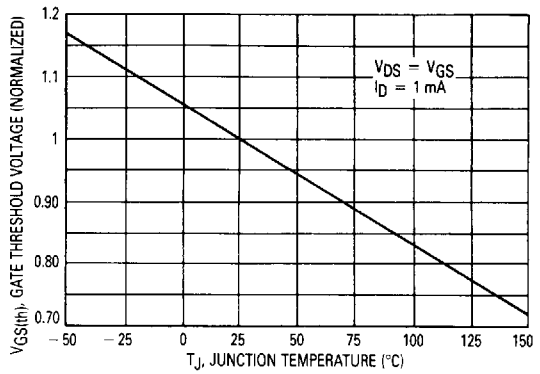


Figure 3. Transfer Characteristics

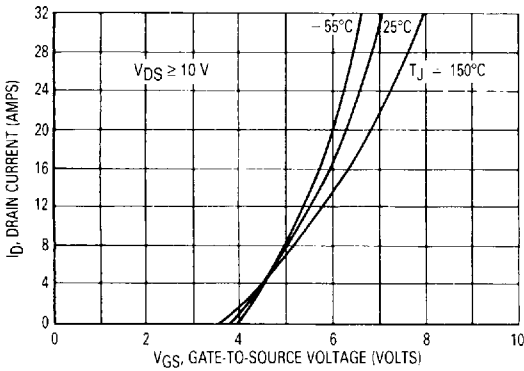


Figure 4. Normalized Breakdown Voltage versus Temperature

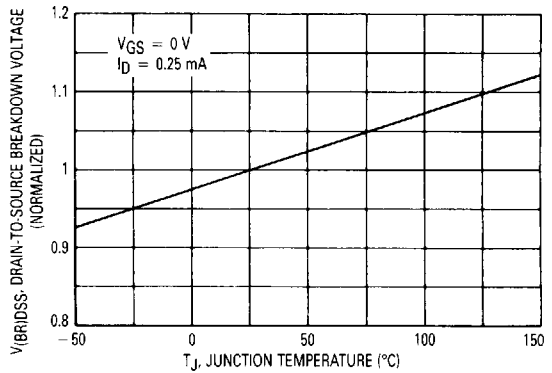


Figure 5. On-Resistance versus Drain Current

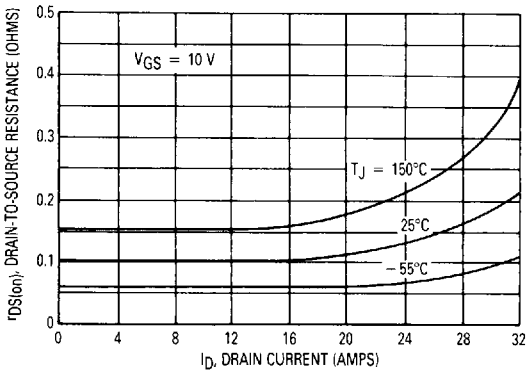
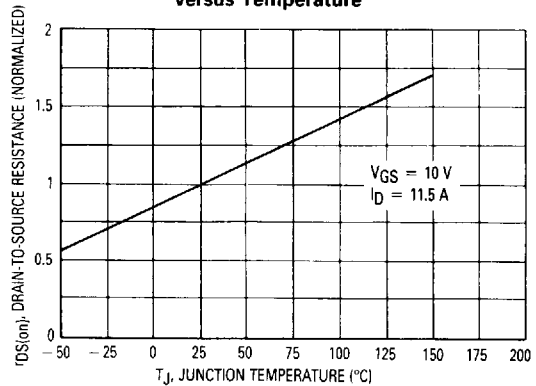


Figure 6. Normalized On-Resistance versus Temperature



SAFE OPERATING AREA INFORMATION

Figure 7. Maximum Rated Forward Biased Safe Operating Area

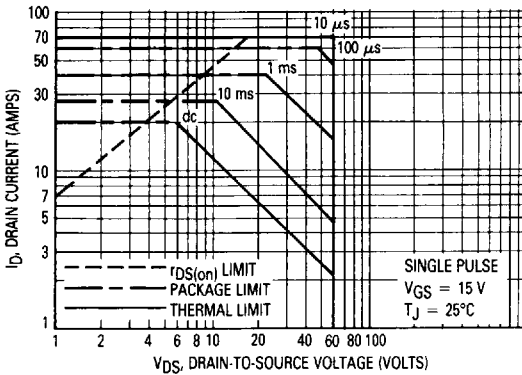
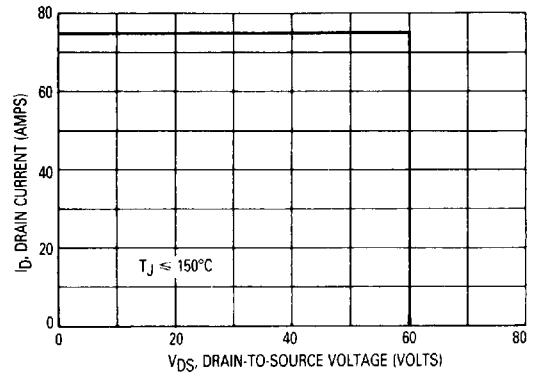


Figure 8. Maximum Rated Switching Safe Operating Area



FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_J(max) - T_C}{R_{\theta JC}}$$

Figure 9. Resistive Switching Time Variation versus Gate Resistance

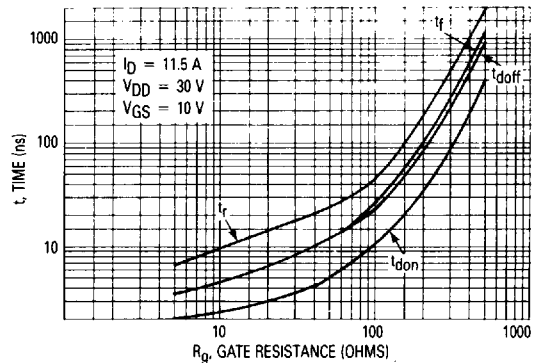


Figure 10. Thermal Response

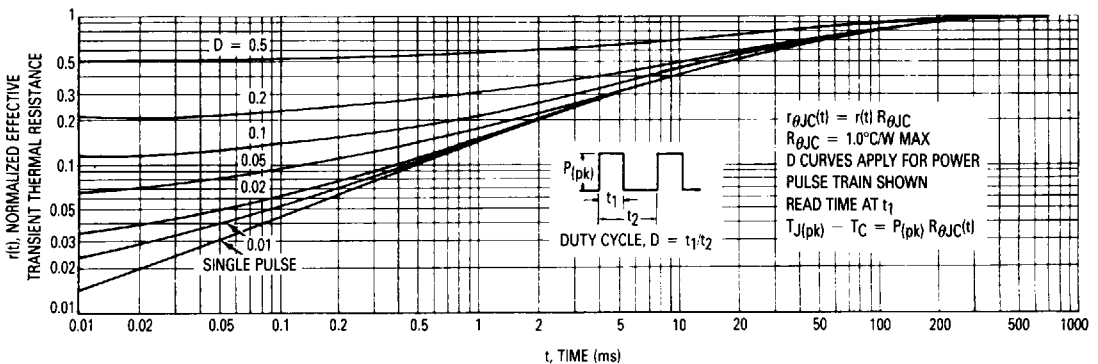


Figure 11. Capacitance Variation

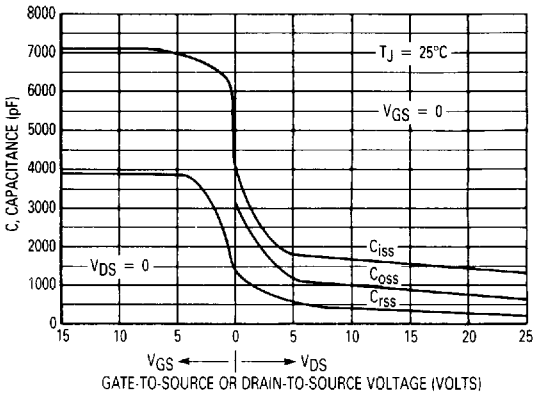
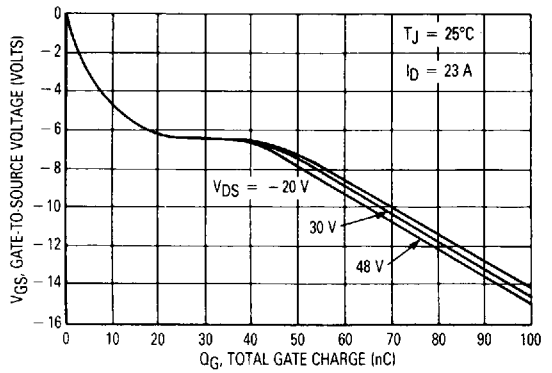


Figure 12. Gate Charge versus Gate-To-Source Voltage



RESISTIVE SWITCHING

Figure 13. Switching Test Circuit

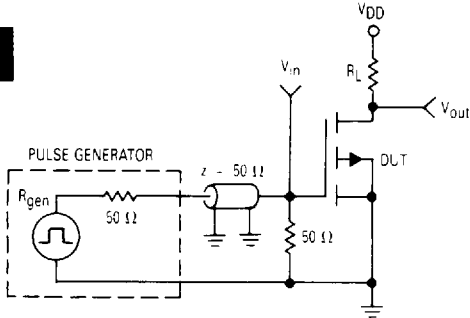
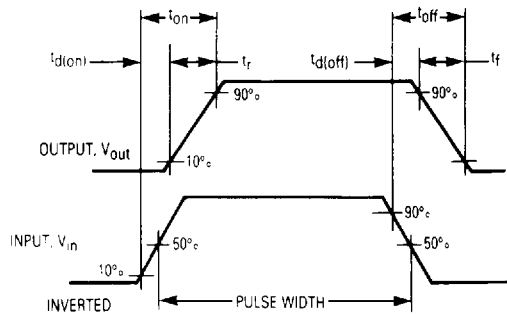


Figure 14. Switching Waveforms



TMOS SOURCE-TO-DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 15. Reversal of the drain voltage will cause current flow in the reverse direction. This diode may be used in circuits

requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

Figure 15. TMOS FET With Source-To-Drain Diode

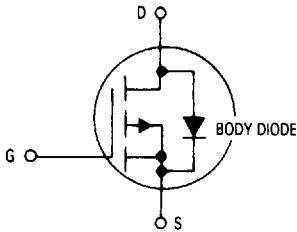


Figure 16. Diode Switching Waveform

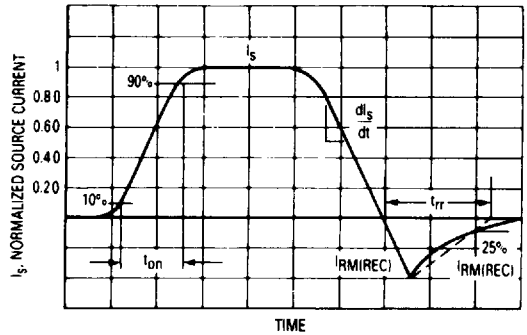


Figure 17. TMOS Diode Switching Test Circuit

NOTE: DUT is Shown as an N-Channel TMOS but can also be a P-Channel when appropriately connected. DUT Driver is the same device as DUT Diode (or Complement for P-Channel DUT Diode)

