T-39-13

MTP30N06E

Designer's Data Sheet

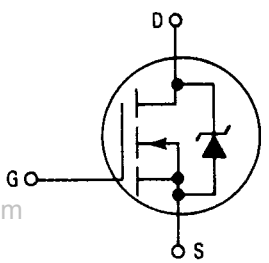
TMOS E-FET
Power Field Effect Transistor
N-Channel Enhancement-Mode Silicon Gate

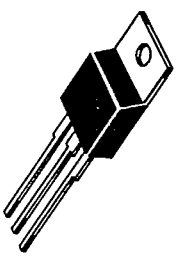
TMOS POWER FET
30 AMPERES
$r_{DS(on)}$ = 0.05 OHM
60 VOLTS

This advanced TMOS E-FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain-to-source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS}, $V_{GS(th)}$ and $V_{DS(on)}$ Specified at Elevated Temperature
- Direct Replacement for IRFZ34

TMOS™





CASE 221A-04
TO-220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate-Source Voltage — Continuous — Pulsed	V_{GS}	±20 ±40	Vdc
Drain Current — Continuous — Pulsed	I_D I_{DM}	30 120	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.8	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 175	°C

UNCLAMPED DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS ($T_J \leq$ 175°C)

Single Pulse Drain-to-Source Avalanche Energy Repetitive Pulse Drain-to-Source Avalanche Energy	W_{DSS} (1) W_{DSS} (2) W_{DSR} (3)	120 30 10	mJ

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

(1) V_{DD} = 25 V, I_D = 30 A, L = 180 μH, Initial T_C = 25°C
(2) V_{DD} = 25 V, I_D = 30 A, L = 45 μH, Initial T_C = 100°C
(3) f = 10 kHz

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 60 V, V_{GS} = 0)	I_{DSS}	—	10	μA
(V_{DS} = 60 V, V_{GS} = 0, T_J = 125°C)		—	80	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mA)	$V_{GS(th)}$	2.0	4.5	Vdc
T_J = 150°C		1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 15 Adc)	$r_{DS(on)}$	—	0.05	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V)	$V_{DS(on)}$	—	1.8	Vdc
(I_D = 30 Adc)				
(I_D = 15 Adc, T_J = 100°C)		—	1.4	
Forward Transconductance (V_{DS} ≥ 8.0 V, I_D = 15 A)	g_{FS}	8.0	—	mhos
DYNAMIC CHARACTERISTICS				
Input Capacitance	C_{iss}	1030 (Typ)	—	pF
Reverse Transfer Capacitance	C_{rss}	95 (Typ)	—	
Output Capacitance	C_{oss}	500 (Typ)	—	
(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz) See Figure 14				
SWITCHING CHARACTERISTICS (T_J = 100°C)				
Turn-On Delay Time	$t_{d(on)}$	18 (Typ)	—	ns
Rise Time	t_r	105 (Typ)	—	
Turn-Off Delay Time	$t_{d(off)}$	30 (Typ)	—	
Fall Time	t_f	45 (Typ)	—	
(V_{DD} = 30 V, I_D = 30 A, V_{GS} = 10 V, R_{gen} = 50 Ohms, R_{GS} = 15.8 Ohms)				
Total Gate Charge	Q_g	29 (Typ)	40	nC
Gate-Source Charge	Q_{gs}	6.5 (Typ)	—	
Gate-Drain Charge	Q_{gd}	15 (Typ)	—	
(V_{DS} = 48 V, I_D = 30 A, V_{GS} = 10 Vdc) See Figures 17 and 18				
SOURCE DRAIN DIODE CHARACTERISTICS*				
Forward On-Voltage (I_S = 30 A, V_{GS} = 0)	V_{SD}	1.15 (Typ)	1.35	Vdc
Forward Turn-On Time	t_{on}	Limited by stray inductance		
Reverse Recovery Time (I_S = 30 A, V_{GS} = 0, dI_S/dt = 100 A/μs, V_R = 30 V)	t_{rr}	110 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-220)				
Internal Drain Inductance	L_d			nH
(Measured from the contact screw on tab to center of die)		3.5 (Typ)	—	
(Measured from the drain lead 0.25" from package to center of die)		4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)	L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL ELECTRICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

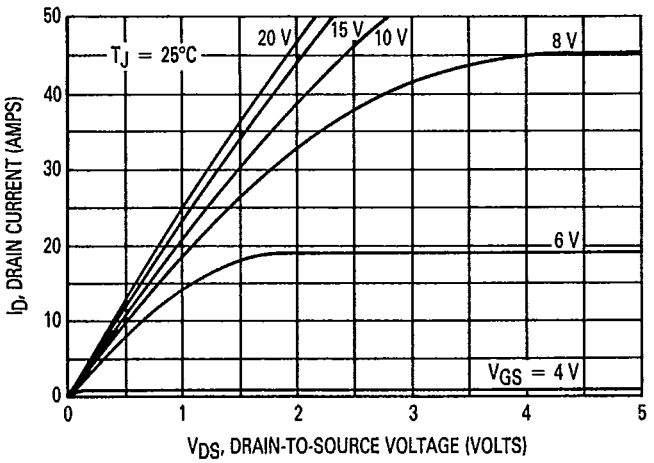


Figure 2. Gate-Threshold Voltage Variation With Temperature

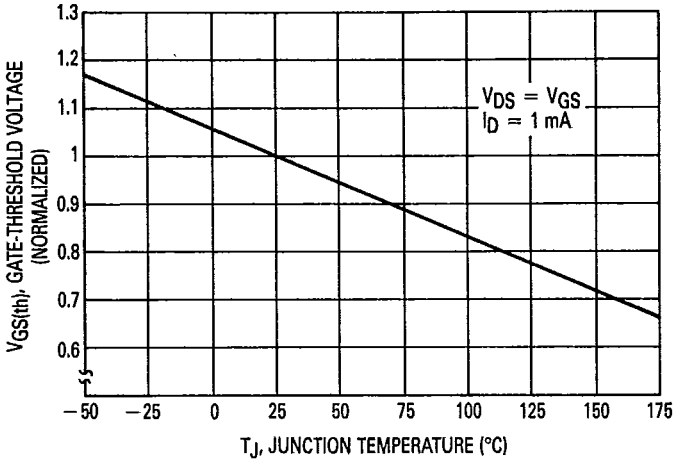


Figure 3. Transfer Characteristics

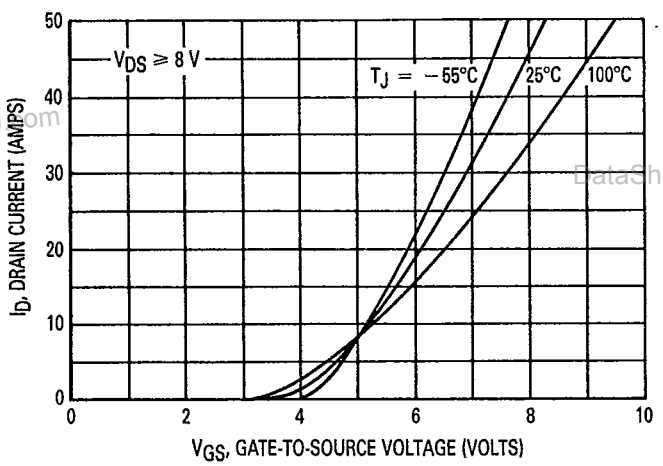


Figure 4. Breakdown Voltage Variation With Temperature

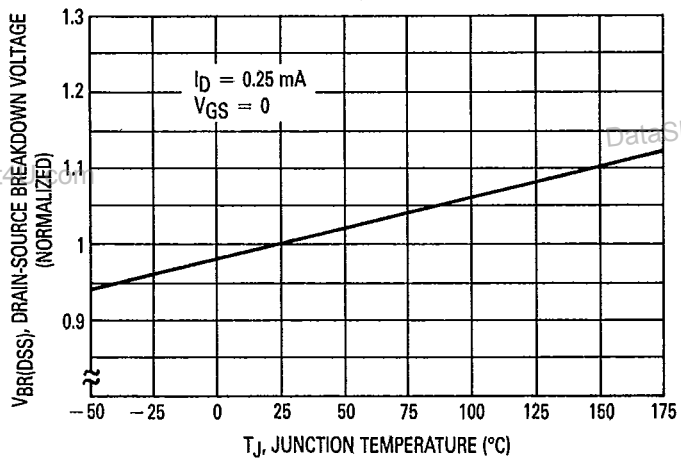


Figure 5. On-Resistance versus Drain Current

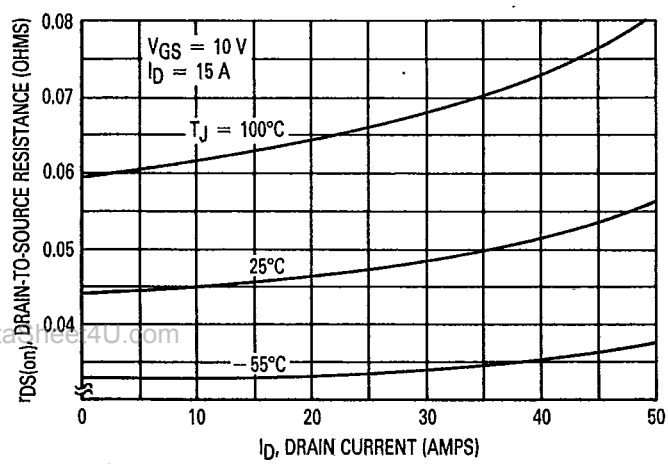
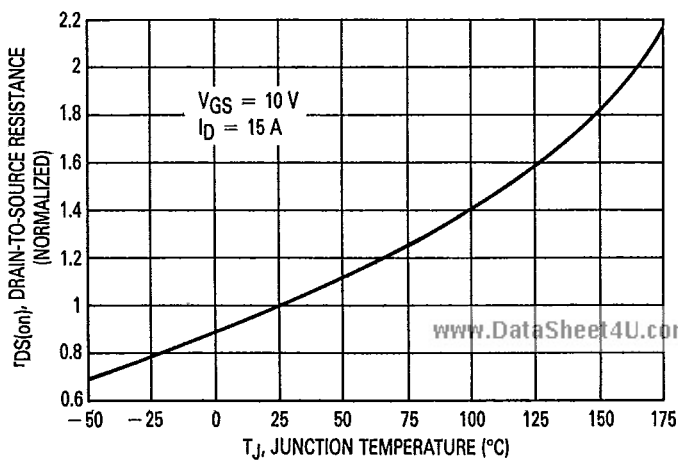


Figure 6. On-Resistance Variation With Temperature



SAFE OPERATING AREA INFORMATION

Figure 7. Maximum Rated Forward Biased Safe Operating Area

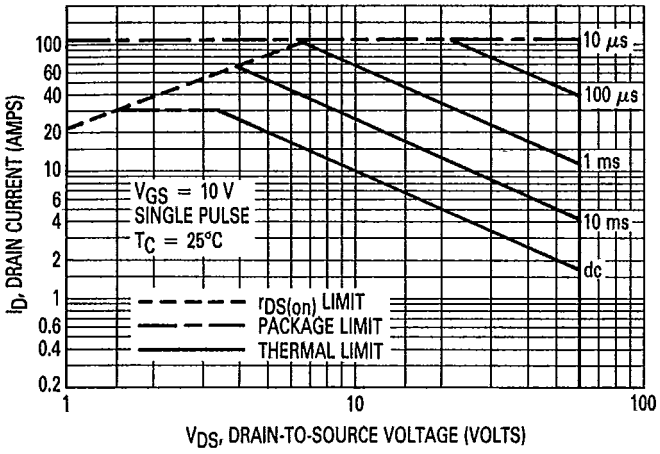
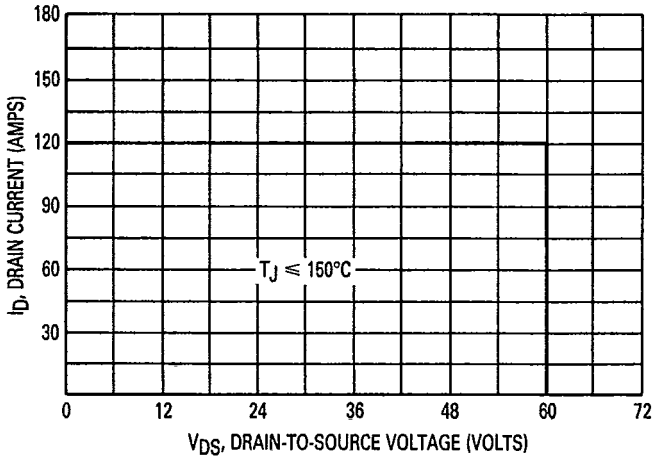


Figure 8. Maximum Rated Switching Safe Operating Area



FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 175°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

Figure 9. Resistive Switching Time Variation versus Gate Resistance

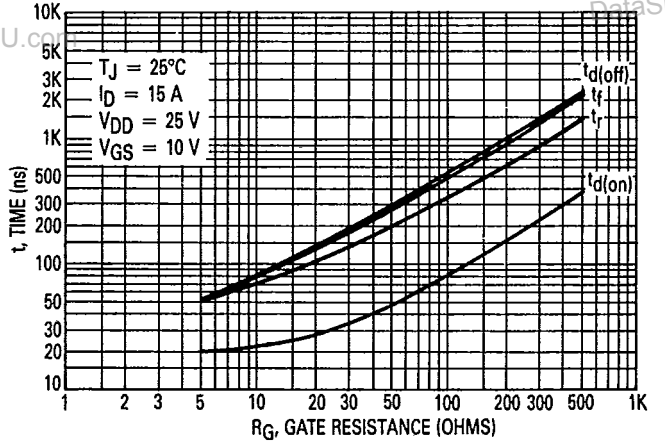
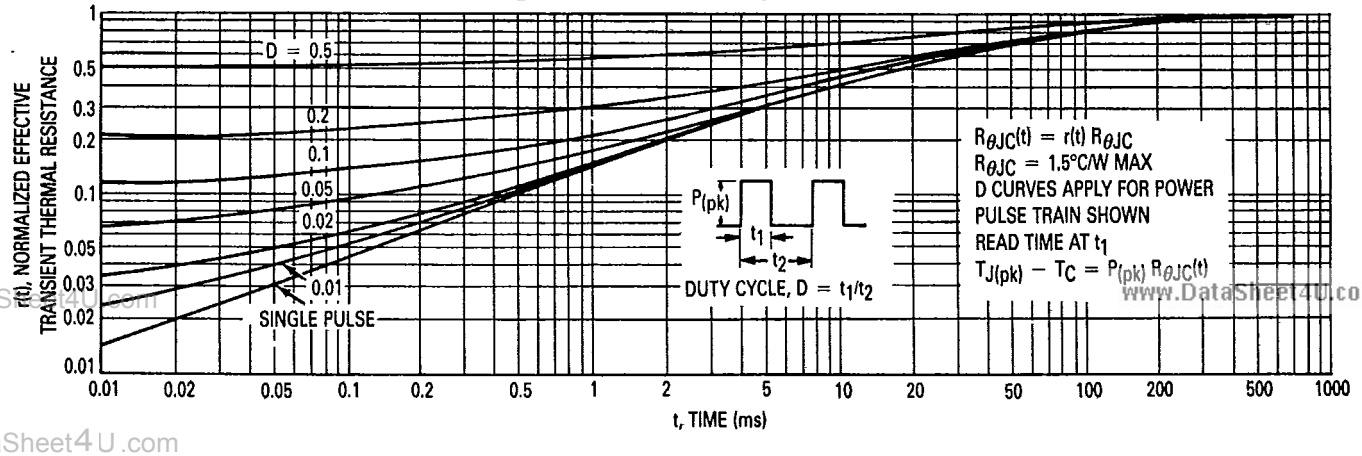


Figure 10. Thermal Response



COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/μs.

Figure 12. Commutating Safe Operating Area (CSOA)

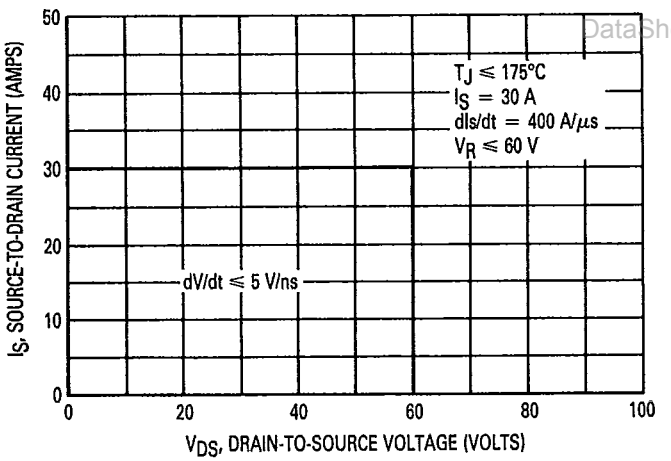


Figure 14. Unclamped Inductive Switching Test Circuit

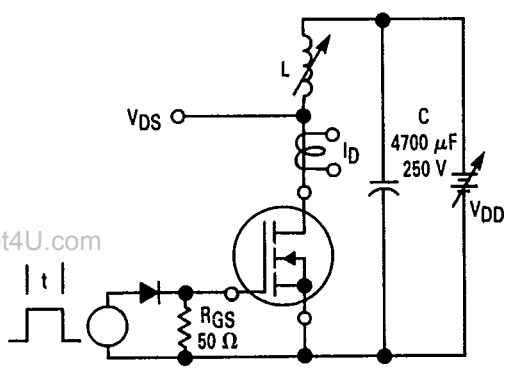


Figure 11. Commutating Waveforms

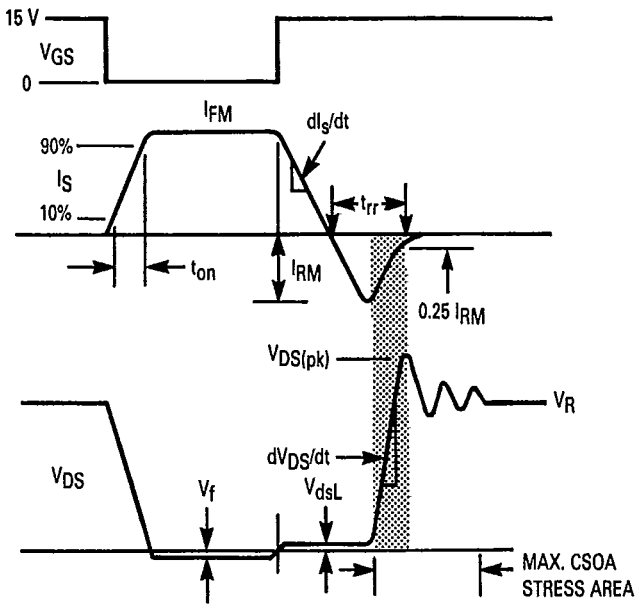


Figure 13. Commutating Safe Operating Area Test Circuit

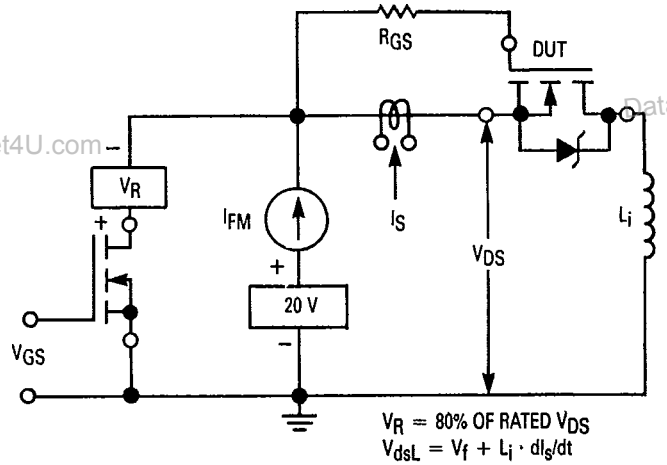


Figure 15. Unclamped Inductive Switching Waveforms

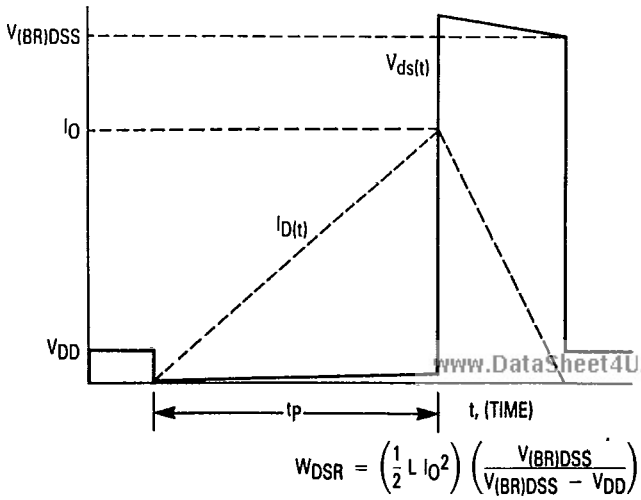


Figure 16. Capacitance Variation

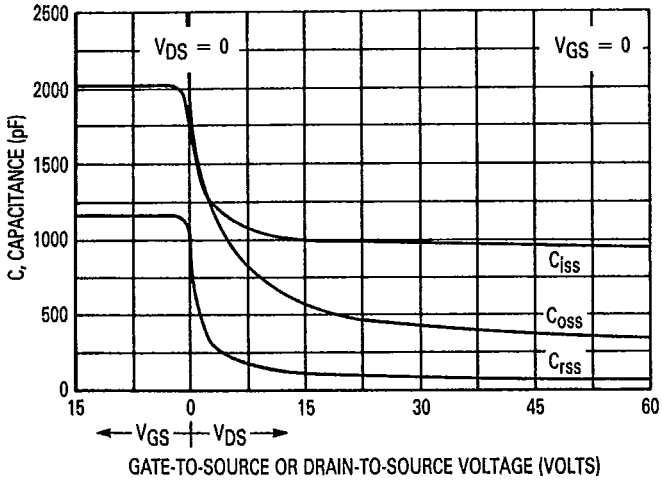


Figure 17. Gate Charge versus Gate-To-Source Voltage

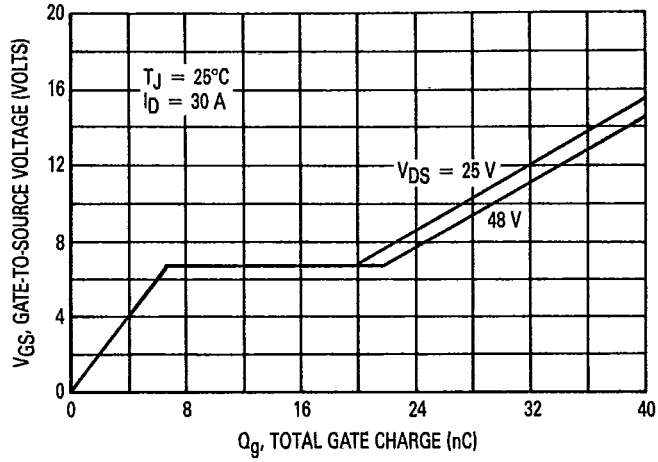
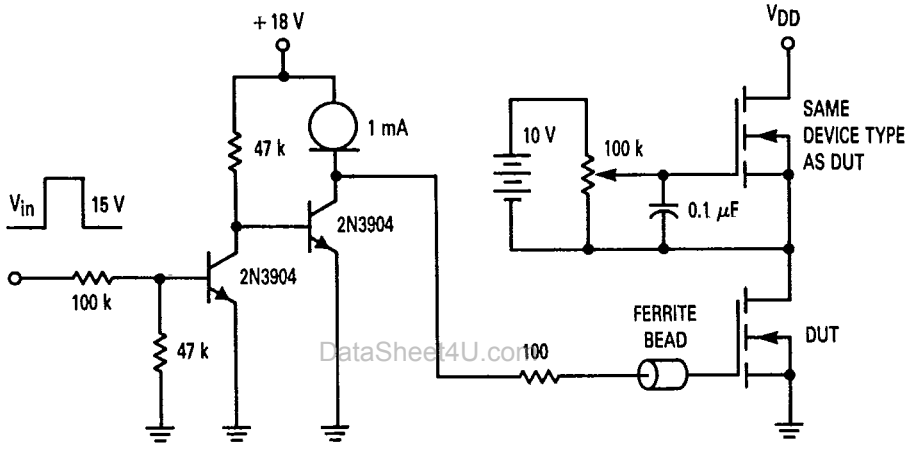


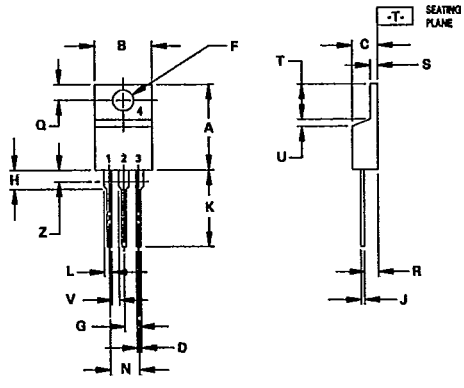
Figure 18. Gate Charge Test Circuit



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

OUTLINE DIMENSIONS

CASE 221A-04
TO-220AB



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

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