MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate with Current Sensing Capability

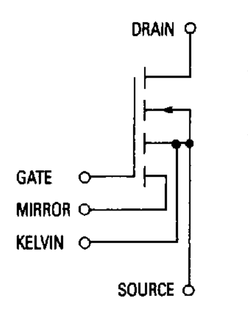
MTP30N08M

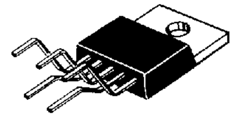
TMOS SENSEFET DEVICE
30 AMPERES
$R_{DS(on)}$ = 0.065 OHM
80 VOLTS

This TMOS Power FET with current sensing capability is designed for all power control applications where it is desirable to sense current such as in power supplies and motor controls. This device allows current sensing with a minimum of power loss.

- "Lossless" Current Sensing for Maximum Efficiency
  - — Sense Current is Reduced by a Factor of 900
- Ideal for Short Circuit/Overload Protection
- Simplifies Many Circuits When Used With Current Mode Integrated Circuits Such as the MC34129
- Kelvin Source Contact to Maximize Accuracy
- Rugged — SOA is Power Dissipation Limited
- Low $R_{DS(on)}$ — 0.065 Ohms Maximum

NOTES:
1. Handling precautions to protect against electrostatic discharge is mandatory.
2. Do not use the mirror FET independent of the power FET
3. It is recommended that the mirror terminal (M) be shorted to the Kelvin Terminal (K) when current sensing is not required





CASE 314B-03

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	80	Vdc
Drain-to-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	80	Vdc
Gate-to-Source Voltage — Continuous — Non-Repetitive ($t_p \leq 50\ \mu s$)	V_{GS}	±20 ±40	Vdc
Drain-to-Mirror Voltage	V_{DMS}	80	Vdc
Gate-to-Mirror Voltage — Continuous — Non-Repetitive ($t_p \leq 50\ \mu s$)	V_{GM}	±20 ±40	Vdc
Drain Current — Continuous — Pulsed	I_D I_{DM}	30 90	Amps
Sense Current — Continuous — Pulsed	I_M I_{MM}	33 100	mA
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case Junction-to-Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{MK} = 0 unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-to-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	80	—	—	Vdc
Zero Gate Voltage Drain Current	I_{DSS}				μAdc
(V_{DS} = 80 V, V_{GS} = 0)		—	—	10	
(V_{DS} = 80 V, V_{GS} = 0, T_J = 125°C)		—	—	100	
Gate-Body Leakage Current — Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	—	100	nAdc
Gate-Body Leakage Current — Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage	$V_{GS(th)}$				Vdc
(V_{DS} = V_{GS}, I_D = 1 mAdc)		2	2.5	4	
(T_J = 125°C)		1.5	—	3.5	
Static Drain-to-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 15 Adc)	$R_{DS(on)}$	—	0.05	0.065	Ohms
Drain-to-Source On-Voltage (V_{GS} = 10 Vdc)	$V_{DS(on)}$				Vdc
(I_D = 30 A)		—	1.5	1.95	
(I_D = 15 A, T_J = 125°C)		—	—	1.95	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 15 Adc)	g_{fs}	10	—	—	mhos
CURRENT SENSING CHARACTERISTICS					
Current Mirror Ratio (Cell Ratio) (R_{SENSE} = 0, I_D = 15 A, V_{GS} = 10 V)	n	900	—	960	—
Mirror Compliance Ratio (V_{GS} = 10 Vdc, I_D = 15 Adc)	K_{mc}	—	0.65	—	—
Source Active Resistance (V_{GS} = 10 Vdc, I_D = 15 Adc, R_S = 10 megohm)	$r_{a(on)}$	—	26	—	mΩ
Mirror Active Resistance (V_{GS} = 10 Vdc, I_D = 15 Adc)	$r_{m(on)}$	—	24	—	Ohms

DYNAMIC CHARACTERISTICS

Characteristics		Symbol	Min	Typ	Max	Unit
Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 f = 1 MHz	C_{iss}	—	—	1800	pF
Output Capacitance		C_{oss}	—	—	900	
Transfer Capacitance		C_{rss}	—	—	400	

SWITCHING CHARACTERISTICS*

Characteristics		Symbol	Min	Typ	Max	Unit
Turn-On Delay Time	V_{DD} = 30 V, I_D = 15 A R_{gen} = 50 Ohms	$t_{d(on)}$	—	25	60	ns
Rise Time		t_r	—	110	200	
Turn-Off Delay Time		$t_{d(off)}$	—	120	200	
Fall Time		t_f	—	65	150	
Total Gate Charge	V_{DS} = 64 V, I_D = 30 A V_{GS} = 10 V	Q_g	—	62	75	nC
Gate-Source Charge		Q_{gs}	—	8	—	
Gate-Drain Charge		Q_{gd}	—	35	—	

SOURCE-DRAIN DIODE CHARACTERISTICS*

Characteristics		Symbol	Min	Typ	Max	Unit
Forward On-Voltage	I_S = 30 A	V_{SD}	—	1.6	2	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance			ns
Reverse Recovery Time		t_{rr}	—	200	—	

*Indicates Pulse Test Pulse Width = 300 μs max, Duty Cycle = 2%.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

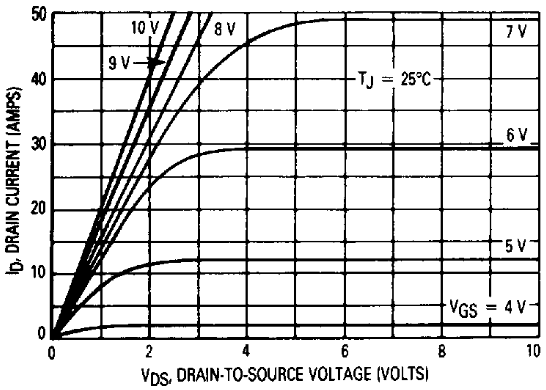


Figure 2. Gate Threshold Voltage Variation with Temperature

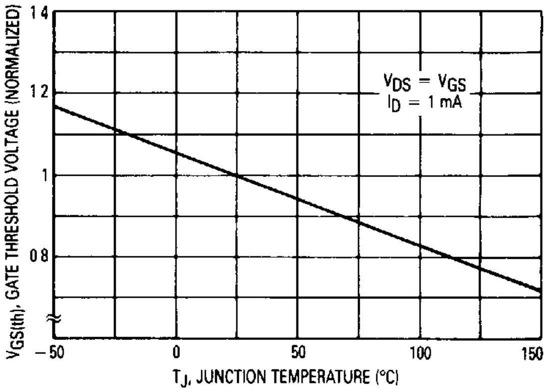


Figure 3. Transfer Characteristics

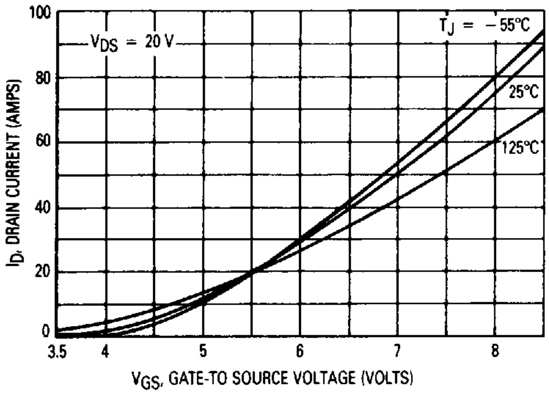


Figure 4. Stored Charge Variation

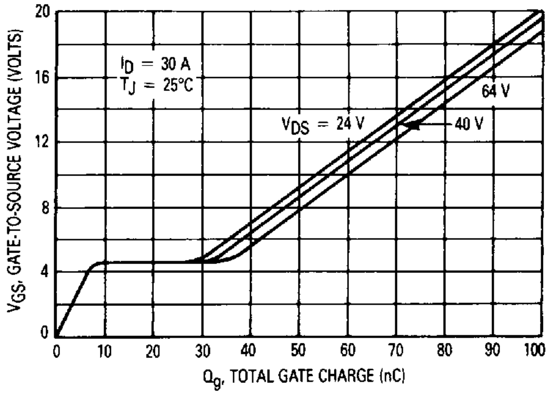


Figure 5. On-Resistance versus Drain Current

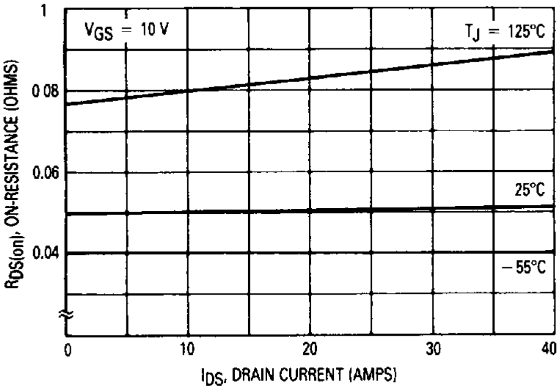
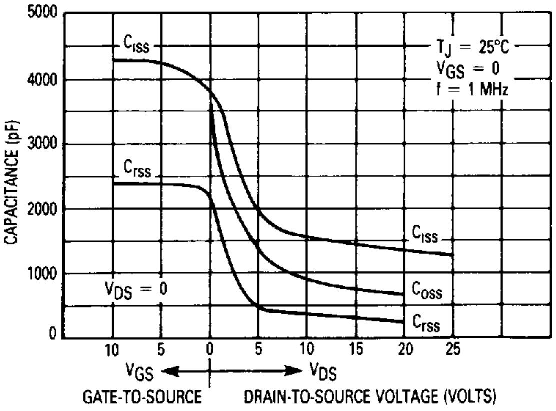
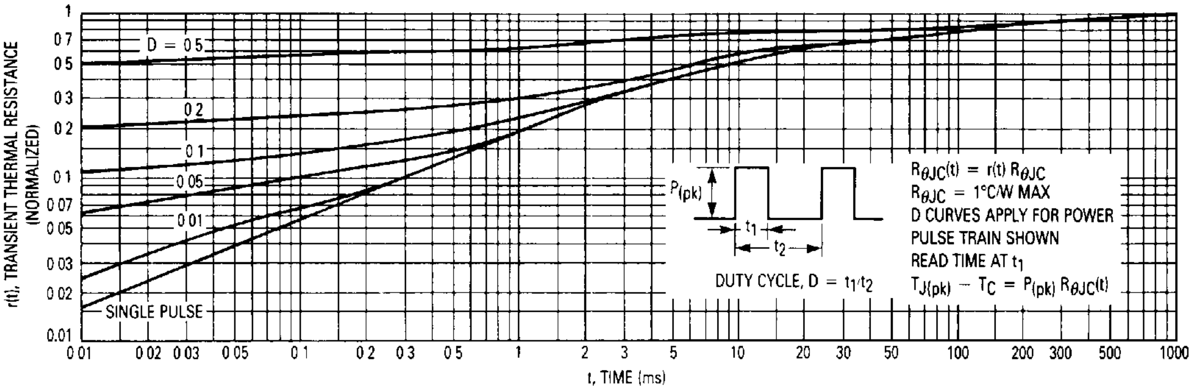


Figure 6. Capacitance Variation



TYPICAL CHARACTERISTICS

Figure 7. Thermal Response



SAFE OPERATING AREA INFORMATION

Figure 8. Maximum Rated Forward Biased Safe Operating Area

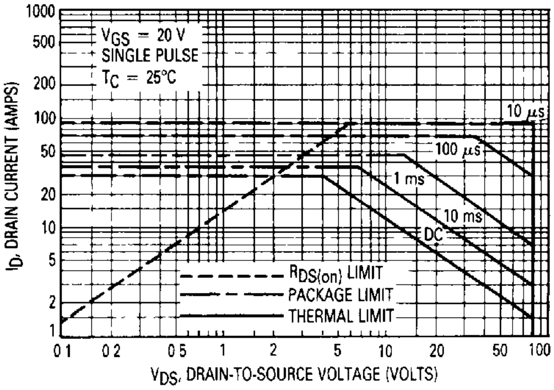
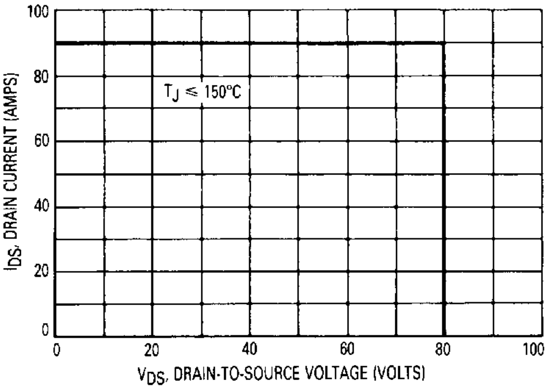


Figure 9. Maximum Rated Switching Safe Operating Area



FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

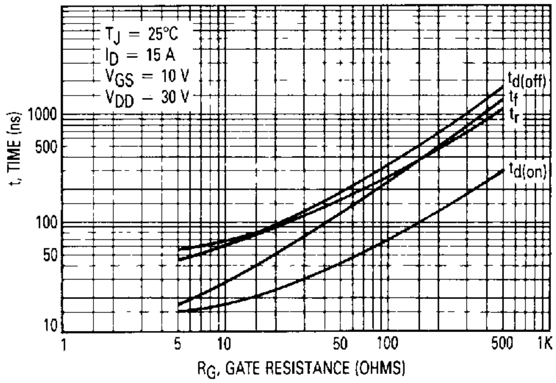
SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

Figure 10. Resistive Switching Time Variation with Gate Resistance



SAFE OPERATING AREA INFORMATION

Figure 11. On-Resistance Variation with Temperature

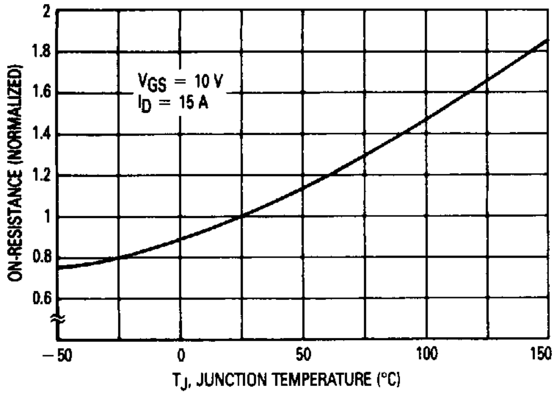


Figure 12. Breakdown Variation with Temperature

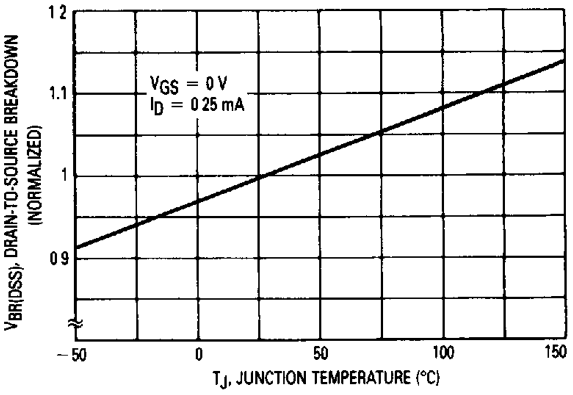


Figure 13. Sense Voltage Variation with Sense Resistance

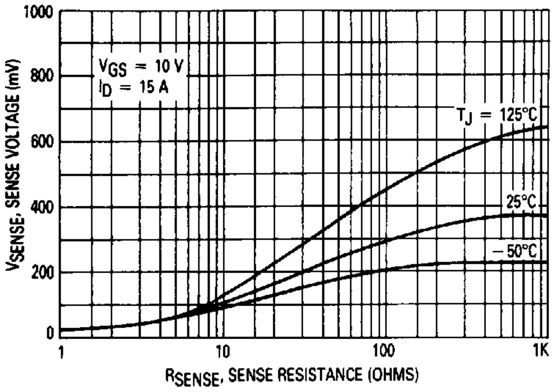


Figure 14. Sense Voltage Variation with Drain Current

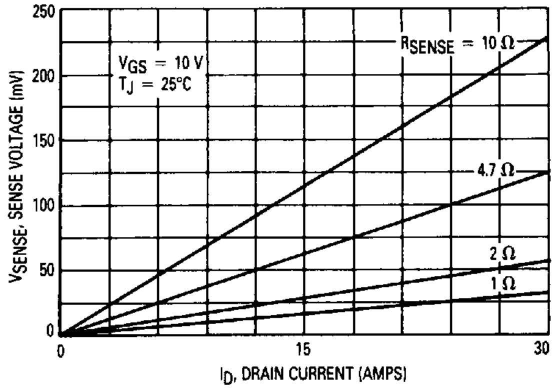


Figure 15. Sense Voltage Variation with Temperature

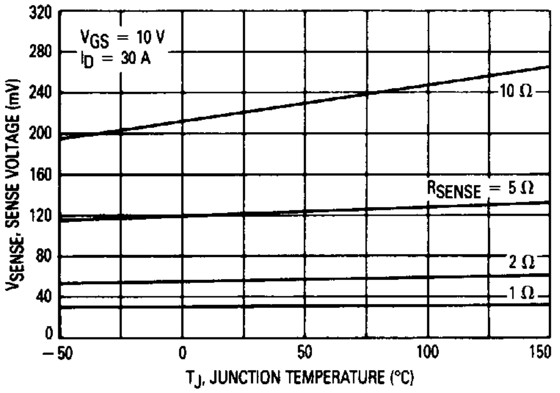


Figure 16. Sense Voltage Variation with Gate-to-Source Voltage

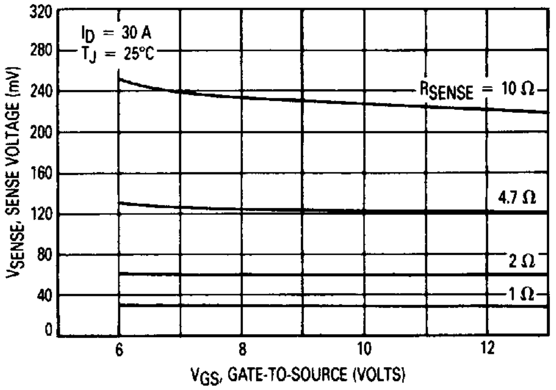


Figure 17. Current Mirror Ratio Variation with Drain Current

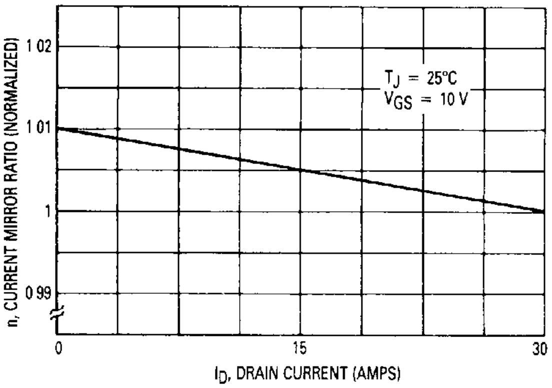


Figure 18. Current Mirror Ratio Variation with Gate-to-Source Voltage

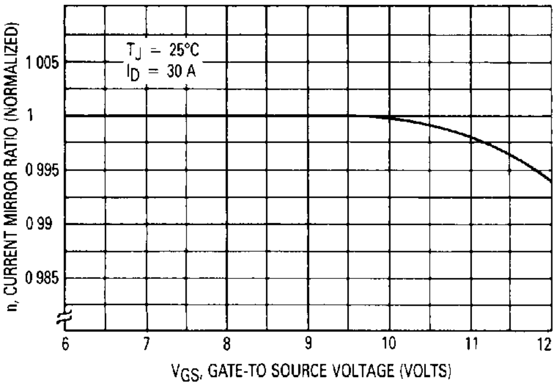
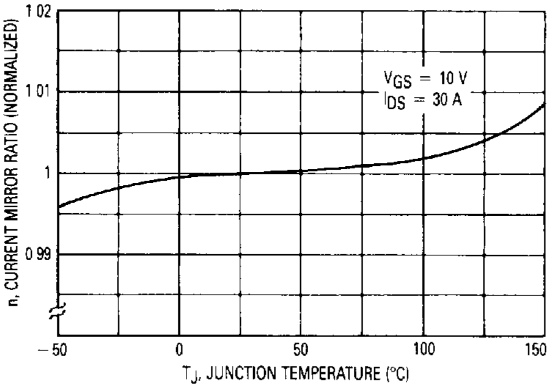


Figure 19. Current Mirror Ratio Variation with Temperature



LOSSLESS CURRENT SENSING

Assuming a fully switched on SENSEFET device, current sensing can be modeled with the simple resistor divider network shown in Figure 20. In this model, r_b is the bulk drain resistance, $r_{m(on)}$ is the active mirror on-resistance, $r_{a(on)}$ is the power section's active on-resistance and r_w is the source wire bond resistance. Using values for $r_{a(on)}$ and $r_{m(on)}$ from the electrical characteristics table; V_{SENSE}, R_{SENSE}, and drain current may be calculated from the following sensing equations.

SENSING EQUATIONS:

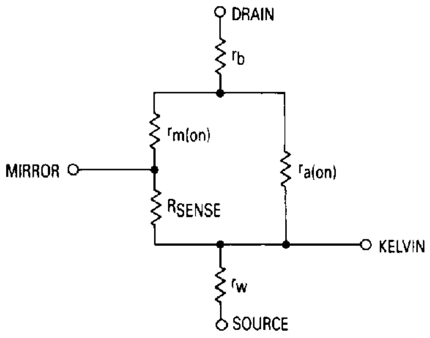
1. $V_{SENSE} = I_D\, r_{a(on)}\, R_{SENSE}/[R_{SENSE} + r_{m(on)}]$
2. $R_{SENSE} = V_{SENSE}\, r_{m(on)}/[I_D\, r_{a(on)} - V_{SENSE}]$
3. $I_D = V_{SENSE}\, (R_{SENSE} + r_{m(on)})/r_{a(on)}\, R_{SENSE}$
4. $n = I_D/I_{SENSE}$; where $R_{SENSE} = 0$
5. $r_{a(on)} = r_{m(on)}/n$

When using these equations there are several factors to keep in mind.

They are described as follows:

- Maximum Sense Voltage: The maximum sense voltage that can appear at the mirror terminal is $(r_{a(on)}/r_{a(on)} + r_b) \times V_{DS(on)}$. This ratio is called the mirror compliance ratio, K_{MC}, and defines the upper boundary for sense voltage.
- Accuracy: Accurate current sensing is based upon the inherent matching of $r_{m(on)}$ with the power section's active on-resistance, $r_{a(on)}$. When $R_{SENSE} = 0$, matching and current sensing accuracy are within ±3%. As R_{SENSE} is increased, sensing accuracy is reduced since mirror current becomes dependent on the ratio of internal on-resistance to an external R_{SENSE}. From a practical point of view, relatively good sensing accuracy (±10%) is maintained up to $R_{SENSE} = r_{m(on)}/2$. As R_{SENSE} is increased beyond $r_{m(on)}$, sensing accuracy decreases rapidly.

Figure 20. SENSEFET Model



- Ground Loop Errors: Lossless current sensing is a technique that looks for 100 mV signals in a loop that may carry tens or even hundreds of amps. The potential for ground loop errors in this kind of an application is a first order design consideration. Internal wire bond resistance, contact resistance, and external wiring resistance are all significant. Therefore, it is important to reference sense voltage measurement circuitry to the Kelvin pin rather than power ground. In addition, referencing gate drive to the Kelvin pin rather than power ground will provide faster switching speeds.
- Noise Suppression: Switching noise is also a first order design issue. Layout, therefore, is critical. In addition, a single pole RC filter between R_{SENSE} and the current sensing circuitry's input terminals is often desirable. A 1 μsec time constant is generally long enough to provide adequate noise suppression and short enough to provide adequate protection during overloads. An illustration is provided in Figure 21.
- Double Pulse Suppression: In PWM circuits it is critically important to include double pulse suppression in the control circuit topology. If the current limit loop is allowed to oscillate at its natural frequency, failure of the SENSEFET device is likely due to excessive power dissipation. By syncing current limiting to the clock with a latch, double pulse suppression architectures solve this problem, and provide effective protection from overload stress.
- Parasitic Diode: In addition to the power section's usual source-drain diode, there is a mirror-drain diode in the sense cells. Like the source-drain diode, the mirror-drain diode conducts during the reverse-mode operation, however, current sense characteristics are defined only in the forward-mode operation.
- Reverse Recovery: In bridge circuits, when a SENSEFET device's source-drain diode is commutated a voltage spike is produced at the mirror. This spike is short since it lasts only for the drain-source diode's reverse recovery time. However, its amplitude can be an order of magnitude larger than normal sense voltages and produce unwanted overcurrent trips. Blanking, filtering, or other suppression techniques may be required in some applications.

Figure 21. SENSEFET Device with Noise Suppression