MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTP3N100

Designer's Data Sheet

Power Field Effect Transistor

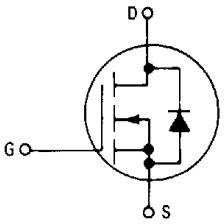
N-Channel Enhancement Mode Silicon Gate

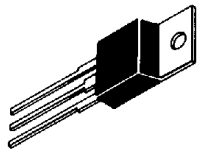
This TMOS Power FET is designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS®

TMOS POWER FET
3 AMPERES
$R_{DS(on)}$ = 4 OHMS
1000 VOLTS





CASE 221A-06
TO-220AB

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	1000	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	1000	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 3 16	Adc
Gate Current — Pulsed	I_{GM}	1.5	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	1000	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)	I_{DSS}	—	0.2	mAdc
(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		—	1	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)	$V_{GS(th)}$	2	4.5	Vdc
(T_J = 100°C)		1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.5 Adc)	$R_{DS(on)}$	—	4	Ohm
(V_{GS} = 10 Vdc, I_D = 2 Adc)		—	—	
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 3 Adc)	$V_{DS(on)}$	—	12	Vdc
(I_D = 1.5 Adc, T_J = 100°C)		—	10	
(I_D = 4 Adc)		—	—	
(I_D = 2 Adc, T_C = 100°C)		—	14	
Forward Transconductance (V_{DS} = 10 V, I_D = 1.5 A)	g_{FS}	2	—	mhos
(V_{DS} = 10 V, I_D = 2 A)		—	—	
DYNAMIC CHARACTERISTICS				
Input Capacitance	C_{iss}	—	1500	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	150	
Reverse Transfer Capacitance	C_{rss}	—	60	
SWITCHING CHARACTERISTICS (T_J = 100°C)				
Turn-On Delay Time	$t_{d(on)}$	—	40	ns
Rise Time (V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figs. 8 and 9.	t_r	—	40	
Turn-Off Delay Time	$t_{d(off)}$	—	250	
Fall Time	t_f	—	75	
Total Gate Charge	Q_g	55 (Typ)	85	nC
Gate-Source Charge (V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 Vdc) See Figs. 10 and 11.	Q_{gs}	30 (Typ)	—	
Gate-Drain Charge	Q_{gd}	25 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS				
Forward On-Voltage	V_{SD}	1.1 (Typ)	1.5	Vdc
Forward Turn-On Time (I_S = Rated I_D, V_{GS} = 0)	t_{on}	200 (Typ)	—	ns
Reverse Recovery Time	t_{rr}	1000 (Typ)	—	ns

TYPICAL CHARACTERISTICS

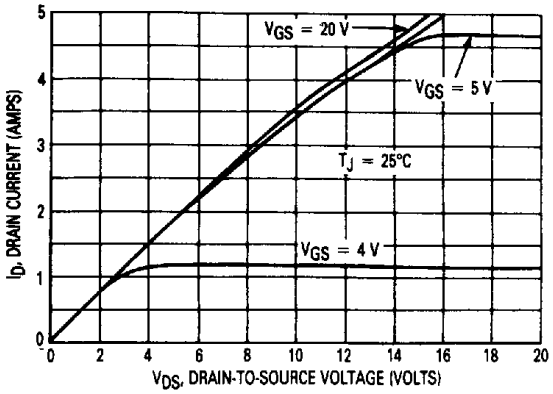

Figure 1. On-Region Characteristics

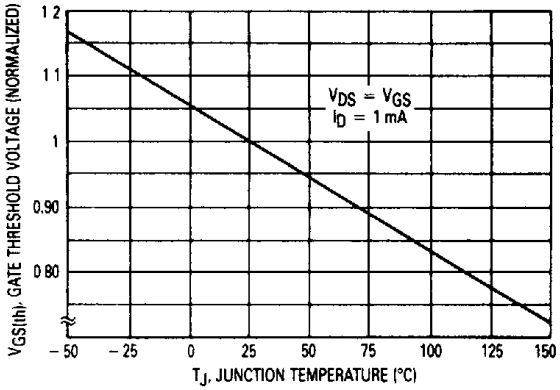

Figure 2. Gate-Threshold Voltage Variation with Temperature

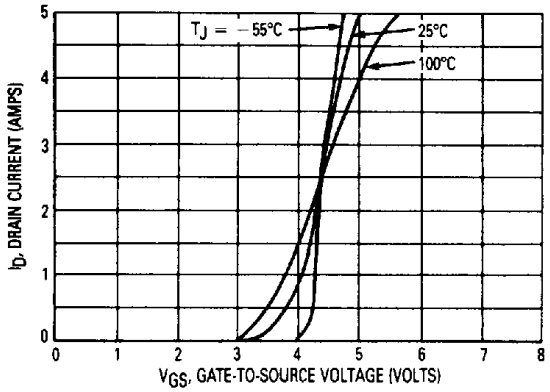

Figure 3. Transfer Characteristics

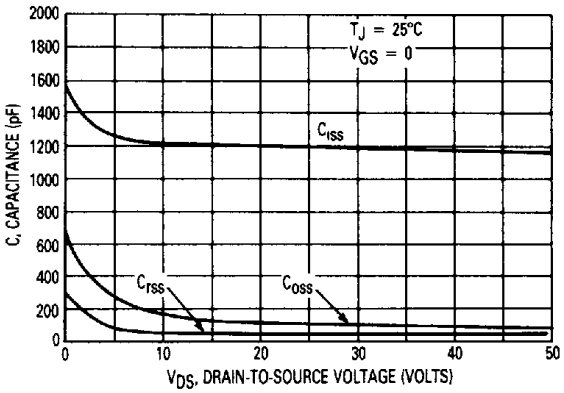

Figure 4. Capacitance Variation

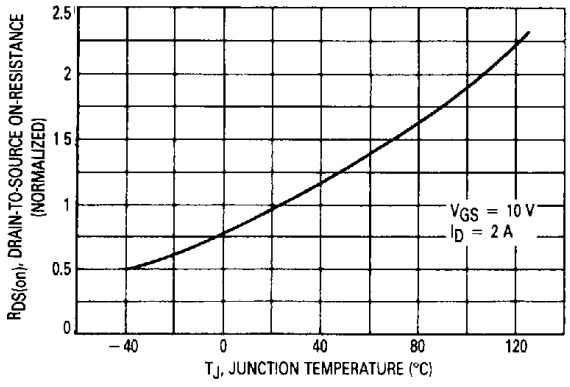

Figure 5. Normalized On-Resistance versus Temperature

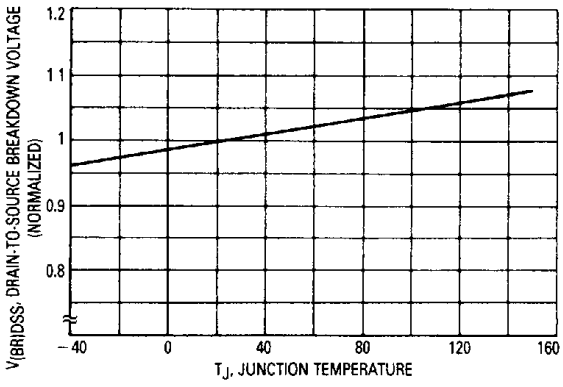

Figure 6. Normalized Breakdown Voltage versus Temperature

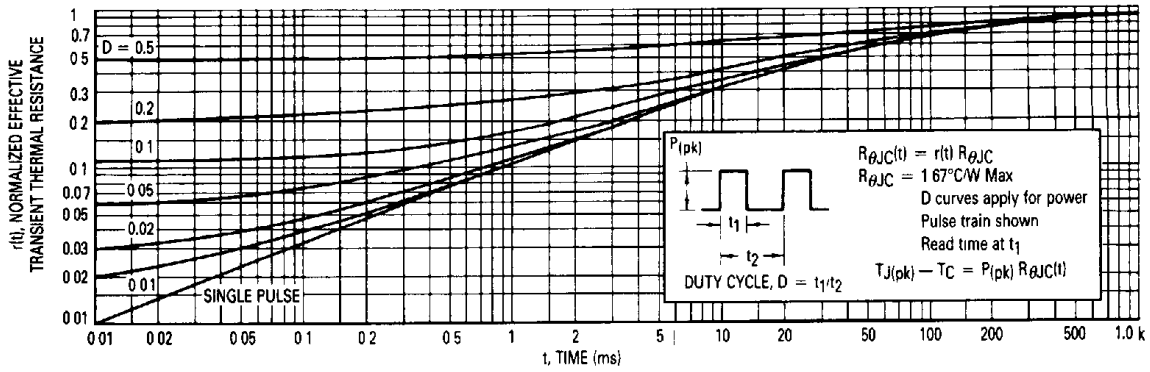

Figure 7. Thermal Response

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RESISTIVE SWITCHING

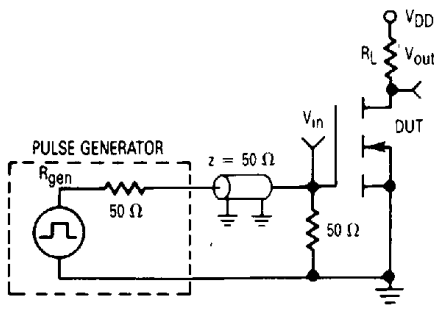


Figure 8. Switching Test Circuit

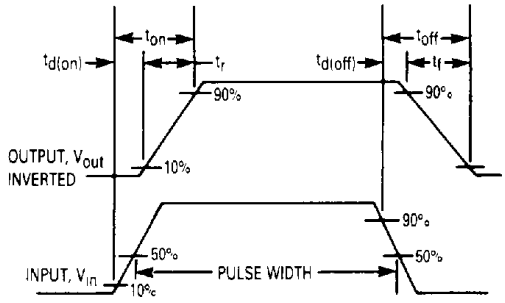


Figure 9. Switching Waveforms

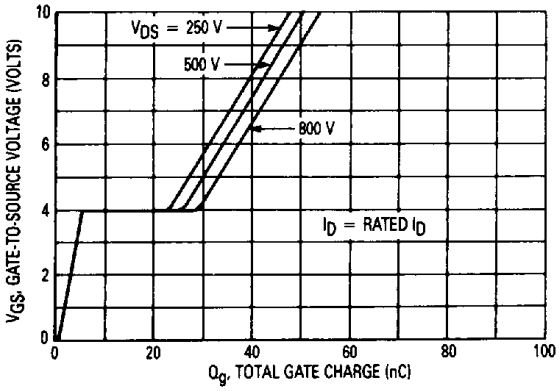
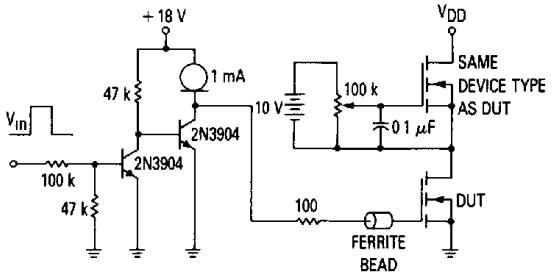


Figure 10. Gate Charge Variation



V_{in} = 15 V_{pk}, PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

Figure 11. Gate Charge Test Circuit

SAFE OPERATING AREA INFORMATION

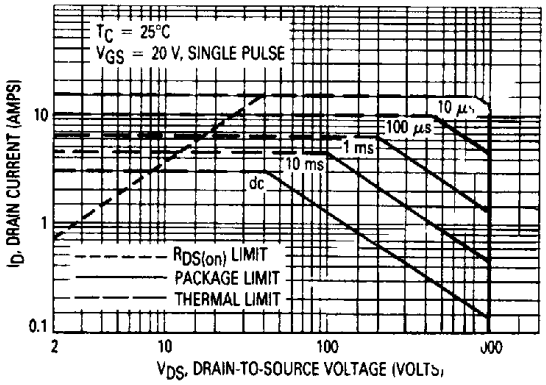


Figure 12. Maximum Rated Forward Biased Safe Operating Area

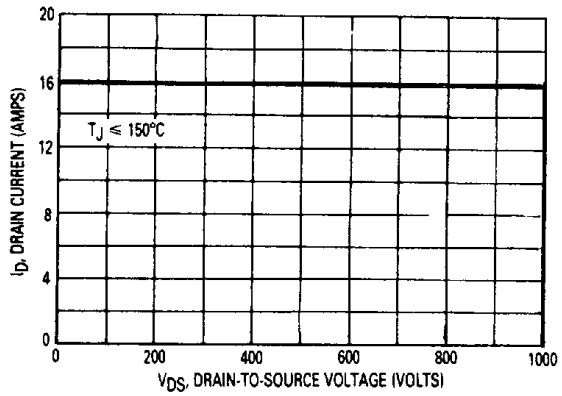


Figure 13. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 11 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figure 11
$T_{J(max)}$ = rated maximum junction temperature
T_C = device case temperature
P_D = rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = rated steady state thermal resistance
r(t) = normalized thermal response from Figure 7

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 12 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 12 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

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