

MOTOROLA
SEMICONDUCTOR
 TECHNICAL DATA

Designer's Data Sheet
Power Field Effect Transistor
N-Channel Enhancement-Mode
Silicon Gate

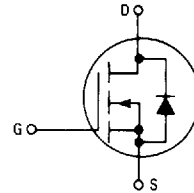
This TMOS Power FET is designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



MTP3N50

TMOS POWER FET
3 AMPERES
 $R_{DS(on)} = 3 \text{ OHMS}$
500 VOLTS

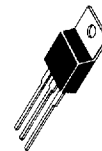


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	500	Vdc
Drain-Gate Voltage ($R_{GS} = 1 \text{ M}\Omega$)	V_{DGR}	500	Vdc
Gate-Source Voltage — Continuous	V_{GS}	± 20	Vdc
— Non-repetitive ($t_p \leq 50 \mu s$)	V_{GSM}	± 40	Vpk
Drain Current			Adc
Continuous	I_D	3	
Pulsed	I_{DM}	10	
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	75	Watts
Derate above $25^\circ C$		0.6	W/ $^\circ C$
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150	$^\circ C$

THERMAL CHARACTERISTICS

Thermal Resistance			$^\circ C/W$
Junction to Case	$R_{\theta JC}$	1.67	
Junction to Ambient TO-220	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	260	$^\circ C$



CASE 221A-06
TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

M1P3N50

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0, I_D = 0.25 \text{ mA}$)	$V_{(BR)DSS}$	500	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = \text{Rated } V_{DSS}, V_{GS} = 0$) ($V_{DS} = 0.8 \text{ Rated } V_{DSS}, V_{GS} = 0, T_J = 125^\circ\text{C}$)	I_{DSS}	—	0.2 1	mAdc
Gate-Body Leakage Current, Forward ($V_{GSF} = 20 \text{ Vdc}, V_{DS} = 0$)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse ($V_{GSR} = 20 \text{ Vdc}, V_{DS} = 0$)	I_{GSSR}	—	100	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1 \text{ mA}$) $T_J = 100^\circ\text{C}$	$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10 \text{ Vdc}, I_D = 1.5 \text{ Adc}$)	$R_{DS(on)}$	—	3	Ohms
Drain-Source On-Voltage ($V_{GS} = 10 \text{ V}$) ($I_D = 3 \text{ Adc}$) ($I_D = 1.5 \text{ Adc}, T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	—	9 7	Vdc
Forward Transconductance ($V_{DS} = 10 \text{ V}, I_D = 1.5 \text{ A}$)	g_{FS}	1	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ $f = 1 \text{ MHz})$ See Figure 11	C_{iss}	—	500	pF
Output Capacitance		C_{oss}	—	150	
Reverse Transfer Capacitance		C_{rss}	—	40	

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time	$(V_{DD} = 25 \text{ V}, I_D = 0.5 \text{ Rated } I_D$ $R_{gen} = 50 \text{ ohms})$ See Figures 9, 13 and 14	$t_{d(on)}$	—	25	ns
Rise Time		t_r	—	30	
Turn-Off Delay Time		$t_{d(off)}$	—	90	
Fall Time		t_f	—	50	
Total Gate Charge	$(V_{DS} = 0.8 \text{ Rated } V_{DSS},$ $I_D = \text{Rated } I_D, V_{GS} = 10 \text{ V})$ See Figure 12	Q_g	16 (Typ)	20	nC
Gate-Source Charge		Q_{gs}	10 (Typ)	—	
Gate-Drain Charge		Q_{gd}	10 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS*

Forward On-Voltage	$(I_S = \text{Rated } I_D$ $V_{GS} = 0)$	V_{SD}	1.1 (Typ)	1.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	500 (Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE (TO-220)

Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L_d	3.5 (Typ) 4.5 (Typ)	—	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)	L_s	7.5 (Typ)	—	

*Pulse Test. Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL ELECTRICAL CHARACTERISTICS

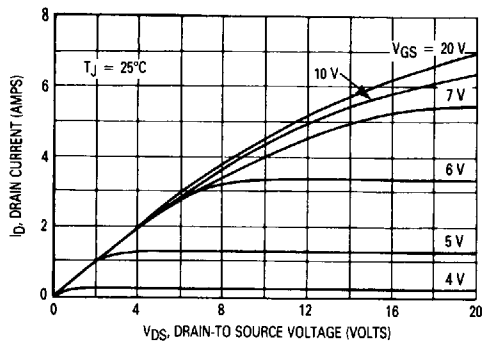


Figure 1. On-Region Characteristics

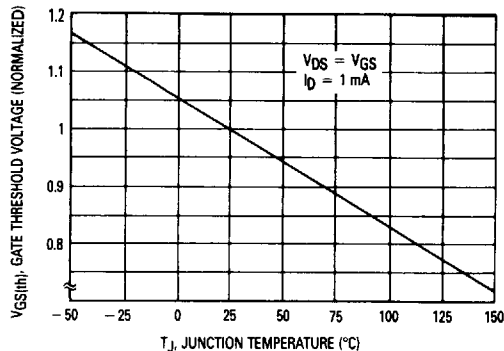


Figure 2. Gate-Threshold Voltage Variation With Temperature

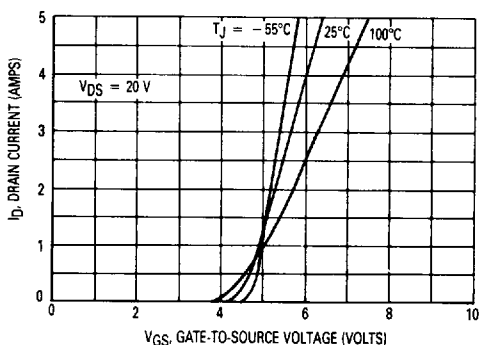


Figure 3. Transfer Characteristics

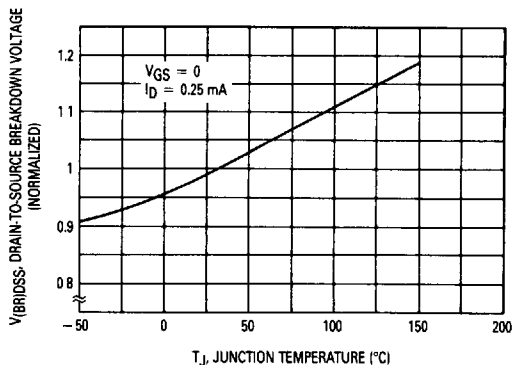


Figure 4. Breakdown Voltage Variation With Temperature

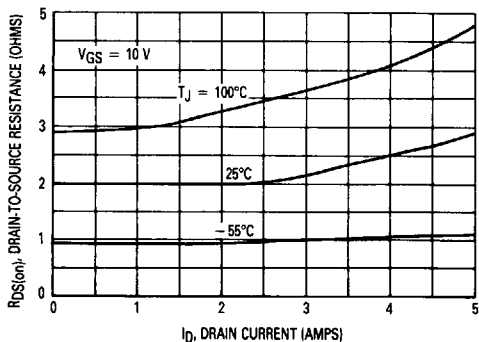


Figure 5. On-Resistance versus Drain Current

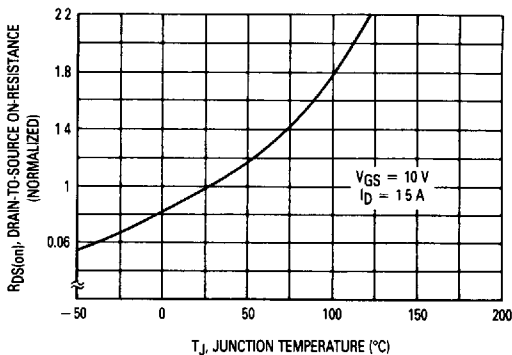


Figure 6. On-Resistance Variation With Temperature

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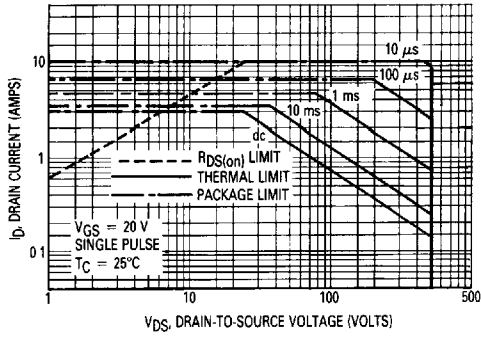


Figure 7. Maximum Rated Forward Biased Safe Operating Area

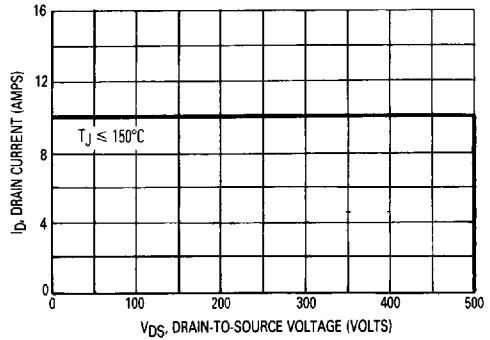


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_J(\text{max}) - T_C}{R_{\theta JC}}$$

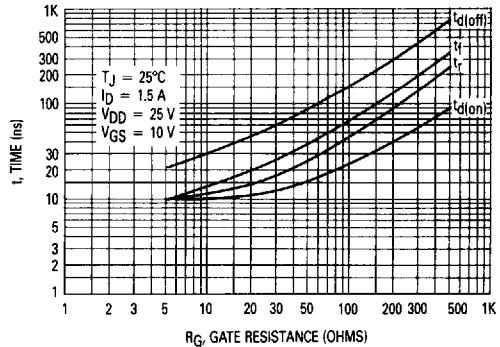


Figure 9. Resistive Switching Time Variation versus Gate Resistance

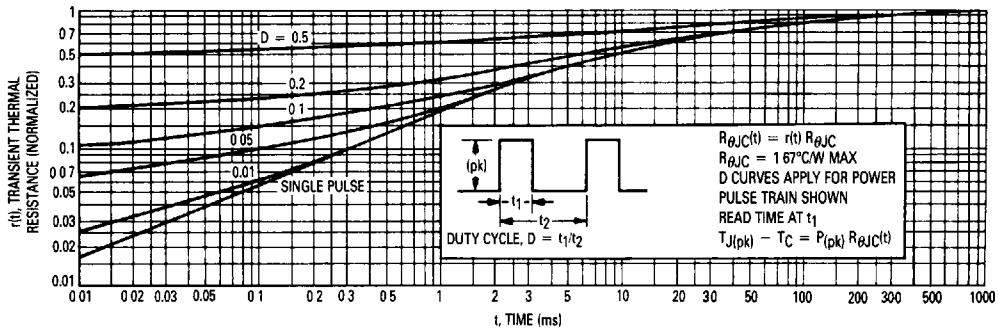


Figure 10. Thermal Response

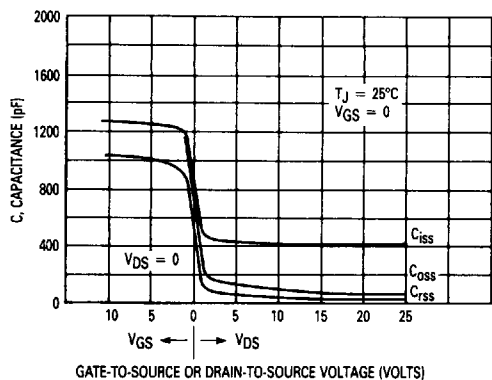


Figure 11. Capacitance Variation

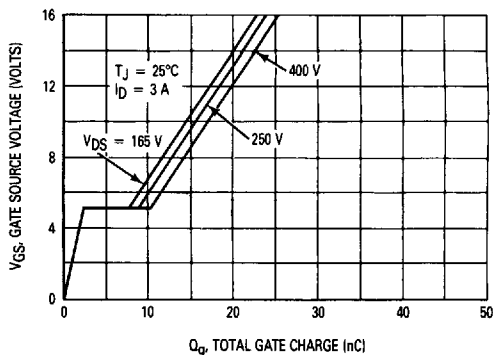


Figure 12. Gate Charge versus Gate-to-Source Voltage

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RESISTIVE SWITCHING

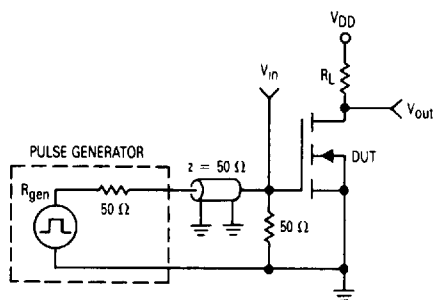


Figure 13. Switching Test Circuit

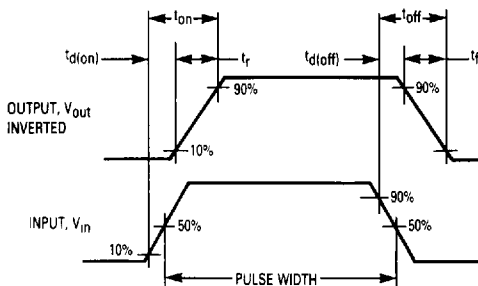


Figure 14. Switching Waveforms

PACKAGE OUTLINE DIMENSIONS AND FOOTPRINTS (continued)

SEATING PLANE -T-

STYLE 5
PIN 1 GATE
2 DRAIN
3 SOURCE
4 DRAIN

NOTES
1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M 1982
2 CONTROLLING DIMENSION INCH
3 DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.64	0.018	0.025
K	12.70	14.27	0.500	0.562
L	1.15	1.52	0.045	0.060
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-06 (TO-220AB)

SEATING PLANE -T-

STYLE 1
PIN 1 GATE
2 DRAIN
3 SOURCE

NOTES
1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M 1982
2 CONTROLLING DIMENSION INCH
3 221D 01 OBSOLETE, NEW STANDARD 221D 02

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.78	15.97	0.621	0.629
B	10.01	10.21	0.394	0.402
C	4.80	4.80	0.189	0.189
D	0.67	0.66	0.026	0.024
F	3.08	3.27	0.121	0.129
G	2.54 BSC	—	0.100 BSC	—
H	3.13	3.27	0.123	0.129
J	0.46	0.64	0.018	0.025
K	12.70	14.27	0.500	0.562
L	1.14	1.52	0.045	0.060
N	5.08 BSC	—	0.200 BSC	—
Q	3.21	3.40	0.126	0.134
R	2.72	2.81	0.107	0.111
S	2.44	2.64	0.096	0.104
U	6.58	6.78	0.259	0.267

0.25 (0.010) (M) B(M) Y

CASE 221D-02 (ISOLATED TO-220 TYPE)

SEATING PLANE -T-

STYLE 5
PIN 1 GATE
2 MIRROR
3 DRAIN
4 KELVIN
5 SOURCE

NOTES
1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M 1982
2 CONTROLLING DIMENSION INCH
3 314B 01 AND 02 OBSOLETE, NEW STANDARD 314B 03
STYLE 1 THRU 4 OBSOLETE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.528	15.570	0.572	0.613
B	9.906	10.541	0.390	0.415
C	4.318	4.572	0.170	0.180
D	0.635	0.965	0.025	0.038
E	1.169	1.397	0.046	0.055
F	21.590	23.749	0.850	0.936
G	1.702 BSC	—	0.067 BSC	—
H	3.800	5.080	0.149	0.200
J	0.381	0.535	0.015	0.021
K	22.860	27.940	0.900	1.100
L	8.052	8.398	0.317	0.370
N	7.674	8.800	0.310	0.346
Q	3.556	3.937	0.140	0.155
U	11.888	12.827	0.468	0.505
V	4.689	5.842	0.185	0.230
W	2.286	2.794	0.090	0.110

0.356 (0.014) (M) T Q (M)

CASE 314B-03 (5-PIN TO-220)

