MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

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MTM8P25
MTP8P25

Designer's Data Sheet

Power Field Effect Transistors

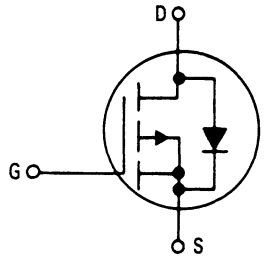
P-Channel Enhancement Mode Silicon Gate TMOS

TMOS™

TMOS POWER FETs
8 AMPERES
$r_{DS(on)}$ = 2 OHMS
250 VOLTS

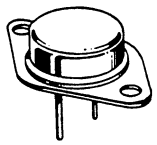
These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and motor drives.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designers Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$, and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



MAXIMUM RATINGS

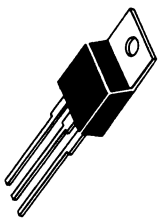
Rating	Symbol	MTM8P25	MTP8P25	Unit
Drain-Source Voltage	V_{DSS}	250		Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	250		Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current — Continuous Pulsed	I_D I_{DM}	8 24		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C



MTM8P25
CASE 1-04
TO-204AA
(TO-3)

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67		°C/W
Junction to Ambient	$R_{\theta JA}$	30	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275		°C



MTP8P25
CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	250	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 0.2 1	mAdc

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(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C	$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4 Adc)	$r_{DS(on)}$	—	2	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 8 Adc) (I_D = 4 Adc, T_J = 100°C)	$V_{DS(on)}$	— —	18 16	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 4 A)	g_{fs}	3	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	2200	pF
Output Capacitance		C_{oss}	—	500	
Reverse Transfer Capacitance		C_{rss}	—	300	

SWITCHING CHARACTERISTICS* (T_J = 100°C)

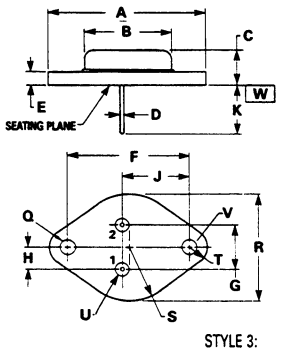
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 11, 12 and 13	$t_{d(on)}$	—	40	ns
Rise Time		t_r	—	100	
Turn-Off Delay Time		$t_{d(off)}$	—	160	
Fall Time		t_f	—	90	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 10	Q_g	20 (Typ)	40	nC
Gate-Source Charge		Q_{gs}	10 (Typ)	—	
Gate-Drain Charge		Q_{gd}	10 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS*

Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0) See Figures 16 and 17	V_{SD}	3 (Typ)	5	Vdc
Forward Turn-On Time		t_{on}	200 (Typ)	—	ns
Reverse Recovery Time		t_{rr}	250 (Typ)	—	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS

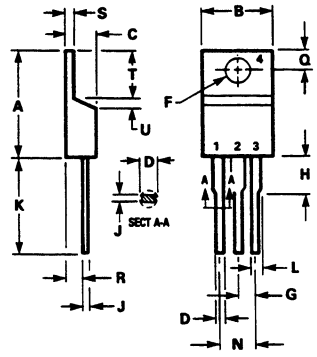


NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q: ⌖ ϕ 0.25 (0.010) Ⓜ W V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS: ⌖ ϕ 0.30 (0.012) Ⓜ W V Ⓜ Q Ⓜ

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

CASE 1-04
TO-204AA
(TO-3)



NOTES:
1. DIMENSION H APPLIES TO ALL LEADS.
2. DIMENSION L APPLIES TO LEADS 1 AND 3.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.60	15.75	0.575	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.93	0.110	0.155
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.14	—	0.045	—
Z	—	2.03	—	0.080

STYLE 5:
PIN 1. GATE 3. SOURCE
2. DRAIN 4. DRAIN

CASE 221A-02
TO-220AB

TYPICAL ELECTRICAL CHARACTERISTICS

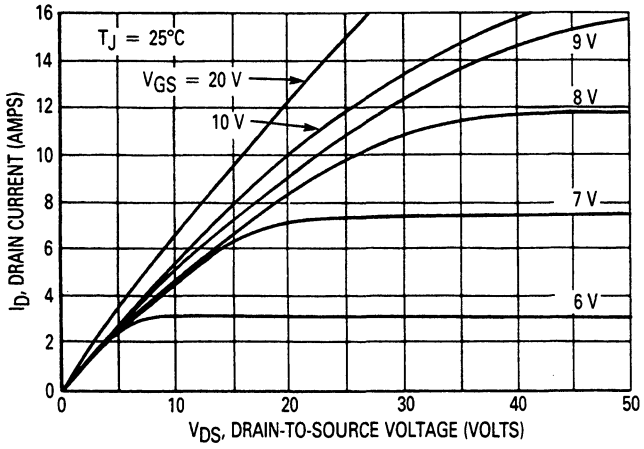


Figure 1. On-Region Characteristics

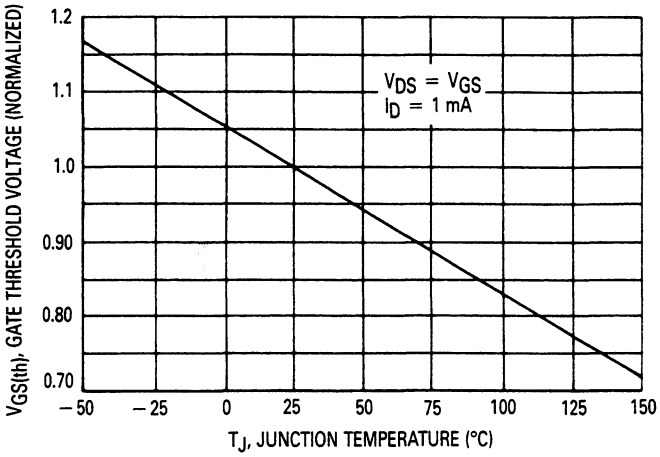


Figure 2. Gate-Threshold Voltage Variation With Temperature

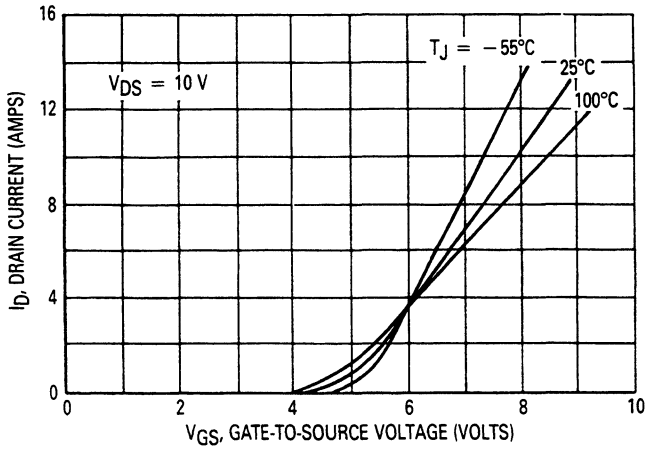


Figure 3. Transfer Characteristics

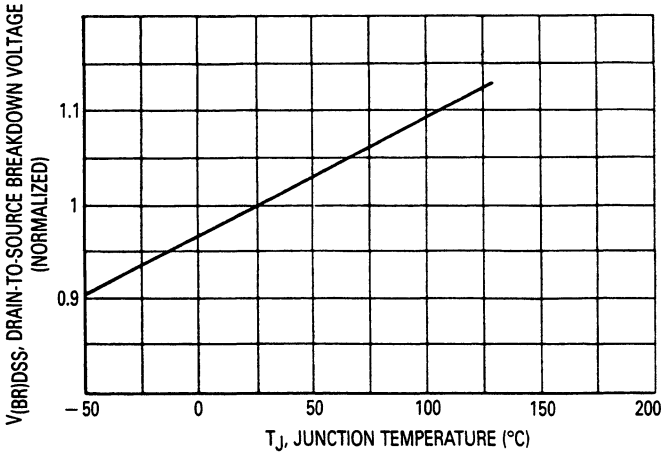


Figure 4. Normalized Breakdown Voltage versus Temperature

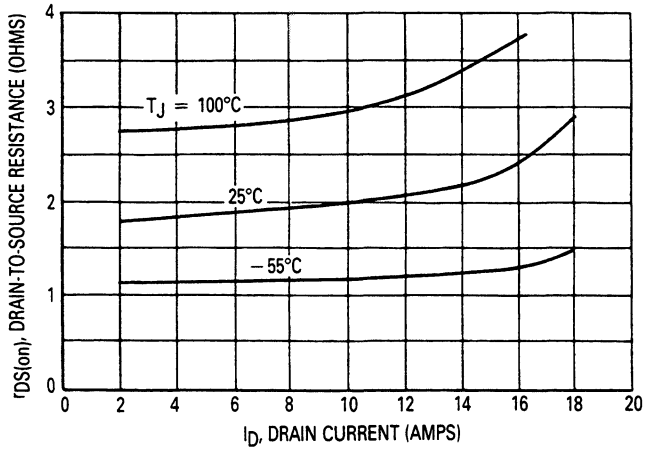


Figure 5. On-Resistance versus Drain Current

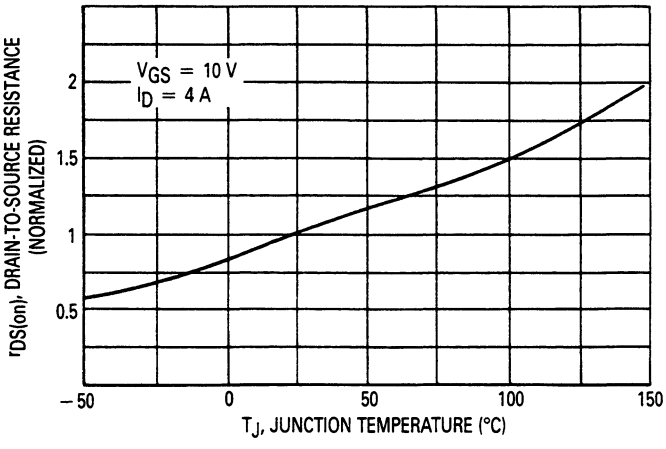


Figure 6. Normalized On-Resistance versus Temperature

SAFE OPERATING AREA INFORMATION

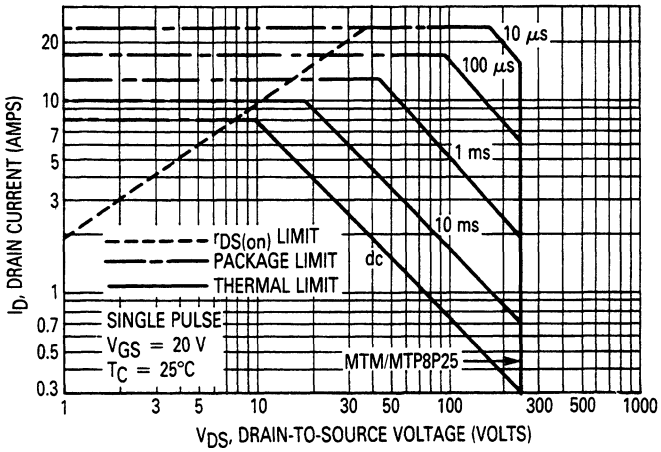


Figure 7. Maximum Rated Forward Bias Safe Operating Area

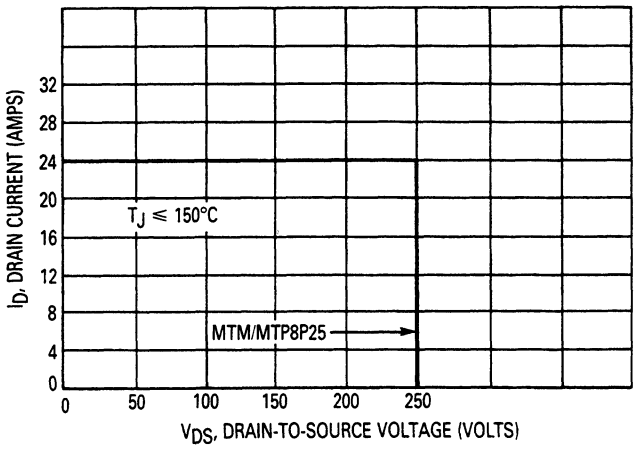


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

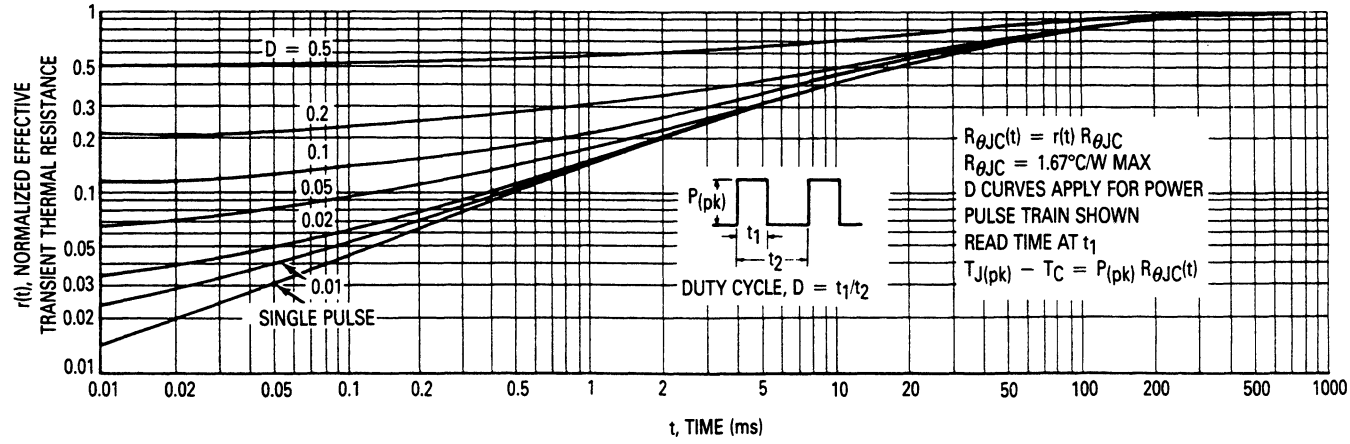


Figure 9. Thermal Response

RESISTIVE SWITCHING

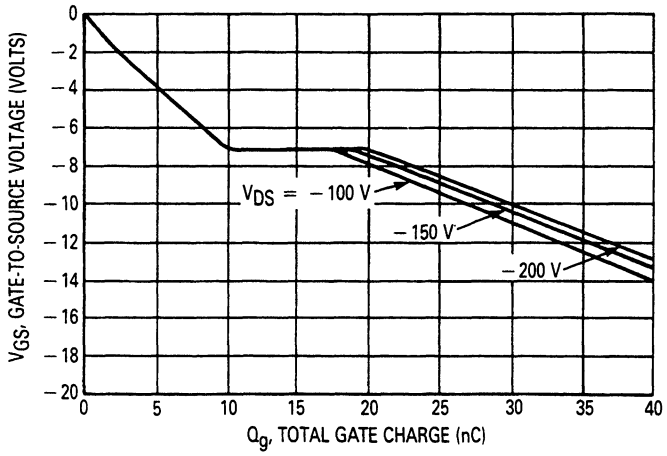


Figure 10. Gate Charge versus Gate-To-Source Voltage

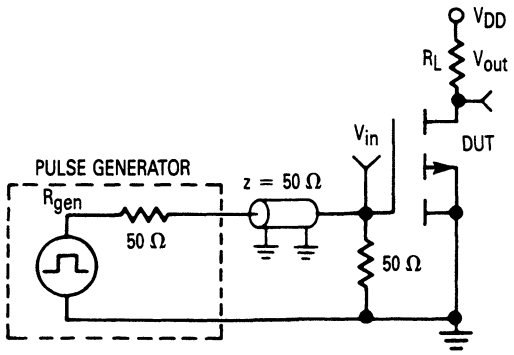


Figure 11. Switching Test Circuit

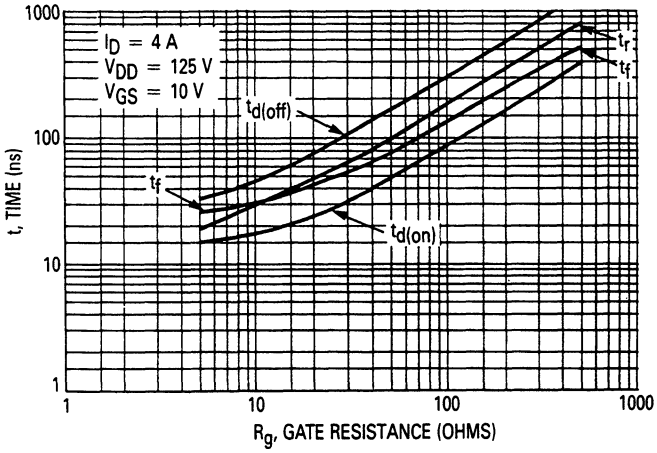


Figure 12. Resistive Switching versus Gate Resistance

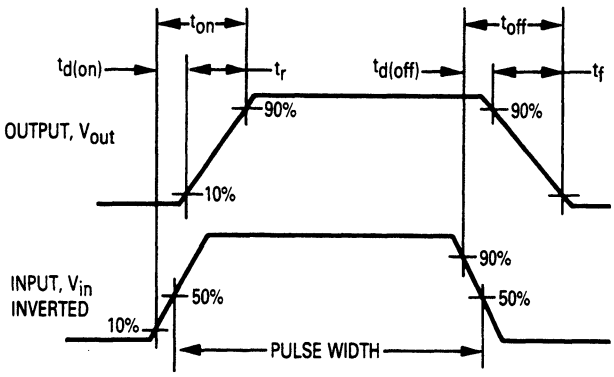


Figure 13. Switching Waveforms

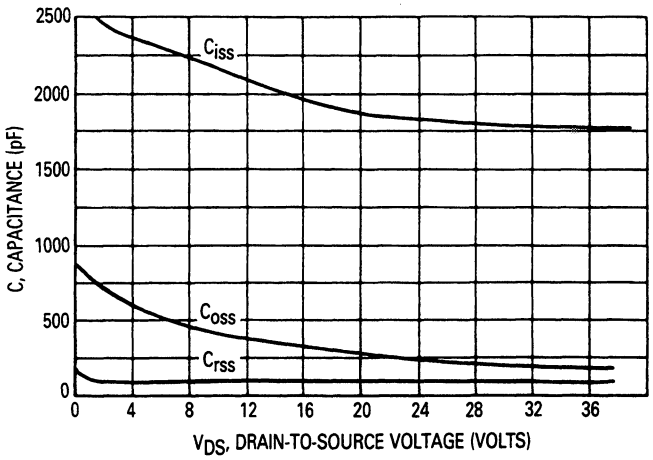


Figure 14. Capacitance Variation

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TMOS SOURCE-TO-DRAIN DIODE CHARACTERISTICS

In the fabrication of a TMOS FET, a diode is formed across the source-to-drain terminals as shown in Figure 15. Reversal of the drain voltage will cause current flow in the reverse direction. This diode may be used in circuits requiring external fast recovery diodes, therefore, typical characteristics of the on voltage, forward turn-on and reverse recovery times are given.

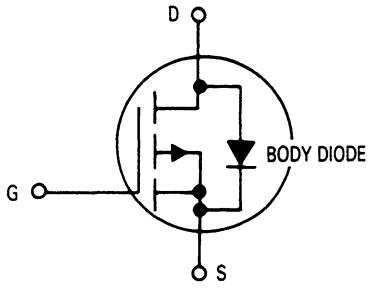

Figure 15. TMOS FET With Source-To-Drain Diode

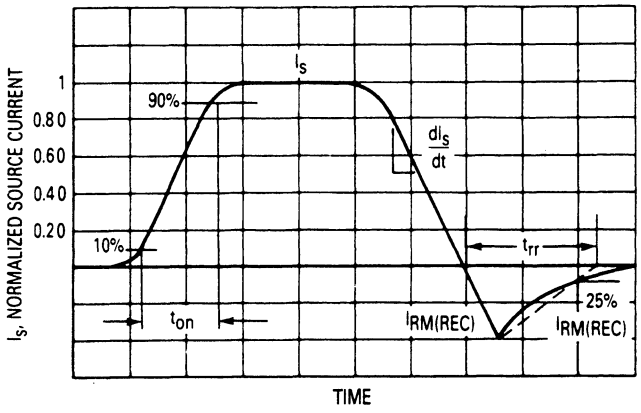

Figure 16. Diode Switching Waveform

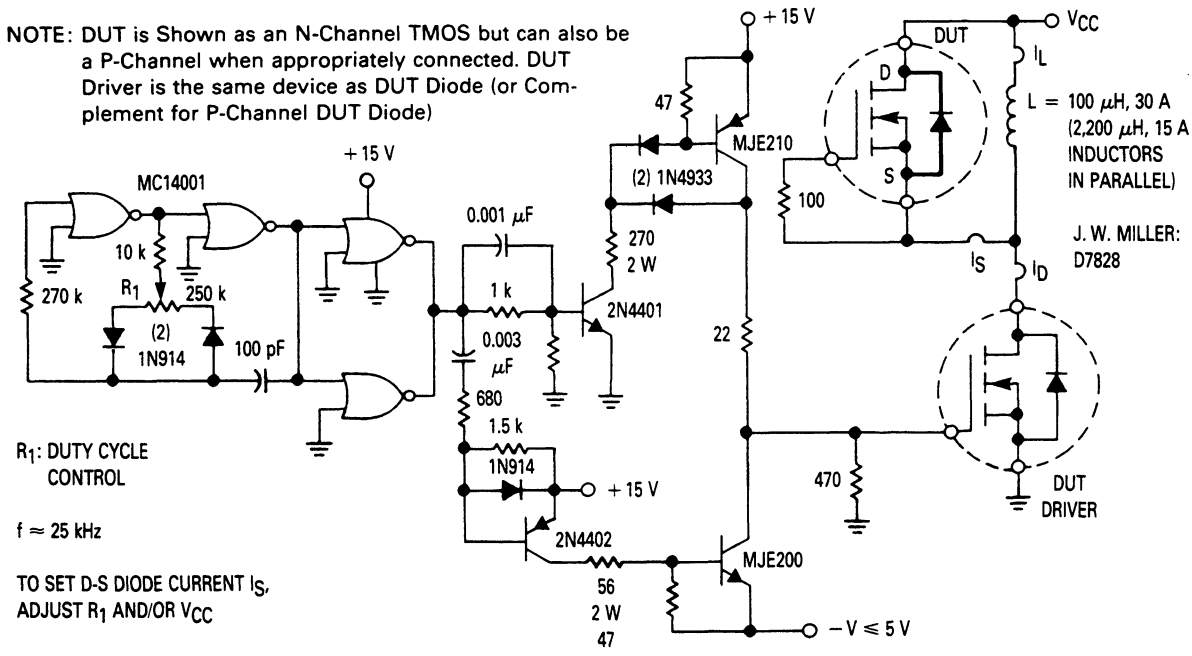

Figure 17. TMOS Diode Switching Test Circuit

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