MYSON TECHNOLOGY

MTV048 (Rev 0.9)

On-Screen-Display Controller for CRT/LCD Monitor

FEATURES

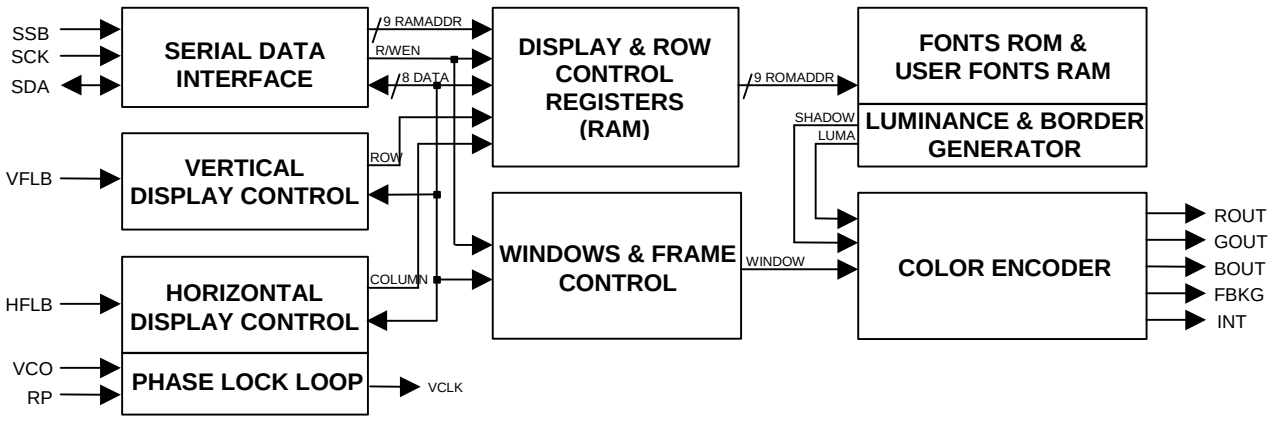
- Software control for CRT/LCD applications.
- Full screen self-test pattern generator with programmable pattern color.
- On-chip PLL circuitry (CRT) or external pixel clock input (LCD) up to 150 MHz.
- Horizontal SYNC input up to 150 KHz.
- Programmable horizontal resolutions up to 1524 dots per display line.
- Full screen display consists of 15 (rows) by 30 (columns).
- 12x16 or 12x18 dot matrix selection.
- A total of 384 fonts including 360 standard fonts, 16 multi-color fonts and 8 user fonts.
- 8 color selections for character foreground, background and window color.
- Character button boxes with programmable box length.
- Character bordering, shadowing and blinking effect for display.
- Full-screen character double width control.
- Double character height and/or width control per row.
- Programmable positioning for display screen center.
- Row to row spacing control per row to avoid expansion distortion.
- 4 programmable background windows with multi-level operation and programmable shadow width/height/color.
- Software clear bit for full-screen erasing.
- Programmable adaptive approach to handle H, V sync collision automatically by hardware.
- Fade-in/fade-out or blend-in/blend-out effects.
- Compatible with SPI bus or I^2C interface with address 7AH (slave address is mask option).
- 5V or 3.3V power supply.
- 16-pin PDIP/SOP package.

GENERAL DESCRIPTION

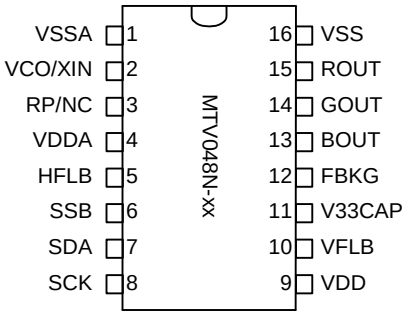
MTV048 is designed for monitor applications to display built-in fonts onto monitor screens. The display operation occurs by transferring data and controls information from the micro controller to RAM through a serial data interface. It can execute a full-screen display automatically, as well as specific functions such as character background, bordering, shadowing, blinking, double height and width, font-by-font color control, button boxes, frame positioning, frame size control by character height and row-to-row spacing, horizontal display resolution, full-screen erasing, fade-in/fade-out effect, windowing effect, shadowing on window and full-screen self-test pattern generator.

MTV048 provides 384 fonts including 360 standard fonts, 16 multi-color fonts and 8 user fonts and 2 font sizes, 12x16 or 12x18 for more efficacious applications. The full OSD menu is formed by 15 rows x 30 columns, which can be positioned anywhere on the monitor screen by changing vertical or horizontal delay.

BLOCK DIAGRAM



1.0 PIN CONNECTION



2.0 PIN DESCRIPTIONS

Name	I/O	Pin NO.	Descriptions
VSS	-	1	**Analog ground.** This ground pin is used for internal analog circuitry.
VCO / XIN	I/O	2	**Voltage control oscillator (bit LCD = 0).** This pin is used to control the internal oscillator frequency by DC voltage input from external low pass filter. **Pixel clock input (bit LCD = 1).** This is a clock input pin. MTV048 can be driven by an external pixel clock source for all the logic inside. The frequency of XIN must be the integral time of pin HFLB.
RP / NC	I/O	3	**Bias Resistor (bit LCD = 0).** The bias resistor is used to regulate the appropriate bias current for internal oscillator to resonate at specific dot frequency. **No connection (bit LCD = 1).**
VDDA	-	4	**Analog power supply.** Positive 5V / 3.3V DC supply for internal analog circuitry. And a 0.1uF decoupling capacitor should be connected across to VDDA and VSSA.
HFLB	I	5	**Horizontal input.** This pin is used to input the horizontal synchronizing signal. It is a leading edge triggered and has an internal pull-up resistor.
SSB	I	6	**Serial interface enable.** It is used to enable the serial data and is also used to select the operation of I^2C or SPI bus. If this pin is left floating, I^2C bus would be enabled. Otherwise the SPI bus is enabled.
SDA	I	7	**Serial data input.** The external data transfer through this pin to internal display registers and control registers. It has an internal pull-up resistor.
SCK	I	8	**Serial clock input.** The clock-input pin is used to synchronize the data transfer. It has an internal pull-up resistor.
VDD	-	9	**Digital power supply.** Positive 5V / 3.3V DC supply for internal digital circuitry and a 0.1uF decoupling capacitor should be connected across to VDD and VSS.
VFLB	I	10	**Vertical input.** This pin is used to input the vertical synchronizing signal. It is leading triggered and has an internal pull-up resistor.

V33CAP	I/O	11	**3.3V Regulator Capacitor connection.** Connect a decoupling capacitor to VSS pin when DC supply = 5V, or connect to 3.3V directly when DC supply = 3.3V.
FBKG	O	12	**Fast Blanking output.** It is used to cut off external R, G, B signals of VGA while this chip is displaying characters or windows.
BOUT	O	13	**Blue color output.** It is a blue color video signal output. And it is a DAC output if bit LCD = 0 or CMOS output if bit LCD =1.
GOUT	O	14	**Green color output.** It is a green color video signal output. And it is a DAC output if bit LCD = 0 or CMOS output if bit LCD =1.
ROUT	O	15	**Red color output.** It is a red color video signal output. And it is a DAC output if bit LCD = 0 or CMOS output if bit LCD =1.
VSS	-	16	**Digital ground.** This ground pin is used for internal digital circuitry.

3.0 FUNCTIONAL DESCRIPTIONS

3.1 Serial Data Interface

The serial data interface receives data transmitted from an external controller. There are 2 types of buses, which can be accessed through the serial data interface. One is SPI bus and the other is I²C bus.

3.1.1 SPI bus

While SSB pin is pulled to "high" or "low" level, the SPI bus operation is selected. And a valid transmission should start pulling SSB to "low" level, enabling MTV048 to receiving mode, and retain at "low" level till the last cycle for a complete data packet transfer. The protocol is shown in Figure 1.

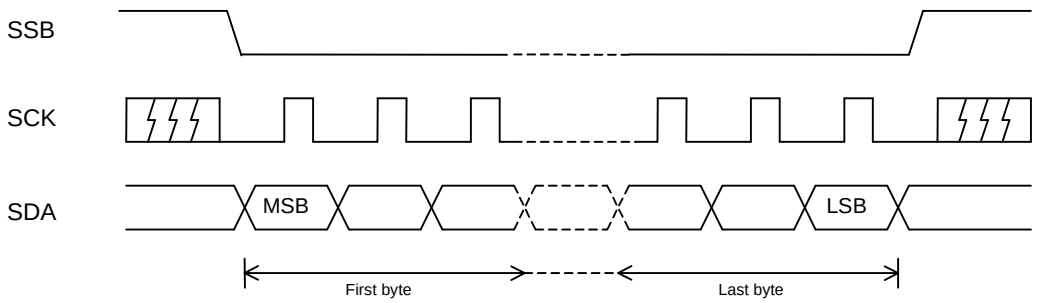


FIGURE 1. Data Transmission Protocol (SPI)

There are three transmission formats, shown as below:
Format (a) R - C - D → R - C - D → R - C - D .....
Format (b) R - C - D → C - D → C - D → C - D .....
Format (c) R - C - D → D → D → D → D → D .....
Where R=Row address, C=Column address, D=Display data

3.1.2 I²C bus

I²C bus operation is only selected when SSB pin is left floating. And a valid transmission should start writing the slave address 7AH to MTV048. The protocol is shown in Figure 2.

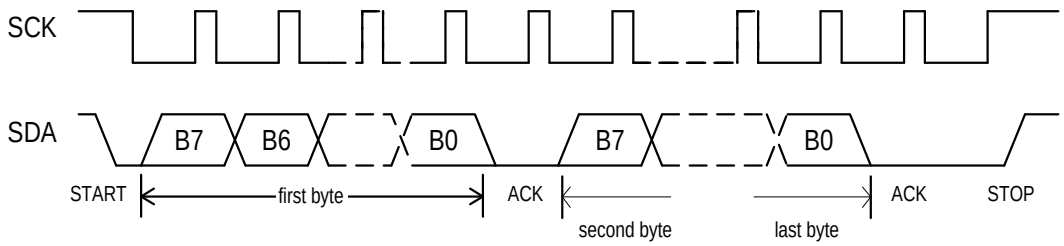


FIGURE 2. Data Transmission Protocol (I^2C)

There are three transmission formats for I^2C write mode, shown as below:
Format (a) S - R - C - D → R - C - D → R - C - D …..
Format (b) S - R - C - D → C - D → C - D → C - D …..
Format (c) S - R - C - D → D → D → D → D → D …..
Where S=Slave address, R=Row address, C=Column address, D=Display data

Each arbitrary length of data packet consists of 3 portions viz, Row address (R), Column address (C), and Display data (D). Format (a) is suitable for updating small amount of data, which will be allocated with a different row address and column address. Format (b) is recommended for updating data that has the same row address but a different column address. Massive data updating or full screen data change should use format (c) to increase transmission efficiency. The row and column address will be incremented automatically when the format (c) is applied. Furthermore, the undefined locations in display or user fonts RAM should be filled with dummy data.

TABLE 1. The Configuration of Transmission Formats

	Address	b7	b6	b5	b4	b3	b2	b1	b0	Format
Address Bytes of Display Reg.	Row	1	0	0	R4	R3	R2	R1	R0	a,b,c
	$Column_{ab}$	0	0	**D8**	C4	C3	C2	C1	C0	a,b
	$Column_c$	0	1	**D8**	C4	C3	C2	C1	C0	c
	Data	D7	D6	D5	D4	D3	D2	D1	D0	a,b,c
Attribute Bytes of Display Reg.	Row	1	0	1	R4	R3	R2	R1	R0	a,b,c
	$Column_{ab}$	0	0	x	C4	C3	C2	C1	C0	a,b
	$Column_c$	0	1	x	C4	C3	C2	C1	C0	c
	Data	D7	D6	D5	D4	D3	D2	D1	D0	a,b,c
User Fonts	Row	1	1	-	-	-	R2	R1	R0	a,b,c
	$Column_{ab}$	0	0	C5	C4	C3	C2	C1	C0	a,b
	$Column_c$	0	1	C5	C4	C3	C2	C1	C0	c
	Data	D7	D6	D5	D4	D3	D2	D1	D0	a,b,c

There are 3 types of data, which should be accessed through the serial data interface. One is **ADDRESS** bytes of display registers, another is **ATTRIBUTE** bytes of display registers, and the other is **user fonts** RAM data. The protocols are all the same except the bit6 and bit5 of row address and the bit5 of column address. The MSB (b7) is used to distinguish row and column addresses when transferring data from external controller. The bit6 of row address is used to distinguish display registers and user fonts RAM data and the bit6 of column address is used to differentiate the column address for format (a), (b) and format (c) respectively. Bit5 of row address for display register is used to distinguish ADDRESS byte when it is set to "0" and ATTRIBUTE byte when it is set to "1". And **at address bytes, bit5 of column address is the MSB (bit8) and data bytes are the 8 LSB (bit7~bit0) of display fonts address** to save half MCU memory for true 392 fonts display. So each one of the 384 fonts can be displayed at the same time. See Table 1. And for format (c), since D8 is filled while program column address of address bytes, the continued data will be the same bank of upper 128 fonts or lower 256 fonts until program column address is of address bytes again.

The data transmission is permitted to change from format (a) to format (b) and (c), or from format (b) to format (a), but not from format (c) back to format (a) and (b). The alternation between transmission formats is configured as the state diagram shown in Figure 3 .

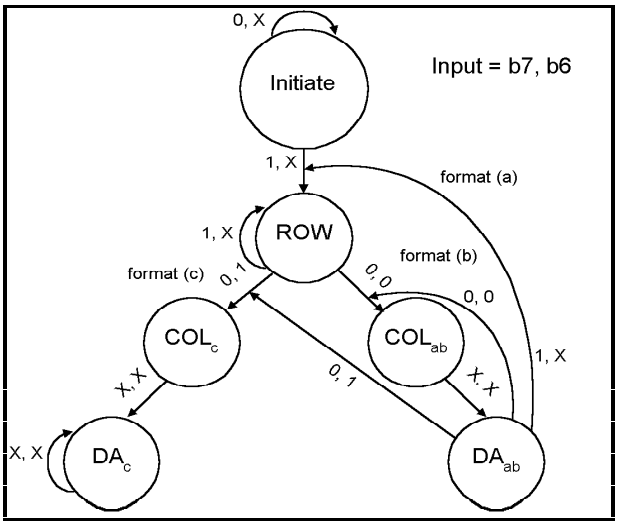


FIGURE 3. Transmission State Diagram

3.2 Address Bus Administrator

The administrator manages bus address arbitration of internal registers or user fonts RAM during external data write in. The external data write through serial data interface to registers must be synchronized by internal display timing. In addition, the administrator also provides automatic increment to address bus when external write using format (c).

3.3 Vertical Display Control

The vertical display control can generate different vertical display sizes for most display standards in current monitors. The vertical display size is calculated with the information of double character height bit (CHS), vertical display height control register (CH6-CH0). The algorithms of repeating character line display are shown as Table 2 and Table 3. The range of programmable vertical size is 270 lines to 2130 lines maximum.

The vertical display center for full screen display could be figured out according to the information of vertical starting position register (VERTD) and VFLB input. The vertical delay starting from the leading edge of VFLB is calculated by using the following equation:

Vertical delay time = (VERTD * 4 + 1) * H Where H = one horizontal line display time

TABLE 2. Repeat Line Weight of Character

CH6 – CH0	Repeat Line Weight
CH6, CH5 = 11	+18*3
CH6, CH5 = 10	+18*2
CH6, CH5 = 0x	+18
CH4 = 1	+16
CH3 = 1	+8
CH2 = 1	+4
CH1 = 1	+2
CH0 = 1	+1

TABLE 3. Repeat Line Number of Character

Repeat Line Weight	Repeat Line #																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
+1	-	-	-	-	-	-	-	-	v	-	-	-	-	-	-	-	-	-
+2	-	-	-	-	v	-	-	-	-	-	-	-	v	-	-	-	-	-
+4	-	-	v	-	-	-	v	-	-	-	v	-	-	-	v	-	-	-
+8	-	v	-	v	-	v	-	v	-	v	-	v	-	v	-	v	-	-
+16	-	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	-
+17	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	-
+18	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v

Note: "v" means the *n*th line in the character would be repeated once, while "-" means the *n*th line in the character would not be repeated.

3.4 Horizontal Display Control

The horizontal display control is used to generate control timing for horizontal display based on double character width bit (CWS), horizontal positioning register (HORD), horizontal resolution register (HORR), and HFLB input. A horizontal display line consists of (HORR*12) dots which include 360 dots for 30 display characters and the remaining dots for blank region. The horizontal delay starting from HFLB leading edge is calculated by using the following equation:

For CRT: Horizontal delay time = (HORD * 6 + 49) * P - phase error detection pulse width
Where P = One pixel display time = One horizontal line display time / (HORR*12)

For LCD: Horizontal delay time = (HORD * 6 + 49) * P
Where P = One XIN pixel display time

3.5 Phase lock loop (PLL)

On-chip PLL generates system clock timing (VCLK) by tracking the input HFLB and horizontal resolution register (HORR). The frequency of VCLK is determined by the following equation:

VCLK Freq. = HFLB Freq. * HORR * 12

The VCLK frequency ranges from 6MHz to 150MHz selected by (VCO1, VCO0). In addition, when HFLB input is not present to MTV048, the PLL will generate a specific system clock, approximately 2.5MHz, by a built-in oscillator to ensure data integrity.

3.6 Display & Row Control Registers

The internal RAM contains display and row control registers. The display registers have 450 locations, which are allocated between (row 0, column 0) to (row 14, column 29), as shown in Figure 4. Each display register has its corresponding character address on ADDRESS byte, its corresponding background color, 1 blink bit and its corresponding color bits on ATTRIBUTE bytes. The row control register is allocated at column 30 for row 0 to row 14, it is used to set character size to each respective row. If double width character is chosen, only even column characters could be displayed on screen and the odd column characters will be hidden.

Row #	Column #		
	0 1 ... 28 29	30	31
0 1 13 14	Character ADDRESS Bytes of Display Registers	ROW CTRL REG	R E S E R V E D

FIGURE 4. ADDRESS Bytes of Display Registers Memory Map

Row #	Column #	
	0 1 ... 28 29	30 31
0 1 13 14	Character ATTRIBUTE Bytes of Display Registers	RESERVED

Row 15	Column #		
	0 ... 11	12 ... 22	23 ... 31
	WINDOW1 ~ WINDOW4	FRAME CTRL REG.	RESERVED

Row 16	Column #		
	0 ... 1	2 ... 4	5 ... 31
	WINDOW SHADOW COLOR	FRAME CTRL REG.	RESERVED

FIGURE 5. ATTRIBUTE Bytes of Display Registers Memory Map

ADDRESS Bytes:

Address registers, (ROW 0 ~ 14, COLUMN 0 ~ 29),

B8	B7	B6	B5	B4	B3	B2	B1	B0
CRADDR								
MSB								LSB

CRADDR - Define OSD character address from address 0 to 383.
= 0 ~ 359 ⇒ 360 standard ROM fonts.
= 360 ~ 367 ⇒ 8 user fonts.
= 368 ~ 383 ⇒ 16 multi-color ROM fonts.

Row control registers (ROW 0 ~ 14, COLUMN 30),

B7	B6	B5	B4	B3	B2	B1	B0
-	-	-	BOX	-	-	CHS	CWS

BOX - Select BGR, BGG, BGB or BOX2, BOX1, BOX0 of attributes bytes to the respective row.
= 0 ⇒ Background color bits BGR, BGG, BGB are selected.
= 1 ⇒ Button boxes bits BOX2, BOX1, BOX0 are selected.

CHS - Define double height character to the respective row.

CWS - Define double width character to the respective row. If double width character is chosen, only even

column characters could be displayed on screen and the odd column characters will be hidden.

ATTRIBUTE Bytes:
Attribute registers, (ROW 0 ~ 14, COLUMN 0 ~ 29),

B7	B6	B5	B4	B3	B2	B1	B0
-	BGR/BOX2	BGG/BOX1	BGB/BOX0	BLINK	R	G	B

BGR, BGG, BGB : These three bits define the background color for their individual relative address characters. If these three bits are set to (0, 0, 0), no background will be shown (transparent). Therefore, a total of 7 background colors can be selected.

BOX2-0 - Select the character button boxes format of its relative address character.
= 0, 0, 0 ⇒ Button boxes is disabled.
= 1, 0, 0 ⇒ Start of depressed button box which is more than 1 character button box.
= 1, 0, 1 ⇒ Start of depressed button box which is only 1 character button box.
= 1, 1, 0 ⇒ Start of raised button box which is more than 1 character button box.
= 1, 1, 1 ⇒ Start of raised button box which is only 1 character button box.
= 0, 1, 0 ⇒ Middle of button box.
= 0, 0, 1 ⇒ End of button box.

BLINK = 1 ⇒ Enable blink effect for its relative address character. And the blinking is alternate per 32 vertical frames.
= 0 ⇒ Disable blink effect for its relative address character.

R, G, B - These three bits are used to specify their individual relative address character foreground color.

3.7 Character Button Boxes Generator

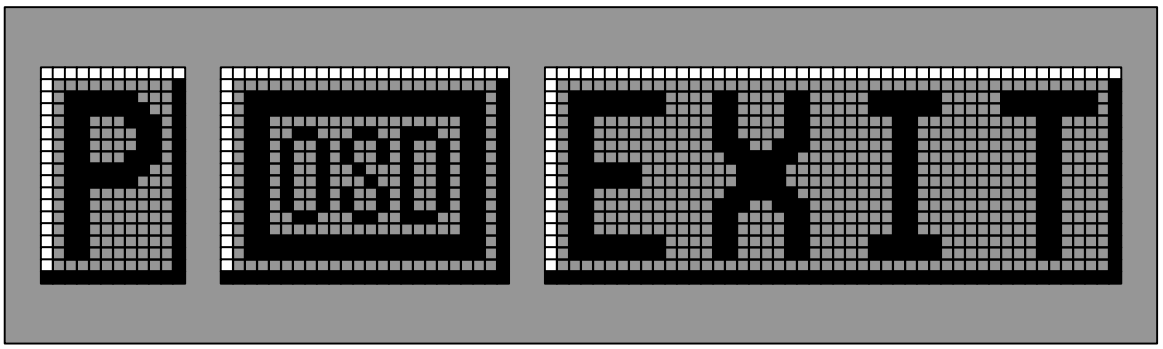
There are 4 character button box generators to generate 4 different types of button boxes including depressed button box with only 1 character, depressed button box with more than 1 character, raised button box with only 1 character, and raised button box with more than 1 character. The button boxes format is defined by (BOX2, BOX1, BOX0) bits of attribute bytes. And these bits are described as below:

1). (1, x, x) means the start of character button box, and than BOX1-0 bits define the format of button box.
2). (0, 1, 0) means the middle of character button box.
3). (0, 0, 1) means the end of character button box.

The length of button box is also software control by (BOX2, BOX1, BOX0) bits. For example, if there is 1 raised button box whose length is equal to 6 characters, these BOX2-0 bits will be (1, 1, 0), (0, 1, 0), (0, 1, 0), (0, 1, 0), (0, 1, 0), (0, 0, 1). And if there is 1 depressed button box whose length is equal to 4 characters, these BOX2-0 bits will be (1, 0, 0), (0, 1, 0), (0, 1, 0), (0, 0, 1). That is, (0, 1, 0) command's number defines the button box length. And only 1 byte, the attribute byte of button box start character, should be modified when changing button box type from raised button to depressed button, or vice versa. This is very easy and useful for software programming.

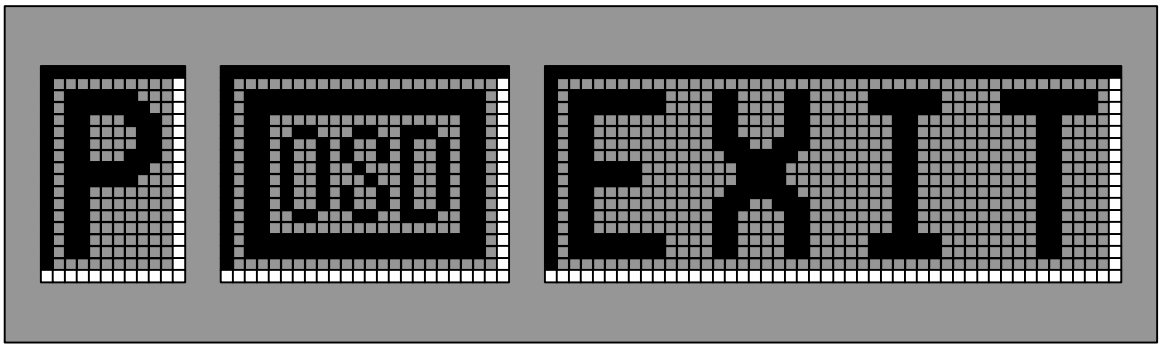
3.8 Character ROM

MTV048 character ROM contains 384 characters and symbols including 360 standard fonts, 8 user fonts and 16 multi-color fonts. The 360 standard fonts are located from address 0 to 359. The 8 user fonts are located from address 360 to 367.And the 16 multi-color fonts are located from address 368 to 383. Each character and symbol consists of 12x18 dots matrix.



B2~B0 = **1, 1, 1** **1, 1, 0** **0, 0, 1** **1, 1, 0** **0, 1, 0** **0, 1, 0** **0, 0, 1**

Raised Button Boxes



BOX2-0 = **1, 0, 1** **1, 0, 0** **0, 0, 1** **1, 0, 0** **0, 1, 0** **0, 1, 0** **0, 0, 1**

Depressed Button Boxes

FIGURE 6. Character Button Boxes

3.9 Multi-Color Font

The color fonts comprise three different R, G, B fonts. When the code of color font is accessed, the separate R/G/B dot pattern is output to corresponding R/G/B outputs. See Figure 7 for the sample displayed color font. Note: No black color can defined in color font, black window underline the color font can make the dots become black in color.

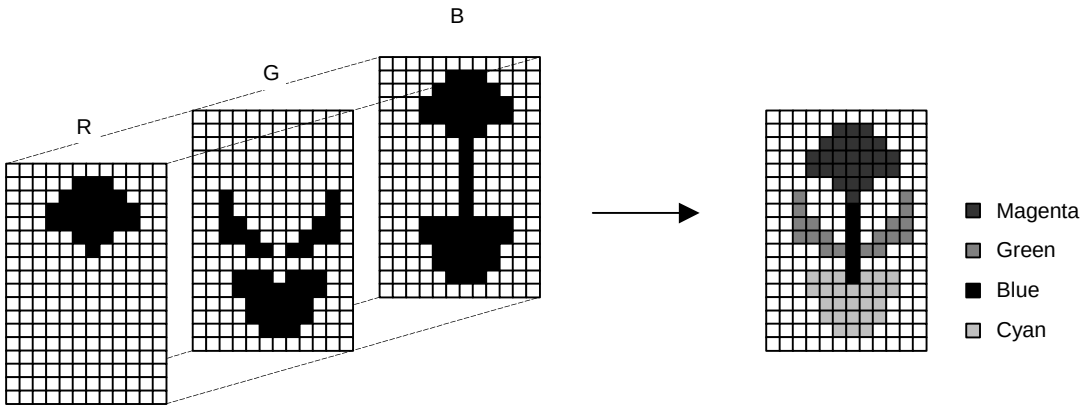


FIGURE 7. Example of Multi-color Font

TABLE 4. The Multi-color Font Color Selection

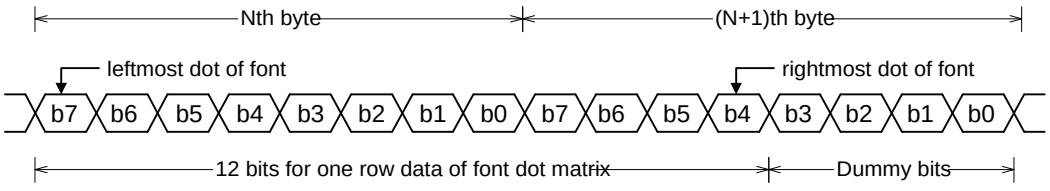
	R	G	B
Background Color	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0
Magenta	1	0	1
Yellow	1	1	0
White	1	1	1

3.10 User fonts RAM

The user fonts RAM have 288 locations, which are allocated between (row 0, column 0) to (row 7, column 35) to specify 8 user programmable fonts, as shown in Figure 6. Each user programmable font consists of 12x18 dot matrix which data are stored in 36 bytes registers. And each line of dot matrix consists of 2 bytes data, which include 4 dummy bits as shown in figure 7 and figure 8. For example, font 0 is stored in row 0 from column 0 to column 35 and font 1 is stored in row 1 from column 0 to column 35, etc.

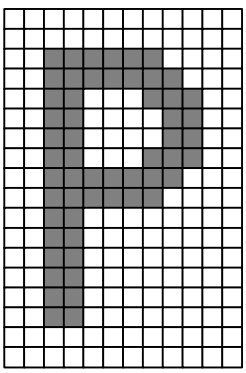
ROW #	COLUMN #	
	0 1 ... 34 35	36 ... 63
0 1 6 7	USER FONTS RAM	RESERVED

FIGURE 6. User Fonts RAM Memory Map



Where N=even number

FIGURE 7. Data Format of User Font Dot Matrix



Column#	Data	Column#	Data
0	00H	1	00H
2	00H	3	00H
4	3FH	5	00H
6	3FH	7	80H
8	31H	9	C0H
10	30H	11	C0H
12	30H	13	C0H
14	31H	15	C0H
16	3FH	17	80H
18	3FH	19	00H
20	30H	21	00H
22	30H	23	00H
24	30H	25	00H
26	30H	27	00H
28	30H	29	00H
30	30H	31	00H
32	00H	33	00H
34	00H	35	00H

FIGURE 8. Example of User Font Programming

3.11 Luminance & Border Generator

There are 3 shift registers included in the design which can shift out of luminance and border dots to color encoder. The bordering and shadowing feature is configured in this block. For bordering effect, the character will be enveloped with blackedge on four sides. For shadowing effect, the character is enveloped with blackedge for right and bottom sides only.

3.12 Window and Frame Control

The display frame position is completely controlled by the contents of VERTD and HORD. The window size and position control are specified in column 0 to 11 on row 15 of memory map, as shown in Figure 5. Window 1 has the highest priority, and window 4 is the least, when two windows are overlapping. More detailed information is described as follows:

1. Window control registers,
ROW 15

	b7	b6	b5	b4	b3	b2	b1	b0
Column 0,3,6 or 9	ROW START ADDR				ROW END ADDR			
	MSB			LSB	MSB			LSB

	b7	b6	b5	b4	b3	b2	b1	b0
Column 1,4,7 or 10	COLUMN START ADDR					WEN	-	WSHD
	MSB				LSB			

	b7	b6	b5	b4	b3	b2	b1	b0
Column 2,5,8 or 11	COLUMN END ADDR					R	G	B
	MSB				LSB			

START(END) ADDR - These addresses are used to specify the window size. It should be noted that when the start address is greater than the end address, the window would be disabled.

WEN - Enable the relative background window display.

WSHD - Enable shadowing on the relative window.

R, G, B - Specify the color of the relative background window.

2. Frame control registers,
ROW 15

	b7	b6	b5	b4	b3	b2	b1	b0
Column 12	VERTD							
	MSB							LSB

VERTD - Specify the starting position for vertical display. The total steps are 256, and the increment of each step is 4 Horizontal display lines. The initial value is 4 after power up.

	b7	b6	b5	b4	b3	b2	b1	b0
Column 13	HORD							
	MSB							LSB

HORD - Define the starting position for horizontal display. The total steps are 256, and the increment of each step is 6 dots. The initial value is 15 after power up.

Column 14	b7	b6	b5	b4	b3	b2	b1	b0
	-	CH6	CH5	CH4	CH3	CH2	CH1	CH0

CH6-CH0 - Define the character vertical height, the height is programmable from 18 to 71 lines. The character vertical height is at least 18 lines if the content of CH6-CH0 is less than 18. For example, when the content is " 2 ", the character vertical height is regarded as equal to 20 lines. And if the content of CH4-CH0 is greater than or equal to 18, it will be regarded as equal to 17. See Table 2 and Table 3 for detail description of this operation.

Column 15	b7	b6	b5	b4	b3	b2	b1	b0
	-	HORR						
		MSB						LSB

(This byte is used only for CRT monitor application.)

HORR - Specify the resolution of a horizontal display line, and the increment of each step is 12 dots. That is, the pixels' number per H line equal to HORR*12. It is recommended that HORR should be greater than or equal to 36 and smaller than 150M / (Hfreq*12). The initial value is 40 after power up.

Column 16	b7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	RSPACE				
				MSB				LSB

RSPACE - Define the row to row spacing in unit of horizontal line. That is, extra RSPACE horizontal lines will be appended below each display row, and the maximum space is 31 lines. The initial value is 0 after power up.

Column 17	b7	b6	b5	b4	b3	b2	b1	b0
	OSDEN	BSEN	SHADOW	FBEN	BLEND	WINCLR	RAMCLR	FBKGC

OSDEN - Activate the OSD operation when this bit is set to "1". The initial value is 0 after power up.

BSEN - Enable the bordering and shadowing effect.

SHADOW - Activate the shadowing effect if this bit is set, otherwise the bordering is chosen.

FBEN - Enable the fade-in/fade-out or blend-in/blend-out effect when OSD is turned on from off state or vice versa.

BLEND - Fade-in/fade-out or blend-in/blend-out effect select bit. Activate the blend-in/blend-out effect if this bit is set, otherwise the fade-in/fade-out function is chosen. This function roughly takes about 0.5 second to fully display the whole menu or to disappear completely.

WENCLR - Clear all WEN bits of window control registers when this bit is set to "1". The initial value is 0 after power up.

RAMCLR - Clear all ADDRESS bytes, BGR, BGG, BGB and BLINK bits of display registers when this bit is set to "1". The initial value is 0 after power up.

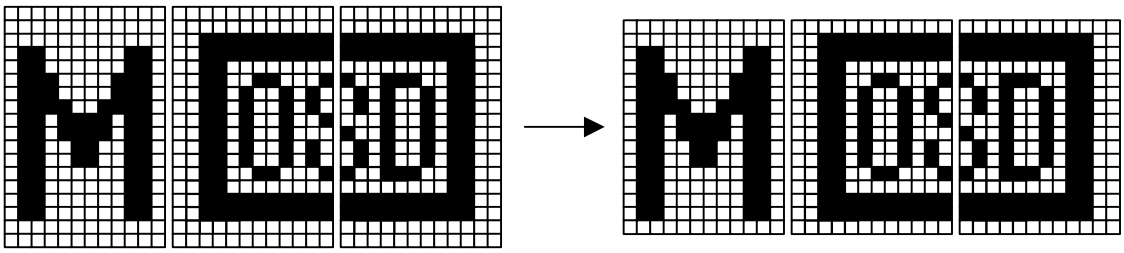
FBKGC - Define the output configuration for FBKG pin. When it is set to "0", the FBKG outputs high during the displaying of characters or windows, otherwise, it outputs high only during the displaying of character.

Column 18	b7	b6	b5	b4	b3	b2	b1	b0
	TRIC	FSS	-	SELVCL/DWE	HSP	VSP	VCO1/-	VCO0/-

(SELVCL, VCO1, VCO0 bits are used for CRT monitor applications only.)
(DWE bit is used only for LCD monitor applications.)

TRIC - Define the driving state of output pins ROUT, GOUT, BOUT and FBKG when OSD is disabled. That is, while OSD is disabled, these four pins will drive low if this bit is set to 1, otherwise these four pins are in high impedance state. The initial value is 0 after power up.

FSS - Font size selection.
= 1 ⇒ 12x18 font size is selected.
= 0 ⇒ 12x16 font size is selected.



Fonts designed to be 12x18 display **12x16 display if FSS=0; first and last lines omitted**

FIGURE 8. 12x18 and 12x16 Fonts

SELVCL - Enable auto detection for horizontal and vertical syncs input edge distortion to avoid unstable Vsync leading mismatch with Hsync signal while the bit is set to "1". The initial value is 0 after power up.

HSP - = 1 ⇒ Accept positive polarity Hsync input.
= 0 ⇒ Accept negative polarity Hsync input.

VSP - = 1 ⇒ Accept positive polarity Vsync input.
= 0 ⇒ Accept negative polarity Vsync input.

VCO1, VCO0 - Select the appropriate curve partitions of VCO frequency to voltage based on HFLB input and horizontal resolution register (HORR). And there are different curve partitions based on different application resister value on pin 3 (pin RP) as below:

(i) 5.6K ohm:	(ii) 3.3K ohm:
= (0, 0) ⇒ 6MHz < Pixel rate ≤ 24MHz	= (0, 0) ⇒ 6MHz < Pixel rate ≤ 28MHz
= (0, 1) ⇒ 24MHz < Pixel rate ≤ 48MHz	= (0, 1) ⇒ 28MHz < Pixel rate ≤ 56MHz
= (1, 0) ⇒ 48MHz < Pixel rate ≤ 96MHz	= (1, 0) ⇒ 56MHz < Pixel rate ≤ 112MHz
= (1, 1) ⇒ 96MHz < Pixel rate ≤ 128MHz	= (1, 1) ⇒ 112MHz < Pixel rate ≤ 150MHz

Where Pixel rate = VCLK Freq = HFLB Freq * HORR * 12
The initial value is (0, 0) after power up.

Notes:

1. That is, if HORR is specified and RP resister = 3.3K ohm, then (VCO1, VCO0)
= (0, 0), if 6000/(HORR * 12) < HFLB Freq (KHz) ≤ 28000/(HORR * 12)
= (0, 1), if 28000/(HORR * 12) < HFLB Freq (KHZ) ≤ 56000/(HORR * 12)
= (1, 0), if 56000/(HORR * 12) < HFLB Freq (KHZ) ≤ 112000/(HORR * 12)
= (1, 1), if 112000/(HORR * 12) < HFLB Freq (KHZ) ≤ 150000/(HORR * 12)
2. It is necessary to wait for the PLL to become stable while (i) the HORR register is changed; (ii) the (VCO1, VCO0) bits is changed; (iii) the horizontal signal (HFLB) is changed.
3. When PLL is unstable, do not write data in any address except Column 15,17,18 of Row 15. If data is written in any other address, a malfunction may occur.

Column 19	b7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	-	CSR	CSG	CSB

CSR, CSG, CSB - Define the color of bordering or shadowing on characters. The initial value is (0, 0, 0) after power up.

Column 20	b7	b6	b5	b4	b3	b2	b1	b0
	FSW	-	-	-	-	FSR	FSG	FSB

FSW - Enable full screen self-test pattern and force the FBKG pin output to high to disable video RGB while this bit is set to "1". The self-test pattern's color is determined by (FSR, FSG, FSB) bits.

FSR, FSG, FSB - Define the color of full screen self-test pattern.

Column 21	b7	b6	b5	b4	b3	b2	b1	b0
	WW41	WW40	WW31	WW30	WW21	WW20	WW11	WW10

WW41, WW40 - Determine the shadow width of window 4 when WSHD bit of window 4 is enabled. Please refer to the table below for more details.

(WW41, WW40)	(0, 0)	(0, 1)	(1, 0)	(1, 1)
Shadow Width (unit in Pixel)	2	4	6	8

WW31, WW30 - Determine the shadow width of window 3 when WSHD bit of window 3 is enabled.
WW21, WW20 - Determine the shadow width of window 2 when WSHD bit of window 2 is enabled.
WW11, WW10 - Determine the shadow width of window 1 when WSHD bit of window 1 is enabled.

Column 22	b7	b6	b5	b4	b3	b2	b1	b0
	WH41	WH40	WH31	WH30	WH21	WH20	WH11	WH10

WH41, WH40 - Determine the shadow height of window 4 when WSHD bit of window 4 is enabled. Please refer to the table below for more details.

(WH41, WH40)	(0, 0)	(0, 1)	(1, 0)	(1, 1)
Shadow Height (unit in Line)	2	4	6	8

WH31, WH30 - Determine the shadow height of window 3 when WSHD bit of window 3 is enabled.
WH21, WH20 - Determine the shadow height of window 2 when WSHD bit of window 2 is enabled.
WH11, WH10 - Determine the shadow height of window 1 when WSHD bit of window 1 is enabled.

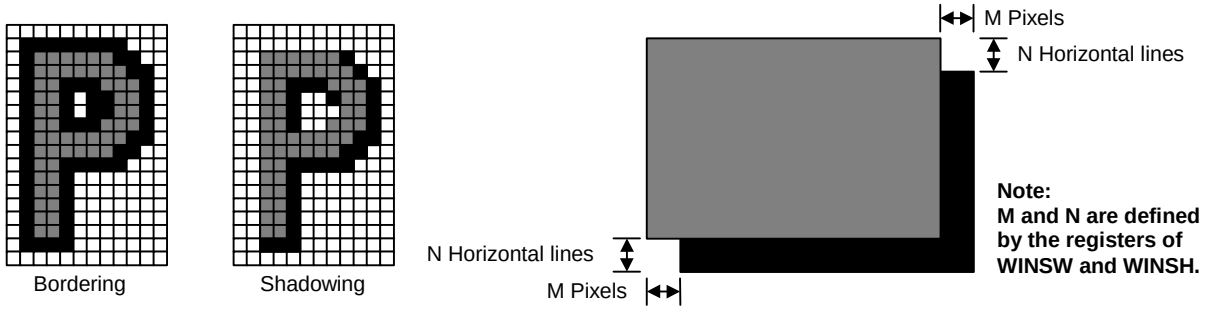


FIGURE 9. Character Bordering and Shadowing and Shadowing on Window

3.13 Color Encoder

The decoder generates the video output to ROUT, GOUT and BOUT by integrating window color, border blackedge, luminance output and color selection output (R, G, B) to form the desired video outputs.

Column 23 ~ column 31 : Reserved.

Note : The register located at column 31 of row 15 is reserved for the testing. Do not program this byte anytime in normal operation.

ROW 16

Column 0	b7	b6	b5	b4	b3	b2	b1	b0
	-	R1	G1	B1	-	R2	G2	B2

R1, G1, B1 - Define the shadow color of window 1. The initial value is (0, 0, 0) after power up.

R2, G2, B2 - Define the shadow color of window 2. The initial value is (0, 0, 0) after power up.

Column 1	b7	b6	b5	b4	b3	b2	b1	b0
	-	R3	G3	B3	-	R4	G4	B4

R3, G3, B3 - Define the shadow color of window 3. The initial value is (0, 0, 0) after power up.

R4, G4, B4 - Define the shadow color of window 4. The initial value is (0, 0, 0) after power up.

Column 2	b7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	-	D2	D1	D0

(This byte is used only for LCD monitor application.)

D3-D0 - These 4 bits define the propagation delay of Rout, Gout, Bout, FBKG and INT outputs to pin XIN input falling edge control registers. Please refer to Figure 12 and Table 8.

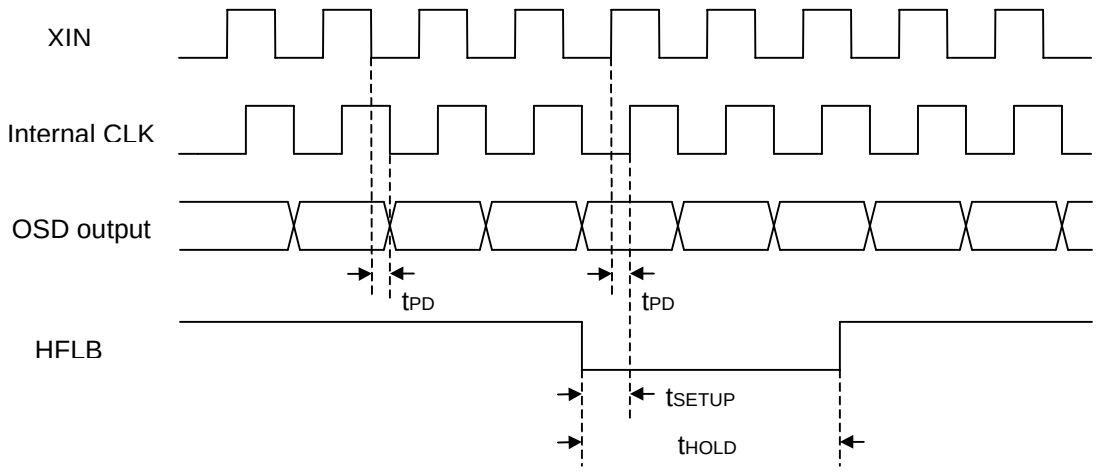


FIGURE 12. Output and HFLB Timing to Pixel Clock

TABLE 7. Output Timing to Pixel Clock

Symbol	(D2, D1, D0)	Min.	Typ.	Max.	Unit
t_{pd}	0	-	TBD	-	ns
	1	-	TBD	-	ns
	2	-	TBD	-	ns
	3	-	TBD	-	ns
	4	-	TBD	-	ns
	5	-	TBD	-	ns
	6	-	TBD	-	ns
	7	-	TBD	-	ns

Column 3 : Reserved.

Column 4	b7	b6	b5	b4	b3	b2	b1	b0
	LCD	-	ID5	ID4	ID3	ID2	ID1	ID0

LCD - OSD application selection.

= 1 ⇒ LCD monitor application selected. The 2nd and 3rd pins are XIN, NC.

= 0 ⇒ CRT monitor application selected. The 2nd and 3rd pins are VCO, RP.

After this bit is changed, the whole chip circuit will be reset to default value except this byte. So this bit also can work as software reset bit. The initial value is 0 after power up.

ID5-ID0 - LCD bit identify bits. LCD bit can be updated to "1" only when ID5-ID0 = (0, 1, 0, 1, 0, 1). And LCD bit can be updated to "0" only when ID5-ID0 = (1, 0, 1, 0, 1, 0).

Column 6 ~ column 31 : Reserved.

4.0 ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage (VDD,VDDA)	-0.3 to +7 V
Voltage with respect to Ground	-0.3 to VDD+0.3 V
Storage Temperature	-65 to +150 °C
Ambient Operating Temperature	0 to +70 °C

5.0 OPERATING CONDITIONS

DC Supply Voltage (VDD,VDDA)	+4.75 to +5.25 V
Operating Temperature	0 to +70 °C

6.0 ELECTRICAL CHARACTERISTICS (Under Operating Conditions)

SYMBOL	PARAMETER	CONDITIONS (NOTES)	MIN.	MAX.	UNITS
V_{IH}	Input High Voltage (pin hflb, vflb, sda, sck)	-	0.6 * VDD	VDD+0.3	V
	Input High Voltage (pin ssb)		0.7 * VDD	VDD+0.3	V
V_{IL}	Input Low Voltage (pin hflb, vflb, sda, sck)	-	VSS-0.3	0.25 * VDD	V
	Input Low Voltage (pin ssb)	-	VSS-0.3	0.2 * VDD	V
V_{OH}	Output High Voltage	$I_{OH} \geq$ -5 mA	VDD-0.8	-	V
V_{OL}	Output Low Voltage	$I_{OL} \leq$ 5 mA	-	0.5	V
V_{ODL}	Open Drain Output Low Voltage	5 mA $\geq I_{ODL}$	-	0.5	V
I_{CC}	Operating Current	Pixel rate=96MHz I_{load} = 0uA	-	25	mA
I_{SB}	Standby Current	Vin = VDD, I_{load} = 0uA	-	12	mA

7.0 SWITCHING CHARACTERISTIC (Under Operating Conditions)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
f_{HFLB}	HFLB input frequency	15	-	150	KHz
T_r	Output rise time	-	-	5	ns
T_f	Output fall time	-	-	5	ns
t_{BCSU}	SSB to SCK set up time	200	-	-	ns
t_{BCH}	SSB to SCK hold time	100	-	-	ns
t_{DCSU}	SDA to SCK set up time	200	-	-	ns
t_{DCH}	SDA to SCK hold time	100	-	-	ns
t_{SCKH}	SCK high time	500	-	-	ns
t_{SCKL}	SCK low time	500	-	-	ns
$t_{SU:STA}$	START condition setup time	500	-	-	ns
$t_{HD:STA}$	START condition hold time	500	-	-	ns
$t_{SU:STO}$	STOP condition setup time	500	-	-	ns
$t_{HD:STO}$	STOP condition hold time	500	-	-	ns

8.0 TIMING DIAGRAMS

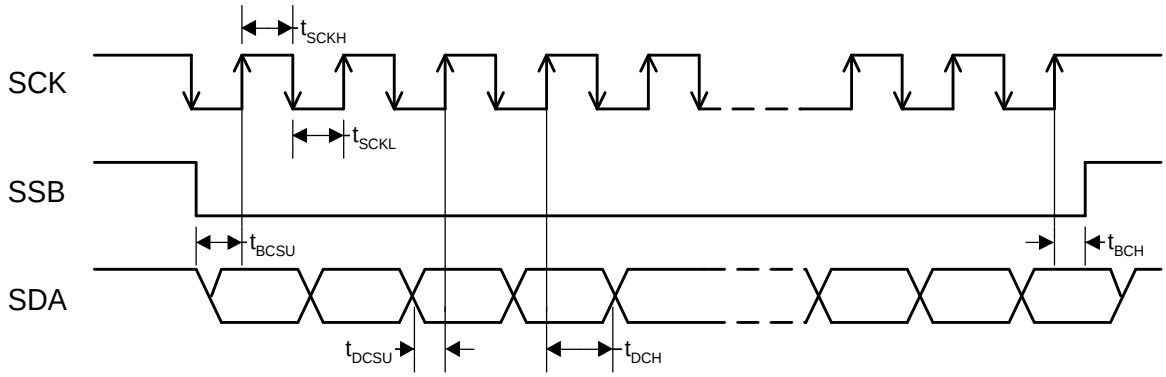


FIGURE 11. Data Interface Timing (SPI)

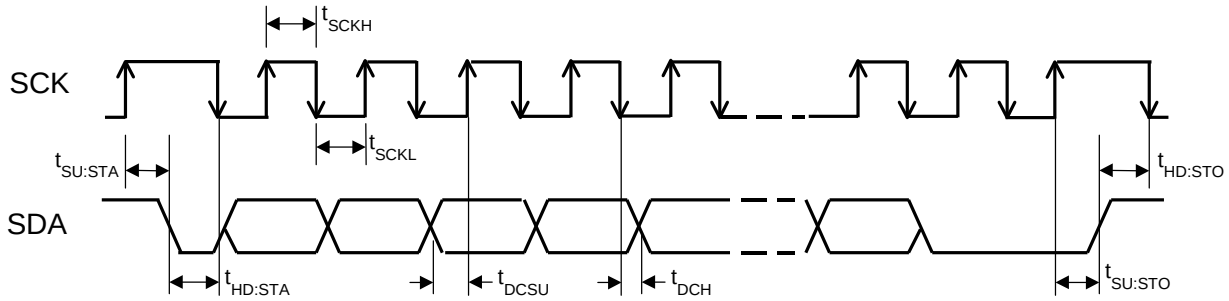
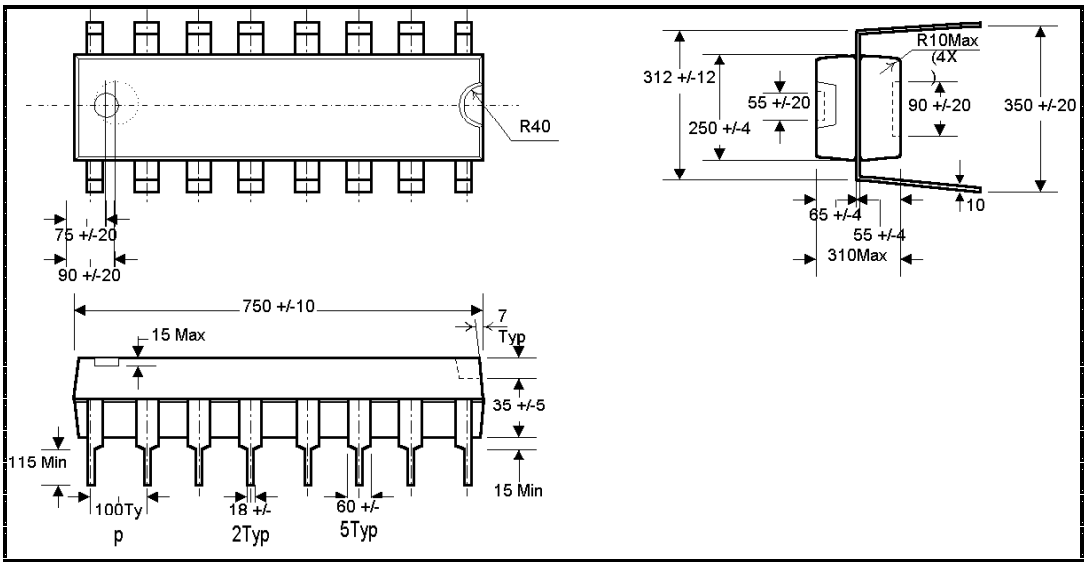


FIGURE 12. Data Interface Timing (I^2C)

9.0 PACKAGE DIMENSION

9.1 16 Pin PDIP 300mil



9.2 16 Pin SOP 300mil